

ITE8716 GP44 (AR1) H : real S3
L : pseudo S3

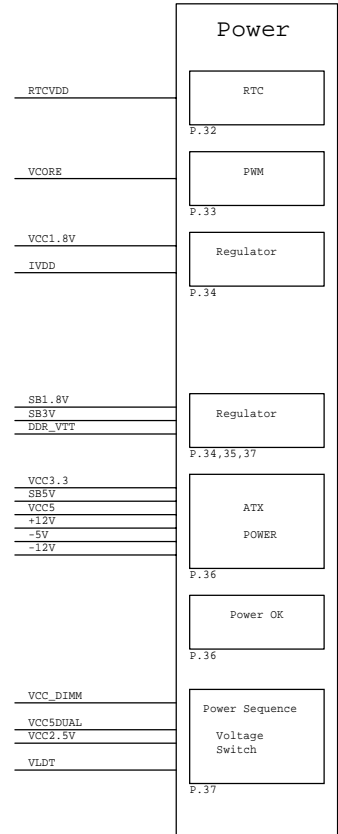
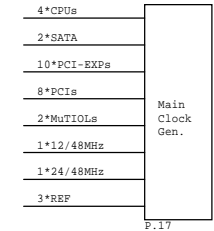
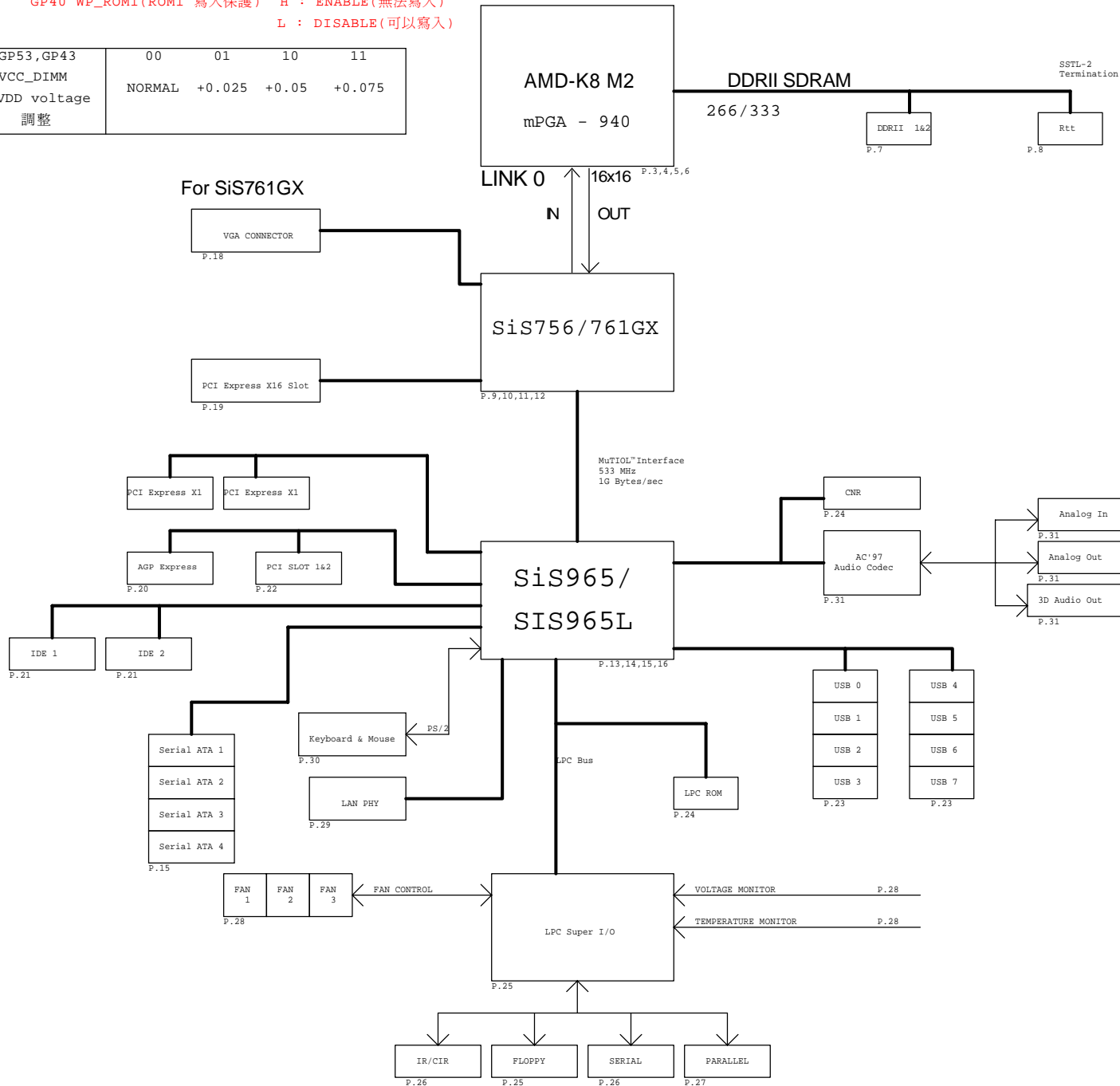
GP42 (AR2) : reserve

GP41 (AR3) : reserve

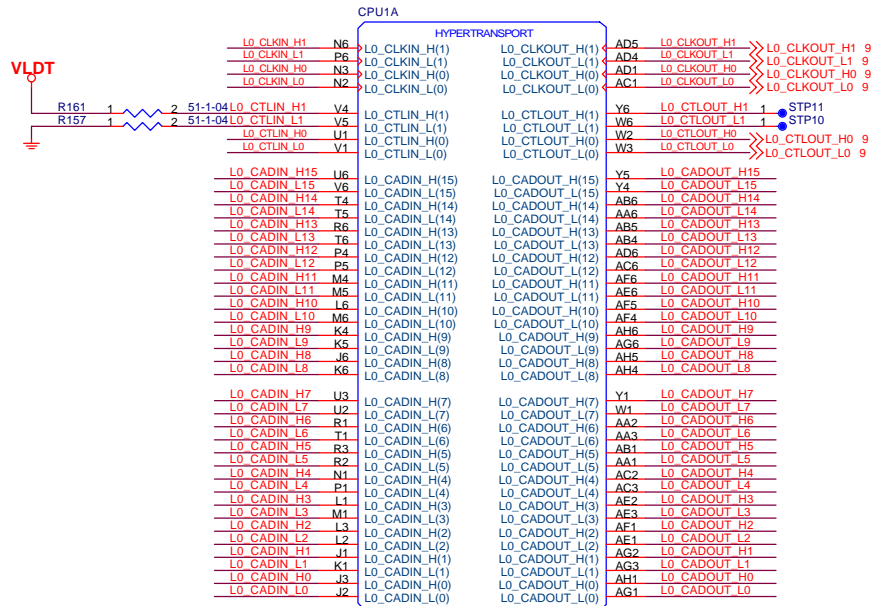
GP40 WP_ROM1(ROM1 寫入保護) H : ENABLE(無法寫入)
L : DISABLE(可以寫入)

GP53,GP43	00	01	10	11
VCC_DIMM	NORMAL	+0.025	+0.05	+0.075
IVDD voltage				
調整				

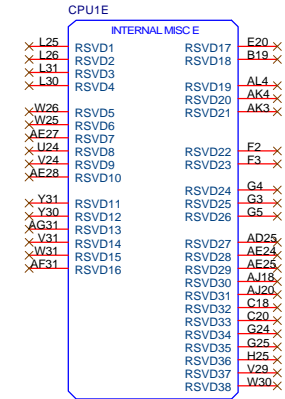
System Block Diagram



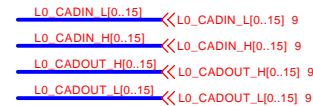
DATE	Rev	Description
12/06/2005	A	1. A33G 由 A31G V1.1 修改而來
03/04/2006	B	1. page32 DEL (Q22,Q21,R192,R186,R189) , ADD D21 2. page34 SB3V 由 Q14(HM2222)+Q12(H431) 改為 Q14(LD1117) 3. page37 Q24 G pin 改接 VCC5 4. page37 EC24 改 1000uF, add EC38,RN41,RN42 5. page36 R178 ?VCCORE 改為 IVDD 6. page28 CPU_FAN1 改為 4pin 7. page29 RTL8201CL 線路變更為 AC131
05/04/2006		1. page37 del R257 2. page37 U11 pin35 改接SB3V



ZIF-940PS-TYC



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7,8 MA0_CLK_H[2..0] << MA0_CLK_H[2..0]
 7,8 MA0_CLK_L[2..0] << MA0_CLK_L[2..0]
 7,8 MA0_CS_L[1..0] << MA0_CS_L[1..0]
 7,8 MA0_ODT0 << MA0_ODT0

7,8 MA_CAS_L << MA_CAS_L
 7,8 MA_WE_L << MA_WE_L
 7,8 MA_RAS_L << MA_RAS_L

7,8 MA_BANK[2..0] << MA_BANK[2..0]

7,8 MA_CKE0 << MA_CKE0

7,8 MA_ADD[15..0] << MA_ADD[15..0]
 7 MA_DQS_H[7..0] << MA_DQS_H[7..0]
 7 MA_DQS_L[7..0] << MA_DQS_L[7..0]
 7 MA_DM[7..0] << MA_DM[7..0]
 7 MA_DATA[63..0] << MA_DATA[63..0]

7,8 MB_CAS_L << MB_CAS_L
 7,8 MB_WE_L << MB_WE_L
 7,8 MB_RAS_L << MB_RAS_L

7,8 MB_BANK[2..0] << MB_BANK[2..0]

7,8 MB_CKE0 << MB_CKE0

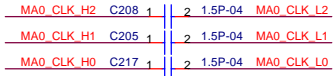
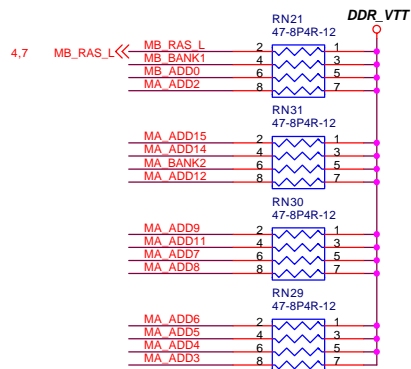
7,8 MB_ADD[15..0] << MB_ADD[15..0]
 7 MB_DQS_H[7..0] << MB_DQS_H[7..0]
 7 MB_DQS_L[7..0] << MB_DQS_L[7..0]
 7 MB_DM[7..0] << MB_DM[7..0]
 7 MB_DATA[63..0] << MB_DATA[63..0]

CPU1B		MEMORY INTERFACE A	
MA0_CLK_H2	AG21	MA0_CLK_H(2)	MA_DATA(63)
MA0_CLK_L2	AG20	MA0_CLK_L(2)	MA_DATA(62)
MA0_CLK_H1	G19	MA0_CLK_H(1)	MA_DATA(61)
MA0_CLK_L1	H19	MA0_CLK_L(1)	MA_DATA(60)
MA0_CLK_H0	U26	MA0_CLK_H(0)	MA_DATA(59)
MA0_CLK_L0	U26	MA0_CLK_L(0)	MA_DATA(58)
MA0_CS_L1	AC25	MA0_CS_L(1)	MA_DATA(57)
MA0_CS_L0	AA24	MA0_CS_L(0)	MA_DATA(56)
MA0_ODT0	AC28	MA0_ODT(0)	MA_DATA(55)
MA1_CLK_H(2)	AE20	MA1_CLK_H(2)	MA_DATA(54)
MA1_CLK_L(2)	AE19	MA1_CLK_L(2)	MA_DATA(53)
MA1_CLK_H(1)	G20	MA1_CLK_H(1)	MA_DATA(52)
MA1_CLK_L(1)	G21	MA1_CLK_L(1)	MA_DATA(51)
MA1_CLK_H(0)	V27	MA1_CLK_H(0)	MA_DATA(50)
MA1_CLK_L(0)	W27	MA1_CLK_L(0)	MA_DATA(49)
MA1_CS_L(1)	AD27	MA1_CS_L(1)	MA_DATA(48)
MA1_CS_L(0)	AA25	MA1_CS_L(0)	MA_DATA(47)
MA1_ODT(0)	AC27	MA1_ODT(0)	MA_DATA(46)
MA_CAS_L	AB25	MA_CAS_L	MA_DATA(45)
MA_WE_L	AB27	MA_WE_L	MA_DATA(44)
MA_RAS_L	AA26	MA_RAS_L	MA_DATA(43)
MA_BANK(2)	N25	MA_BANK(2)	MA_DATA(42)
MA_BANK(1)	Y27	MA_BANK(1)	MA_DATA(41)
MA_BANK(0)	AA27	MA_BANK(0)	MA_DATA(40)
MA_CKE(1)	L27	MA_CKE(1)	MA_DATA(39)
MA_CKE(0)	M25	MA_CKE(0)	MA_DATA(38)
MA_ADD(15)	M27	MA_ADD(15)	MA_DATA(37)
MA_ADD(14)	N24	MA_ADD(14)	MA_DATA(36)
MA_ADD(13)	AC26	MA_ADD(13)	MA_DATA(35)
MA_ADD(12)	N26	MA_ADD(12)	MA_DATA(34)
MA_ADD(11)	P25	MA_ADD(11)	MA_DATA(33)
MA_ADD(10)	Y25	MA_ADD(10)	MA_DATA(32)
MA_ADD(9)	N24	MA_ADD(9)	MA_DATA(31)
MA_ADD(8)	R24	MA_ADD(8)	MA_DATA(30)
MA_ADD(7)	P27	MA_ADD(7)	MA_DATA(29)
MA_ADD(6)	R25	MA_ADD(6)	MA_DATA(28)
MA_ADD(5)	R26	MA_ADD(5)	MA_DATA(27)
MA_ADD(4)	R27	MA_ADD(4)	MA_DATA(26)
MA_ADD(3)	T25	MA_ADD(3)	MA_DATA(25)
MA_ADD(2)	U25	MA_ADD(2)	MA_DATA(24)
MA_ADD(1)	T27	MA_ADD(1)	MA_DATA(23)
MA_ADD(0)	W24	MA_ADD(0)	MA_DATA(22)
MA_DQS_H(7)	AD15	MA_DQS_H(7)	MA_DATA(21)
MA_DQS_L(7)	AE15	MA_DQS_L(7)	MA_DATA(20)
MA_DQS_H(6)	AG18	MA_DQS_H(6)	MA_DATA(19)
MA_DQS_L(6)	AG19	MA_DQS_L(6)	MA_DATA(18)
MA_DQS_H(5)	AG24	MA_DQS_H(5)	MA_DATA(17)
MA_DQS_L(5)	AG25	MA_DQS_L(5)	MA_DATA(16)
MA_DQS_H(4)	AG27	MA_DQS_H(4)	MA_DATA(15)
MA_DQS_L(4)	AG28	MA_DQS_L(4)	MA_DATA(14)
MA_DQS_H(3)	D29	MA_DQS_H(3)	MA_DATA(13)
MA_DQS_L(3)	C29	MA_DQS_L(3)	MA_DATA(12)
MA_DQS_H(2)	D25	MA_DQS_H(2)	MA_DATA(11)
MA_DQS_L(2)	E19	MA_DQS_L(2)	MA_DATA(10)
MA_DQS_H(1)	F19	MA_DQS_H(1)	MA_DATA(9)
MA_DQS_L(1)	F15	MA_DQS_L(1)	MA_DATA(8)
MA_DQS_H(0)	G15	MA_DQS_H(0)	MA_DATA(7)
MA_DQS_L(0)	G15	MA_DQS_L(0)	MA_DATA(6)
MA_DM(7)	AE15	MA_DM(7)	MA_DATA(5)
MA_DM(6)	AE19	MA_DM(6)	MA_DATA(4)
MA_DM(5)	AJ25	MA_DM(5)	MA_DATA(3)
MA_DM(4)	AH29	MA_DM(4)	MA_DATA(2)
MA_DM(3)	B29	MA_DM(3)	MA_DATA(1)
MA_DM(2)	E24	MA_DM(2)	MA_DATA(0)
MA_DM(1)	E18	MA_DM(1)	
MA_DM(0)	H15	MA_DM(0)	
MA_DATA(63)	AE14	MA_DATA(63)	
MA_DATA(62)	AG14	MA_DATA(62)	
MA_DATA(61)	AG16	MA_DATA(61)	
MA_DATA(60)	AD17	MA_DATA(60)	
MA_DATA(59)	AD14	MA_DATA(59)	
MA_DATA(58)	AE13	MA_DATA(58)	
MA_DATA(57)	AG15	MA_DATA(57)	
MA_DATA(56)	AE16	MA_DATA(56)	
MA_DATA(55)	AG17	MA_DATA(55)	
MA_DATA(54)	AE18	MA_DATA(54)	
MA_DATA(53)	AG22	MA_DATA(53)	
MA_DATA(52)	AE17	MA_DATA(52)	
MA_DATA(51)	AE17	MA_DATA(51)	
MA_DATA(50)	AE21	MA_DATA(50)	
MA_DATA(49)	AE21	MA_DATA(49)	
MA_DATA(48)	AE21	MA_DATA(48)	
MA_DATA(47)	AE23	MA_DATA(47)	
MA_DATA(46)	AE23	MA_DATA(46)	
MA_DATA(45)	AJ26	MA_DATA(45)	
MA_DATA(44)	AG26	MA_DATA(44)	
MA_DATA(43)	AE22	MA_DATA(43)	
MA_DATA(42)	AG23	MA_DATA(42)	
MA_DATA(41)	AH25	MA_DATA(41)	
MA_DATA(40)	AE25	MA_DATA(40)	
MA_DATA(39)	AJ28	MA_DATA(39)	
MA_DATA(38)	AJ29	MA_DATA(38)	
MA_DATA(37)	AE29	MA_DATA(37)	
MA_DATA(36)	AE26	MA_DATA(36)	
MA_DATA(35)	AJ27	MA_DATA(35)	
MA_DATA(34)	AG29	MA_DATA(34)	
MA_DATA(33)	AE27	MA_DATA(33)	
MA_DATA(32)	E29	MA_DATA(32)	
MA_DATA(31)	E28	MA_DATA(31)	
MA_DATA(30)	D27	MA_DATA(30)	
MA_DATA(29)	C27	MA_DATA(29)	
MA_DATA(28)	G26	MA_DATA(28)	
MA_DATA(27)	F27	MA_DATA(27)	
MA_DATA(26)	C28	MA_DATA(26)	
MA_DATA(25)	E27	MA_DATA(25)	
MA_DATA(24)	F25	MA_DATA(24)	
MA_DATA(23)	E25	MA_DATA(23)	
MA_DATA(22)	D23	MA_DATA(22)	
MA_DATA(21)	E26	MA_DATA(21)	
MA_DATA(20)	C26	MA_DATA(20)	
MA_DATA(19)	G23	MA_DATA(19)	
MA_DATA(18)	F23	MA_DATA(18)	
MA_DATA(17)	E22	MA_DATA(17)	
MA_DATA(16)	E21	MA_DATA(16)	
MA_DATA(15)	F17	MA_DATA(15)	
MA_DATA(14)	G17	MA_DATA(14)	
MA_DATA(13)	G22	MA_DATA(13)	
MA_DATA(12)	F21	MA_DATA(12)	
MA_DATA(11)	G18	MA_DATA(11)	
MA_DATA(10)	E17	MA_DATA(10)	
MA_DATA(9)	G16	MA_DATA(9)	
MA_DATA(8)	E15	MA_DATA(8)	
MA_DATA(7)	G13	MA_DATA(7)	
MA_DATA(6)	H13	MA_DATA(6)	
MA_DATA(5)	H17	MA_DATA(5)	
MA_DATA(4)	E16	MA_DATA(4)	
MA_DATA(3)	E14	MA_DATA(3)	
MA_DATA(2)	G14	MA_DATA(2)	
MA_DATA(1)	J28	MA_DATA(1)	
MA_DATA(0)	J27	MA_DATA(0)	
MA_DM(8)	J25	MA_DM(8)	
MA_CHECK(7)	K25	MA_CHECK(7)	
MA_CHECK(6)	J26	MA_CHECK(6)	
MA_CHECK(5)	G28	MA_CHECK(5)	
MA_CHECK(4)	G27	MA_CHECK(4)	
MA_CHECK(3)	L24	MA_CHECK(3)	
MA_CHECK(2)	K27	MA_CHECK(2)	
MA_CHECK(1)	H29	MA_CHECK(1)	
MA_CHECK(0)	H27	MA_CHECK(0)	

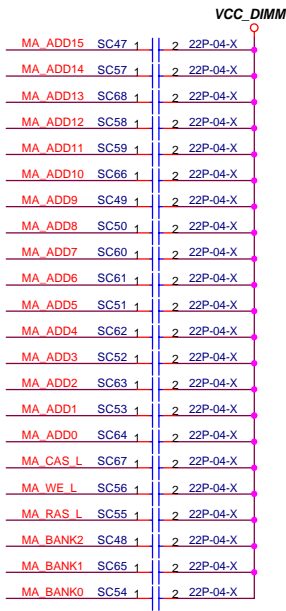
ZIF-940PS-TYC

CPU1C		MEMORY INTERFACE B	
MB0_CLK_H2	AJ19	MB0_CLK_H(2)	MB_DATA(63)
MB0_CLK_L2	AK19	MB0_CLK_L(2)	MB_DATA(62)
MB0_CLK_H1	A18	MB0_CLK_H(1)	MB_DATA(61)
MB0_CLK_L1	U30	MB0_CLK_L(1)	MB_DATA(60)
MB0_CLK_H0	U30	MB0_CLK_H(0)	MB_DATA(59)
MB0_CLK_L0	U30	MB0_CLK_L(0)	MB_DATA(58)
MB0_CS_L1	AE30	MB0_CS_L(1)	MB_DATA(57)
MB0_CS_L0	AC31	MB0_CS_L(0)	MB_DATA(56)
MB0_ODT0	AD29	MB0_ODT(0)	MB_DATA(55)
MB1_CLK_H(2)	AL19	MB1_CLK_H(2)	MB_DATA(54)
MB1_CLK_L(2)	AL18	MB1_CLK_L(2)	MB_DATA(53)
MB1_CLK_H(1)	C19	MB1_CLK_H(1)	MB_DATA(52)
MB1_CLK_L(1)	D19	MB1_CLK_L(1)	MB_DATA(51)
MB1_CLK_H(0)	W29	MB1_CLK_H(0)	MB_DATA(50)
MB1_CLK_L(0)	W28	MB1_CLK_L(0)	MB_DATA(49)
MB1_CS_L(1)	AE29	MB1_CS_L(1)	MB_DATA(48)
MB1_CS_L(0)	AB31	MB1_CS_L(0)	MB_DATA(47)
MB1_ODT(0)	AD31	MB1_ODT(0)	MB_DATA(46)
MB_CAS_L	AC29	MB_CAS_L	MB_DATA(45)
MB_WE_L	AC30	MB_WE_L	MB_DATA(44)
MB_RAS_L	AB29	MB_RAS_L	MB_DATA(43)
MB_BANK(2)	N31	MB_BANK(2)	MB_DATA(42)
MB_BANK(1)	AA31	MB_BANK(1)	MB_DATA(41)
MB_BANK(0)	AA28	MB_BANK(0)	MB_DATA(40)
MB_CKE(1)	M31	MB_CKE(1)	MB_DATA(39)
MB_CKE(0)	M29	MB_CKE(0)	MB_DATA(38)
MB_ADD(15)	N28	MB_ADD(15)	MB_DATA(37)
MB_ADD(14)	N29	MB_ADD(14)	MB_DATA(36)
MB_ADD(13)	AE31	MB_ADD(13)	MB_DATA(35)
MB_ADD(12)	N30	MB_ADD(12)	MB_DATA(34)
MB_ADD(11)	P29	MB_ADD(11)	MB_DATA(33)
MB_ADD(10)	AA29	MB_ADD(10)	MB_DATA(32)
MB_ADD(9)	P31	MB_ADD(9)	MB_DATA(31)
MB_ADD(8)	R29	MB_ADD(8)	MB_DATA(30)
MB_ADD(7)	R28	MB_ADD(7)	MB_DATA(29)
MB_ADD(6)	R31	MB_ADD(6)	MB_DATA(28)
MB_ADD(5)	R30	MB_ADD(5)	MB_DATA(27)
MB_ADD(4)	T31	MB_ADD(4)	MB_DATA(26)
MB_ADD(3)	T29	MB_ADD(3)	MB_DATA(25)
MB_ADD(2)	U29	MB_ADD(2)	MB_DATA(24)
MB_ADD(1)	U28	MB_ADD(1)	MB_DATA(23)
MB_ADD(0)	AA30	MB_ADD(0)	MB_DATA(22)
MB_DQS_H(7)	AK13	MB_DQS_H(7)	MB_DATA(21)
MB_DQS_L(7)	AJ13	MB_DQS_L(7)	MB_DATA(20)
MB_DQS_H(6)	AK17	MB_DQS_H(6)	MB_DATA(19)
MB_DQS_L(6)	AH17	MB_DQS_L(6)	MB_DATA(18)
MB_DQS_H(5)	AK23	MB_DQS_H(5)	MB_DATA(17)
MB_DQS_L(5)	AL23	MB_DQS_L(5)	MB_DATA(16)
MB_DQS_H(4)	AL28	MB_DQS_H(4)	MB_DATA(15)
MB_DQS_L(4)	AL29	MB_DQS_L(4)	MB_DATA(14)
MB_DQS_H(3)	D31	MB_DQS_H(3)	MB_DATA(13)
MB_DQS_L(3)	C31	MB_DQS_L(3)	MB_DATA(12)
MB_DQS_H(2)	C23	MB_DQS_H(2)	MB_DATA(11)
MB_DQS_L(2)	D17	MB_DQS_L(2)	MB_DATA(10)
MB_DQS_H(1)	C17	MB_DQS_H(1)	MB_DATA(9)
MB_DQS_L(1)	C14	MB_DQS_L(1)	MB_DATA(8)
MB_DQS_H(0)	C13	MB_DQS_H(0)	MB_DATA(7)
MB_DQS_L(0)	C13	MB_DQS_L(0)	MB_DATA(6)
MB_DM(7)	AJ14	MB_DM(7)	MB_DATA(5)
MB_DM(6)	AH17	MB_DM(6)	MB_DATA(4)
MB_DM(5)	AJ23	MB_DM(5)	MB_DATA(3)
MB_DM(4)	AK29	MB_DM(4)	MB_DATA(2)
MB_DM(3)	C30	MB_DM(3)	MB_DATA(1)
MB_DM(2)	A23	MB_DM(2)	MB_DATA(0)
MB_DM(1)	B17	MB_DM(1)	
MB_DM(0)	B13	MB_DM(0)	
MB_DATA(63)	AH13	MB_DATA(63)	
MB_DATA(62)	AL13	MB_DATA(62)	
MB_DATA(61)	AL15	MB_DATA(61)	
MB_DATA(60)	AL15	MB_DATA(60)	
MB_DATA(59)	AG13	MB_DATA(59)	
MB_DATA(58)	AL14	MB_DATA(58)	
MB_DATA(57)	AK15	MB_DATA(57)	
MB_DATA(56)	AL16	MB_DATA(56)	
MB_DATA(55)	AL17	MB_DATA(55)	
MB_DATA(54)	AK21	MB_DATA(54)	
MB_DATA(53)	AL21	MB_DATA(53)	
MB_DATA(52)	AH15	MB_DATA(52)	
MB_DATA(51)	AJ16	MB_DATA(51)	
MB_DATA(50)	AH13	MB_DATA(50)	
MB_DATA(49)	AH13	MB_DATA(49)	
MB_DATA(48)	AL20	MB_DATA(48)	
MB_DATA(47)	AJ22	MB_DATA(47)	
MB_DATA(46)	AL22	MB_DATA(46)	
MB_DATA(45)	AL24	MB_DATA(45)	
MB_DATA(44)	AK25	MB_DATA(44)	
MB_DATA(43)	AJ21	MB_DATA(43)	
MB_DATA(42)	AH21	MB_DATA(42)	
MB_DATA(41)	AH23	MB_DATA(41)	
MB_DATA(40)	AJ24	MB_DATA(40)	
MB_DATA(39)	AL27	MB_DATA(39)	
MB_DATA(38)	AK27	MB_DATA(38)	
MB_DATA(37)	AH31	MB_DATA(37)	
MB_DATA(36)	AG30	MB_DATA(36)	
MB_DATA(35)	AL25	MB_DATA(35)	
MB_DATA(34)	AJ26	MB_DATA(34)	
MB_DATA(33)	AJ30	MB_DATA(33)	
MB_DATA(32)	AJ31	MB_DATA(32)	
MB_DATA(31)	E31	MB_DATA(31)	
MB_DATA(30)	E30	MB_DATA(30)	
MB_DATA(29)	B27	MB_DATA(29)	
MB_DATA(28)	A27	MB_DATA(28)	
MB_DATA(27)	F28	MB_DATA(27)	
MB_DATA(26)	F31	MB_DATA(26)	
MB_DATA(25)	A29	MB_DATA(25)	
MB_DATA(24)	A28	MB_DATA(24)	
MB_DATA(23)	A25	MB_DATA(23)	
MB_DATA(22)	A24	MB_DATA(22)	
MB_DATA(21)	C22	MB_DATA(21)	
MB_DATA(20)	D21	MB_DATA(20)	
MB_DATA(19)	A26	MB_DATA(19)	
MB_DATA(18)	B25	MB_DATA(18)	
MB_DATA(17)	B23	MB_DATA(17)	
MB_DATA(16)	A22	MB_DATA(16)	
MB_DATA(15)	B21	MB_DATA(15)	
MB_DATA(14)	A20	MB_DATA(14)	
MB_DATA(13)	C18	MB_DATA(13)	
MB_DATA(12)	D15	MB_DATA(12)	
MB_DATA(11)	C21	MB_DATA(11)	
MB_DATA(10)	A21	MB_DATA(10)	
MB_DATA(9)	A17	MB_DATA(9)	
MB_DATA(8)	A16	MB_DATA(8)	
MB_DATA(7)	A14	MB_DATA(7)	
MB_DATA(6)	E13	MB_DATA(6)	
MB_DATA(5)	F13	MB_DATA(5)	
MB_DATA(4)	C15	MB_DATA(4)	
MB_DATA(3)	A15	MB_DATA(3)	
MB_DATA(2)	A13	MB_DATA(2)	
MB_DATA(1)	D13	MB_DATA(1)	
MB_DATA(0)		MB_DATA(0)	
MB_DQS_H(8)	J31	MB_DQS_H(8)	
MB_DQS_L(8)	J30	MB_DQS_L(8)	
MB_DM(8)	J29	MB_DM(8)	
MB_CHECK(7)	K29	MB_CHECK(7)	
MB_CHECK(6)	K31	MB_CHECK(6)	
MB_CHECK(5)	G30	MB_CHECK(5)	
MB_CHECK(4)	G29	MB_CHECK(4)	
MB_CHECK(3)	L29	MB_CHECK(3)	
MB_CHECK(2)	L28	MB_CHECK(2)	
MB_CHECK(1)	H31	MB_CHECK(1)	
MB_CHECK(0)	G31	MB_CHECK(0)	

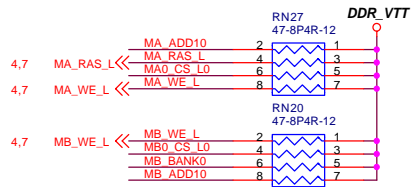
ZIF-940PS-TYC



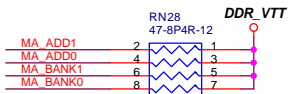
4.7 MA0_CLK_H[2..0] << MA0_CLK_H[2..0]
 4.7 MA0_CLK_L[2..0] << MA0_CLK_L[2..0]



4.7 MA_ADD[15..0] << MA_ADD[15..0]

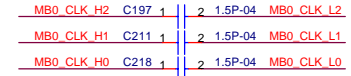
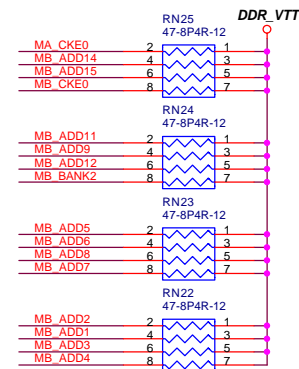


4.7 MA_BANK[2..0] << MA_BANK[2..0]

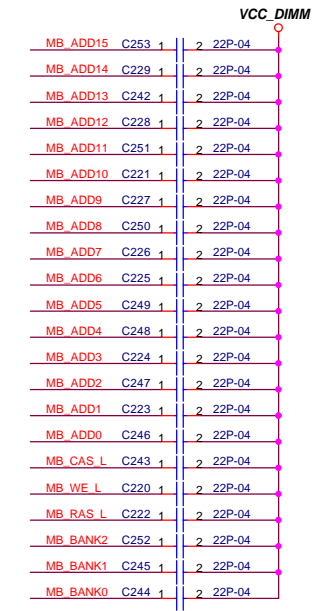


4.7 MA_CKE0 << MA_CKE0
 4.7 MA0_ODT0 << MA0_ODT0

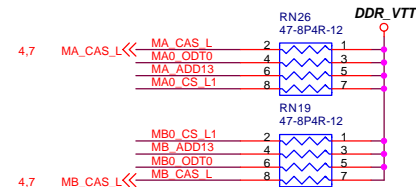
4.7 MA0_CS_L[1..0] << MA0_CS_L[1..0]



4.7 MB0_CLK_H[2..0] << MB0_CLK_H[2..0]
 4.7 MB0_CLK_L[2..0] << MB0_CLK_L[2..0]



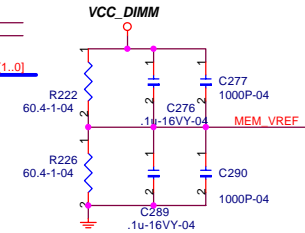
4.7 MB_ADD[15..0] << MB_ADD[15..0]



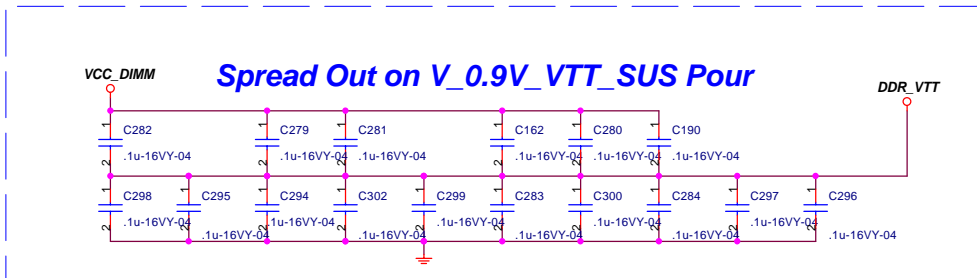
4.7 MB_BANK[2..0] << MB_BANK[2..0]

4.7 MB_CKE0 << MB_CKE0
 4.7 MB0_ODT0 << MB0_ODT0

4.7 MB0_CS_L[1..0] << MB0_CS_L[1..0]



7 MEM_VREF << MEM_VREF

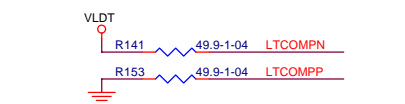
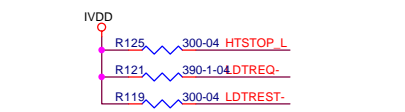
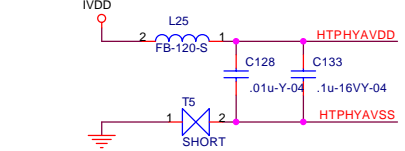
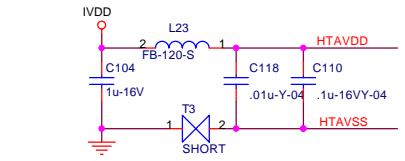


3 L0_CADIN_L[0..15] >> L0_CADIN_L[0..15]
 3 L0_CADIN_H[0..15] >> L0_CADIN_H[0..15]
 3 L0_CADOUT_H[0..15] >> L0_CADOUT_H[0..15]
 3 L0_CADOUT_L[0..15] >> L0_CADOUT_L[0..15]

3 L0_CLKIN_L0 >> L0_CLKIN_L0
 3 L0_CLKIN_H0 >> L0_CLKIN_H0
 3 L0_CLKIN_L1 >> L0_CLKIN_L1
 3 L0_CLKIN_H1 >> L0_CLKIN_H1
 3 L0_CTLIN_L0 >> L0_CTLIN_L0
 3 L0_CTLIN_H0 >> L0_CTLIN_H0

17 NBCLKC >> NBCLKC
 17 NBCLKT >> NBCLKT

L20, L23, C90 need POLY



C114 near to R119

L0_CADOUT_H0	AE32	LRCAD_P0
L0_CADOUT_H1	AD34	LRCAD_P1
L0_CADOUT_H2	AB32	LRCAD_P2
L0_CADOUT_H3	AA34	LRCAD_P3
L0_CADOUT_H4	V34	LRCAD_P4
L0_CADOUT_H5	T32	LRCAD_P5
L0_CADOUT_H6	R34	LRCAD_P6
L0_CADOUT_H7	N32	LRCAD_P7
L0_CADOUT_H8	AC30	LRCAD_P8
L0_CADOUT_H9	AB29	LRCAD_P9
L0_CADOUT_H10	Y30	LRCAD_P10
L0_CADOUT_H11	U30	LRCAD_P11
L0_CADOUT_H12	T29	LRCAD_P12
L0_CADOUT_H13	P30	LRCAD_P13
L0_CADOUT_H14	N29	LRCAD_P14
L0_CADOUT_H15	L30	LRCAD_P15
L0_CADOUT_L0	AD32	LRCAD_N0
L0_CADOUT_L1	AC34	LRCAD_N1
L0_CADOUT_L2	AA32	LRCAD_N2
L0_CADOUT_L3	Y34	LRCAD_N3
L0_CADOUT_L4	U34	LRCAD_N4
L0_CADOUT_L5	R32	LRCAD_N5
L0_CADOUT_L6	P34	LRCAD_N6
L0_CADOUT_L7	M32	LRCAD_N7
L0_CADOUT_L8	AC31	LRCAD_N8
L0_CADOUT_L9	AA29	LRCAD_N9
L0_CADOUT_L10	Y31	LRCAD_N10
L0_CADOUT_L11	U31	LRCAD_N11
L0_CADOUT_L12	R29	LRCAD_N12
L0_CADOUT_L13	P31	LRCAD_N13
L0_CADOUT_L14	M29	LRCAD_N14
L0_CADOUT_L15	L31	LRCAD_N15

3 L0_CLKOUT_L0	>>	L0_CLKOUT_L0	V32	LRCLK_N0
3 L0_CLKOUT_H0	>>	L0_CLKOUT_H0	W32	LRCLK_P0
3 L0_CLKOUT_L1	>>	L0_CLKOUT_L1	V29	LRCLK_N1
3 L0_CLKOUT_H1	>>	L0_CLKOUT_H1	W29	LRCLK_P1
3 L0_CTLOUT_L0	>>	L0_CTLOUT_L0	L34	LRCTL_N
3 L0_CTLOUT_H0	>>	L0_CTLOUT_H0	M34	LRCTL_P
HTCLKN		C18		HTCLKN
HTCLKP		B18		HTCLKP
HTAVDD		C17		HTAVDD
HTAVSS		A18		HTAVSS
HTPHYAVDD		A17		HTPHYAVDD
HTPHYAVSS		B17		HTPHYAVSS
5 HTSTOP_L	>>	HTSTOP_L	F18	LDTSTOP#
14 LDTRREQ-	>>	LDTRREQ-	D18	LDTRREQ#
5 LDTRREST-	>>	LDTRREST-	E18	LDTRSET#

19 PETP[0..15] >> PETP[0..15]
 19 PETN[0..15] >> PETN[0..15]
 17 PECLK0 >> PECLK0
 17 PECLK-0 >> PECLK-0

A23	L0_CADIN_L0	LRCAD_L0
A24	L0_CADIN_L1	LRCAD_L1
A28	L0_CADIN_L3	LRCAD_L3
A29	L0_CADIN_L4	LRCAD_L4
A30	L0_CADIN_L5	LRCAD_L5
A32	L0_CADIN_L6	LRCAD_L6
A33	L0_CADIN_L7	LRCAD_L7
A34	L0_CADIN_L8	LRCAD_L8
A35	L0_CADIN_L9	LRCAD_L9
A36	L0_CADIN_L10	LRCAD_L10
A37	L0_CADIN_L11	LRCAD_L11
A38	L0_CADIN_L12	LRCAD_L12
A39	L0_CADIN_L13	LRCAD_L13
A40	L0_CADIN_L14	LRCAD_L14
A41	L0_CADIN_L15	LRCAD_L15
A42	L0_CADIN_H0	LRCAD_H0
A43	L0_CADIN_H1	LRCAD_H1
A44	L0_CADIN_H2	LRCAD_H2
A45	L0_CADIN_H3	LRCAD_H3
A46	L0_CADIN_H4	LRCAD_H4
A47	L0_CADIN_H5	LRCAD_H5
A48	L0_CADIN_H6	LRCAD_H6
A49	L0_CADIN_H7	LRCAD_H7
A50	L0_CADIN_H8	LRCAD_H8
A51	L0_CADIN_H9	LRCAD_H9
A52	L0_CADIN_H10	LRCAD_H10
A53	L0_CADIN_H11	LRCAD_H11
A54	L0_CADIN_H12	LRCAD_H12
A55	L0_CADIN_H13	LRCAD_H13
A56	L0_CADIN_H14	LRCAD_H14
A57	L0_CADIN_H15	LRCAD_H15

LTCAD_N0	LRCAD_N0
LTCAD_N1	LRCAD_N1
LTCAD_N2	LRCAD_N2
LTCAD_N3	LRCAD_N3
LTCAD_N4	LRCAD_N4
LTCAD_N5	LRCAD_N5
LTCAD_N6	LRCAD_N6
LTCAD_N7	LRCAD_N7
LTCAD_N8	LRCAD_N8
LTCAD_N9	LRCAD_N9
LTCAD_N10	LRCAD_N10
LTCAD_N11	LRCAD_N11
LTCAD_N12	LRCAD_N12
LTCAD_N13	LRCAD_N13
LTCAD_N14	LRCAD_N14
LTCAD_N15	LRCAD_N15
LTCAD_P0	LRCAD_P0
LTCAD_P1	LRCAD_P1
LTCAD_P2	LRCAD_P2
LTCAD_P3	LRCAD_P3
LTCAD_P4	LRCAD_P4
LTCAD_P5	LRCAD_P5
LTCAD_P6	LRCAD_P6
LTCAD_P7	LRCAD_P7
LTCAD_P8	LRCAD_P8
LTCAD_P9	LRCAD_P9
LTCAD_P10	LRCAD_P10
LTCAD_P11	LRCAD_P11
LTCAD_P12	LRCAD_P12
LTCAD_P13	LRCAD_P13
LTCAD_P14	LRCAD_P14
LTCAD_P15	LRCAD_P15

J34	LRCOMP
L34	LRCTL_N
M34	LRCTL_P
V32	LRCLK_N0
W32	LRCLK_P0
V29	LRCLK_N1
W29	LRCLK_P1
C18	HTCLKN
B18	HTCLKP
C17	HTAVDD
A18	HTAVSS
A17	HTPHYAVDD
B17	HTPHYAVSS
F18	LDTSTOP#
D18	LDTRREQ#
E18	LDTRSET#

J1	PETP0
K1	PETP1
L1	PETP2
M1	PETP3
N1	PETP4
P1	PETP5
Q1	PETP6
R1	PETP7
S1	PETP8
T1	PETP9
U1	PETP10
V1	PETP11
W1	PETP12
X1	PETP13
Y1	PETP14
Z1	PETP15
A2	PETN0
B2	PETN1
C2	PETN2
D2	PETN3
E2	PETN4
F2	PETN5
G2	PETN6
H2	PETN7
J2	PETN8
K2	PETN9
L2	PETN10
M2	PETN11
N2	PETN12
P2	PETN13
Q2	PETN14
R2	PETN15
H2	PECLKN
H1	REFCLKP
Y2	PCIEAVDD
Y1	PCIEAVSS
AA3	PCIESET0
AA4	PCIESET1
H2	PECLK-0
H1	REFCLKP
Y2	PCIEAVDD
Y1	PCIEAVSS
AA3	PCIESET0
AA4	PCIESET1

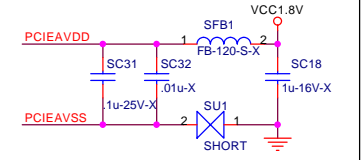
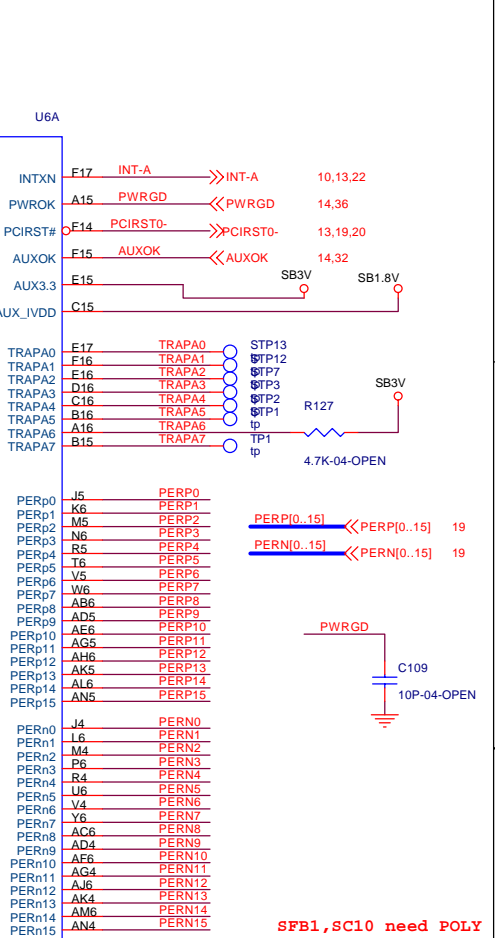
LDT_TX

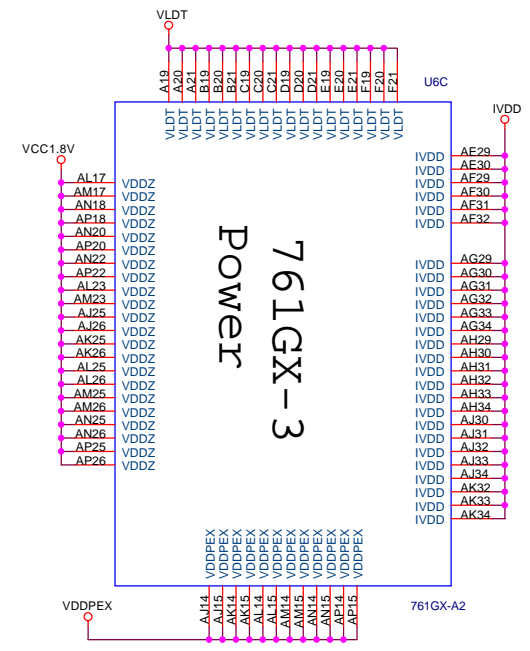
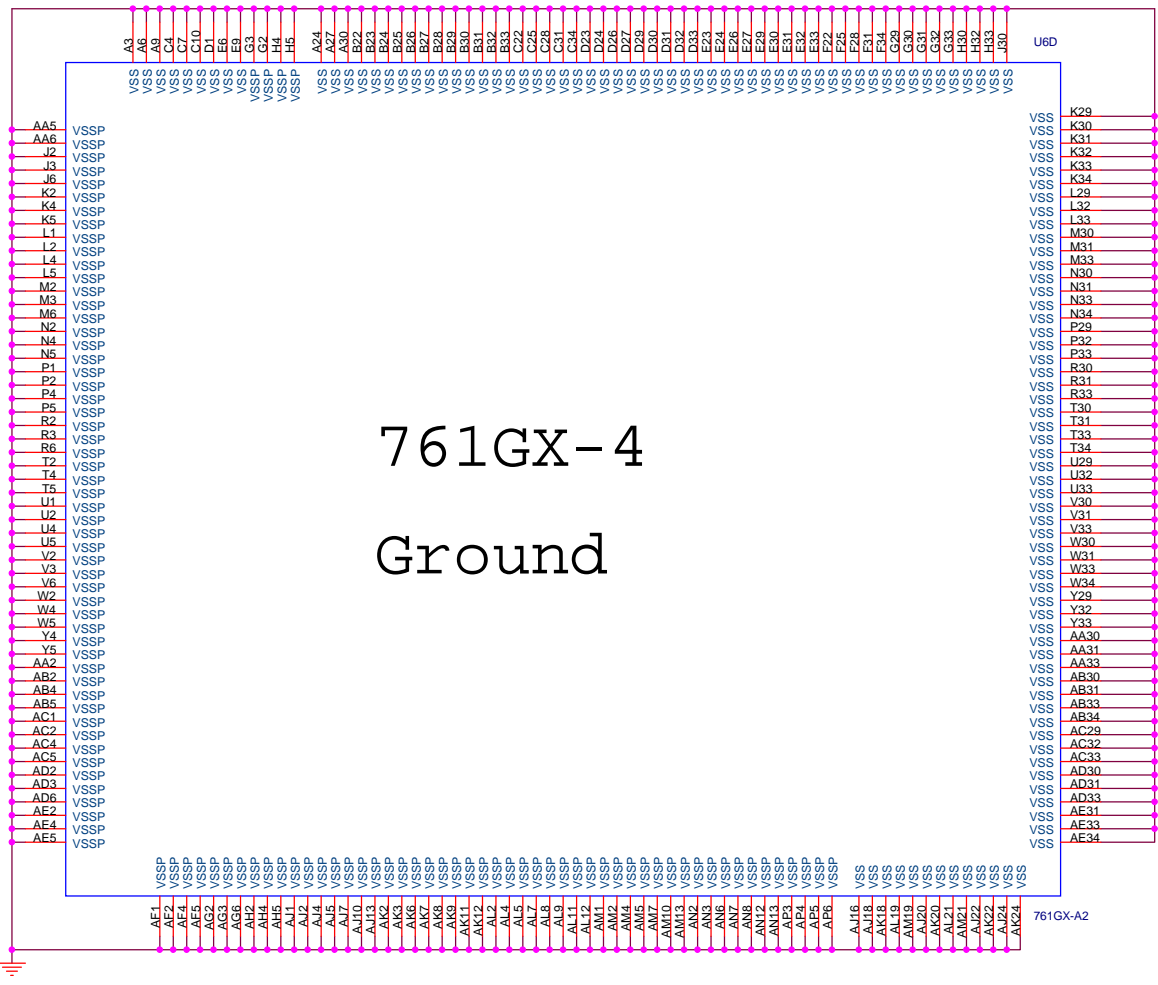
LDT_RX

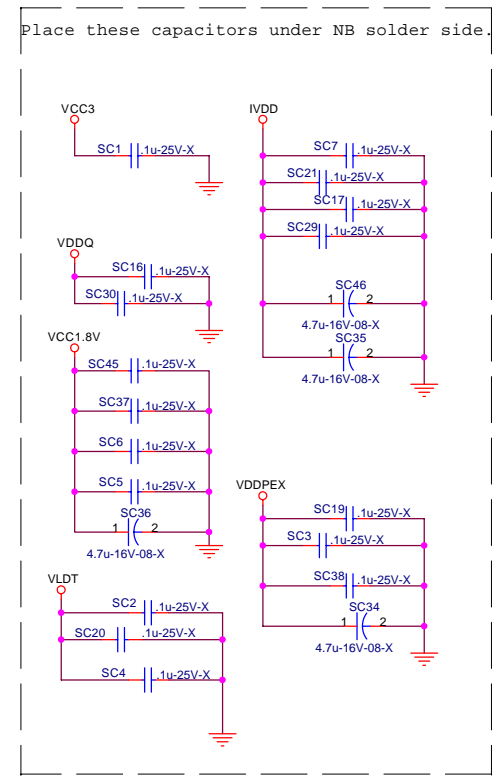
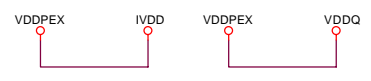
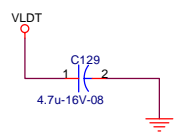
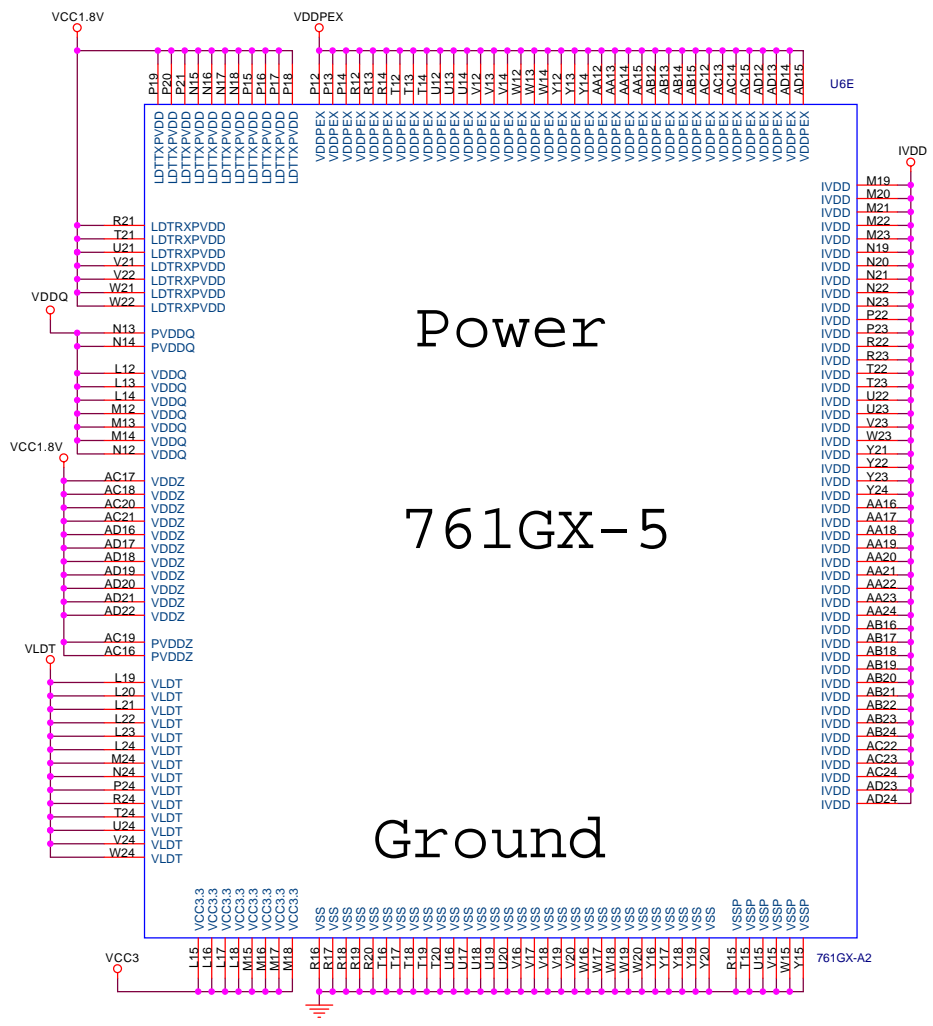
761GX-1

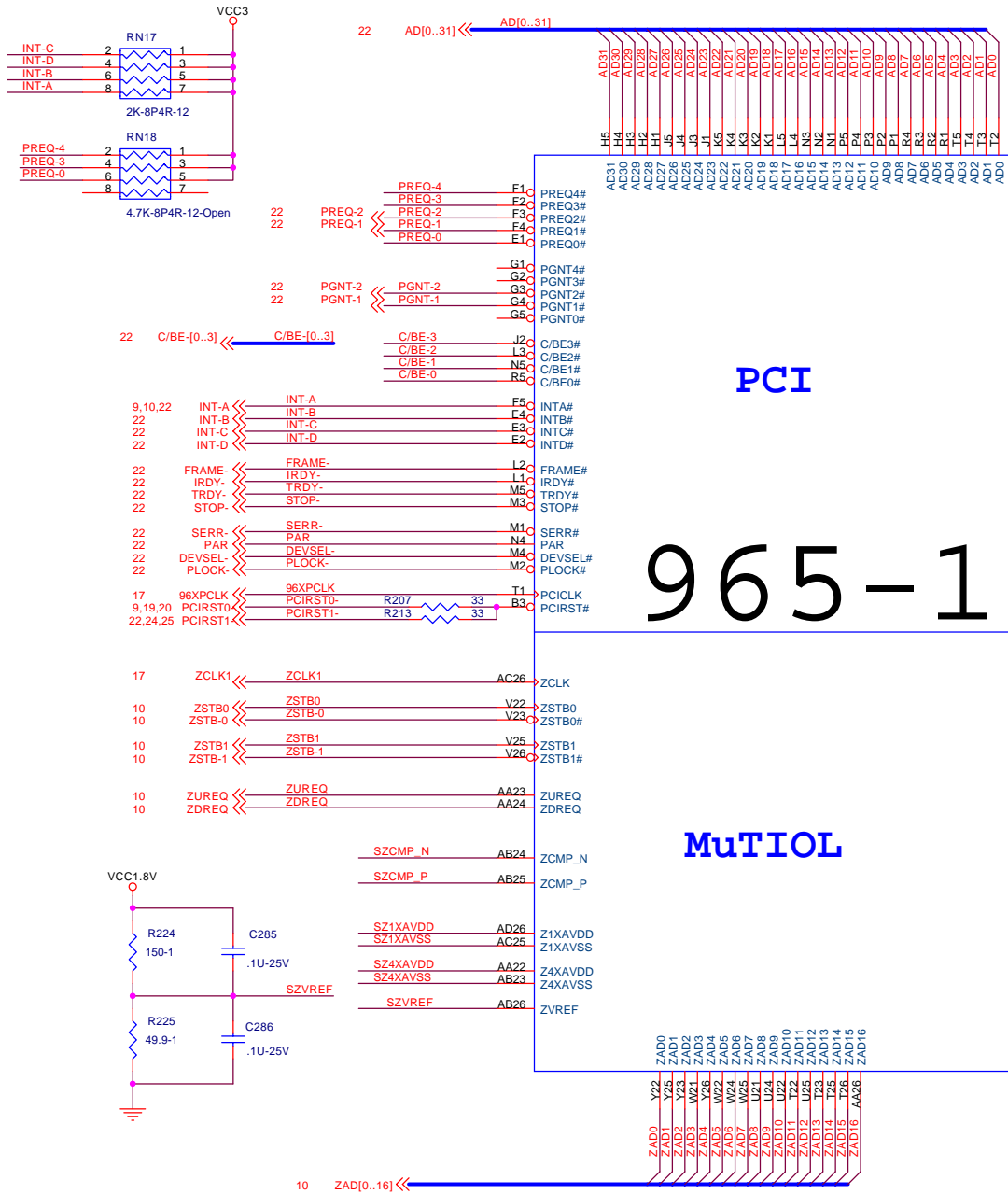
PCI Express_TX

PCI Express_RX







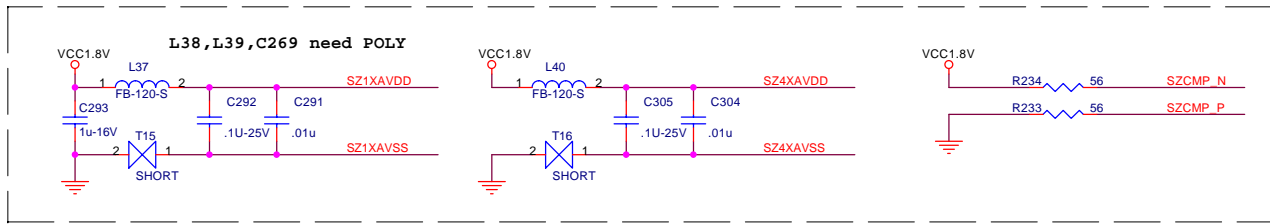
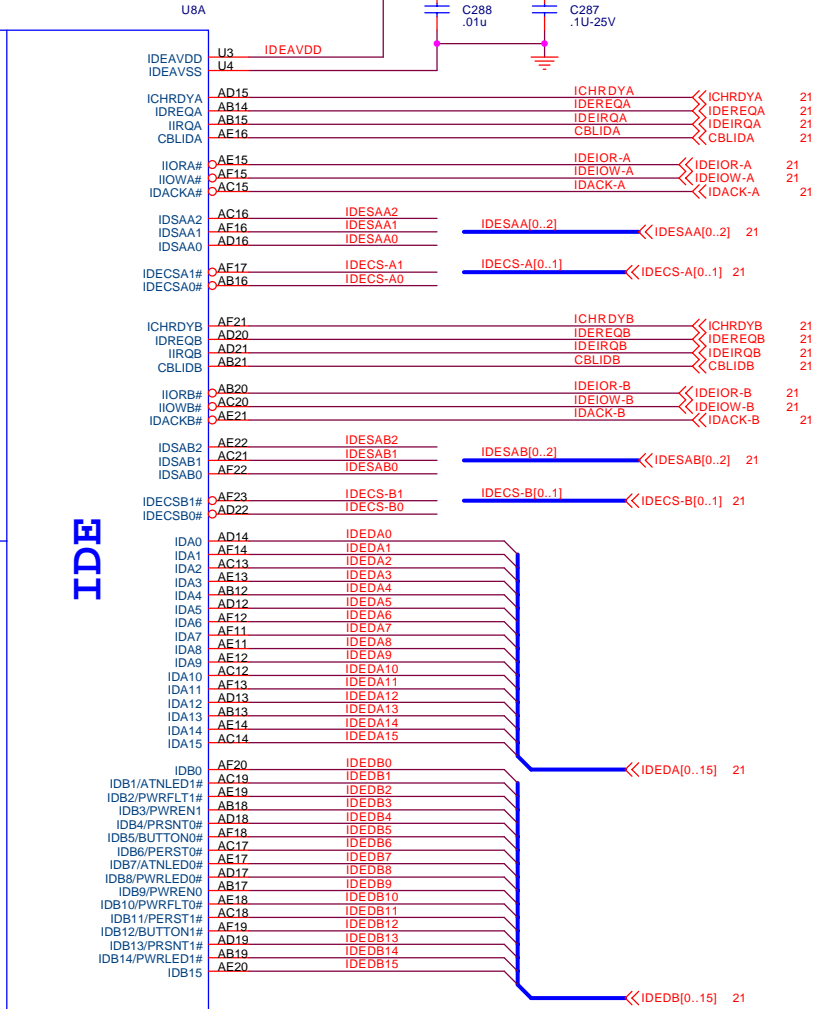


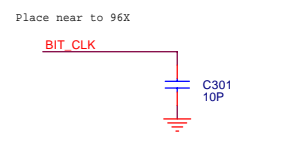
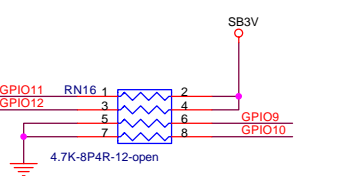
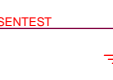
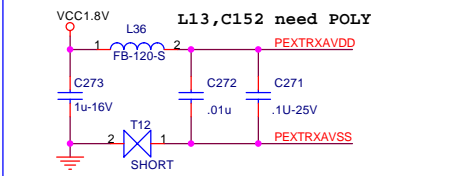
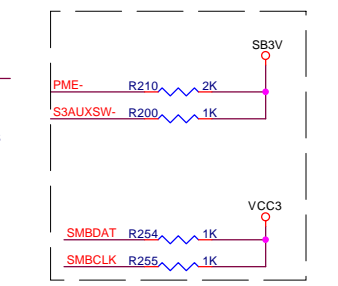
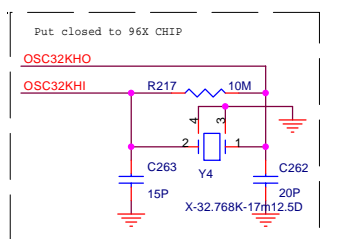
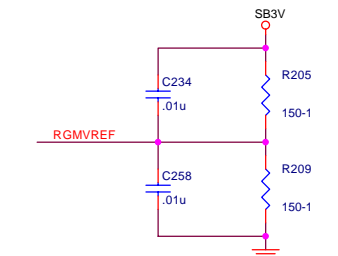
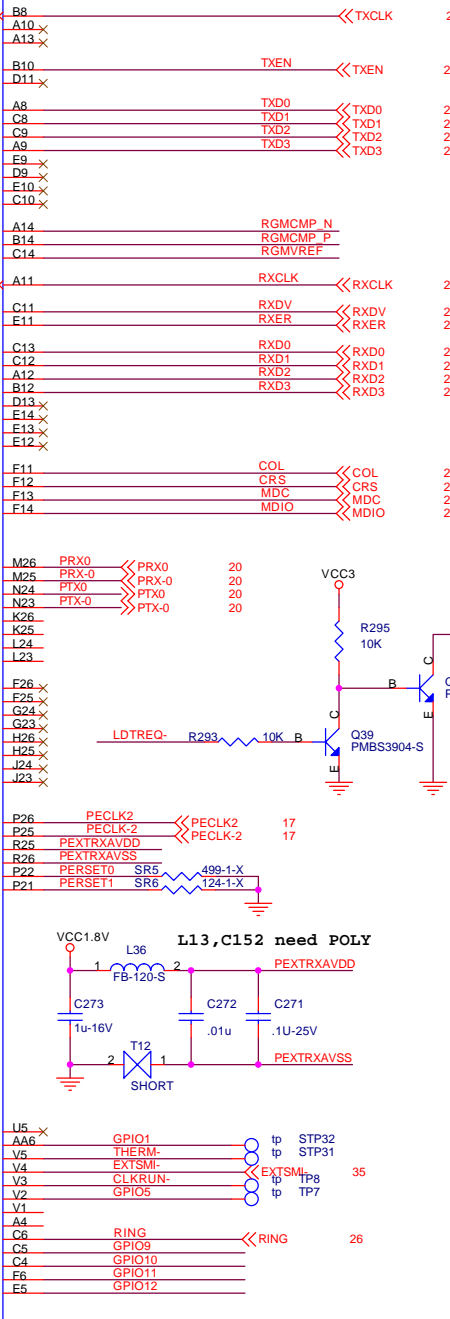
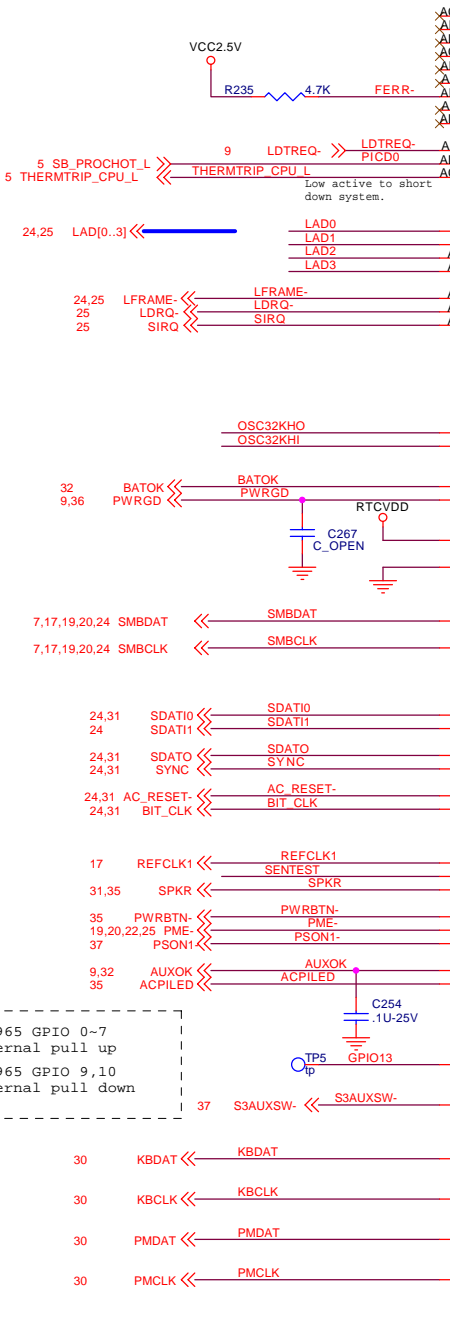
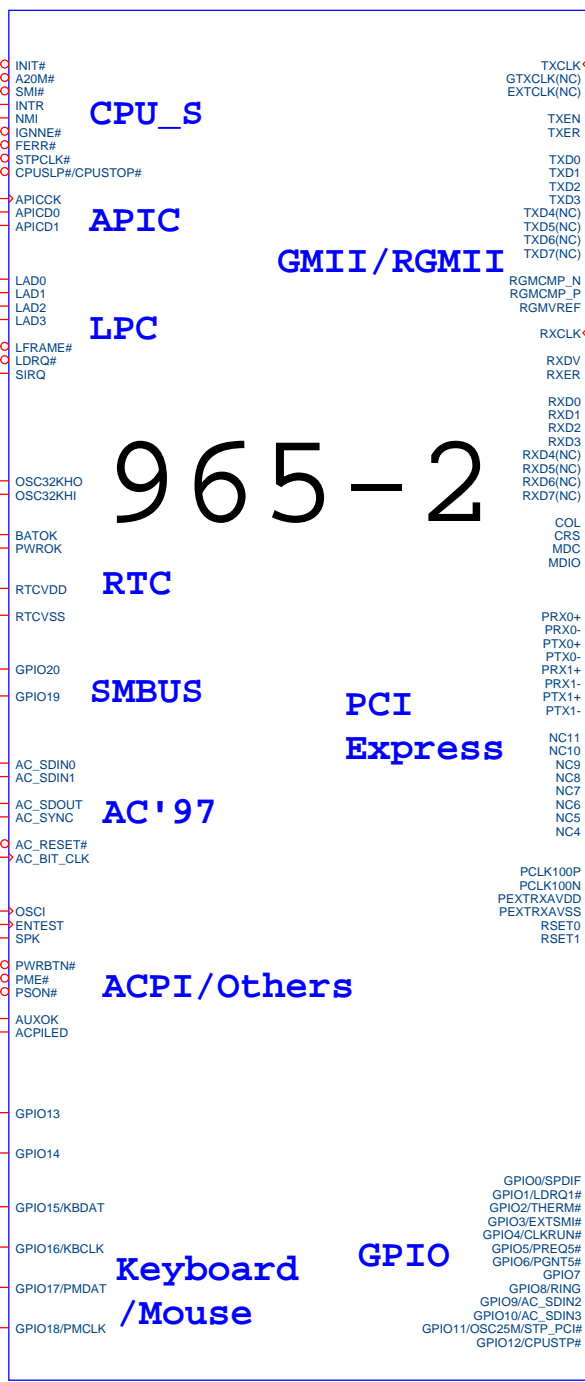
965-1

PCI

MuTIOL

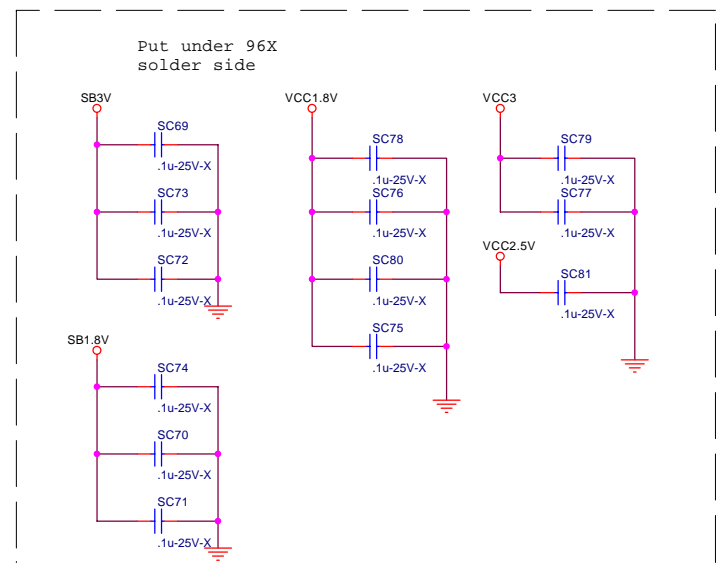
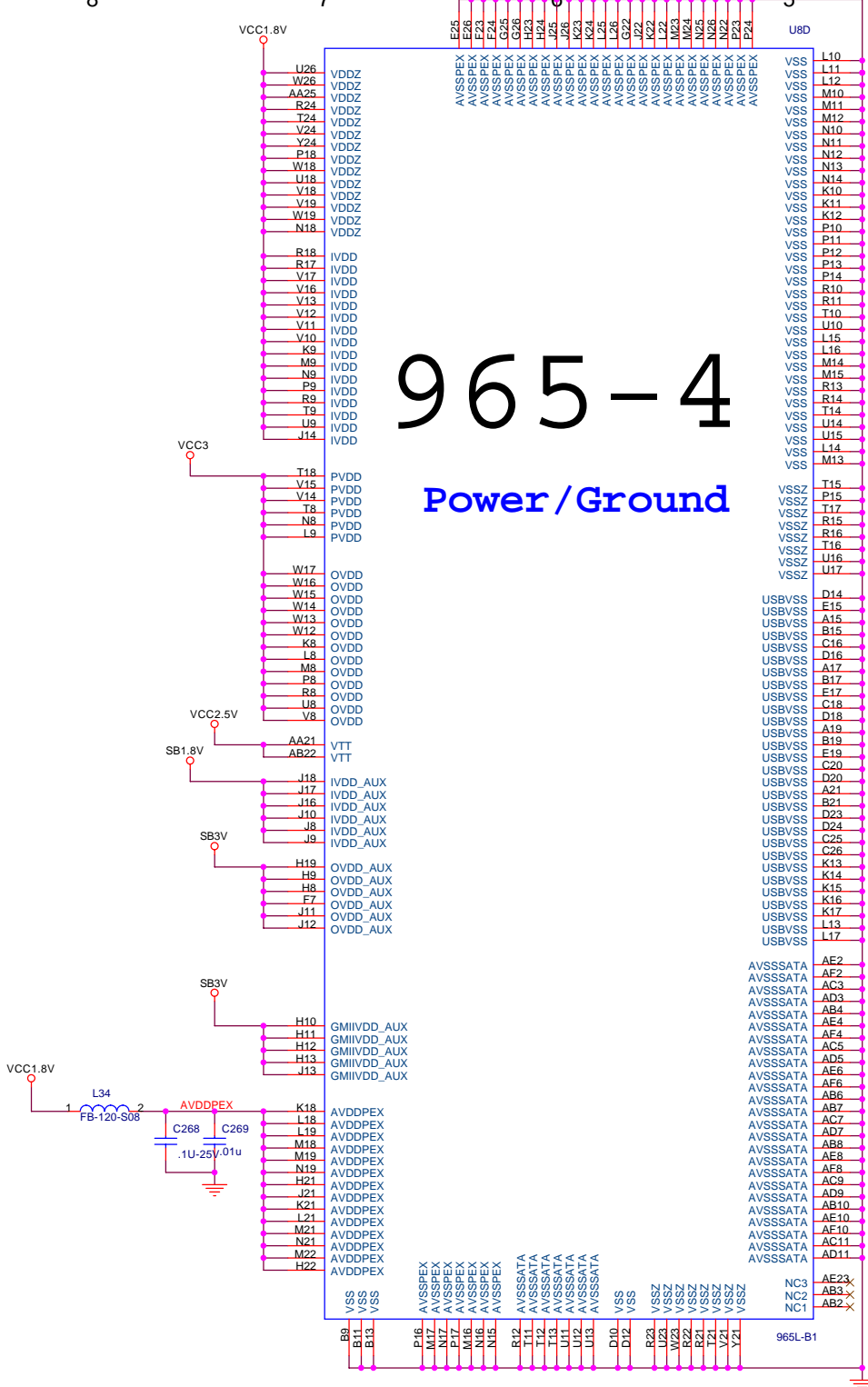
IDE





965-4

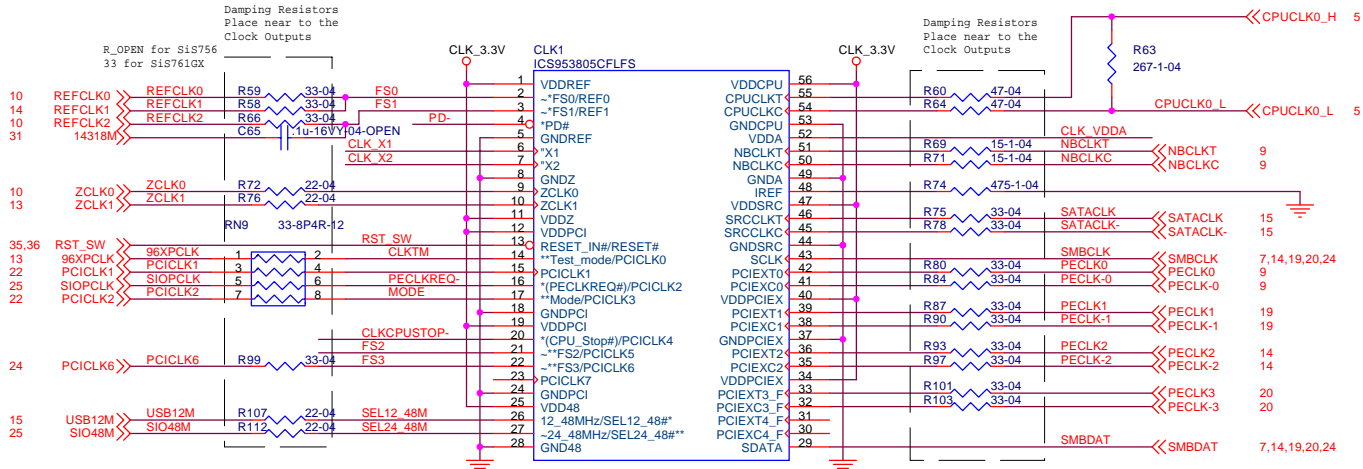
Power / Ground



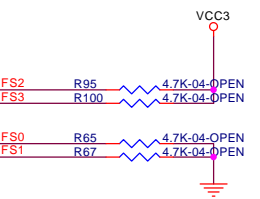
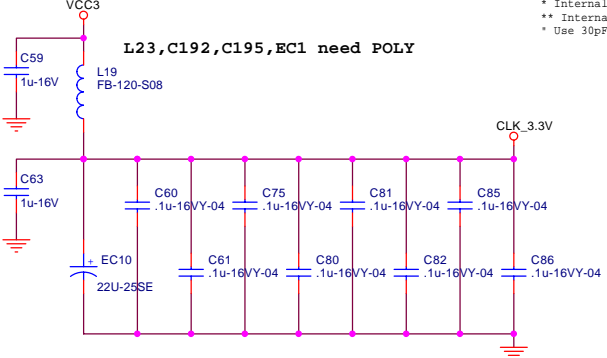
Main Clock Generator

OPTIONS

1. ICS953803



* Internal Pull-Up Resistor
 ** Internal Pull-Down Resistor
 * Use 30pF external capacitance

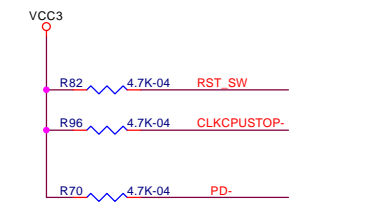
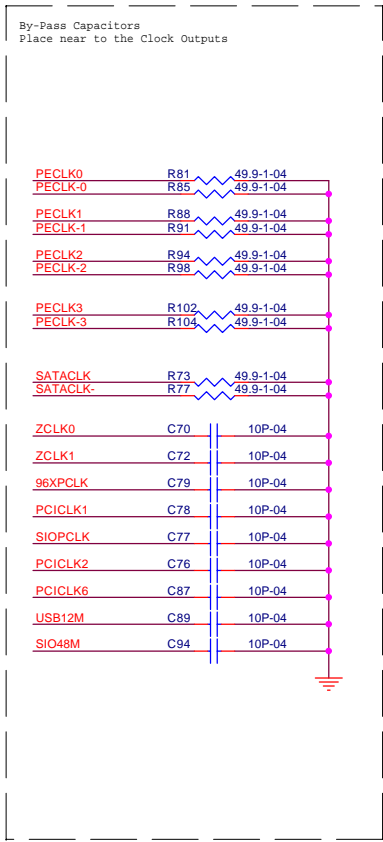


Frequency Selection

Different clock generator with different frequency define table

SIS 756/761GX CLOCK									
(FS3)	(FS2)	(FS1)	(FS0)	CPULCK (MHz)	NbCLK (MHz)	SRC (MHz)	ZCLK (MHz)	PEI-EX (MHz)	PCI (MHz)
0	0	0	0	100.00	100.00	100.00	133.33	100.00	33.33
0	0	1	0	133.33	133.33	100.00	133.33	100.00	33.33
0	0	1	1	166.66	166.66	100.00	133.33	100.00	33.33
0	0	1	1	200.00	200.00	100.00	133.33	100.00	33.33
0	1	0	0	250.00	250.00	100.00	133.33	100.00	33.33
0	1	0	1	266.66	266.66	100.00	133.33	100.00	33.33
0	1	1	0	333.33	333.33	100.00	133.33	100.00	33.33
0	1	1	1	400.00	400.00	100.00	133.33	100.00	33.33
1	0	0	0	100.00	125.00	100.00	133.33	100.00	33.33
1	0	0	1	133.33	166.66	100.00	133.33	100.00	33.33
1	0	1	0	166.66	222.22	100.00	133.33	100.00	33.33
1	0	1	1	200.00	250.00	100.00	133.33	100.00	33.33
1	1	0	0	250.00	333.33	100.00	133.33	100.00	33.33
1	1	0	1	266.66	400.00	100.00	133.33	100.00	33.33
1	1	1	0	333.33	500.00	100.00	133.33	100.00	33.33
1	1	1	1	100.00	125.00	100.00	133.33	100.00	33.33

SIS 756/761GX CLOCK									
(FS3)	(FS2)	(FS1)	(FS0)	CPULCK (MHz)	NbCLK (MHz)	SRC (MHz)	ZCLK (MHz)	PCI-EX (MHz)	PCI (MHz)
0	0	0	0	133.33	166.66	100.00	133.33	100.00	33.33
0	0	0	1	166.66	222.22	100.00	133.33	100.00	33.33
0	0	1	0	200.00	250.00	100.00	133.33	100.00	33.33
0	0	1	1	250.00	333.33	100.00	133.33	100.00	33.33
0	1	0	0	266.66	400.00	100.00	133.33	100.00	33.33
0	1	0	1	333.33	500.00	100.00	133.33	100.00	33.33
0	1	1	0	134.66	134.66	100.00	134.66	101.00	33.66
0	1	1	1	168.33	168.33	100.00	134.66	101.00	33.66
1	0	0	0	202.00	202.00	100.00	134.66	101.00	33.66
1	0	0	1	252.50	252.50	100.00	134.66	101.00	33.66
1	0	1	0	134.66	168.33	100.00	134.66	101.00	33.66
1	0	1	1	168.33	224.44	100.00	134.66	101.00	33.66
1	1	0	0	202.00	252.50	100.00	134.66	101.00	33.66
1	1	0	1	252.50	336.66	100.00	134.66	101.00	33.66
1	1	1	0	206.00	206.00	100.00	137.33	103.00	34.33
1	1	1	1	206.00	257.50	100.00	137.33	103.00	34.33

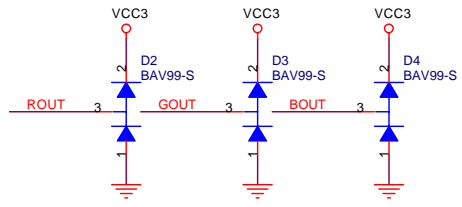
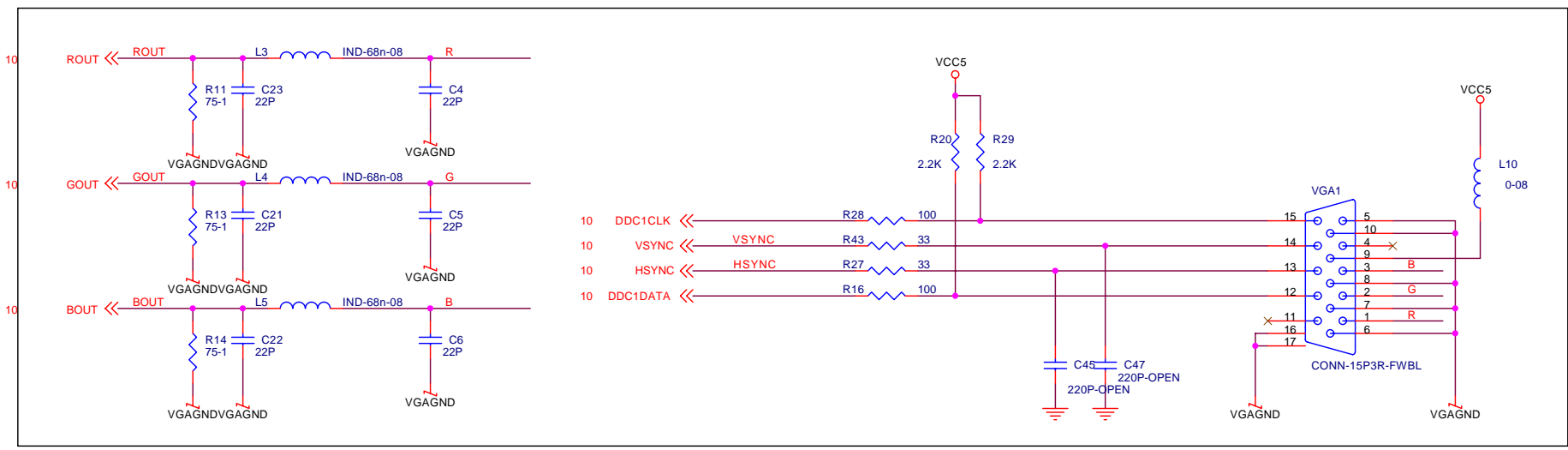



Elitegroup Computer Systems

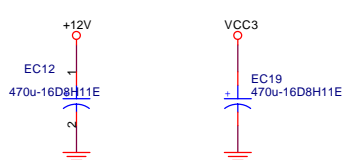
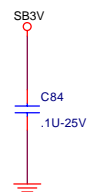
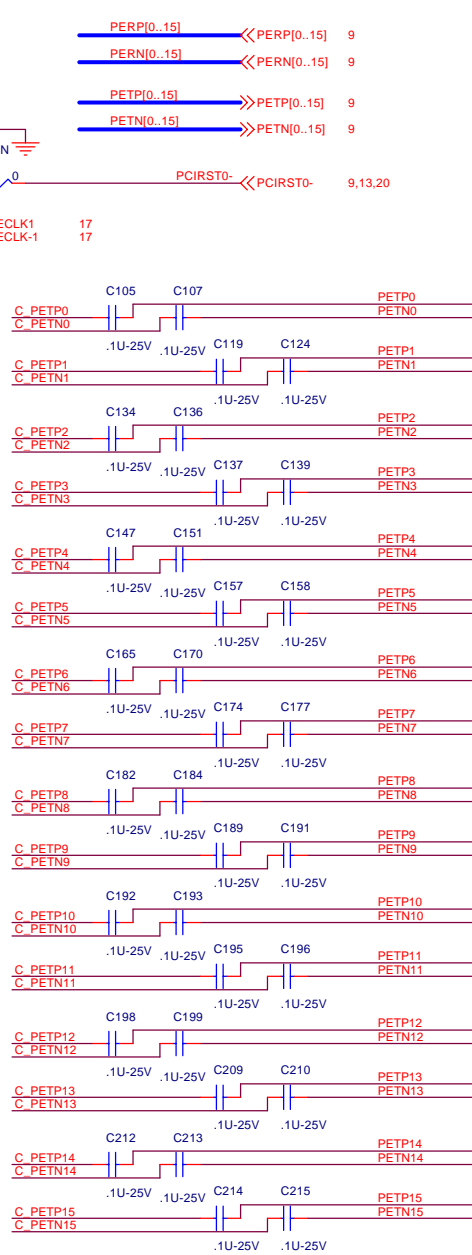
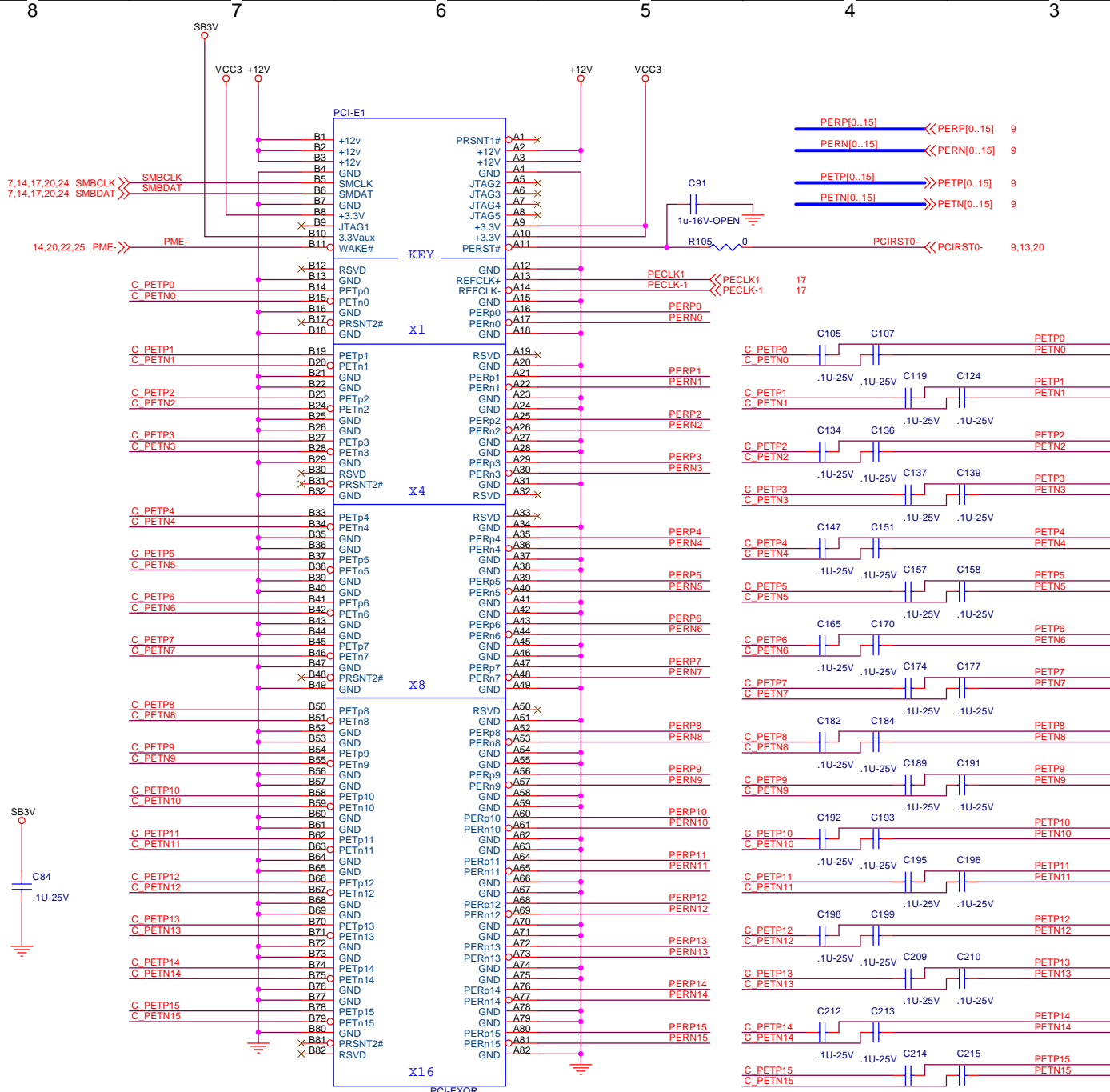
Title: **Clock Generator**

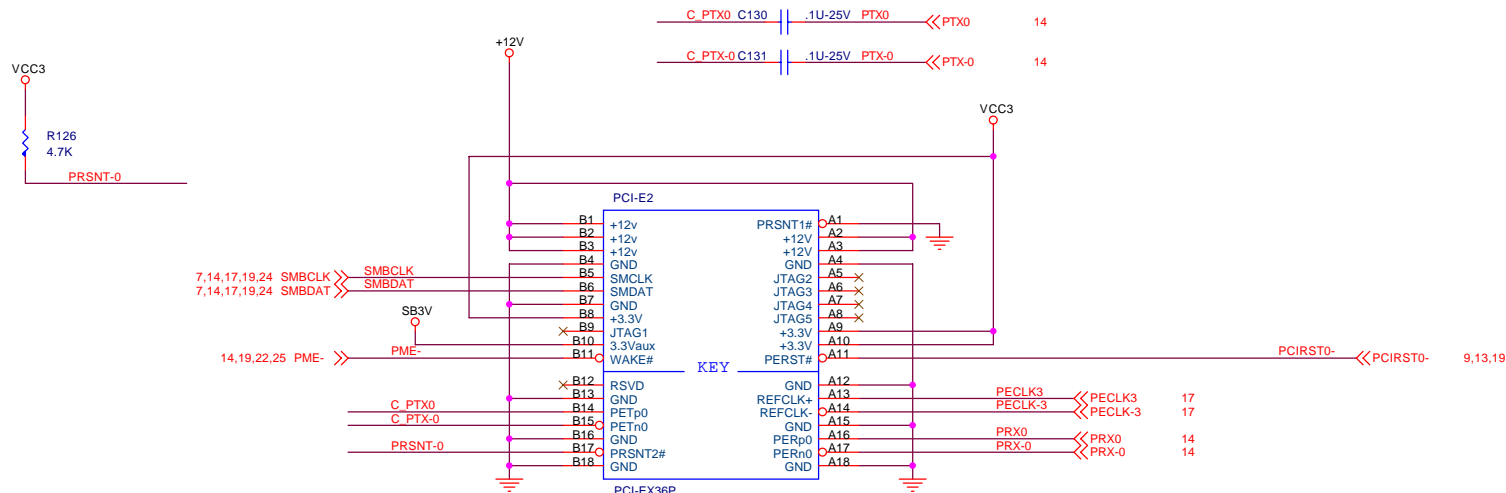
Size: Custom | Document Number: **A33G** | Rev: 1.0

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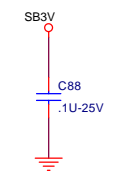
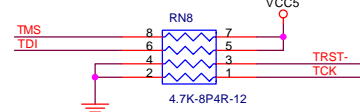
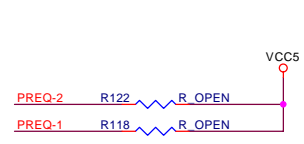
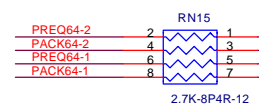
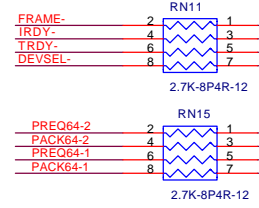
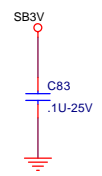
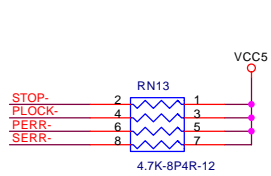
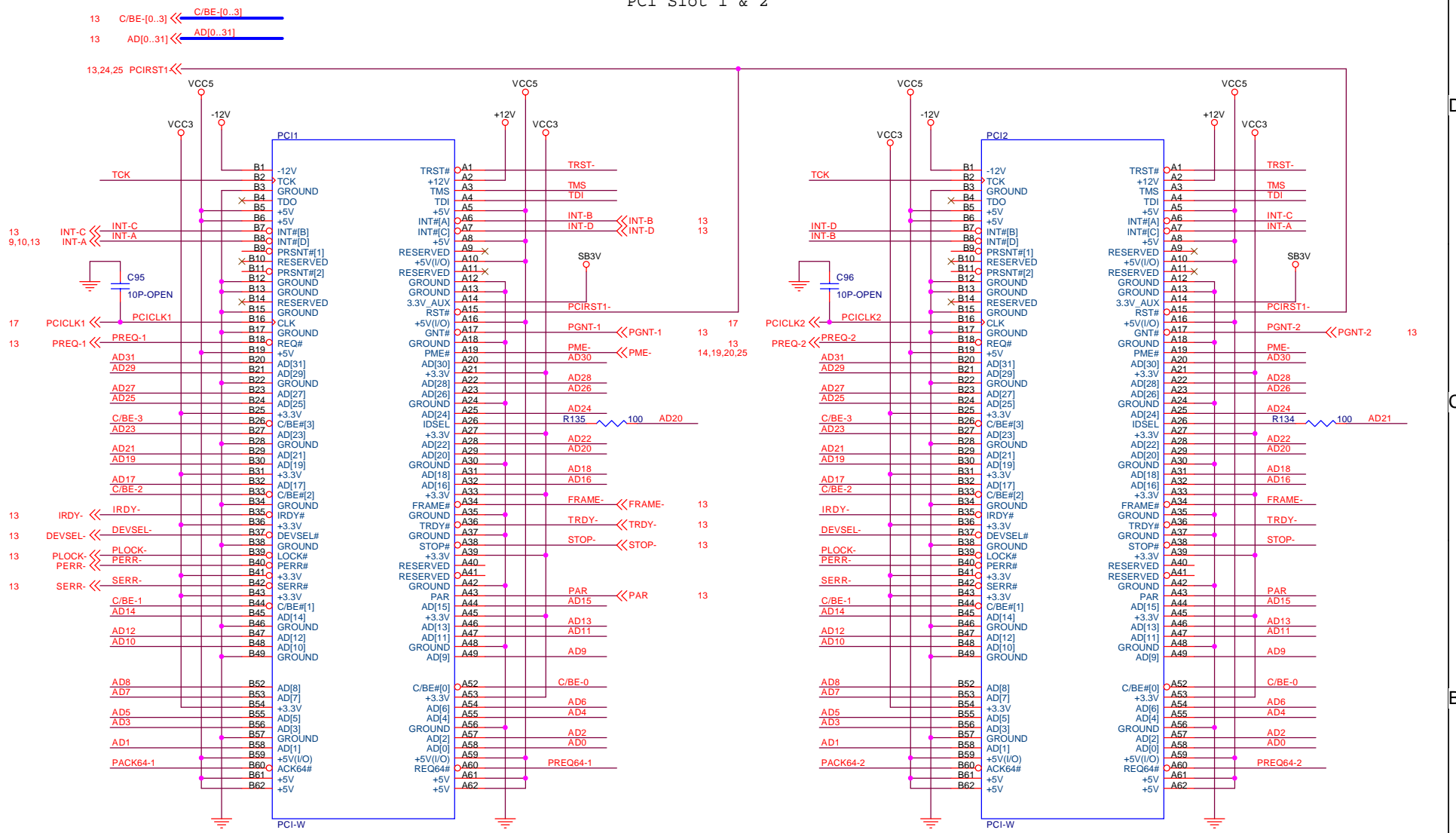


 Elitegroup Computer Systems		Title	
		VGA CONNECTOR	
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PCI Slot 1 & 2

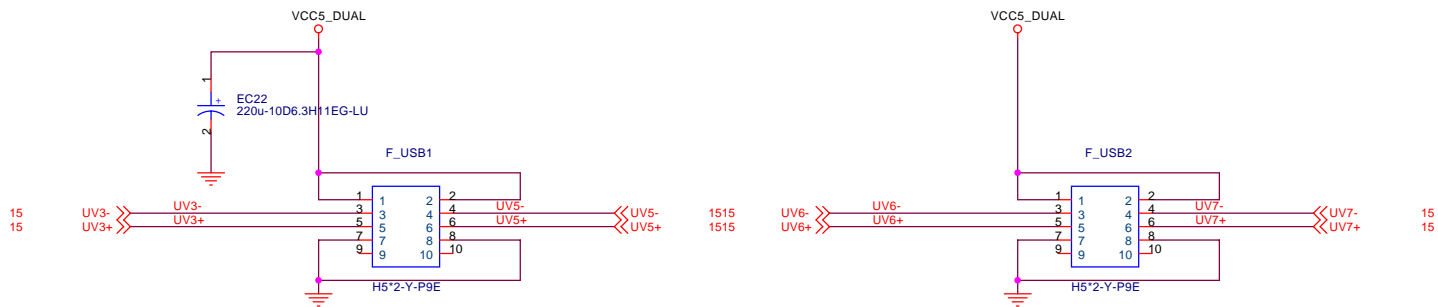
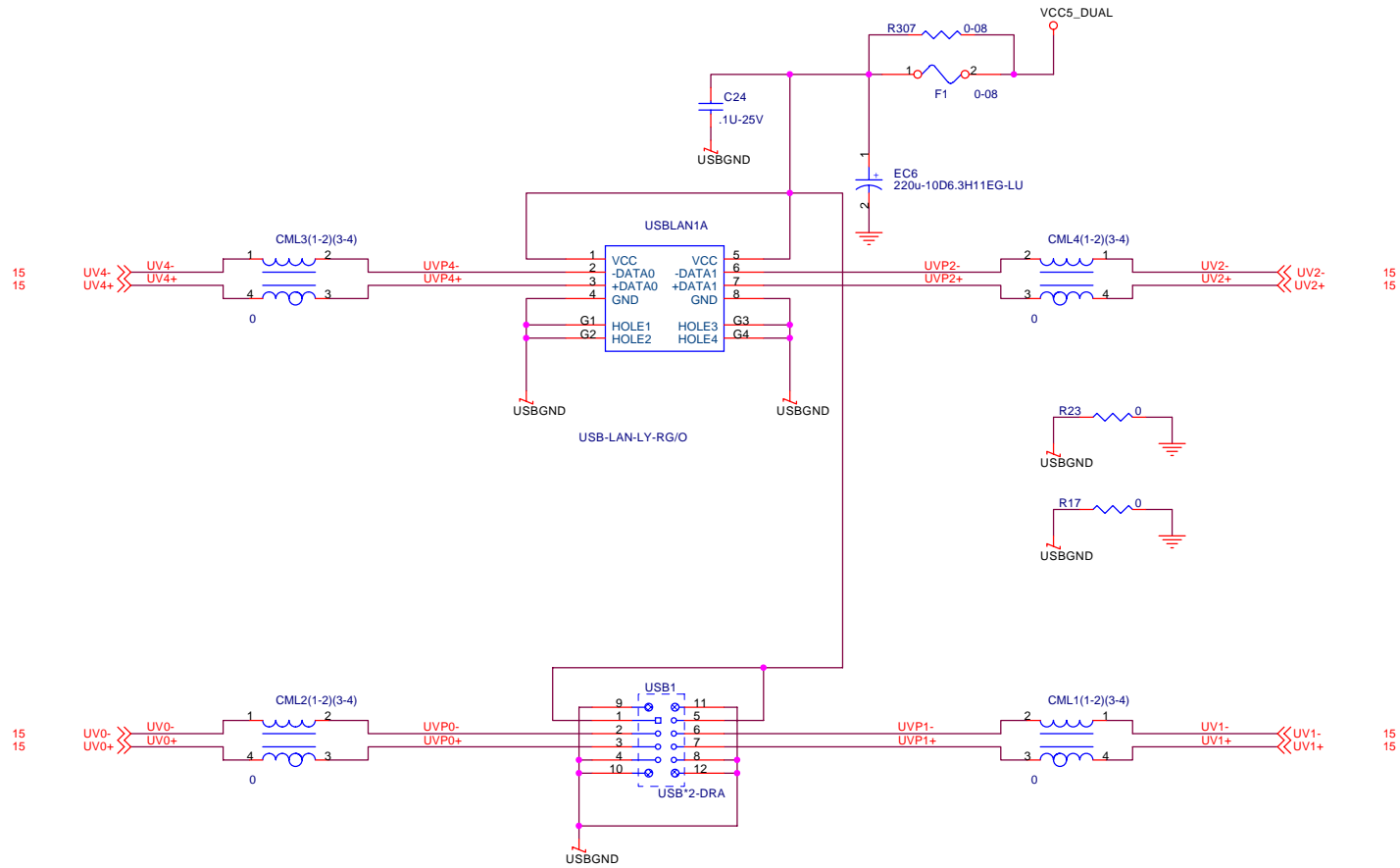


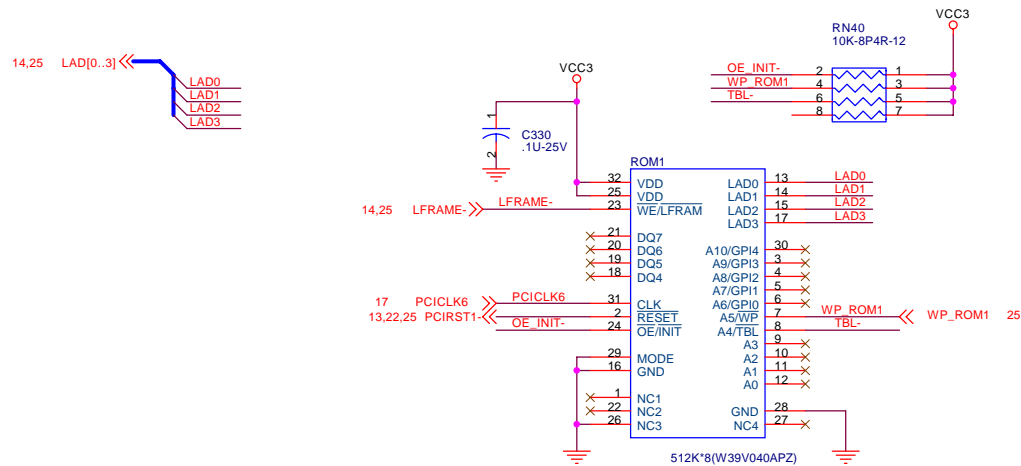
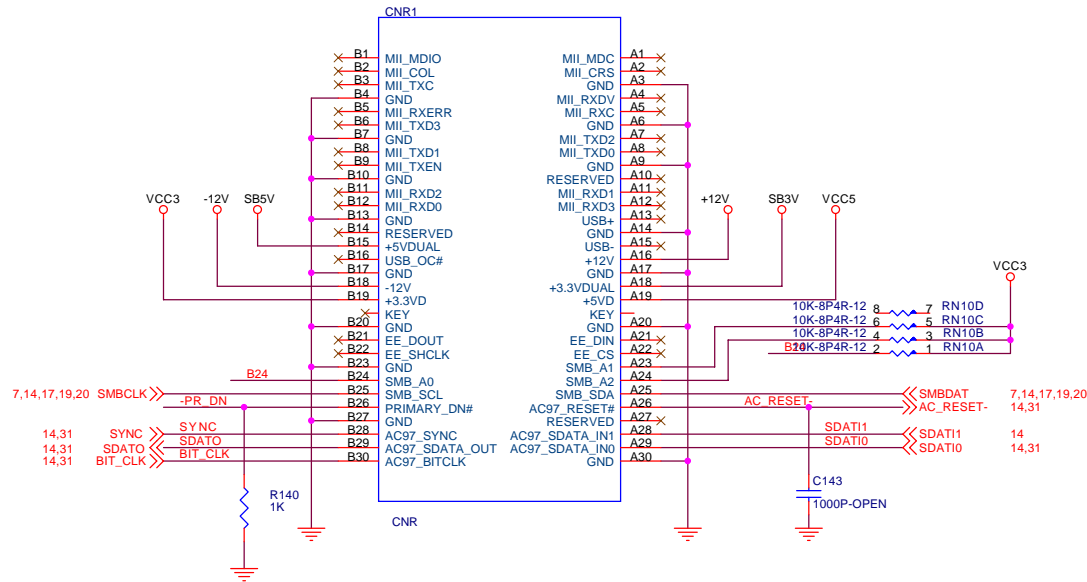
FCS Elitegroup Computer Systems

Title: PCI Slot 1 and 2

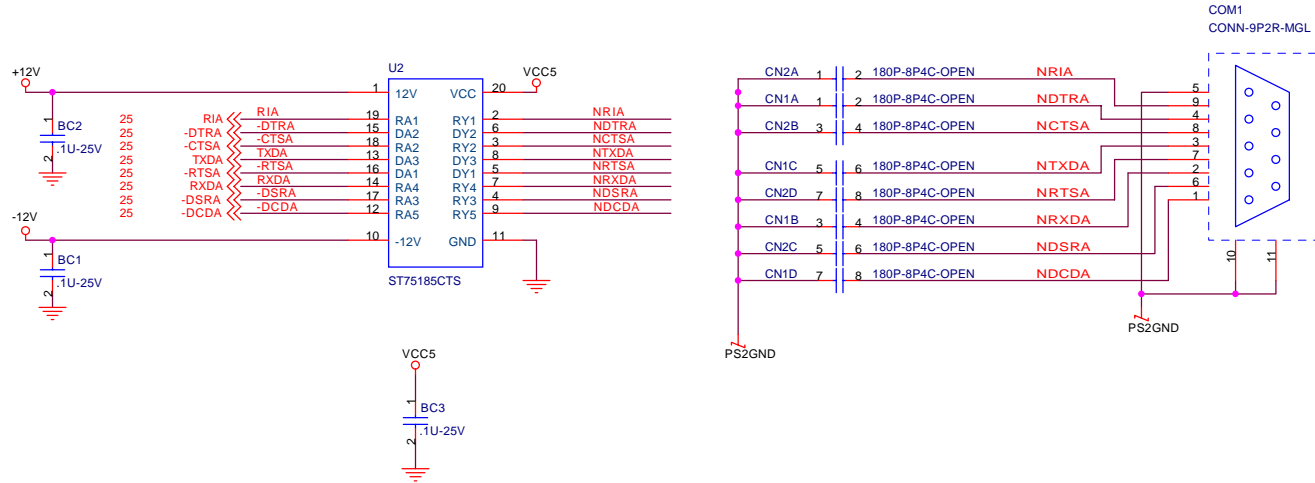
Size: Custom Document Number: A33G Rev: 1.0

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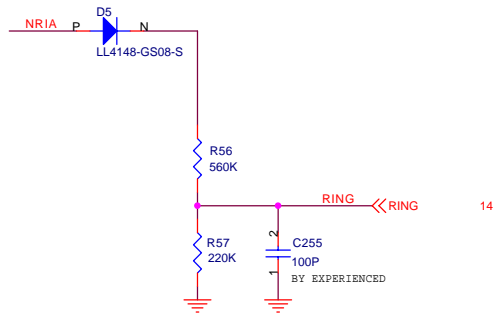




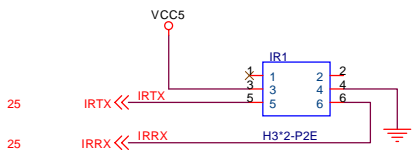
COM



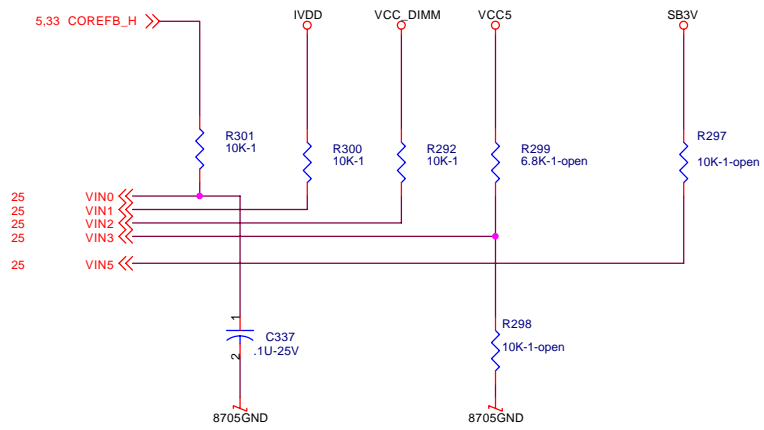
FOR MODEM WAKE-UP FUNCTION



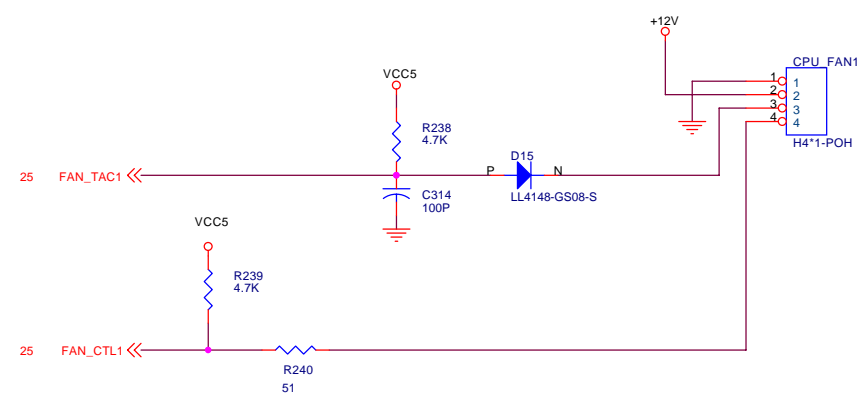
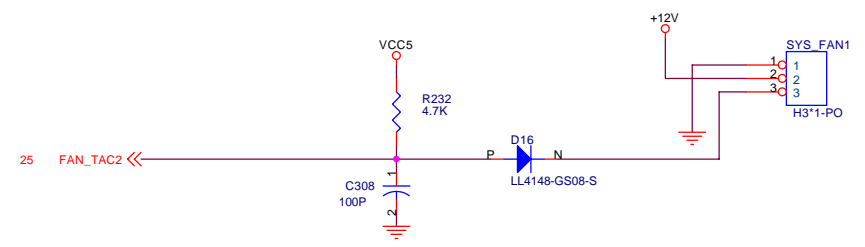
IR CONNECTOR



Voltage Monitor

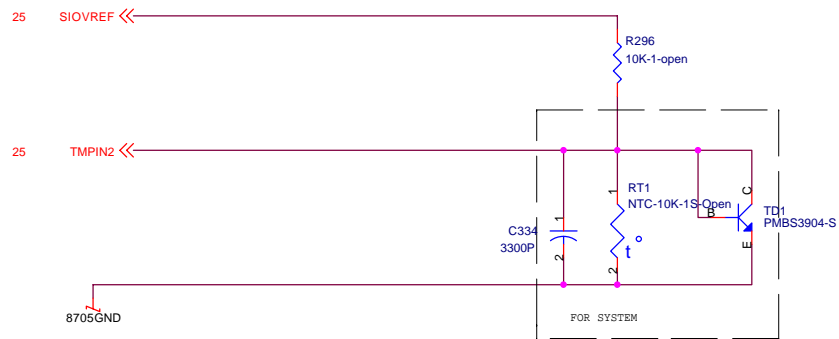


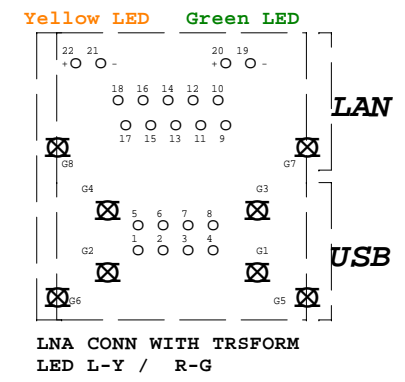
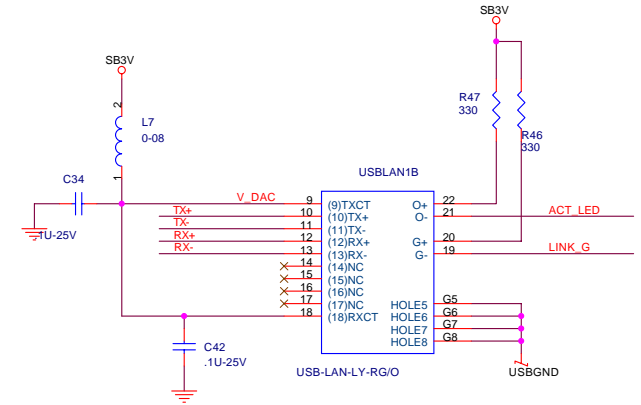
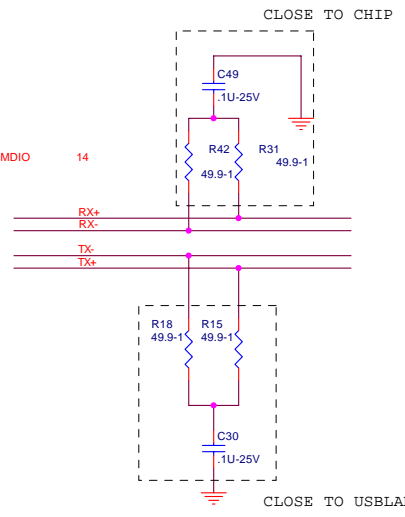
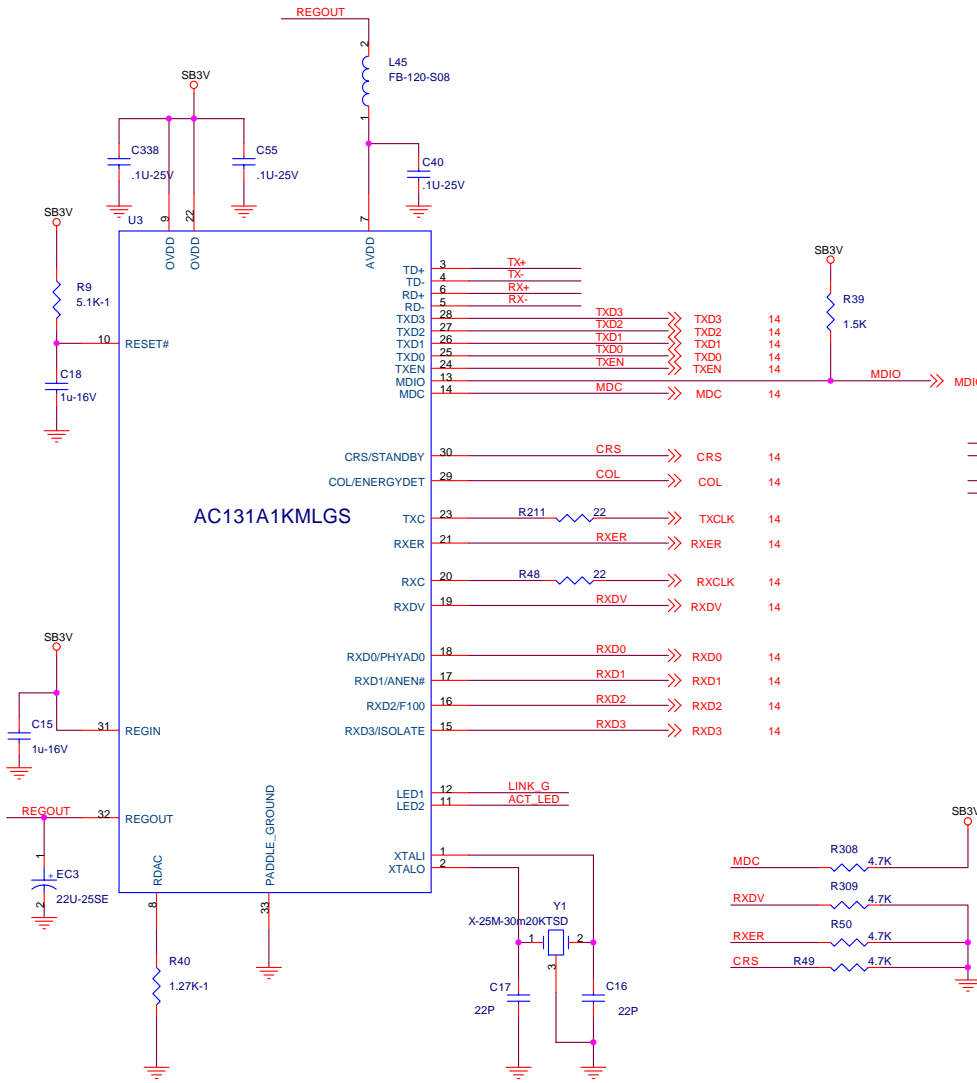
FAN Input and Output

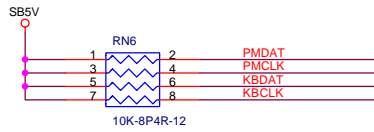


Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode

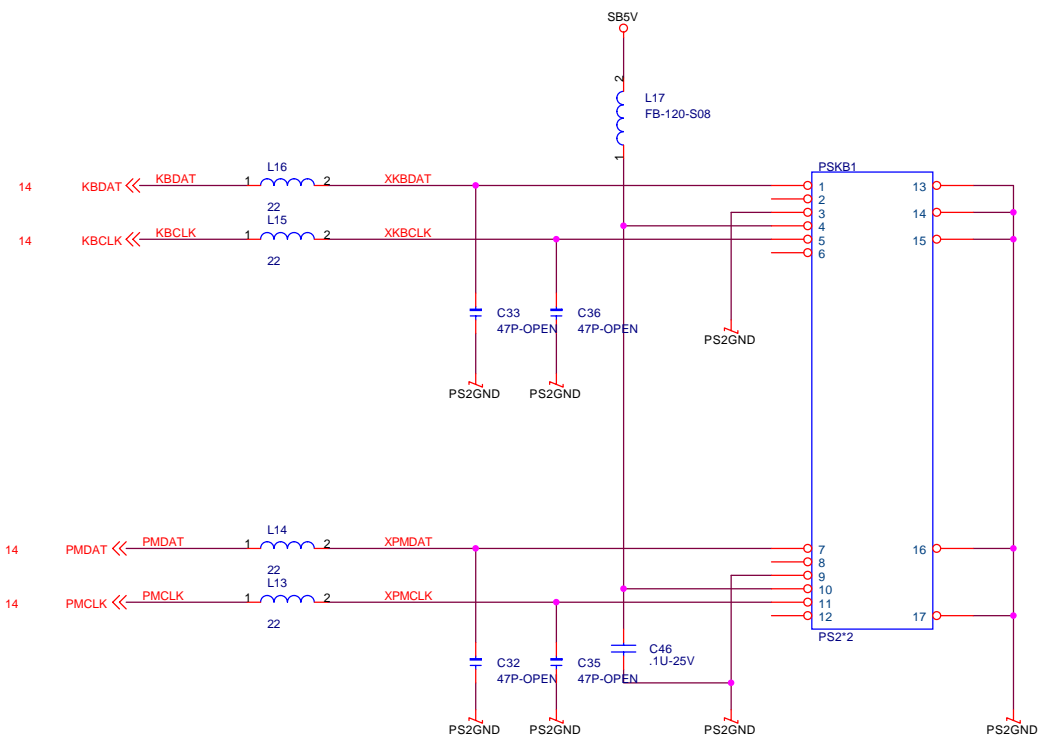




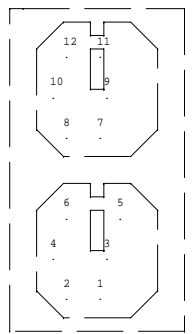


North Bridge Hardware Trap

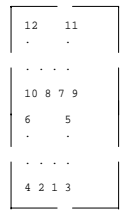
Symbol	Description	Default
DLLCN-	CPUCCLK/SCLK PLL/DLL Circuit Enable 1: Disable 0: Enable	Internal Pull Down
TMODE0	Internal Test Modes 1: Test Mode 0: Normal	Internal Pull Down
TMODE1	Test Mode Selection 1: Mode 1 0: Mode 0	Internal Pull Down
TMODE2	Test Mode Enable 1: Enable 0: Disable	Internal Pull Down
TRAP[1..0]	NB ASLCLK Request Select 00: 133 MHz 01: 166/200 MHz 10: 66 MHz 11: 100 MHz	Internal Pull Down
TRAP2	NB ASL Serial Mode Initialization Enable 1: Packet mode 0: Serial mode	Internal Pull Down
TRAP[4..3]	Reserved	Internal Pull Down
TRAP5	PCIE PLL Bypass	Internal Pull Down
TRAP6	PCIE Symlock Test	Internal Pull Down
TRAP[8..7]	PCIE TX Fix Out	Internal Pull Down
TRAP[11..9]	Trap PLLLX Frequency Ratio Ratio 0 Ratio 1 000: divide 1 / divide 1 001: divide 2 / divide 2 010: divide 3 / divide 3 011: divide 4 / divide 4 100: divide 4 / divide 5	Internal Pull Down
TRAP[13..12]	Trap PLL2X Gain 00: PLL2X 200MHz 10: PLL2X 800MHz 11: PLL2X 1000MHz	Internal Pull Down
TRAP14	HyperTransport PLL Frequency Ratio Select 0: by logic decoded 1: by trapped	Internal Pull Down
TRAP15	HyperTransport PLL Gain Select 0: by logic decoded 1: by trapped	Internal Pull Down
TRAPA[1..0]	Trap PLL2X Frequency Ratio 0 00: divide 1 01: divide 2 10: divide 3 11: divide 4	Internal Pull Down
TRAPA[4..2]	Trap PLL2X Frequency Ratio 1 000: divide 1 001: divide 2 010: divide 3 011: divide 4 100: divide 5	Internal Pull Down
TRAPA[6..5]	TRAP PLLLX Gain 10: PLLLX 200MHz 11: PLLLX 250MHz (Recom. Value: 10)	Internal Pull Down
TRAPA7	For Internal Test	Internal Pull Down



CONNECTOR VIEW



TOP VIEW



	0	1	Default	internal pull-low (30-50K Ohm)
SPKR(First Flash Memory cycle type selection) LPC Memory Cycle			0	Yes
SDATO(Trap from)	ROM	PCI AD	0	Yes
OC45-(SB debug mode)	enable	disable	1	No

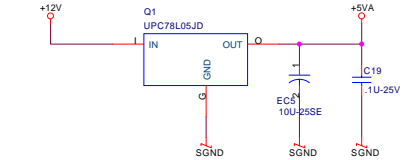
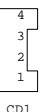
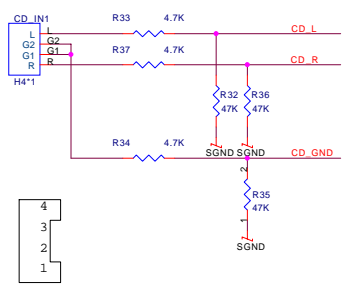
NOTE:
SIS IS NOT RESPONSIBLE FOR ANY ERRORS OR OMISSIONS IN THESE SCHEMATICS. THIS IS AN EXAMPLE ONLY.

Elitegroup Computer Systems

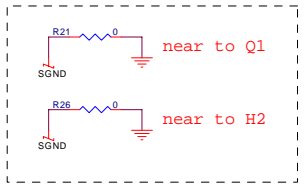
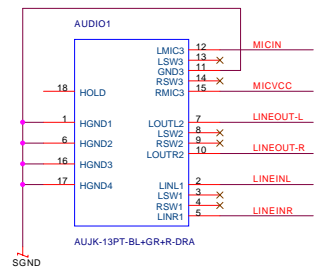
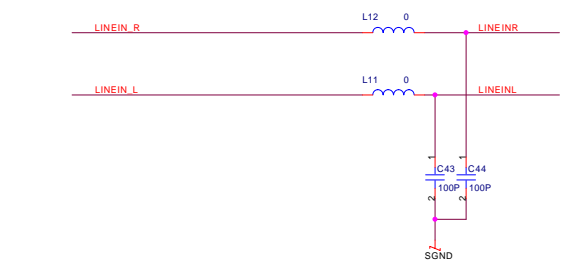
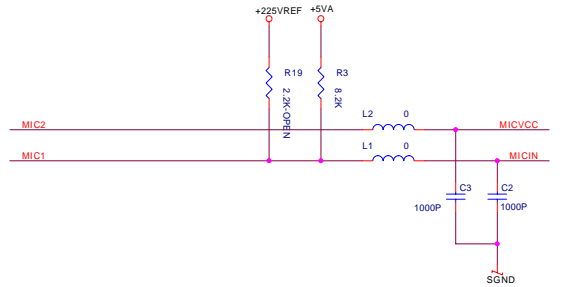
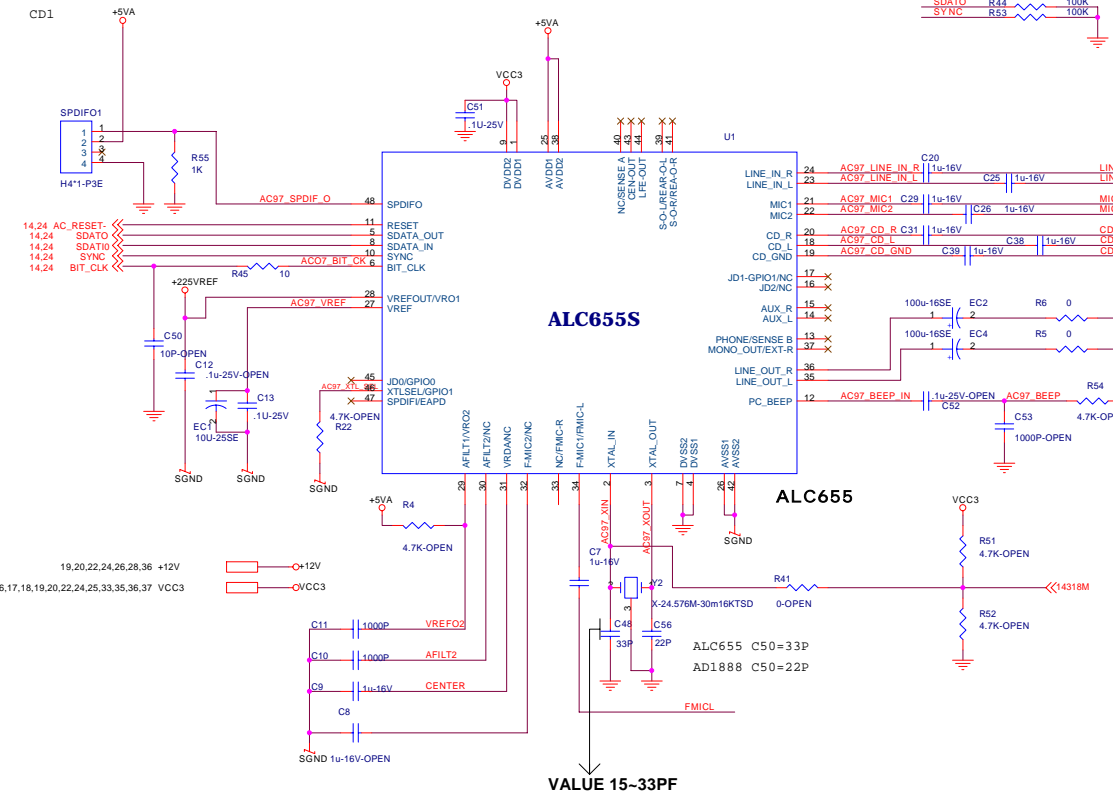
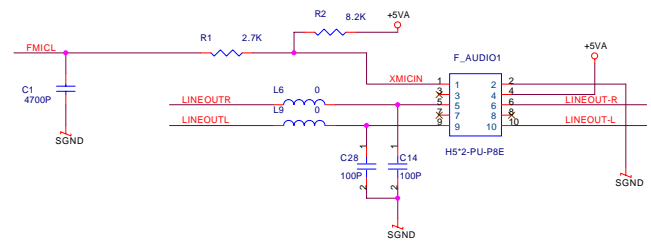
Title: **KEYBOARD & MOUSE CONNECTORS**

Size: Custom Document Number: **A33G** Rev: 1.0

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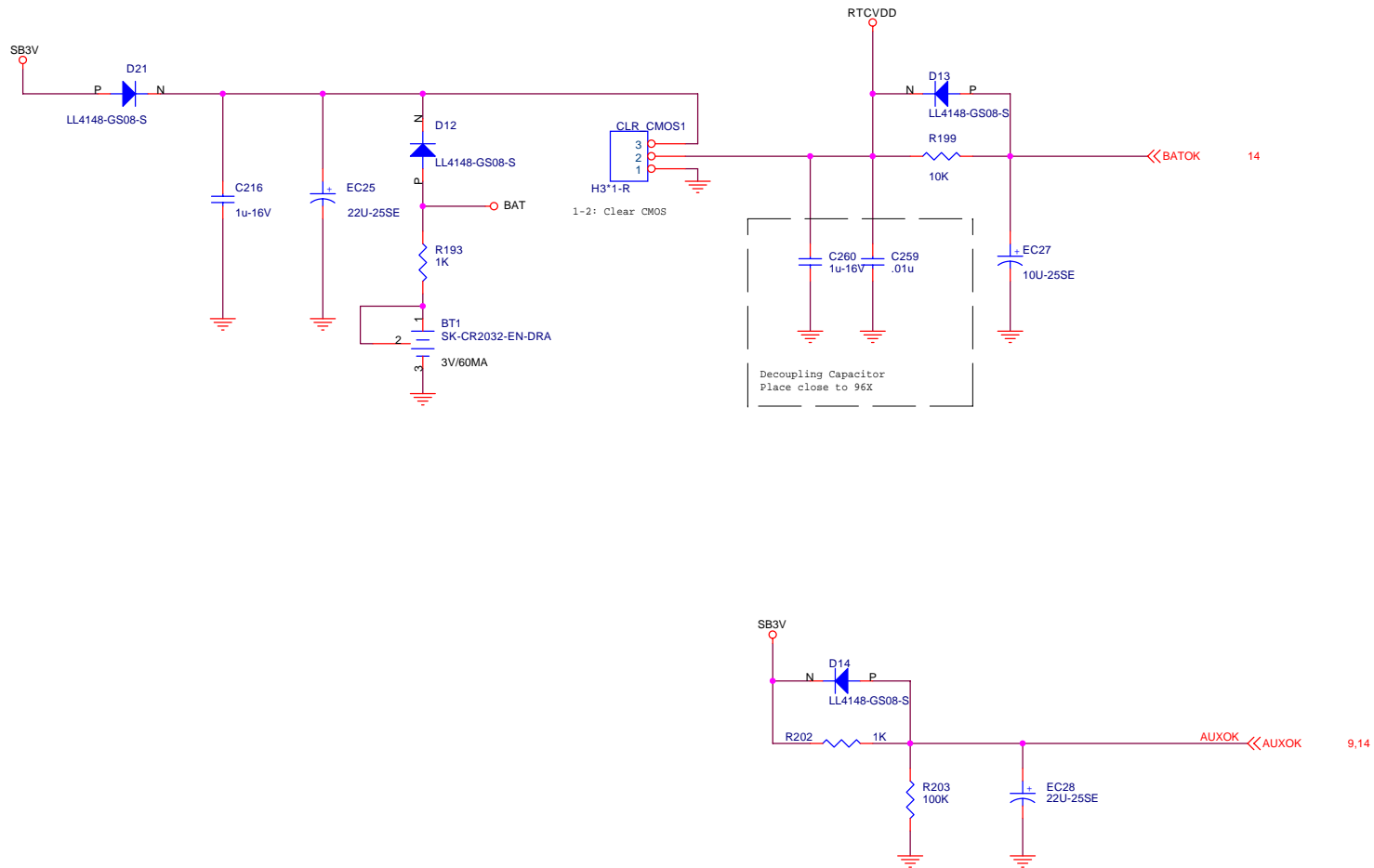
請在 INNER Q1 PIN 2 的地方留一 >90 mils 的通道...GND = SGND

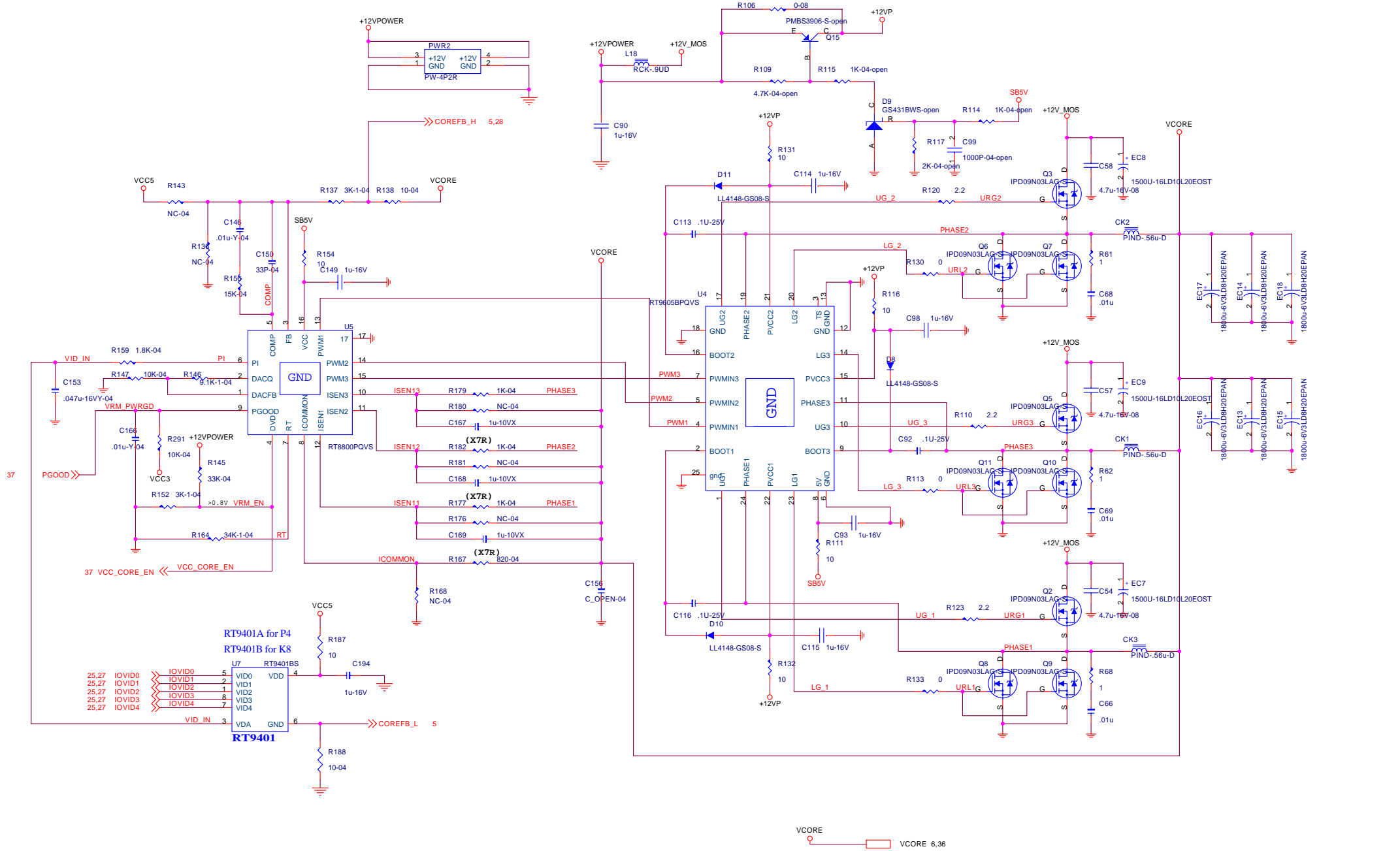


RTC

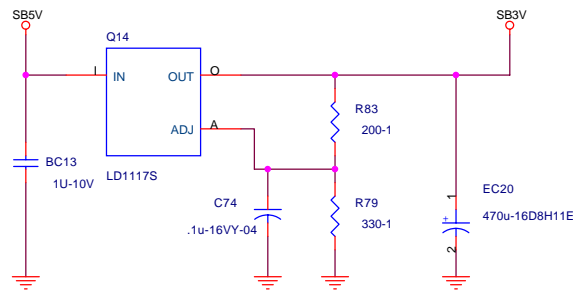
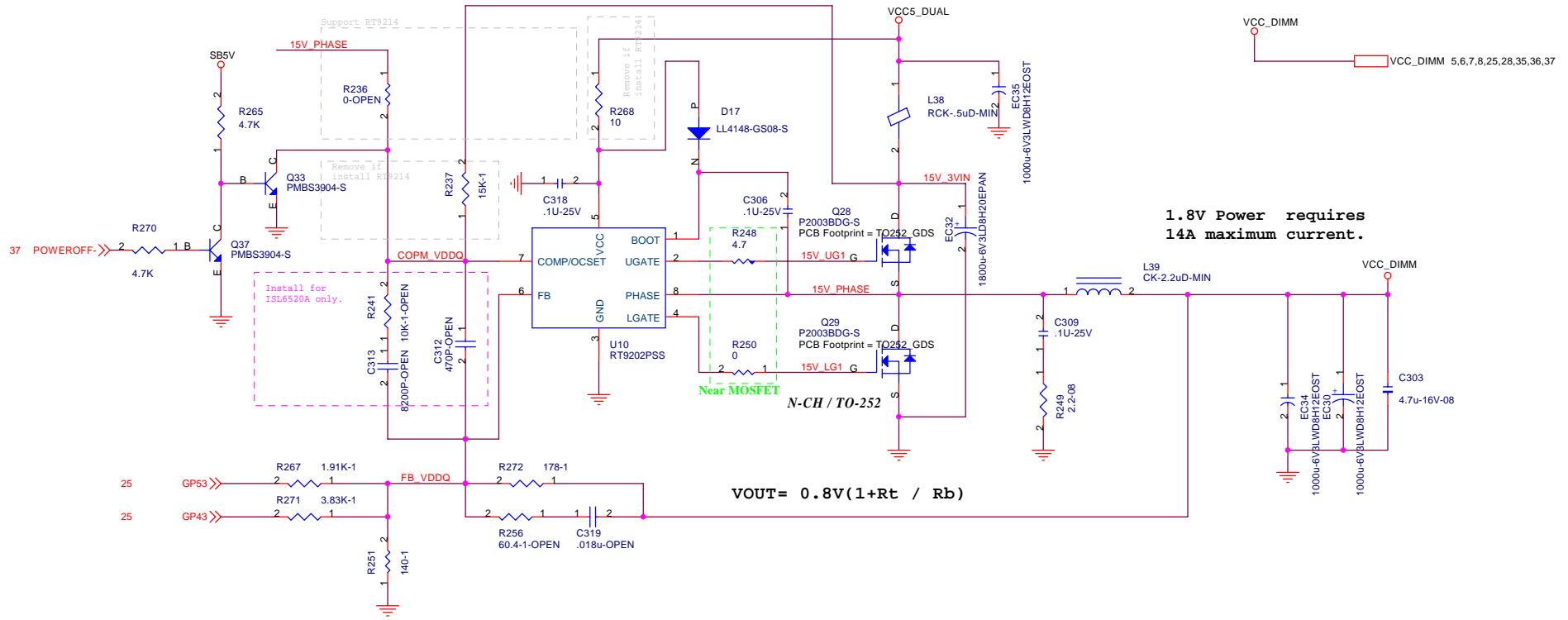
NOTE!

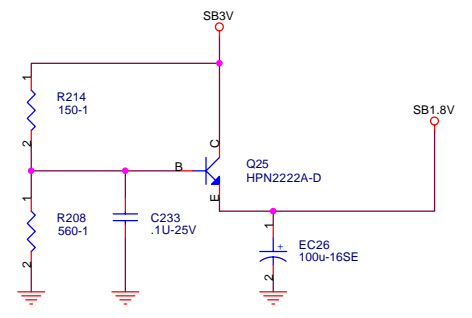
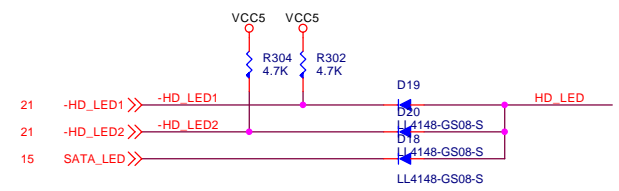
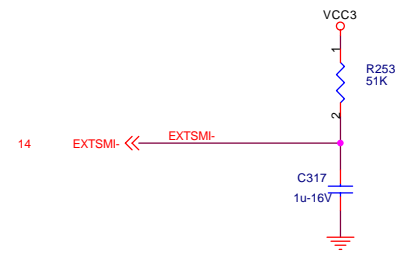
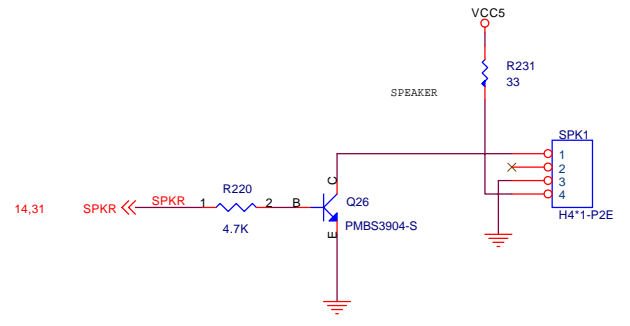
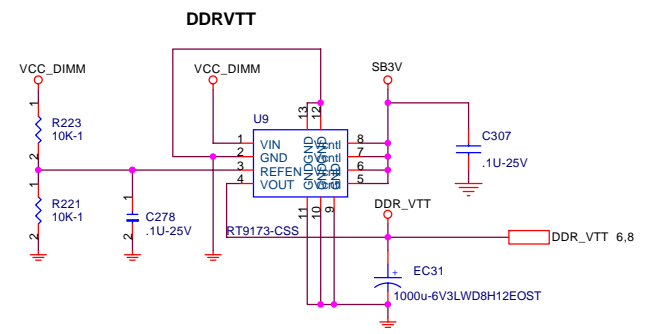
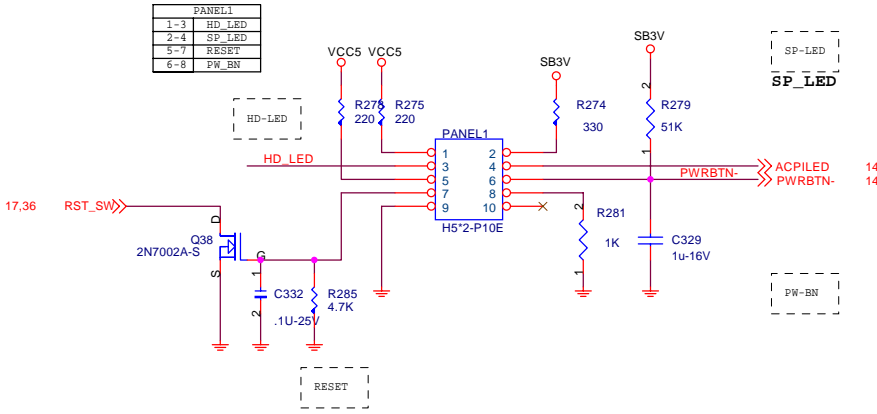
- 1.The RTCVDD is 3V
 - 2.Decoupling capacitor must be close to 965 RTCVDD pin.
 - 3.RTC circuit must strictly follow SiS's recommended design
- SiS is not responsible for RTC problems from foreign designs.

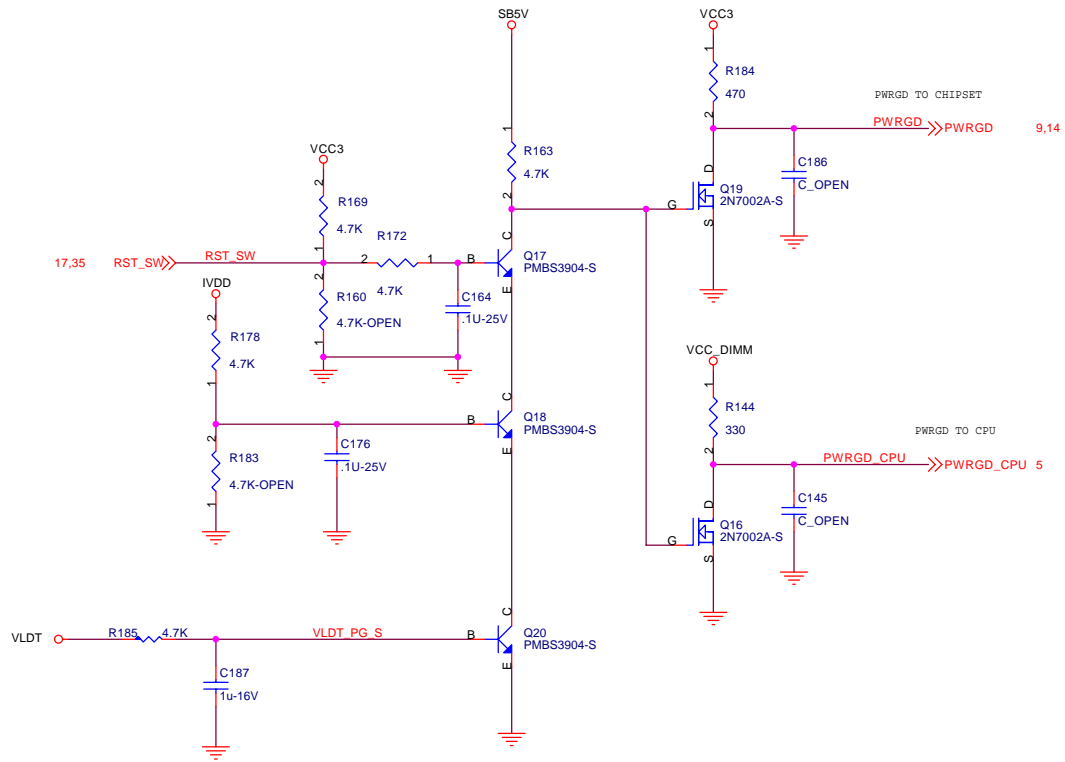
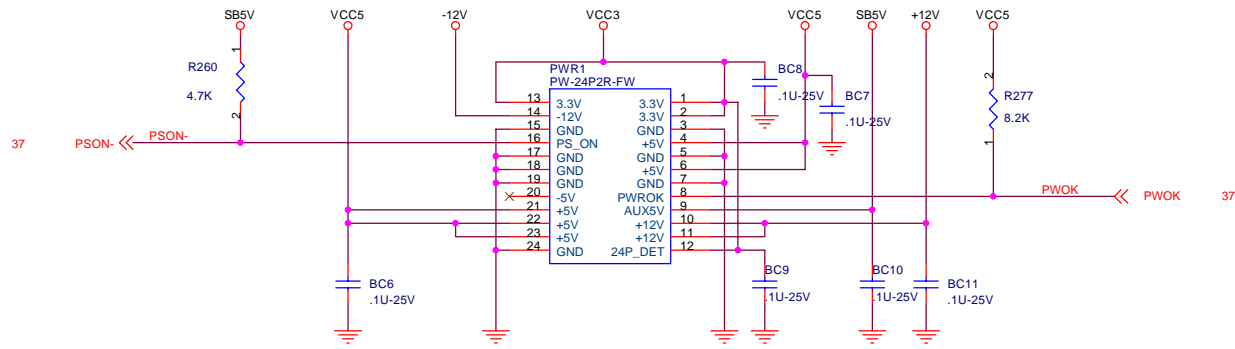


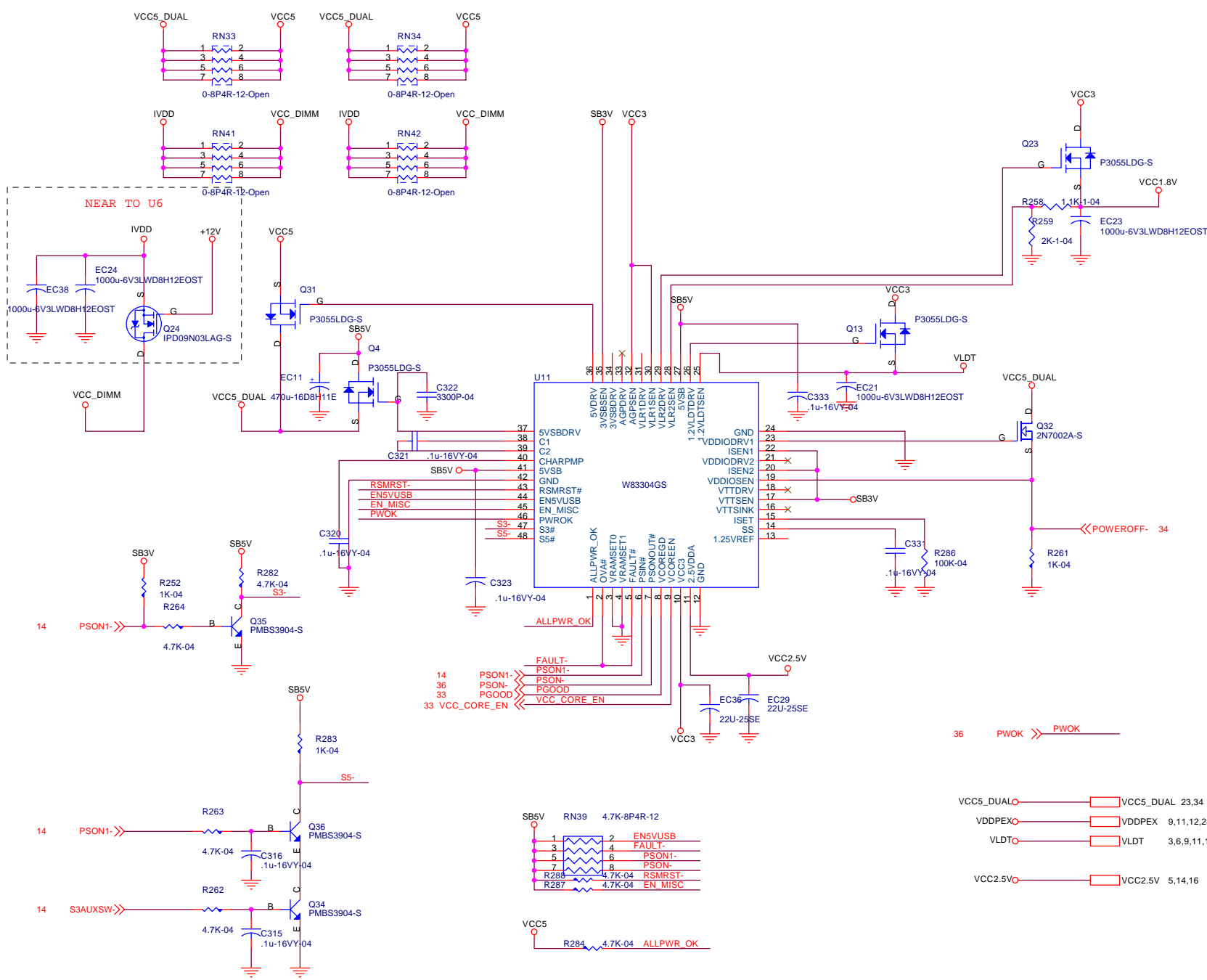


U17 只能使用 5V,那是不是那些零件不需要









- VCC5_DUAL <input type="checkbox"/> VCC5_DUAL 23,34
- VDDPEX <input type="checkbox"/> VDDPEX 9,11,12,28
- VLDT <input type="checkbox"/> VLDT 3,6,9,11,12,36
- VCC2.5V <input type="checkbox"/> VCC2.5V 5,14,16