


GIGABYTE GA-8I848P-G Schematics

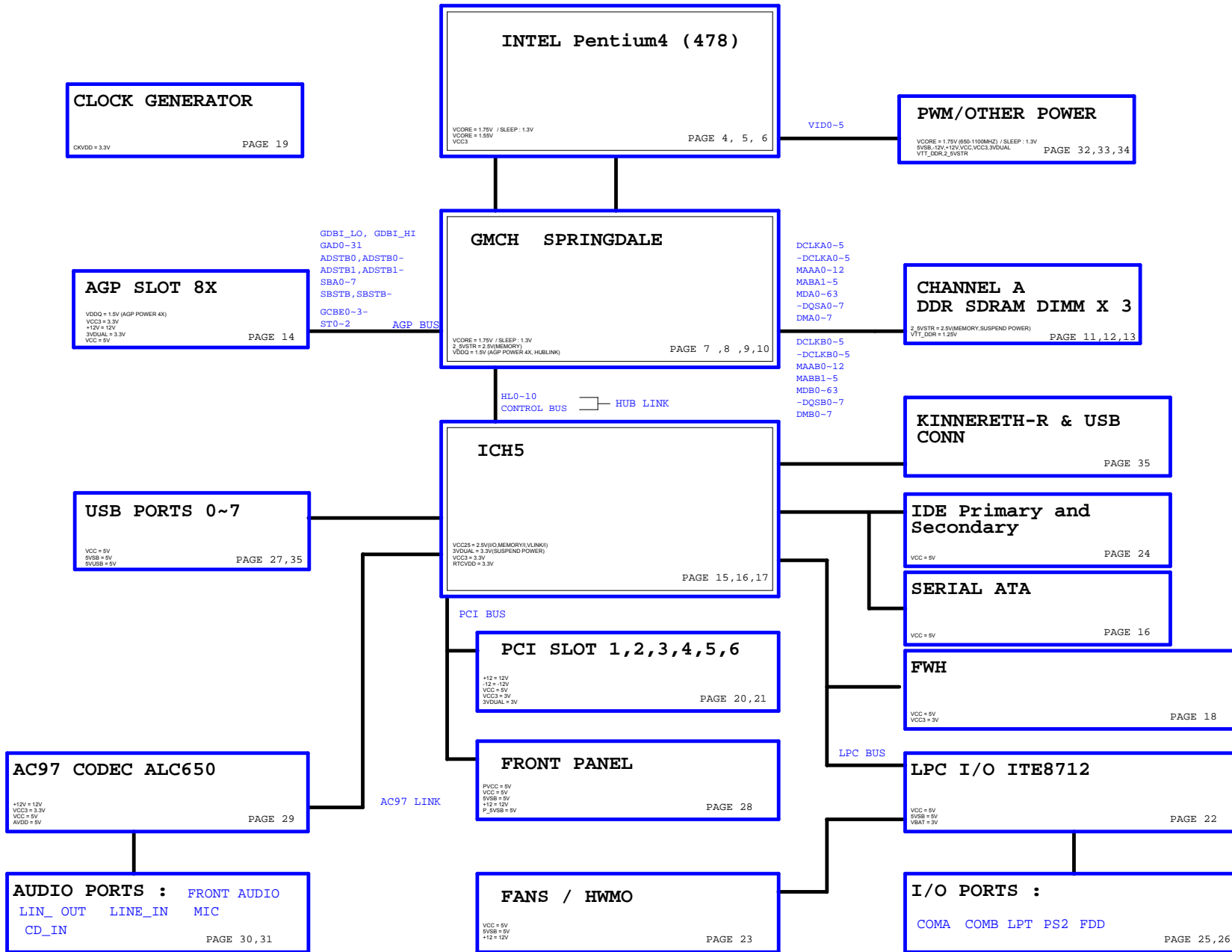
Revision 2.01

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	P4_478A
05	P4_478B
06	P4_478C
07	SPRINGDALE HOST
08	SPRINGDALE DDR
09	SPRINGDALE AGP, HUB, CSA, VGA
10	SPRINGDALE PWR
11	DDR1,2 CHANNEL A
12	DDR3 CHANNEL A
13	DDR TERMINATION
14	AGP
15	ICH5 PCI, USB, HUB, LAN
16	ICH5 IDE, GPIO, SATA, CTRL
17	ICH5 VCC, GND
18	FWH
19	ICS952603 CLOCK GEN
20	PCI1_2
21	PCI3_4
22	PCI5_6

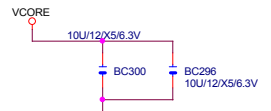
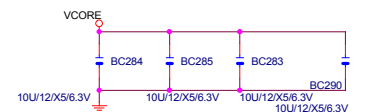
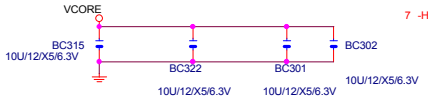
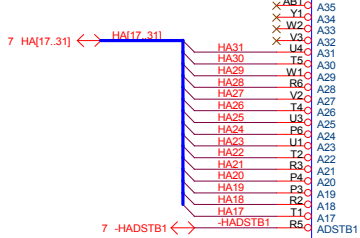
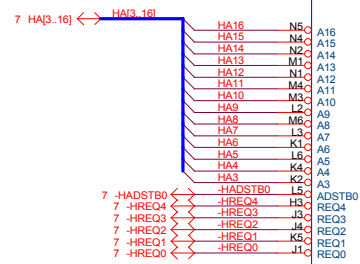
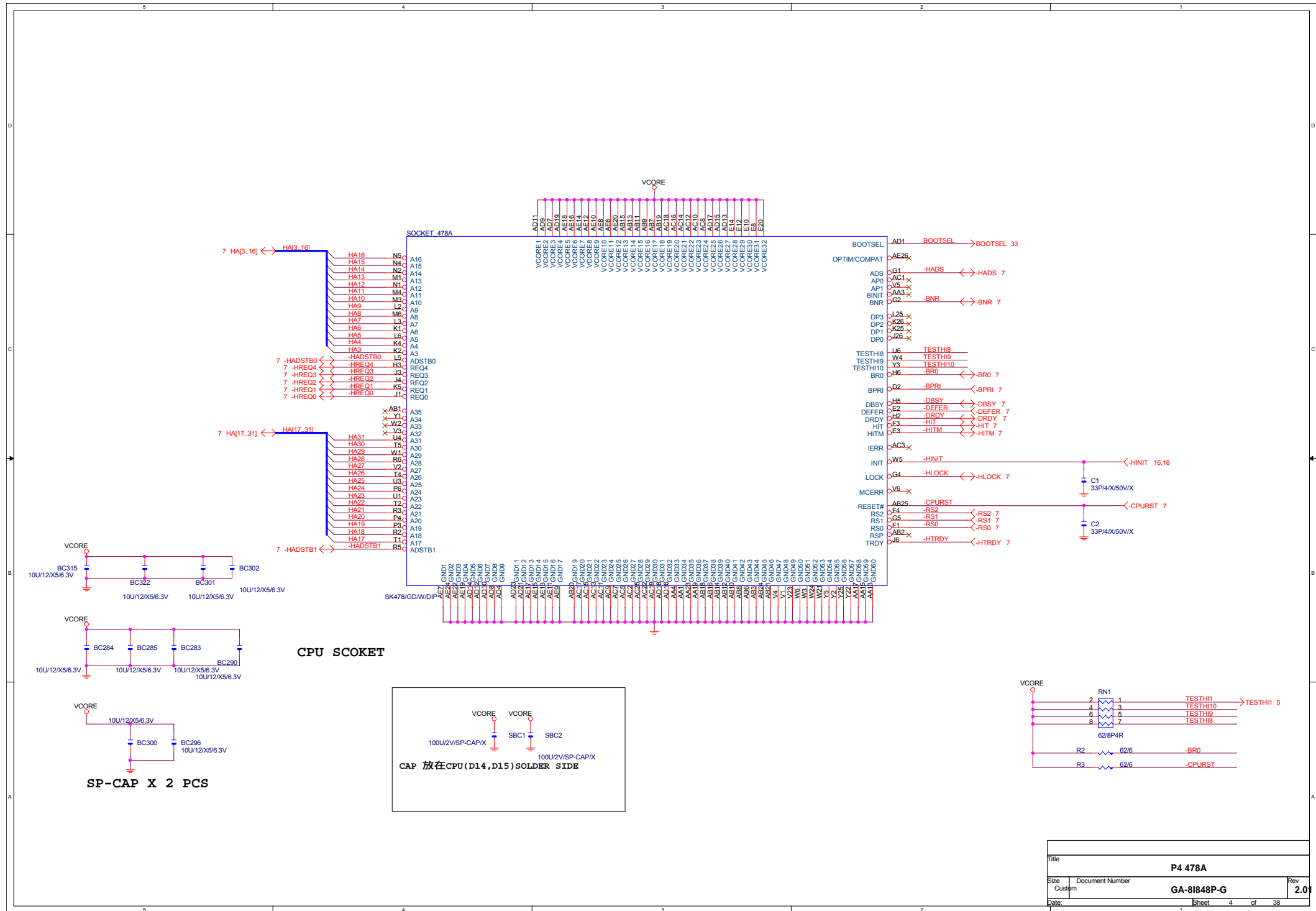
SHEET	TITLE
23	CODEC
24	AUDIO JACK, L_OUT, F_AUDIO
25	ITE 8712
26	COM_LPT
27	IDE
28	FAN/HWMO
29	KB_PS2
30	FPANEL
31	USB CONN
32	DDR POWER
33	VCORE POWER
34	ATX, OTHERS POWER
35	KINNERETH-R LNA(CSA-1)
36	KINNERETH-R LNA(CSA-2)
37	KINNERETH-R LNA(CSA-3)

		COMPONENT SIDE (1 oz. Copper) VCC SIDE (1 oz. Copper) GND SIDE (1 oz. Copper) SOLDER SIDE (1 oz. Copper)
GIGABYTE CORP.		
Title: COVER SHEET		
Size: Custom	Document Number: GA-8I848P-G	Rev: 2.01
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BLOCK DIAGRAM

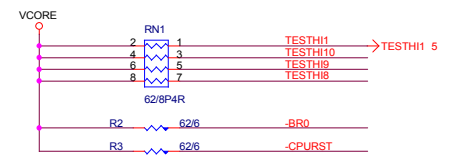
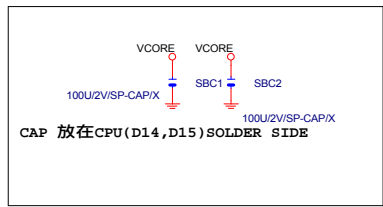


GIGABYTE CORP.			
BOM & PCB MODIFY HISTORY			
File	Document Number	Rev	
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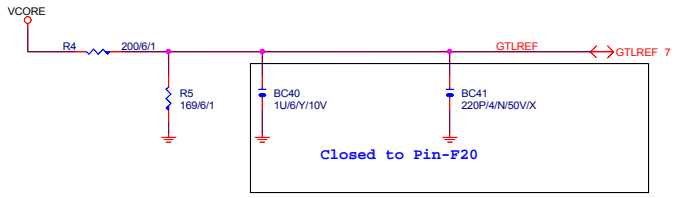


SP-CAP X 2 PCS

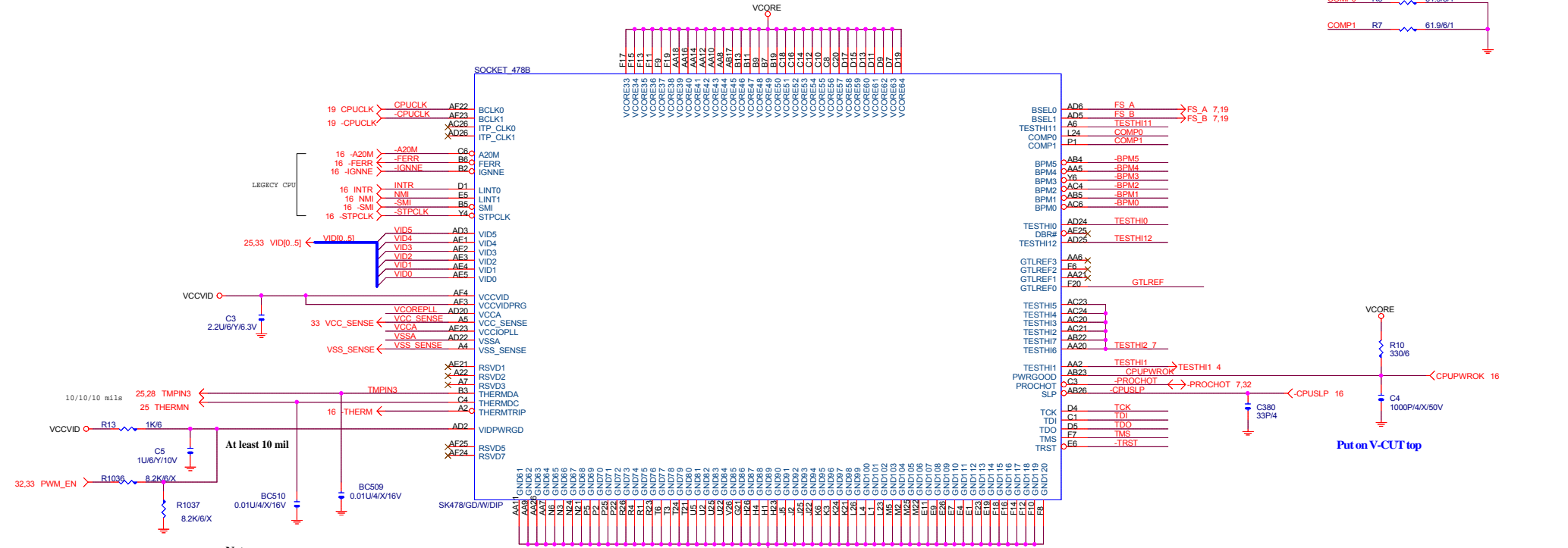
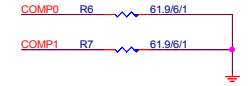
CPU SCKOET



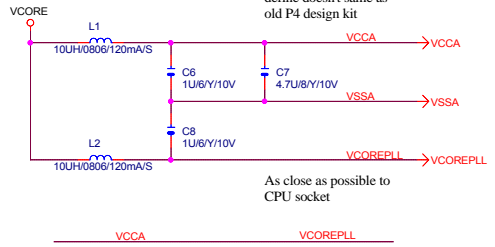
Title			P4 478A		
Size	Document Number				Rev
Custom	GA-81848P-G				2.01
Date:	Sheet 4 of 38				



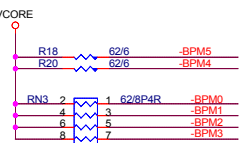
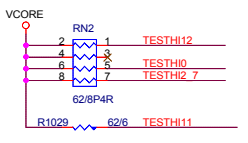
Place outside of CPU socket



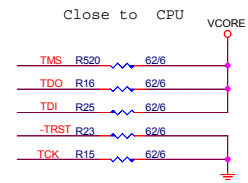
Note:
VCCA & VCOREPLL
define doesn't same as
old P4 design kit



Trace width doesn't
less than 12 Mil



Close to CPU

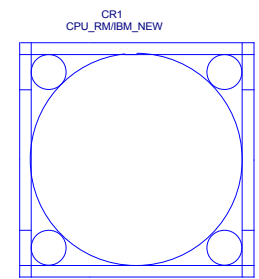
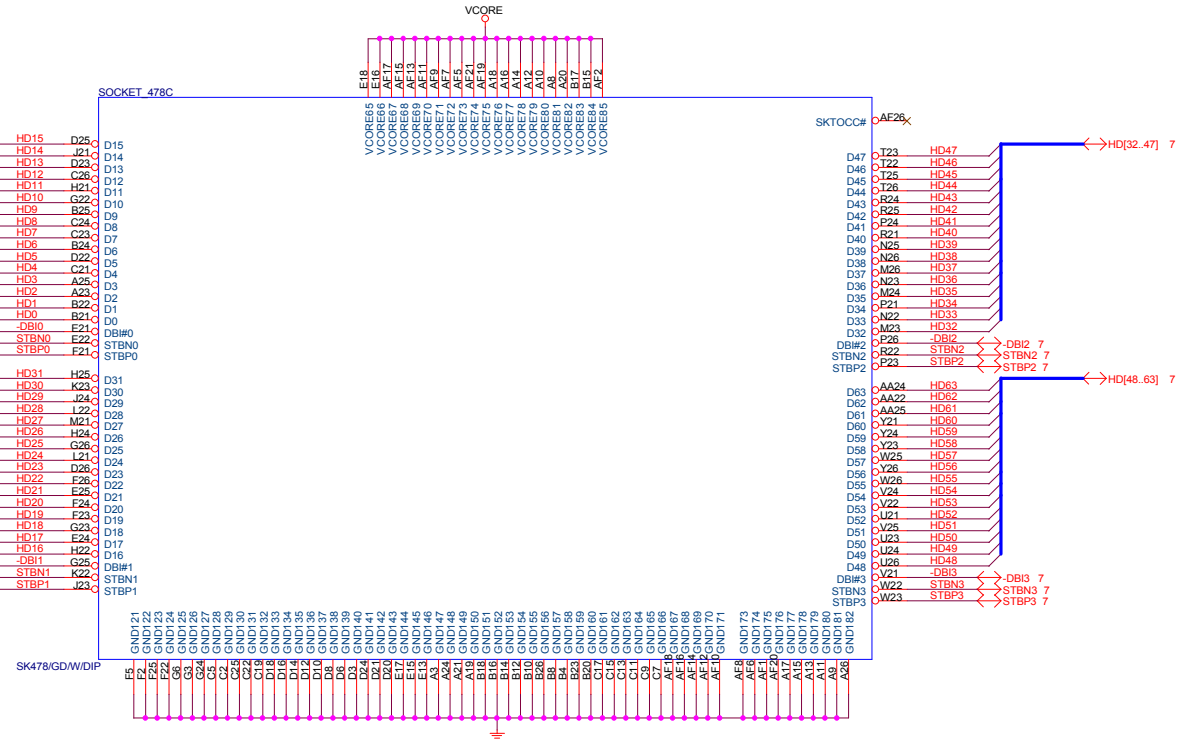
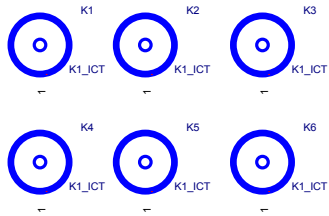


Close to CPU

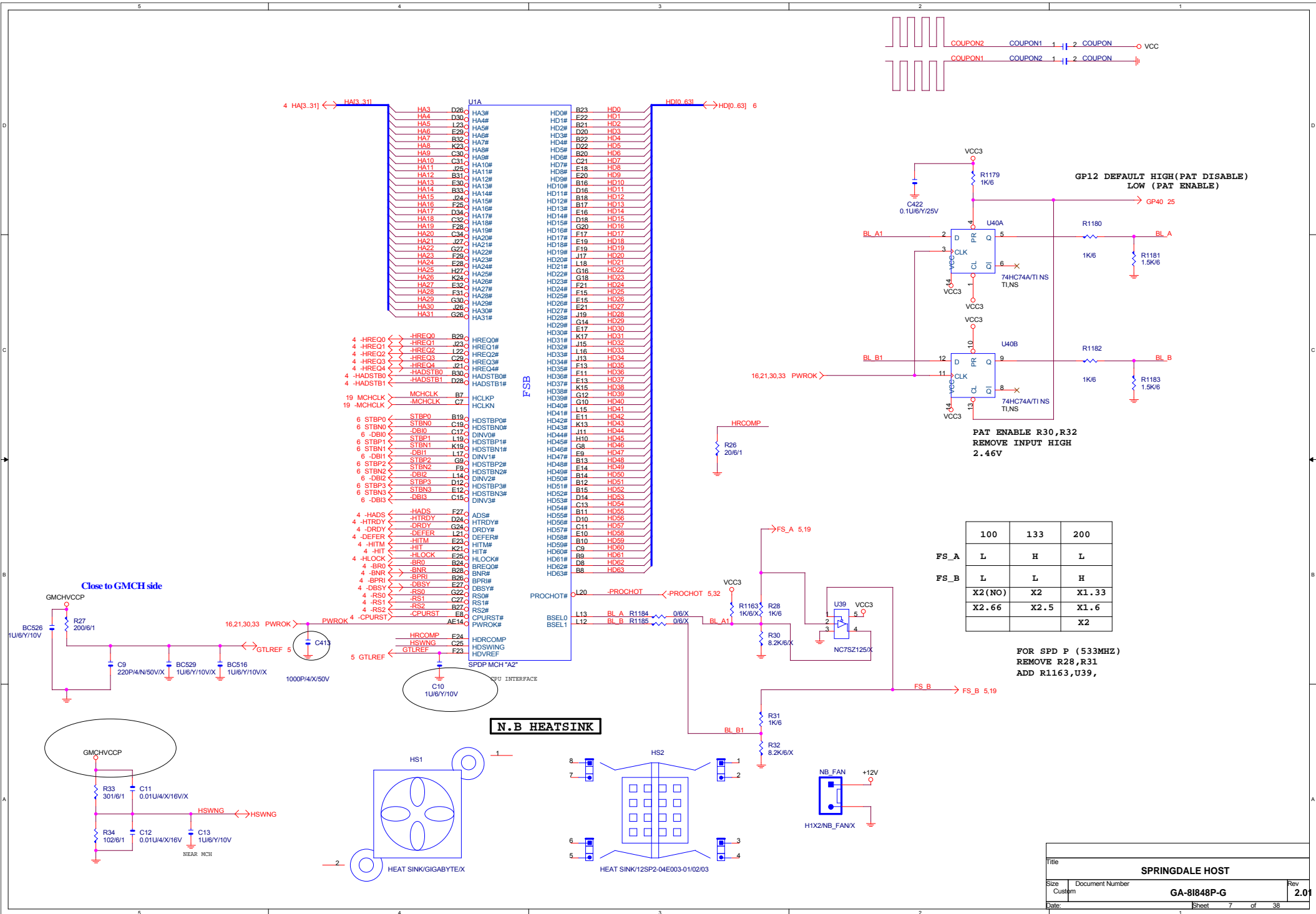


Pull up must place end
of route

Title		
P4 478B		
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Title			P4 478C		
Size	Document Number				Rev
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Date:	Sheet 6 of 38				



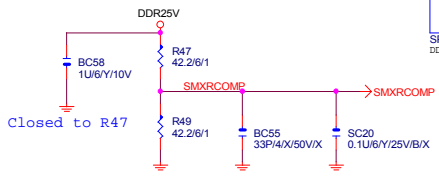
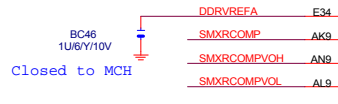
	100	133	200
FS_A	L	H	L
FS_B	L	L	H
X2 (NO)	X2	X2	X1.33
X2.66	X2.5	X2	X1.6

FOR SPD P (533MHZ)
REMOVE R28,R31
ADD R1163,U39,

11.12.13 MAAA[0..12] <-> MAAA0_121
 11.12.13 MABA[1..5] <-> MABA1_51
 11.12.13 DMA[0..7] <-> DMA0_71
 11.12.13 MDA[0..63] <-> MDA0_631
 11.12.13 DQSA[0..7] <-> DQSA0_71

11.12.13 -SWEA <-> SWEA AB34
 11.12.13 -SCASA <-> SCASA Y34
 11.12.13 -SRASA <-> SRASA AC33
 11.12.13 SBA[A0] <-> SBA_A0 AH34
 11.12.13 SBA[A1] <-> SBA_A1 AH34
 11.13 -CSA0 <-> CSA0 AA34
 11.13 -CSA1 <-> CSA1 Y32
 11.12.13 -CSA2 <-> CSA2 Y32
 11.12.13 -CSA3 <-> CSA3 W34
 11.13 CKEA0 <-> CKEA0 AL20
 11.13 CKEA1 <-> CKEA1 AN19
 11.12.13 CKEA2 <-> CKEA2 AM20
 11.12.13 CKEA3 <-> CKEA3 AP20

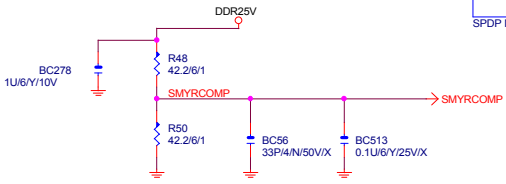
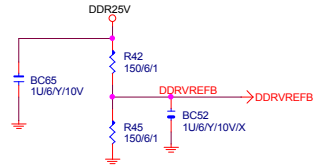
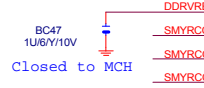
11 -DCLKA0 <-> DCLKA0 AK32
 11 -DCLKA0 <-> DCLKA0 AK31
 11 -DCLKA1 <-> DCLKA1 AP17
 11 -DCLKA1 <-> DCLKA1 AN17
 11 -DCLKA2 <-> DCLKA2 N33
 11 -DCLKA2 <-> DCLKA2 N34
 11.12 -DCLKA3 <-> DCLKA3 AK34
 11.12 -DCLKA3 <-> DCLKA3 AK33
 11.12 -DCLKA4 <-> DCLKA4 AM16
 11.12 -DCLKA4 <-> DCLKA4 AL16
 11.12 -DCLKA5 <-> DCLKA5 P31
 11.12 -DCLKA5 <-> DCLKA5 P32
 11.12 -DCLKA5 <-> DCLKA5 P32



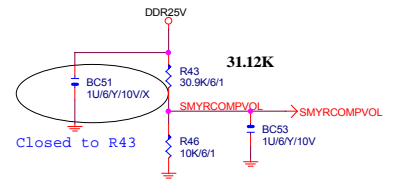
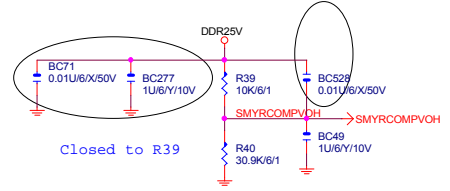
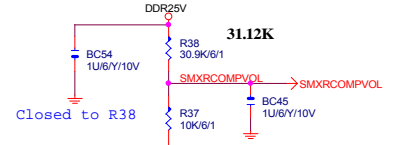
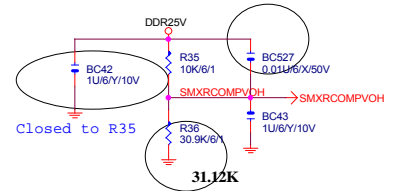
U1B			U1C		
MAAA0	AL34	SMAA_A0	SDQS_A0	AN11	DQSA0
MAAA1	AL33	SMAA_A1	SDM_A0	AP12	MDA0
MAAA2	AK29	SMAA_A2	SDQ_A0	AP10	MDA0
MAAA3	AN31	SMAA_A3	SDQ_A1	AP11	MDA1
MAAA4	AL30	SMAA_A4	SDQ_A2	AM12	MDA2
MAAA5	AL26	SMAA_A5	SDQ_A3	AN13	MDA3
MAAA6	AL28	SMAA_A6	SDQ_A4	AM10	MDA4
MAAA7	AN25	SMAA_A7	SDQ_A4	AL10	MDA5
MAAA8	AP26	SMAA_A8	SDQ_A7	AL12	MDA6
MAAA9	AP24	SMAA_A9	SDQ_A6	AP13	MDA7
MAAA10	AL33	SMAA_A10	SDQ_A7		
MAAA11	AN23	SMAA_A11	SDQS_A1	AP15	DQSA1
MAAA12	AN21	SMAA_A12	SDM_A1	AP16	DMA1
MABA1	AL34	SMAB_A1	SDQ_A8	AP14	MDA8
MABA2	AM34	SMAB_A2	SDQ_A9	AM14	MDA9
MABA3	AP32	SMAB_A3	SDQ_A10	AL18	MDA10
MABA4	AP31	SMAB_A4	SDQ_A11	AP19	MDA11
MABA5	AM26	SMAB_A5	SDQ_A12	AL14	MDA12
			SDQ_A13	AN15	MDA13
			SDQ_A14	AP18	MDA14
			SDQ_A15	AM18	MDA15
			SDQS_A2	AP23	DQSA2
			SDM_A2	AM24	DMA2
			SDQ_A16	AP22	MDA16
			SDQ_A17	AM22	MDA17
			SDQ_A18	AL24	MDA18
			SDQ_A19	AN27	MDA19
			SDQ_A20	AP21	MDA20
			SDQ_A21	AL22	MDA21
			SDQ_A22	AP25	MDA22
			SDQ_A23	AP27	MDA23
			SDQS_A3	AM30	DQSA3
			SDM_A3	AP30	DMA3
			SDQ_A24	AP28	MDA24
			SDQ_A25	AP29	MDA25
			SDQ_A26	AP33	MDA26
			SDQ_A27	AM33	MDA27
			SDQ_A28	AM28	MDA28
			SDQ_A29	AN29	MDA29
			SDQ_A30	AM31	MDA30
			SDQ_A31	AN34	MDA31
			SDQS_A4	AF34	DQSA4
			SDM_A4	AF31	DMA4
			SDQ_A32	AH32	MDA32
			SDQ_A33	AC34	MDA33
			SDQ_A34	AF32	MDA34
			SDQ_A35	AD32	MDA35
			SDQ_A36	AH31	MDA36
			SDQ_A37	AC33	MDA37
			SDQ_A38	AE34	MDA38
			SDQ_A39	AD34	MDA39
			SDQS_A5	V34	DQSA5
			SDM_A5	W33	DMA5
			SDQ_A40	AC34	MDA40
			SDQ_A41	AB31	MDA41
			SDQ_A42	V32	MDA42
			SDQ_A43	V31	MDA43
			SDQ_A44	AD31	MDA44
			SDQ_A45	AB32	MDA45
			SDQ_A46	U34	MDA46
			SDQ_A47	U33	MDA47
			SDQS_A6	M32	DQSA6
			SDM_A6	M34	DMA6
			SDQ_A48	T34	MDA48
			SDQ_A49	T32	MDA49
			SDQ_A50	K34	MDA50
			SDQ_A51	K32	MDA51
			SDQ_A52	T31	MDA52
			SDQ_A53	P34	MDA53
			SDQ_A54	L34	MDA54
			SDQ_A55	L33	MDA55
			SDQS_A7	H31	DQSA7
			SDM_A7	H32	DMA7
			SDQ_A56	J33	MDA56
			SDQ_A57	H34	MDA57
			SDQ_A58	E33	MDA58
			SDQ_A59	F33	MDA59
			SDQ_A60	K31	MDA60
			SDQ_A61	J34	MDA61
			SDQ_A62	G34	MDA62
			SDQ_A63	F34	MDA63

DDR Channel A

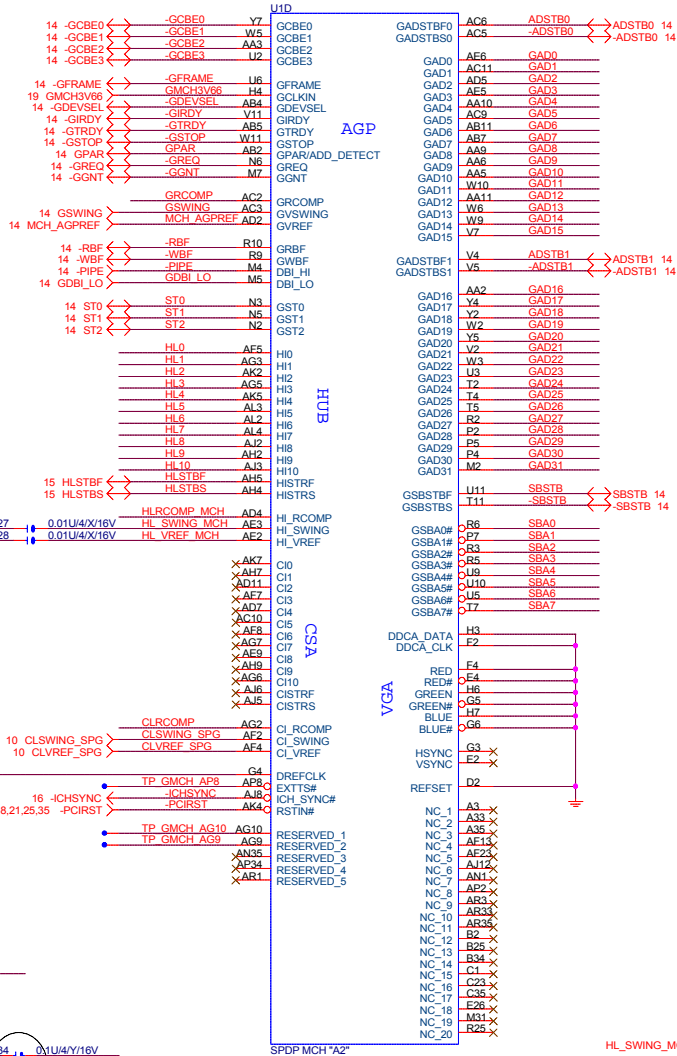
DDR Channel B



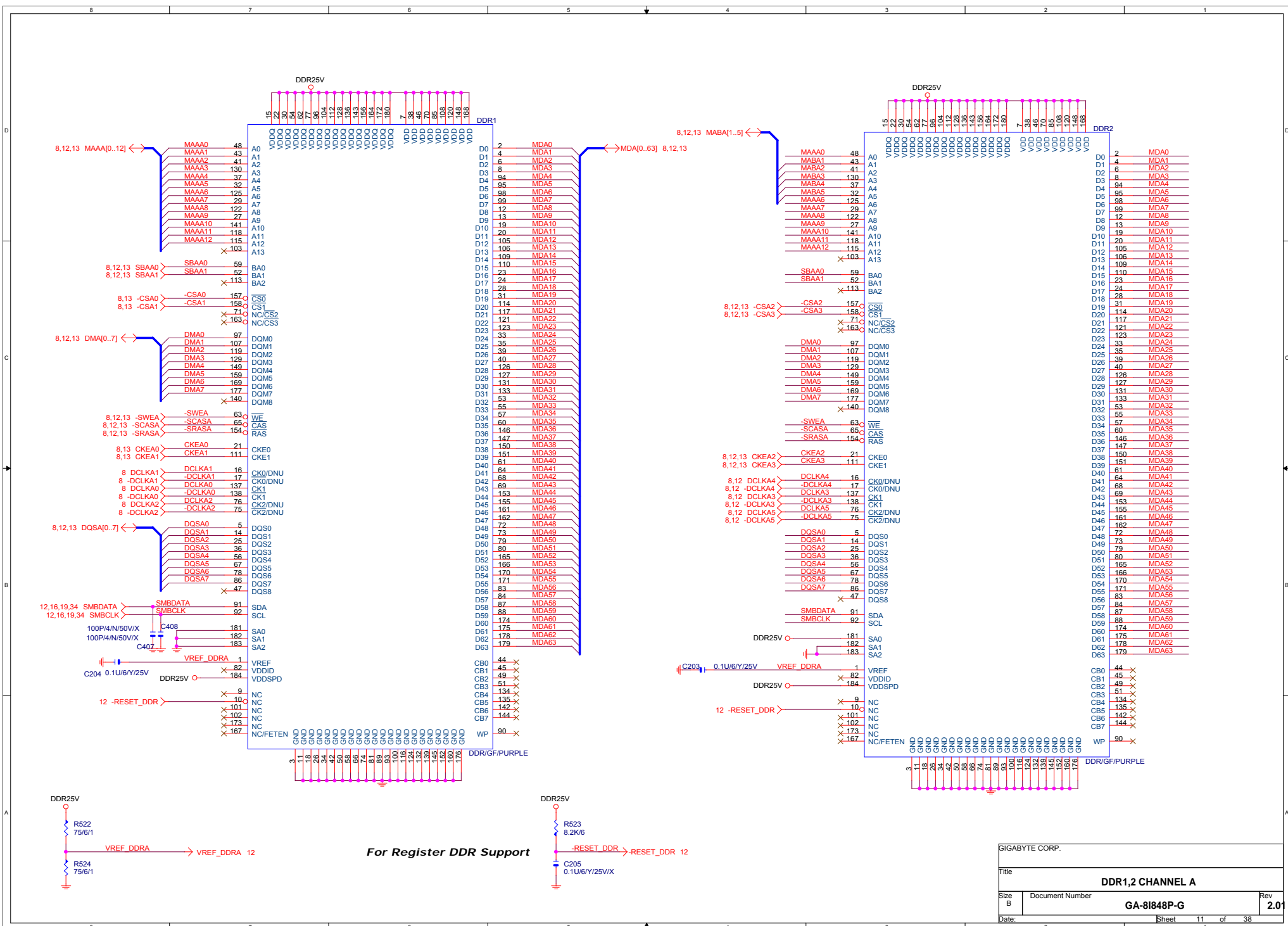
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SDQS_B0	AE15	AG31			
SDM_B0	AE16	AG11			
SDQ_B0	AL10	AL10			
SDQ_B1	AE15	AE15			
SDQ_B2	AE16	AE16			
SDQ_B3	AE17	AE17			
SDQ_B4	AE18	AE18			
SDQ_B5	AE19	AE19			
SDQ_B6	AE20	AE20			
SDQ_B7	AE21	AE21			
SDQS_B1	AG13	AG13			
SDM_B1	AG14	AG14			
SDQ_B8	AE17	AE17			
SDQ_B9	AE18	AE18			
SDQ_B10	AE19	AE19			
SDQ_B11	AE20	AE20			
SDQ_B12	AE21	AE21			
SDQ_B13	AE22	AE22			
SDQ_B14	AE23	AE23			
SDQ_B15	AE24	AE24			
SDQS_B2	AG21	AG21			
SDM_B2	AG22	AG22			
SDQ_B16	AE19	AE19			
SDQ_B17	AE20	AE20			
SDQ_B18	AE21	AE21			
SDQ_B19	AE22	AE22			
SDQ_B20	AE23	AE23			
SDQ_B21	AE24	AE24			
SDQ_B22	AE25	AE25			
SDQ_B23	AE26	AE26			
SDQS_B3	AH27	AH27			
SDM_B3	AH28	AH28			
SDQ_B24	AK25	AK25			
SDQ_B25	AH26	AH26			
SDQ_B26	AE27	AE27			
SDQ_B27	AE28	AE28			
SDQ_B28	AJ26	AJ26			
SDQ_B29	AJ27	AJ27			
SDQ_B30	AD26	AD26			
SDQ_B31	AE28	AE28			
SDQS_B4	AD29	AD29			
SDM_B4	AC31	AC31			
SDQ_B32	AE30	AE30			
SDQ_B33	AC34	AC34			
SDQ_B34	AC35	AC35			
SDQ_B35	Y29	Y29			
SDQ_B36	AE31	AE31			
SDQ_B37	AE32	AE32			
SDQ_B38	AA26	AA26			
SDQ_B39	AA27	AA27			
SDQS_B5	U30	U30			
SDM_B5	U31	U31			
SDQ_B40	AA30	AA30			
SDQ_B41	W30	W30			
SDQ_B42	U27	U27			
SDQ_B43	T25	T25			
SDQ_B44	Y29	Y29			
SDQ_B45	U25	U25			
SDQ_B46	R27	R27			
SDQ_B47	R27	R27			
SDQS_B6	L27	L27			
SDM_B6	M29	M29			
SDQ_B48	P29	P29			
SDQ_B49	R30	R30			
SDQ_B50	K28	K28			
SDQ_B51	L30	L30			
SDQ_B52	R31	R31			
SDQ_B53	R26	R26			
SDQ_B54	P25	P25			
SDQ_B55	L32	L32			
SDQS_B7	J30	J30			
SDM_B7	J31	J31			
SDQ_B56	K30	K30			
SDQ_B57	H29	H29			
SDQ_B58	F32	F32			
SDQ_B59	N25	N25			
SDQ_B60	M25	M25			
SDQ_B61	M25	M25			
SDQ_B62	J29	J29			
SDQ_B63	G32	G32			



14 GAD[0..31] ↔ GAD[0..31]
 14 SBA[0..7] ↔ SBA[0..7]
 15 HL[0..10] ↔ HL[0..10]



Title		
SPRINGDALE AGP,HUB,CSA,VGA		
Size	Document Number	Rev
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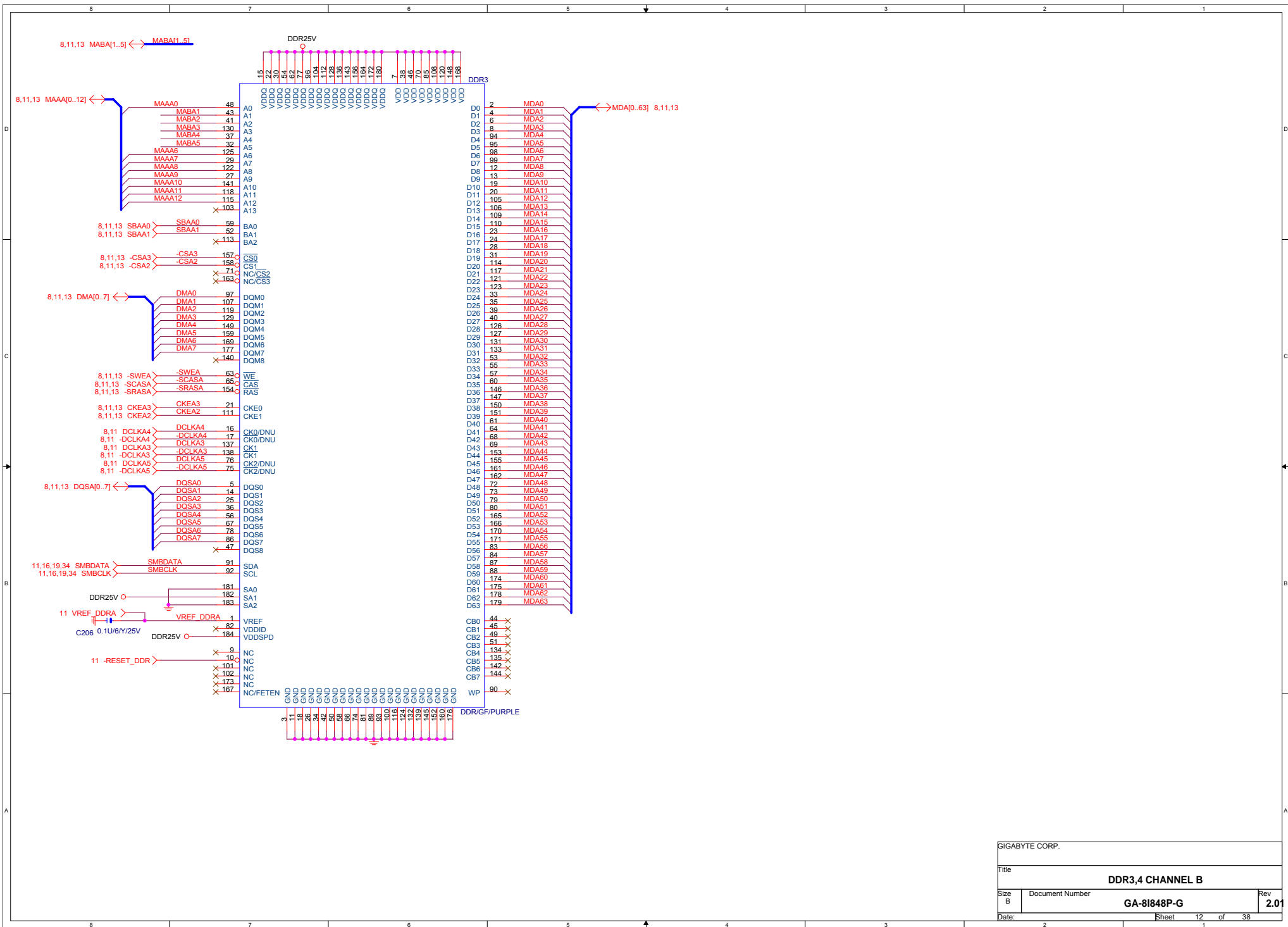
For Register DDR Support

SIGABYTE CORP.

Title: **DDR1,2 CHANNEL A**

Size B: Document Number: **GA-81848P-G** Rev: **2.01**

Date: _____ Sheet 11 of 38

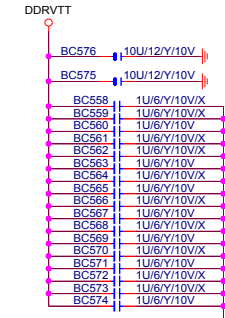
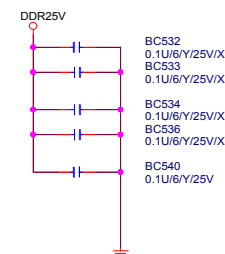
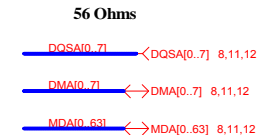
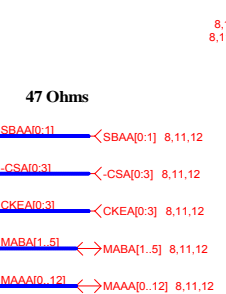
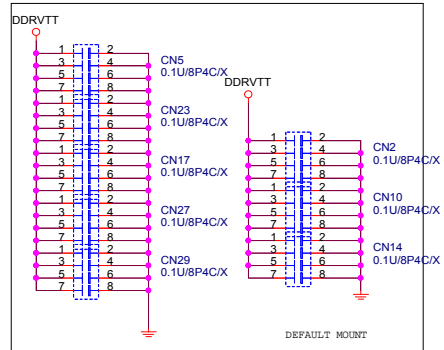
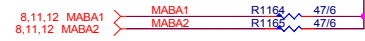
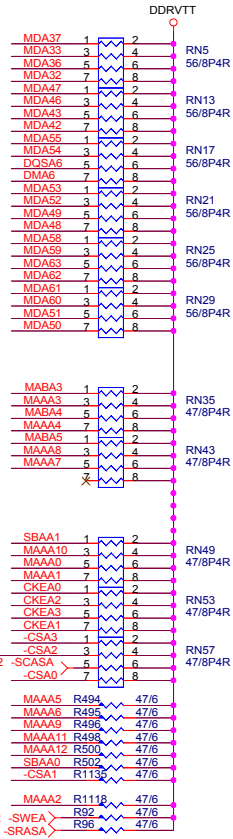
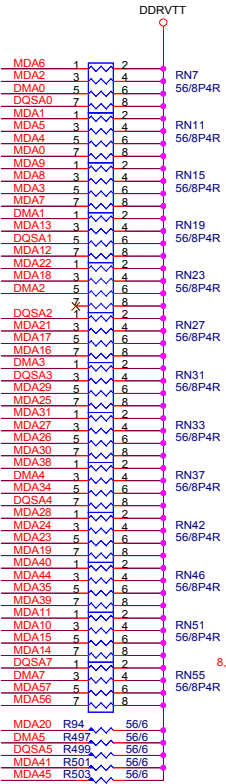
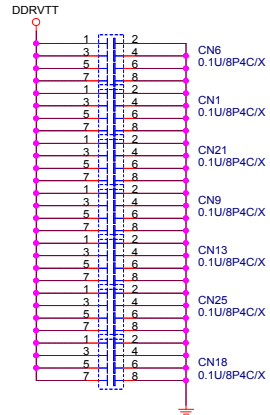


DDRVTT Decouple

DDR TERMINATION CHANNEL A

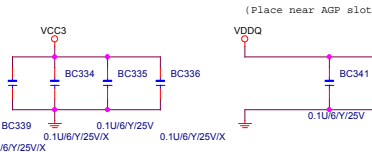
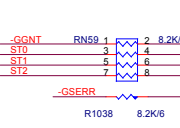
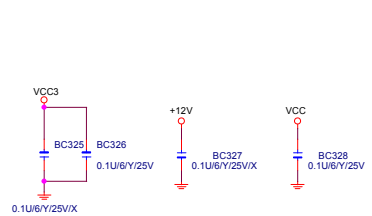
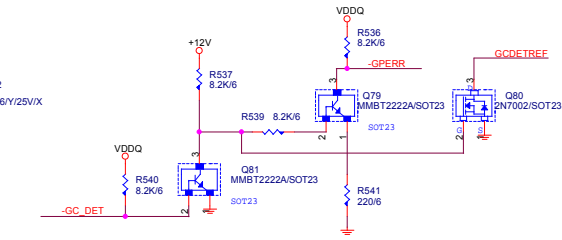
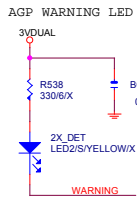
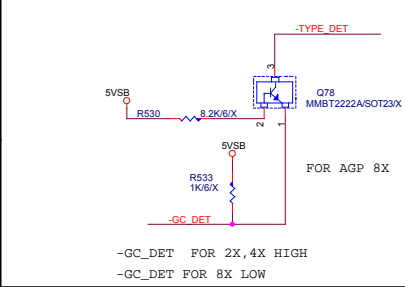
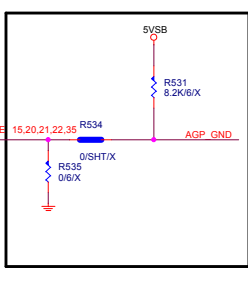
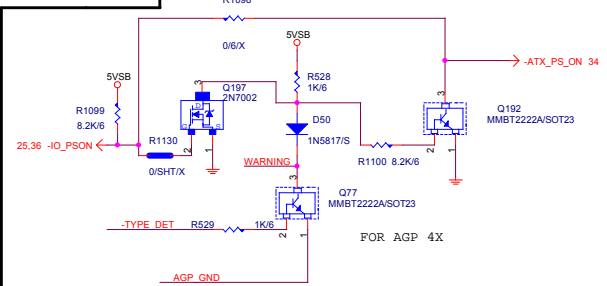
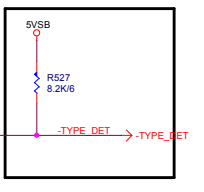
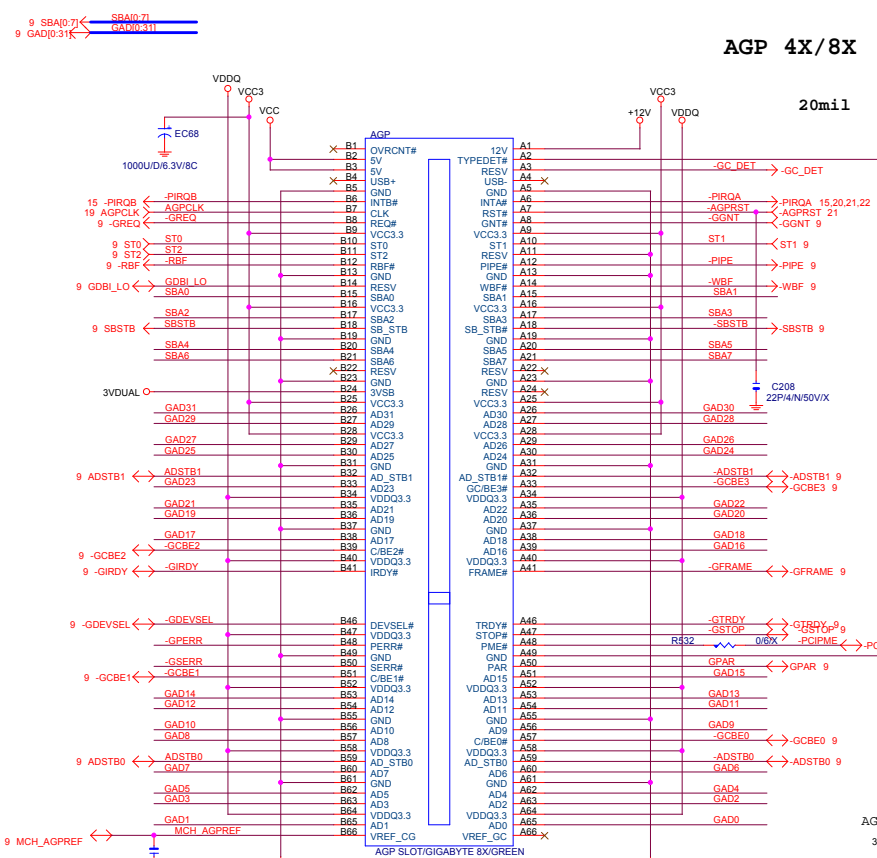
DDRVTT Decouple

CHANNEL B



AGP 4X/8X

20mil

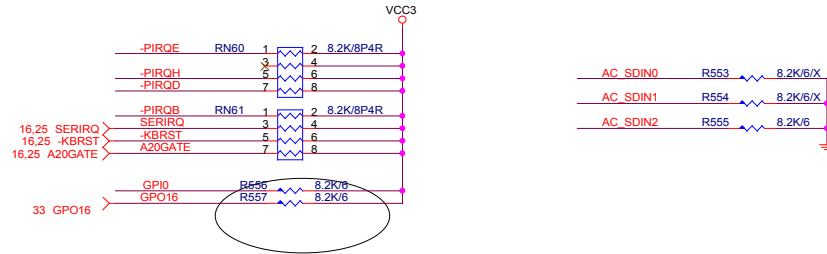


Place 1 at each pair of 3.3V pins

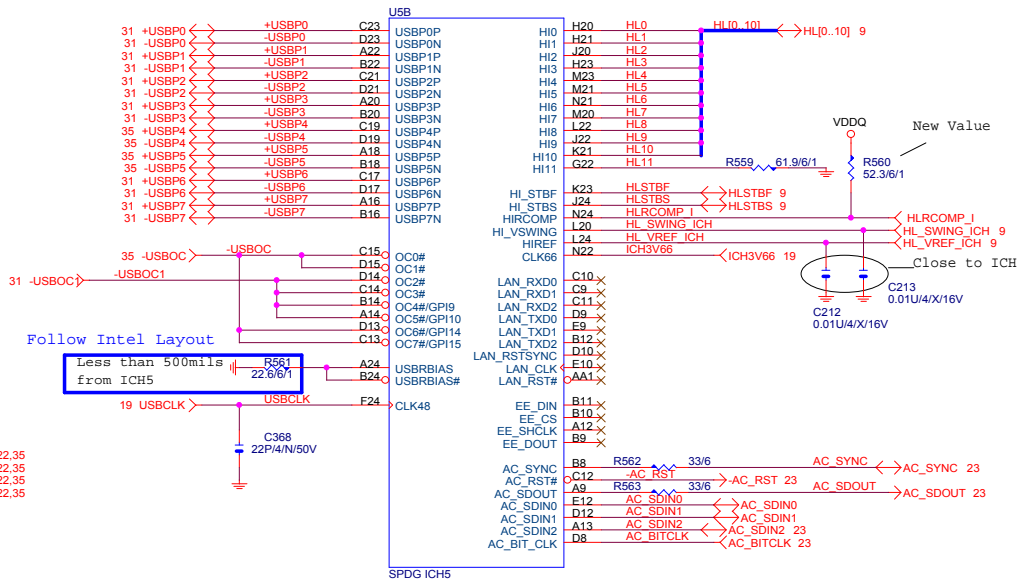
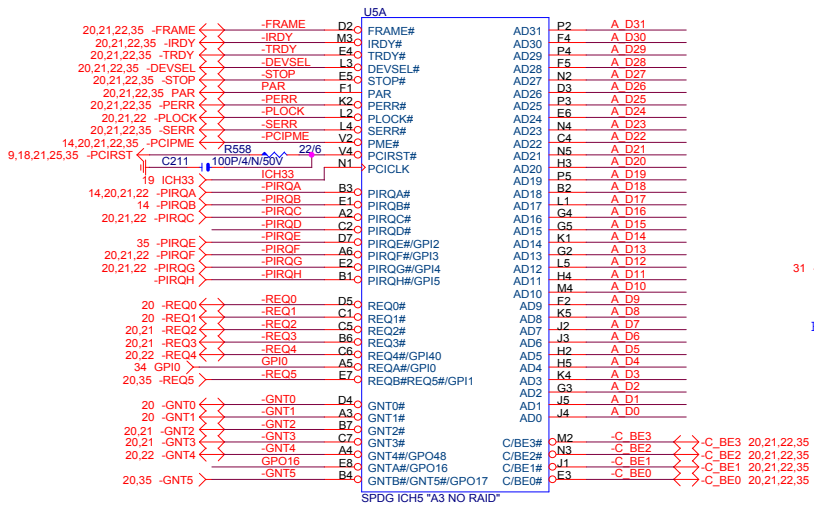
Place 1 at each pair of VDDQ pins
Place an additional for spread from A14 - A33

At least 15mils

GIGABYTE CORP.		
AGP SLOT		
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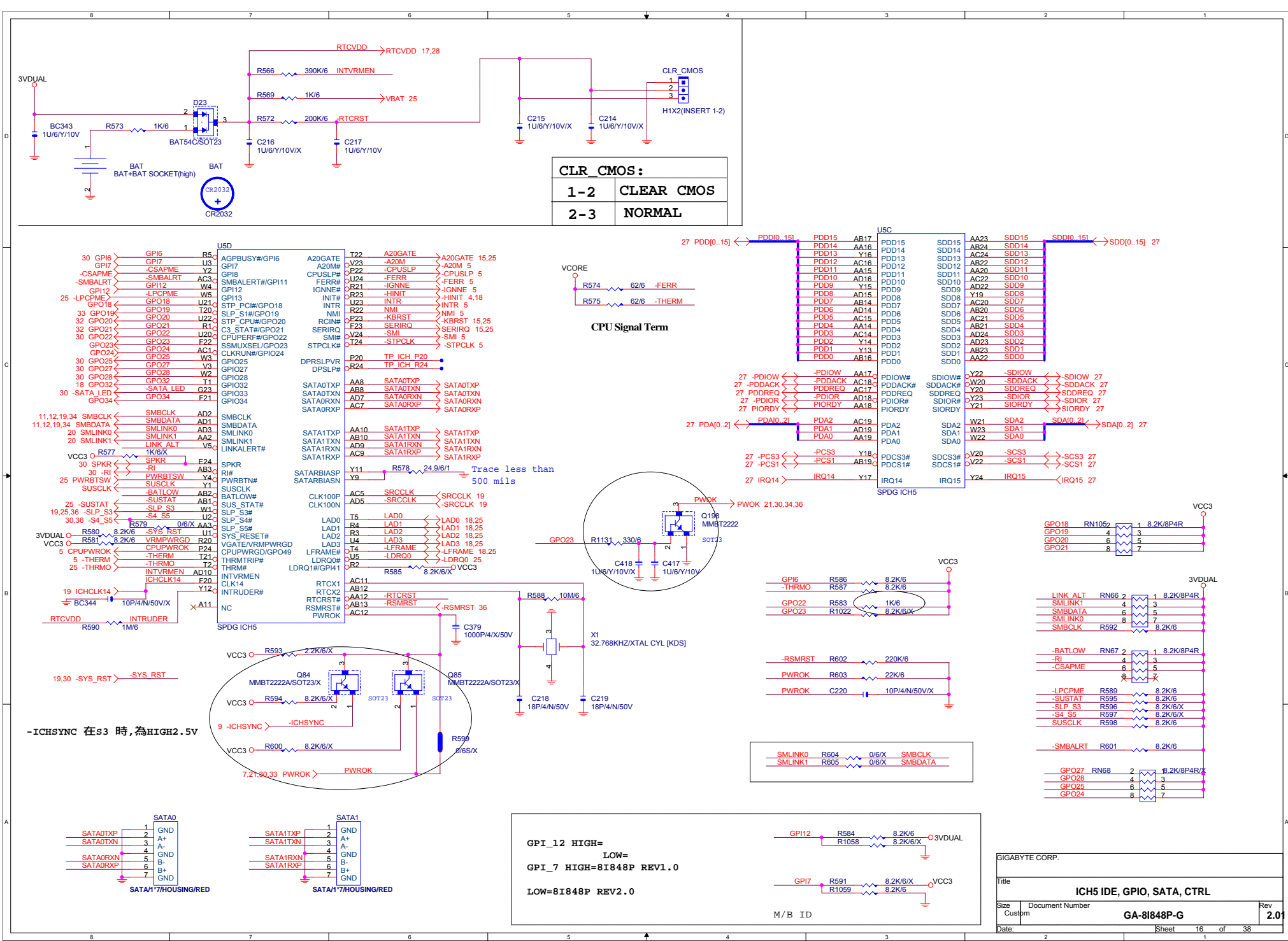


A_D10_311 <-> A_D10_31] 20,21,22,35



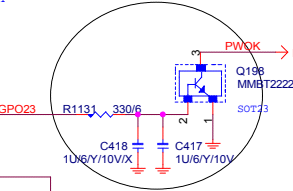
Follow Intel Layout

Less than 500mils from ICH5

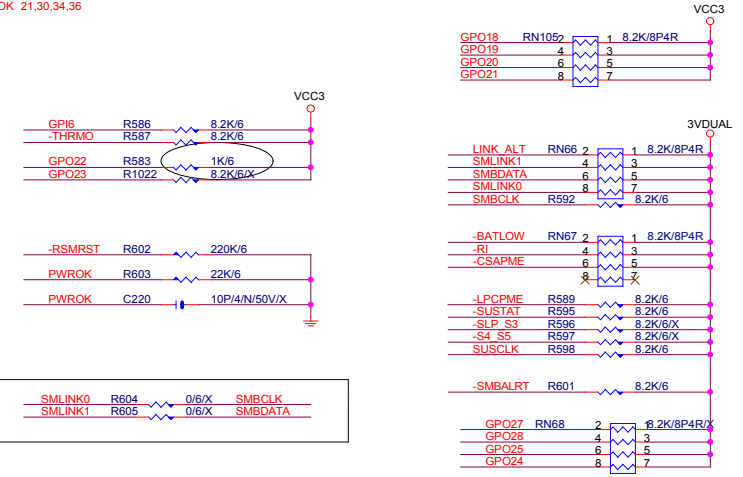
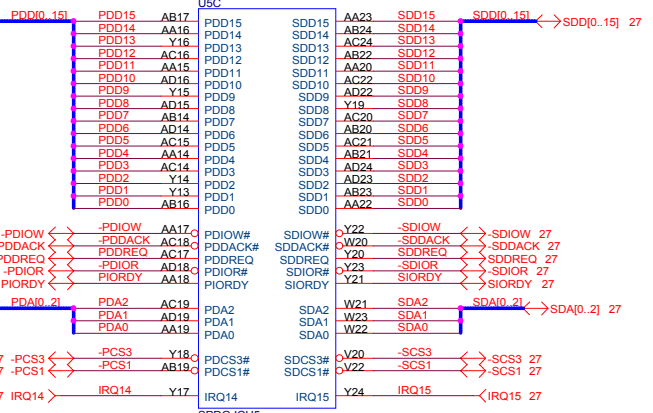


CLR_CMOS :	
1-2	CLEAR CMOS
2-3	NORMAL

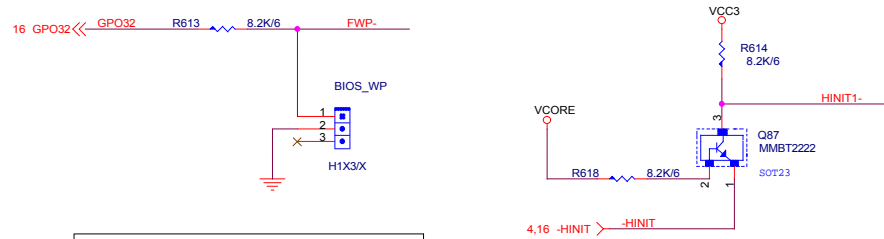
CPU Signal Term



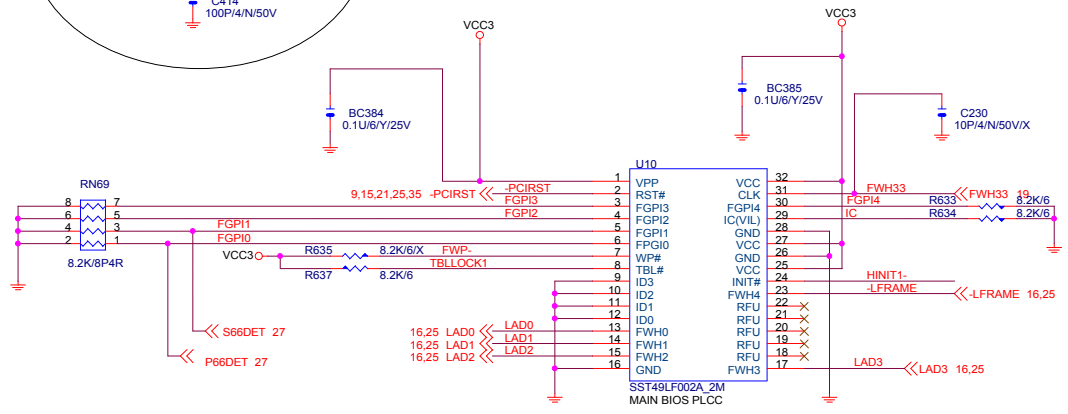
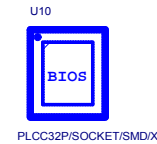
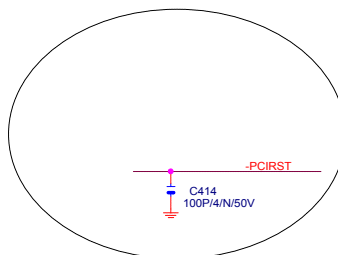
GPI_12 HIGH=
 LOW=
 GPI_7 HIGH=8I848P REV1.0
 LOW=8I848P REV2.0



GIGABYTE CORP.	
Title: ICH5 IDE, GPIO, SATA, CTRL	
Size: Custom	Document Number: GA-8I848P-G
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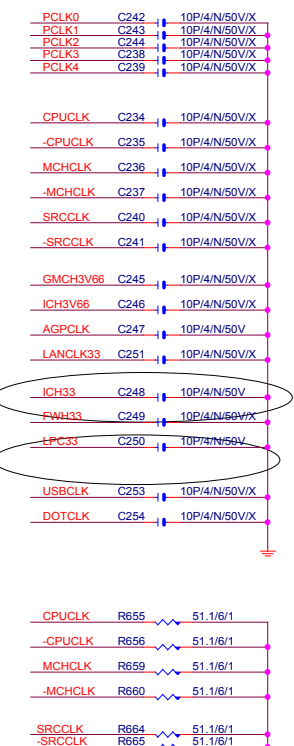
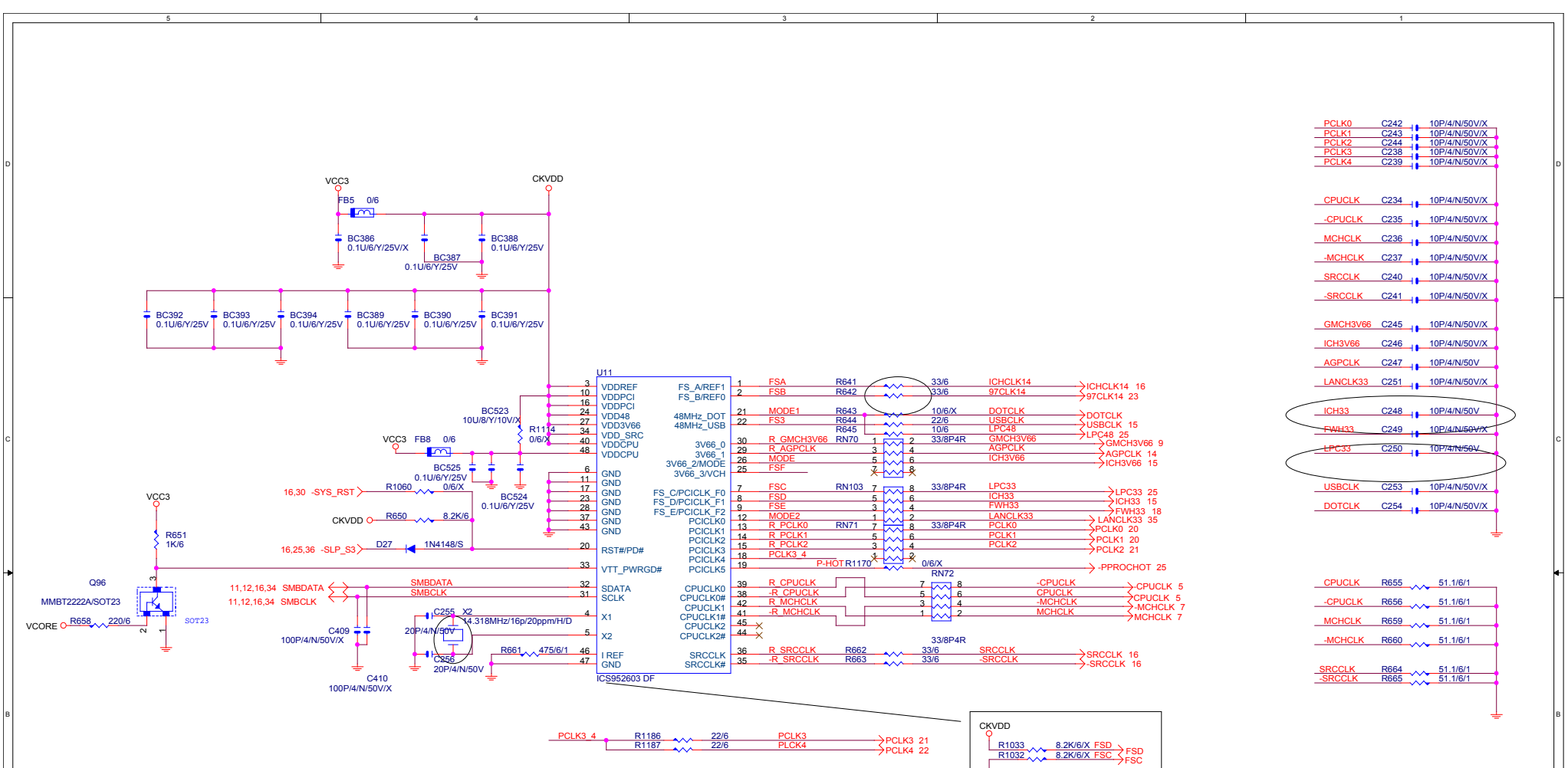


BIOS_WP :	
1-2	WRITE PROTECT
2-3	DISABLE



ADD WINBOUD FWH SEC. SOURCE

GIGABYTE CORP.		
Title		
FWH		
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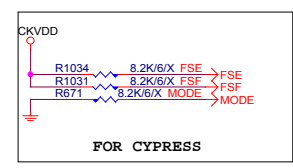
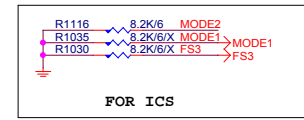
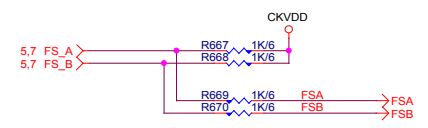
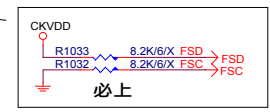
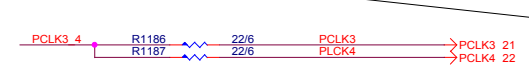


CYPRESS CY28405

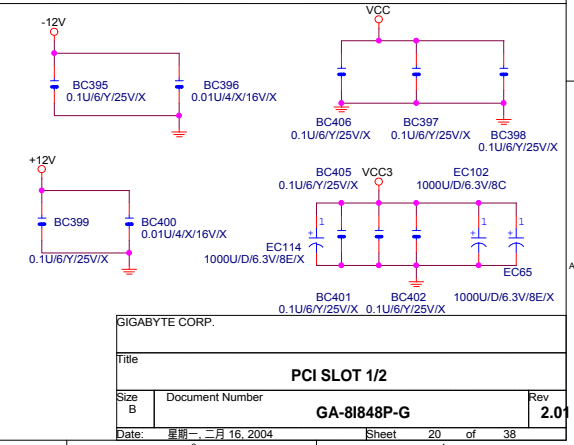
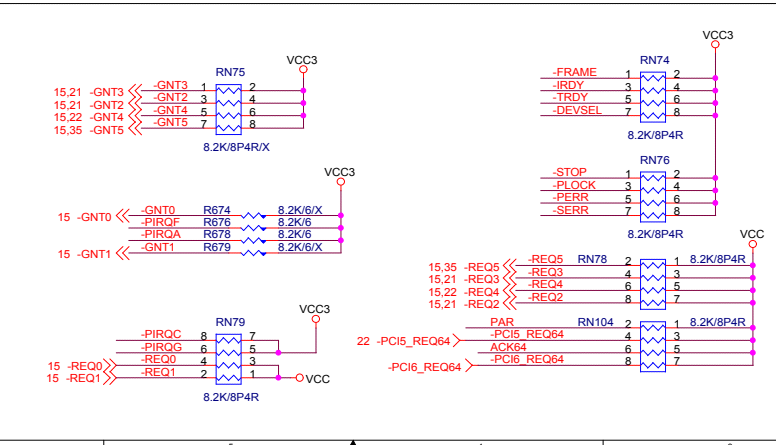
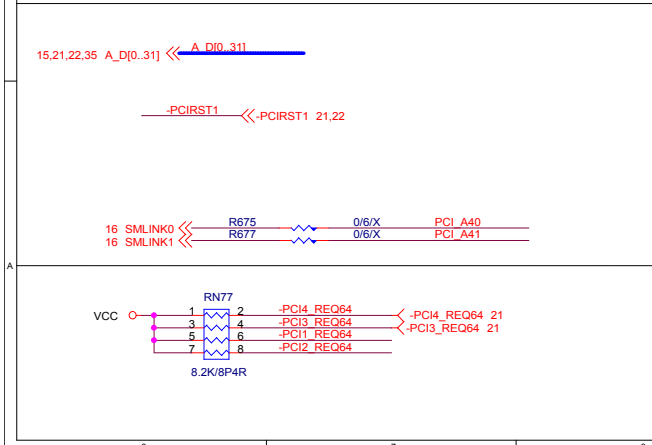
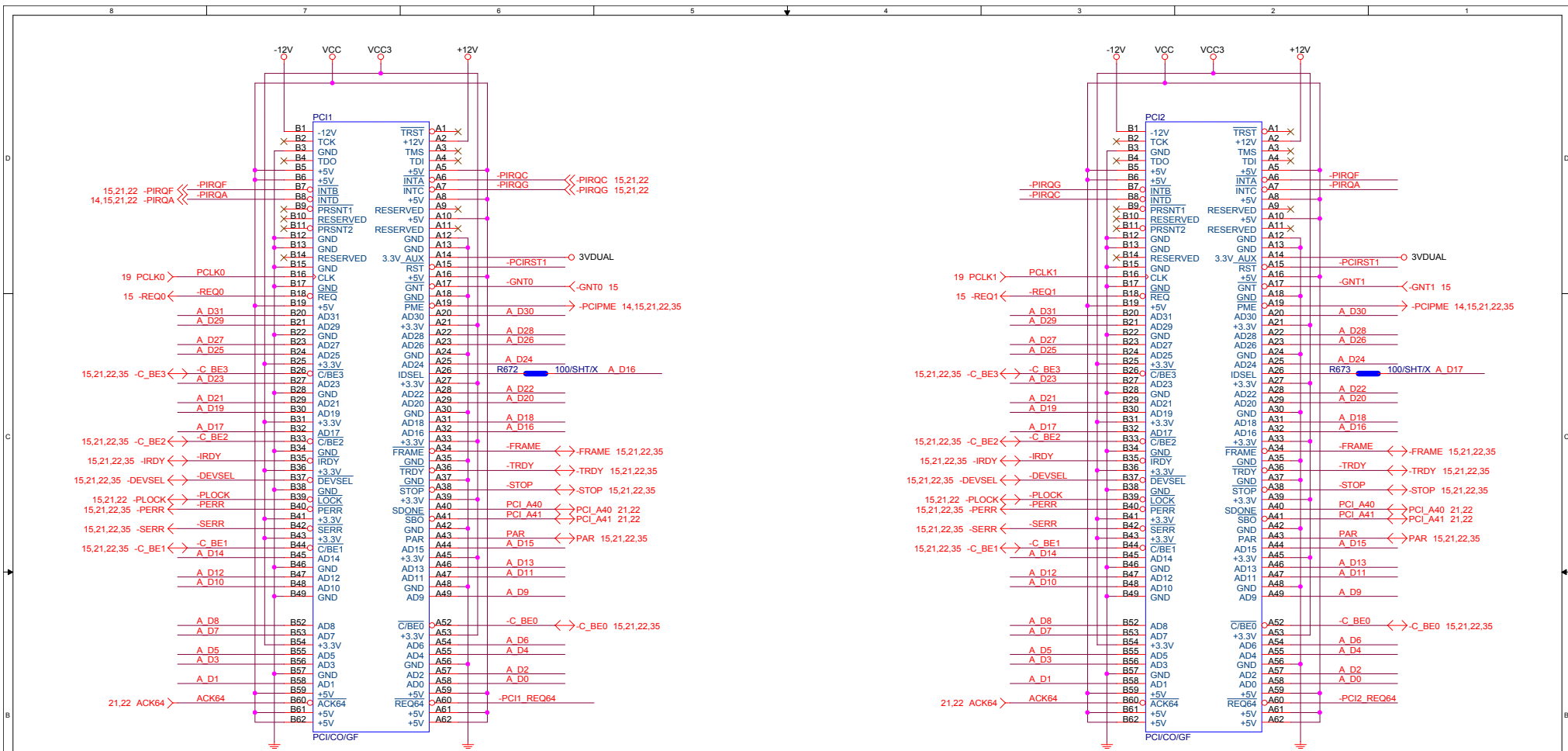
FS_E	FS_D	FS_C	FS_A	FS_B	Clock
1	1	0	0	0	100MHz
1	1	0	1	0	133MHz
1	1	0	1	1	166MHz
1	1	0	0	1	200MHz

ICS952603

FS_D	FS_3	FS_C	FS_A	FS_B	Clock
1	0	0	0	0	100MHz
1	0	0	1	0	133MHz
1	0	0	1	1	166MHz
1	0	0	0	1	200MHz

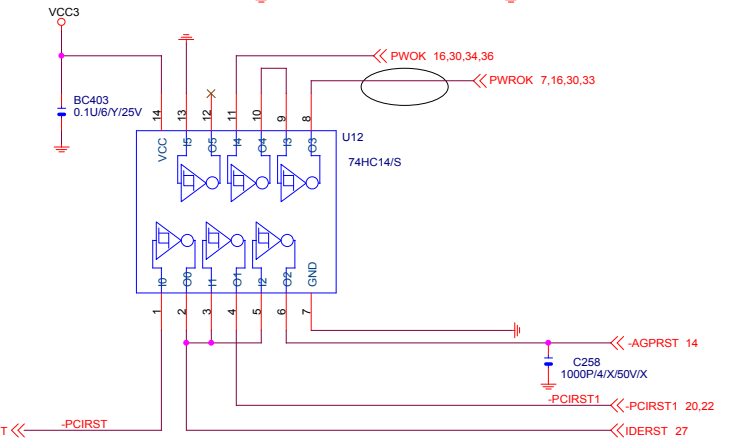
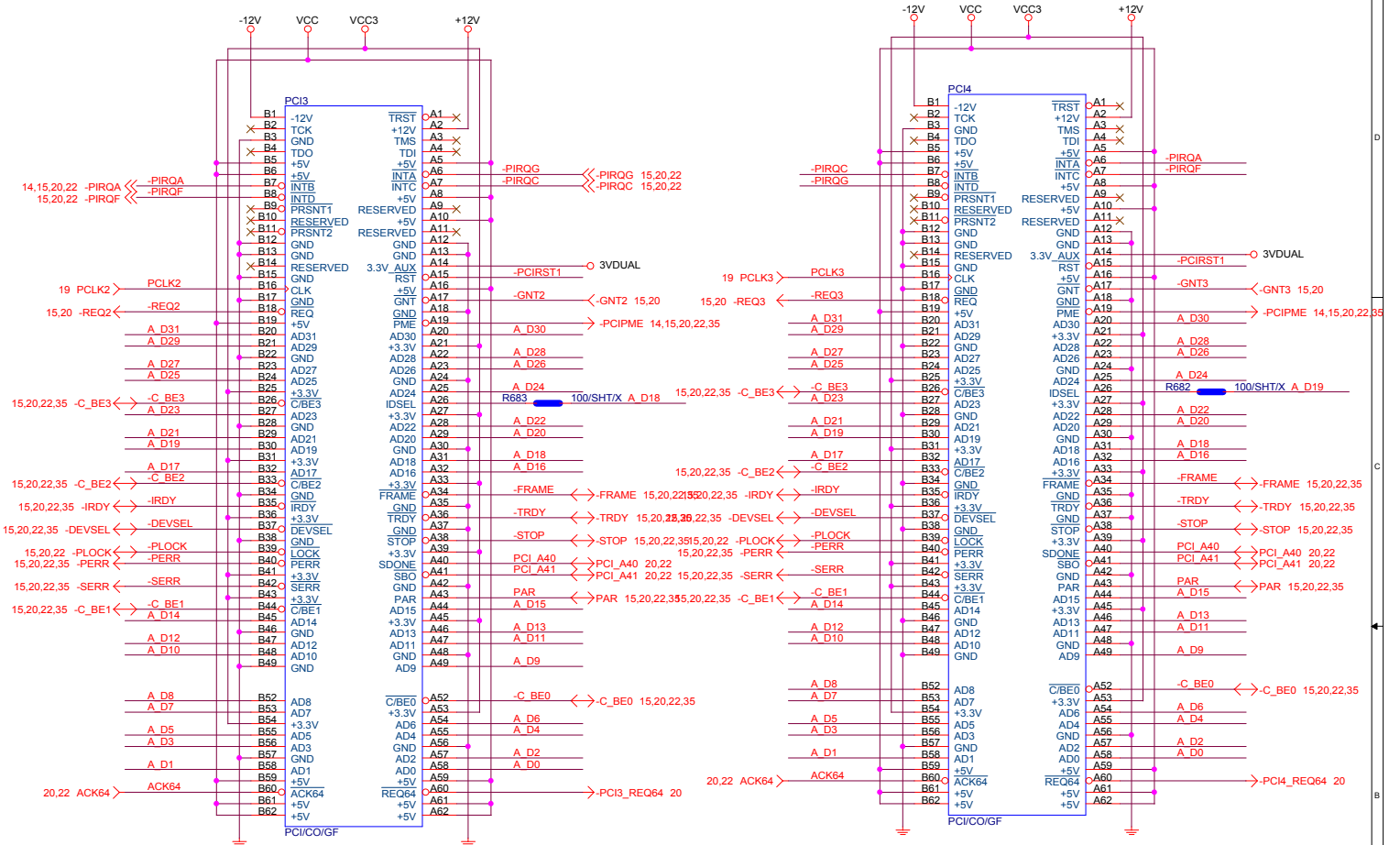


CY28405 上 R1031,R1034,R671
 不上R1030,R1035
 ICS952616上R1030,R1035
 不上 R1031,R1034,R671



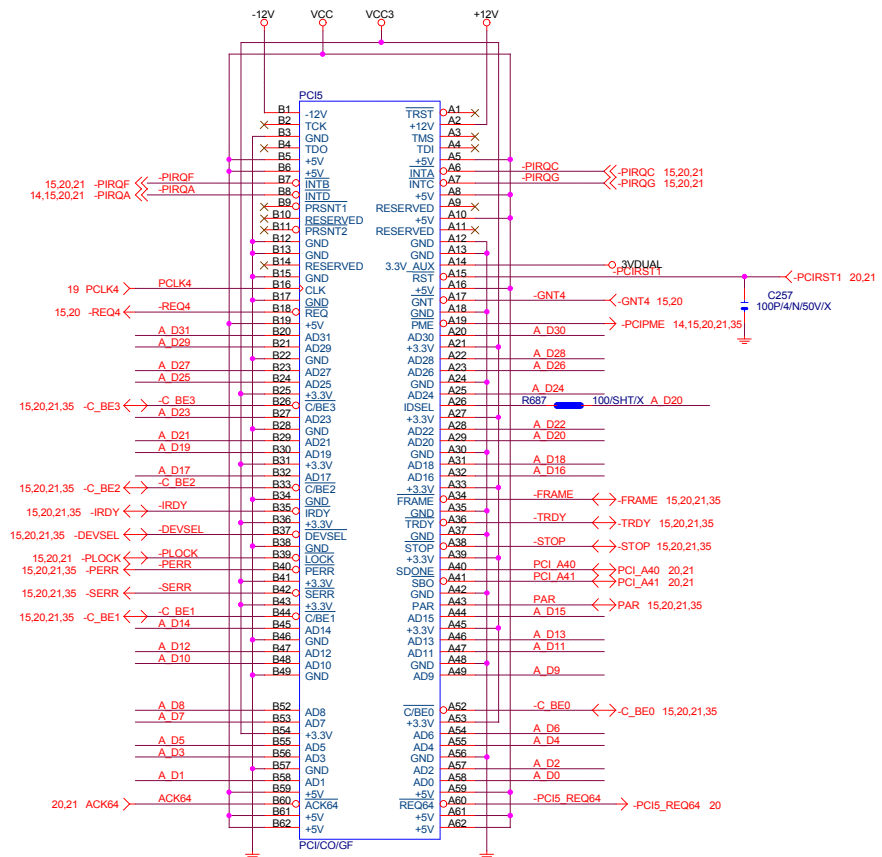
GIGABYTE CORP.		
PCI SLOT 1/2		
Title		
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15,20,22,35 A_D[0..31] << A_D[0..31]



GIGABYTE CORP.		
Title		
PCI SLOT 3/4		
Size	Document Number	Rev
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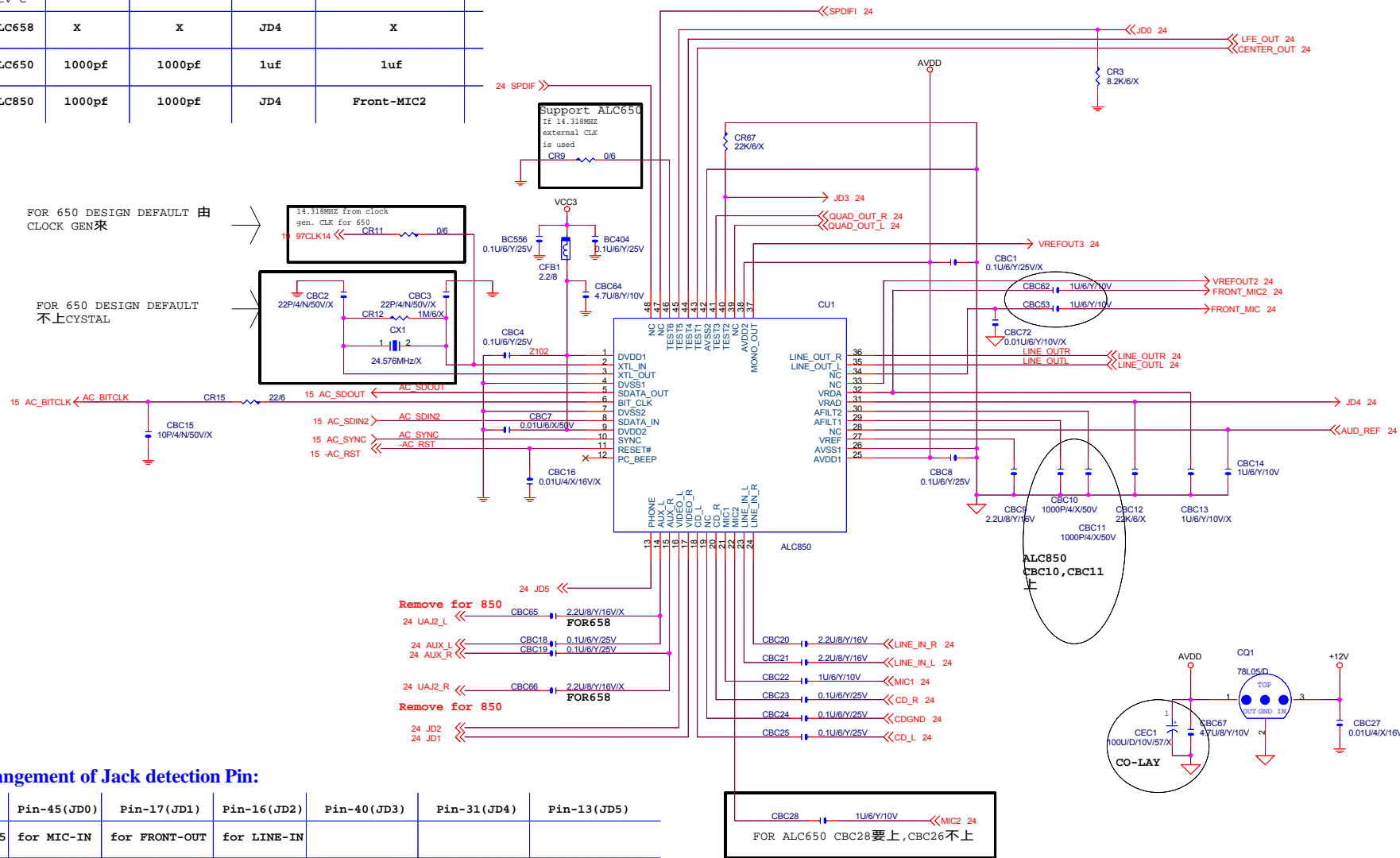
15,20,21,35 A_D[0..31] << A_D[0..31]



GIGABYTE CORP.			
Title			
PCI SLOT 5/6			
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Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf
ALC850	1000pf	1000pf	JD4	Front-MIC2

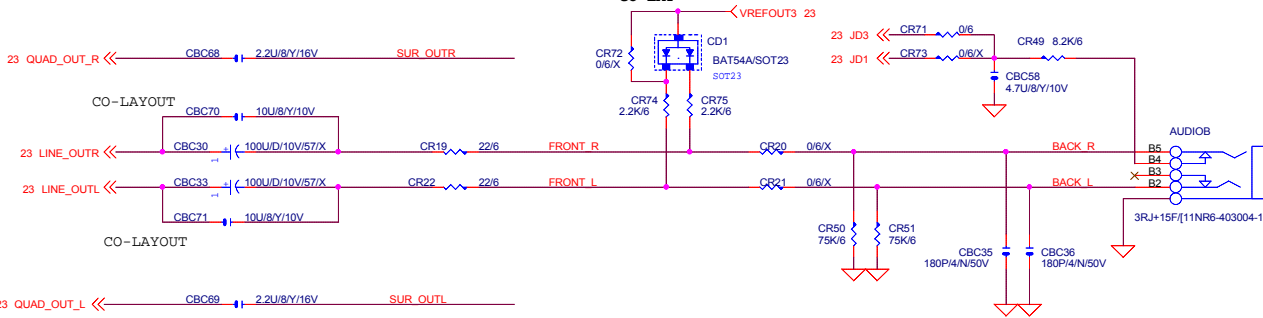


Arrangement of Jack detection Pin:

	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT External pull high is needed	for LINE-IN External pull high is needed	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT	for LINE-IN	for SurrBack Out

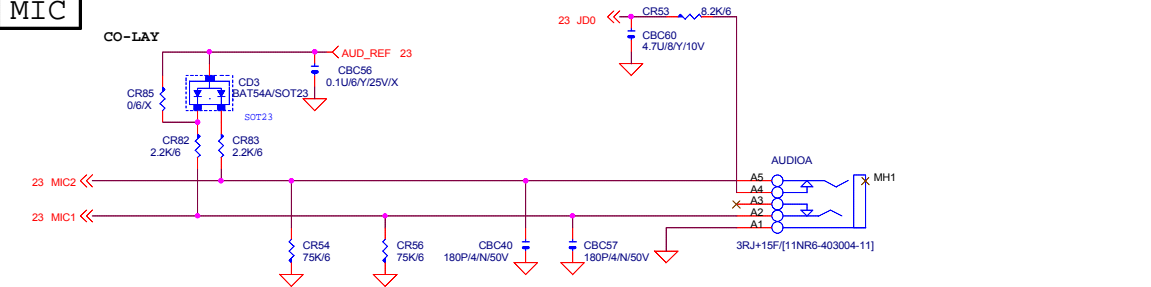
LINE OUT

JDO,JD2,GPIO0 為偵測DEVICE INPUT 時由LOW TO HIGH Edge trigger(pop manual) 1/2(3.14)RC=1/2(3.14)8.2K*4.7U=4.3HZ以上AC 信號全部衰減 TO 0V 不會造成JDO 誤動作(無device 時play wav)



LINE OUT SENSING
R>4K OHM=>POWER SPEAKER
4K OHM>R>400 OHM=>MICROPHONE
R<400 OHM=>HEADPHONE

MIC



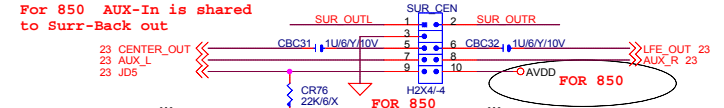
MICROPHONE IN SENSING(當INPUT)(利用vref 偏壓與CR43,CR32 並聯求出阻抗)
7.1k ohm>R>2.3k ohm==>microphone in
R<2.3k ohm or R>7.1k ohm==>unknown device

MICROPHONE IN SENSING(當OUTPUT)
R>4K OHM=>POWER SPEAKER
4K OHM>R>400 OHM=>MICROPHONE
R<400 OHM=>HEADPHONE

2x5 header for 850

For 850 if JD5 = low AUX-In is configured as input
For 850 if JD5 = high AUX-In is configured as output, Surr-Back out

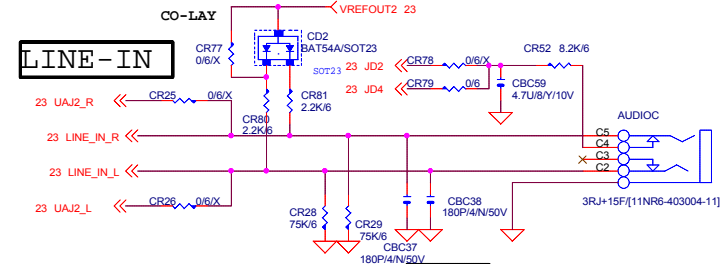
For 850 AUX-In is shared to Surr-Back out



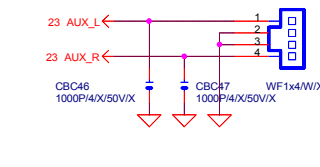
LINE IN SENSING(當OUTPUT)
R>4K OHM=>POWER SPEAKER
4K OHM>R>400 OHM=>MICROPHONE
R<400 OHM=>HEADPHONE

LINE IN SENSING(當INPUT)
swing of input signal>-40dbv(10mv)==>line in device active
swing of input signal<-40dbv(10mv)==>unknown line in device

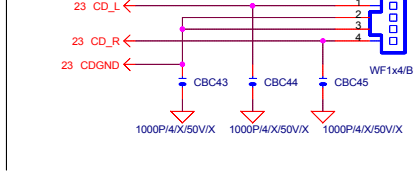
LINE-IN



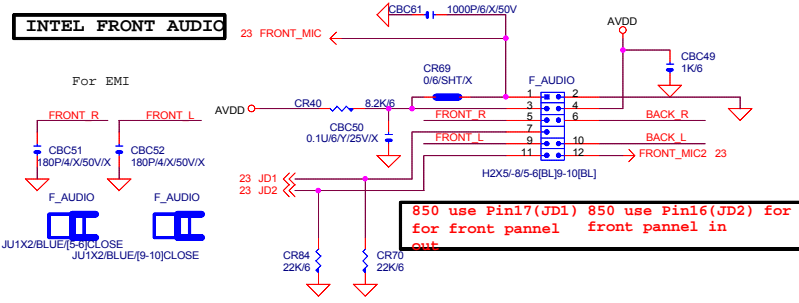
AUX IN DEFAULT NO POP



CD IN

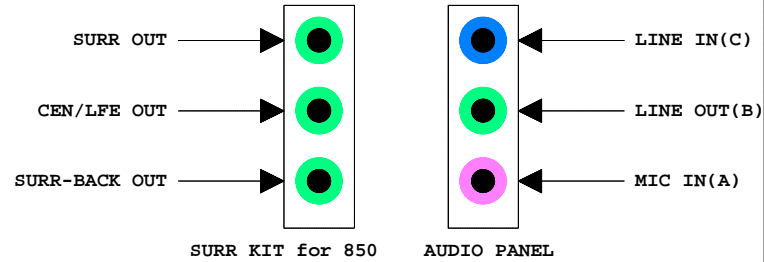
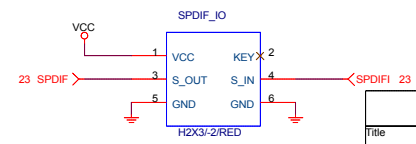


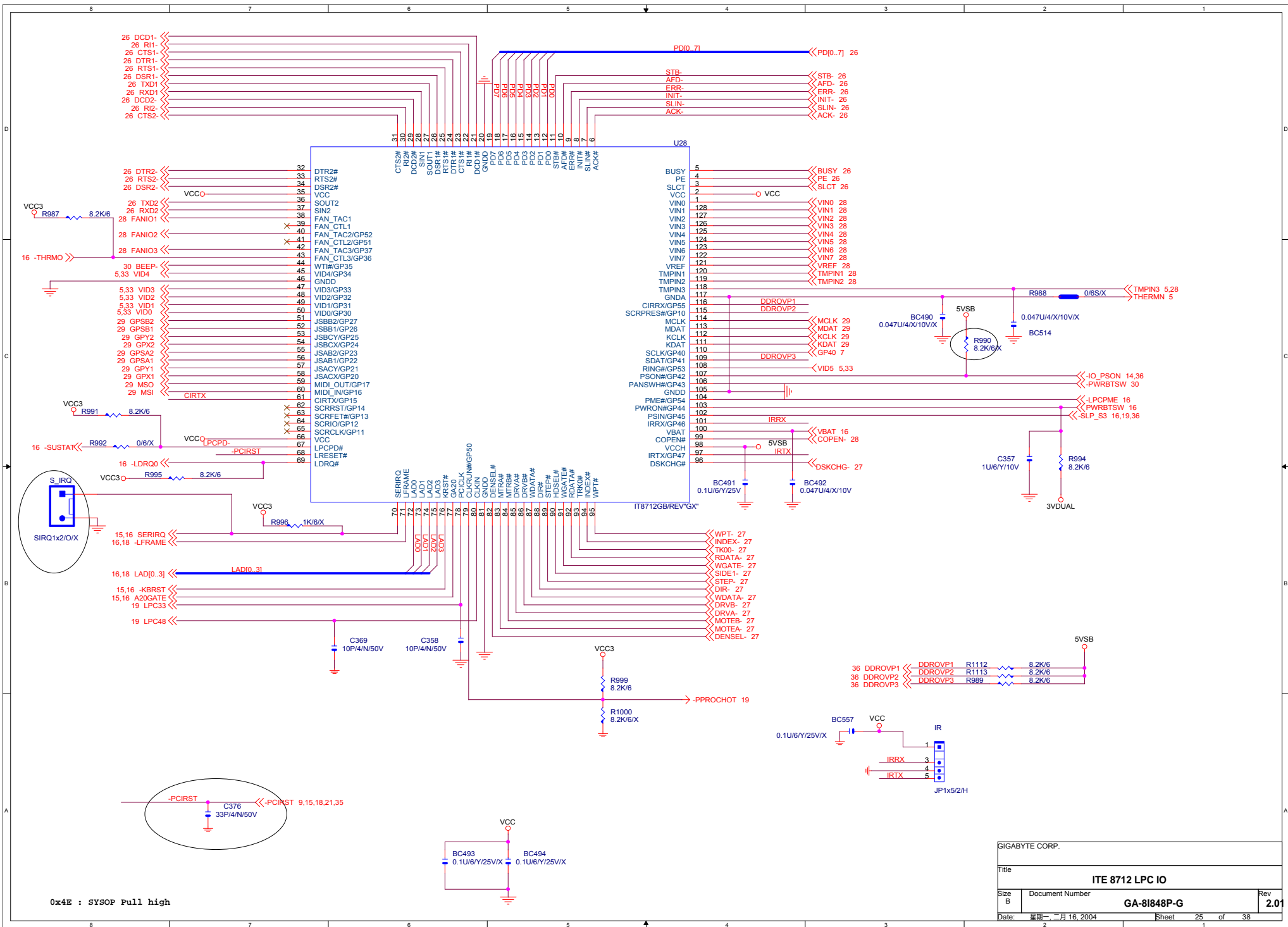
INTEL FRONT AUDIO



850 use Pin17(JD1) 850 use Pin16(JD2) for front panel front panel in out

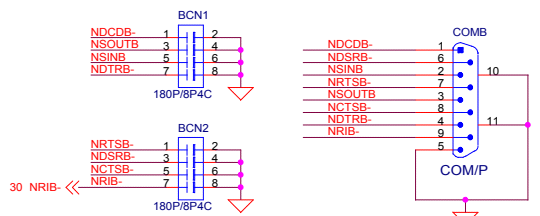
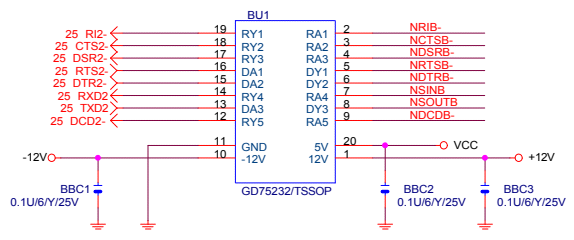
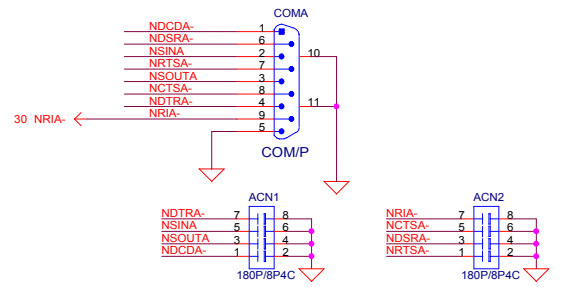
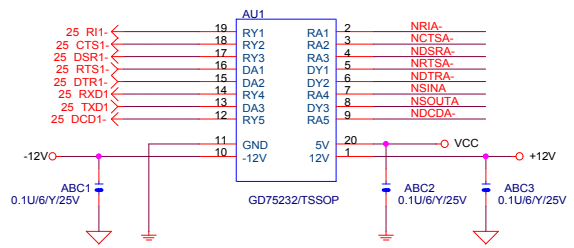
SPDIF IO





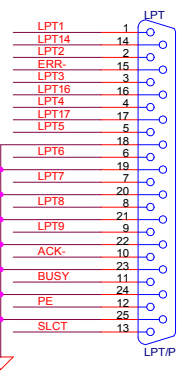
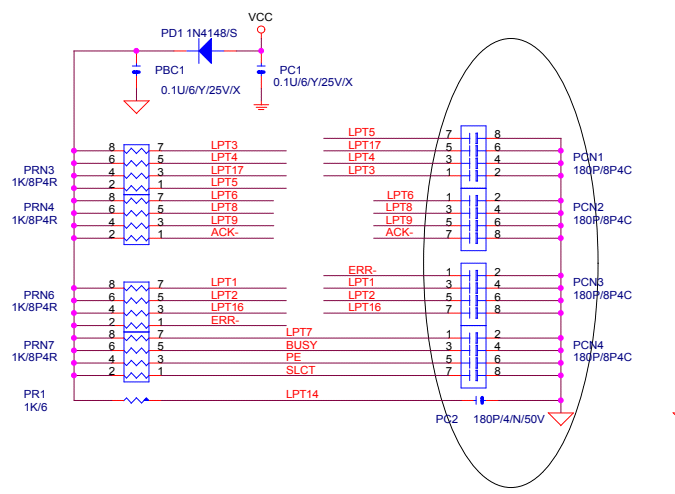
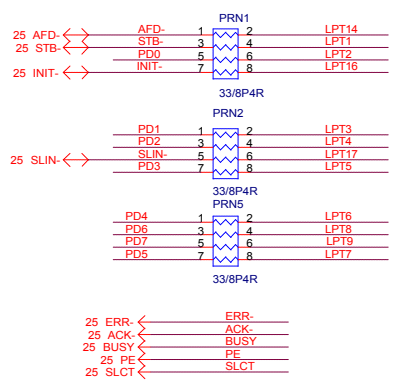
0x4E : SYSOP Pull high

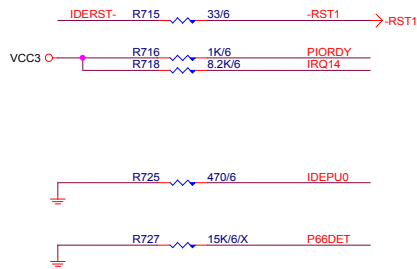
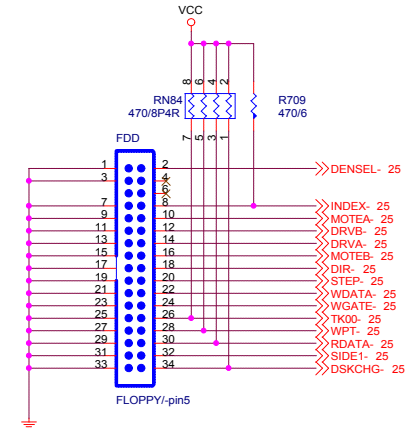
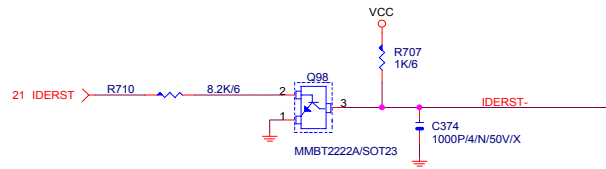
SIGABYTE CORP.		
Title ITE 8712 LPC IO		
Size B	Document Number GA-81848P-G	Rev 2.01
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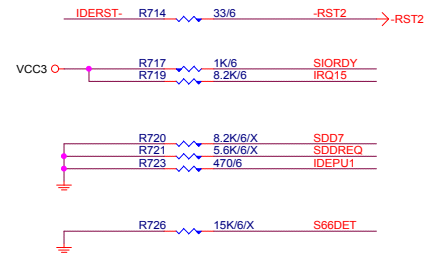
PLACE NEAR VGA_COM CONNECTOR

25 PD[0..7] ↔ PD[0..7]

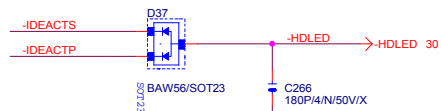
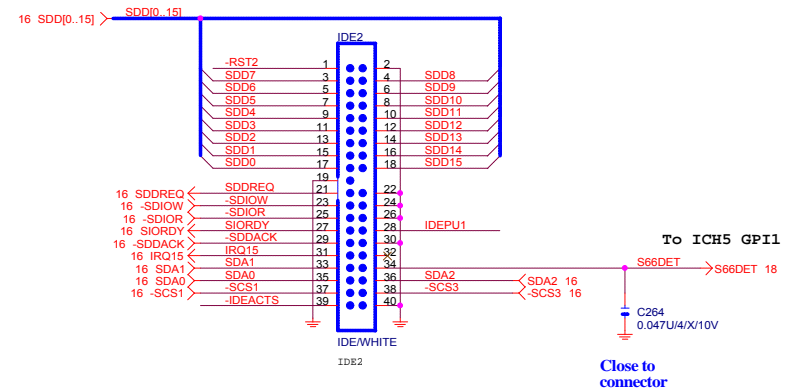
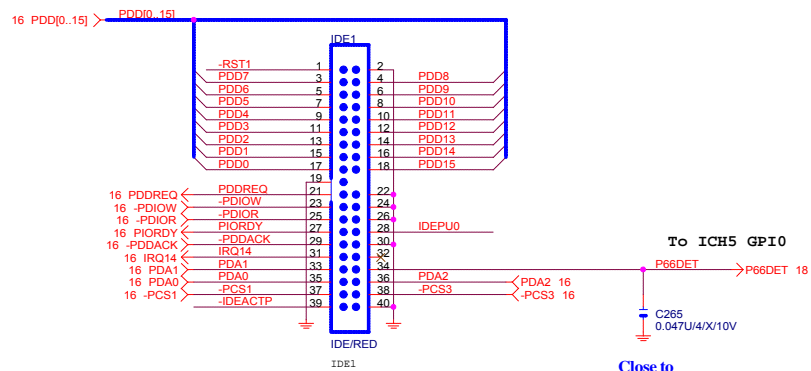




PRIMARY IDE CONNECTOR

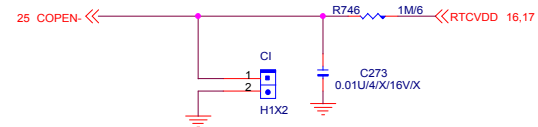
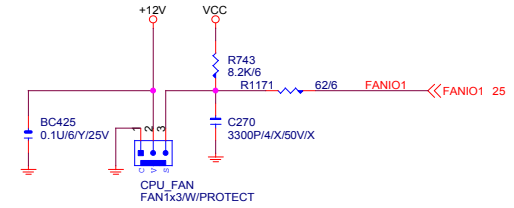
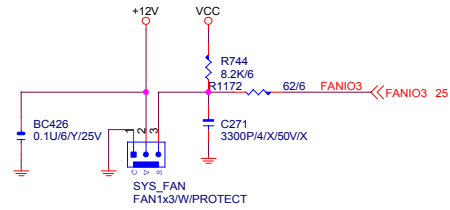
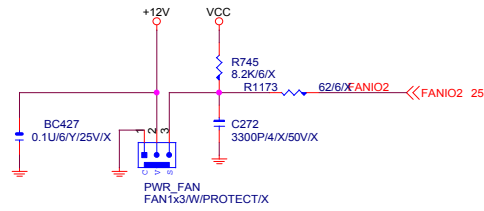
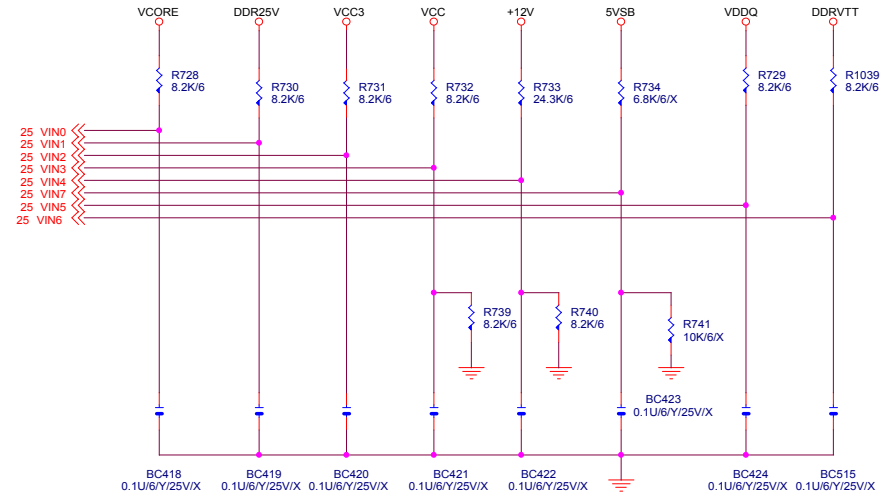
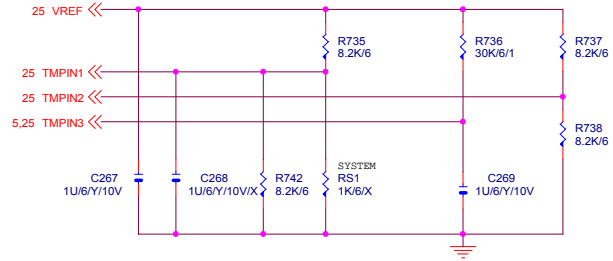


SECONDARY IDE CONNECTOR



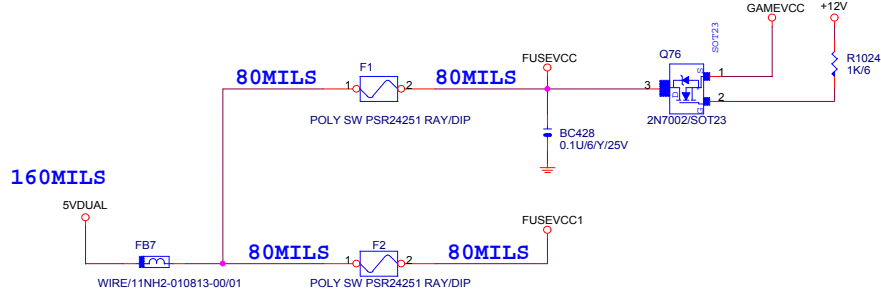
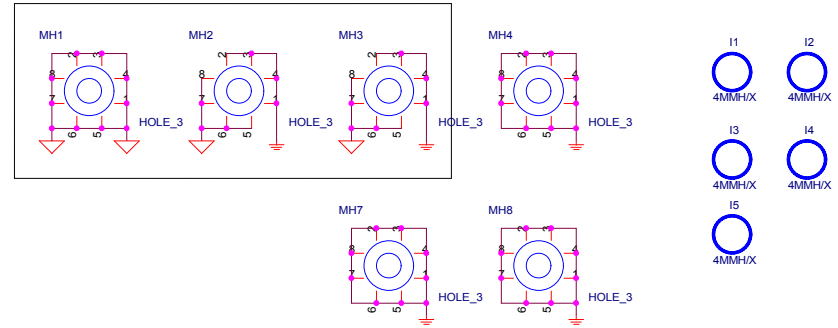
GIGABYTE CORP.		
Title		
IDE CONNECTOR		
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Hardware Monitor circuits

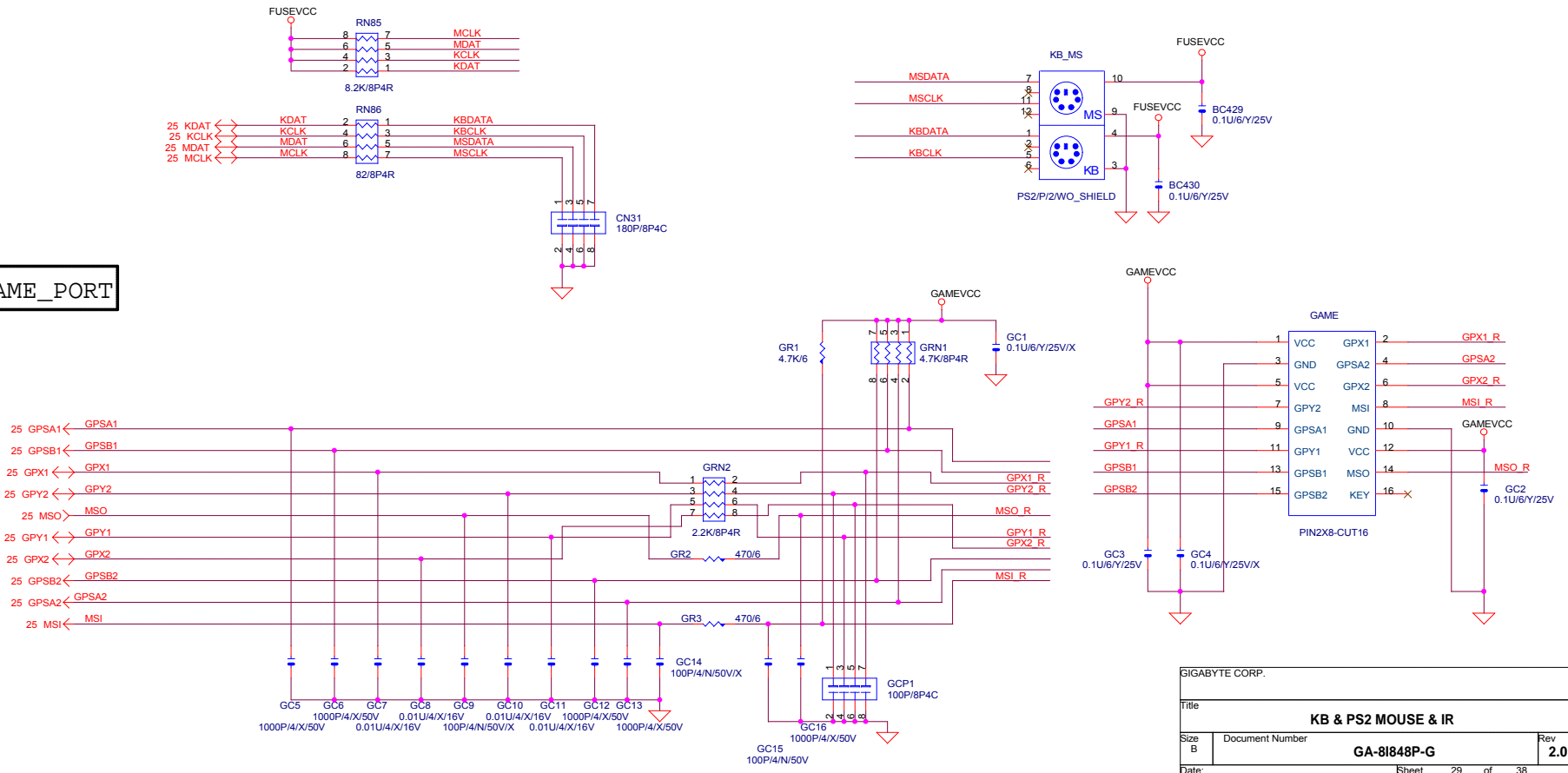


SIGABYTE CORP.		
Title		
FAN/HWMO		
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ATX AGND 與 GND 切割必須有三個

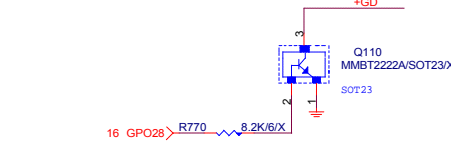
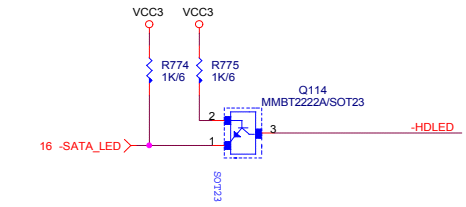
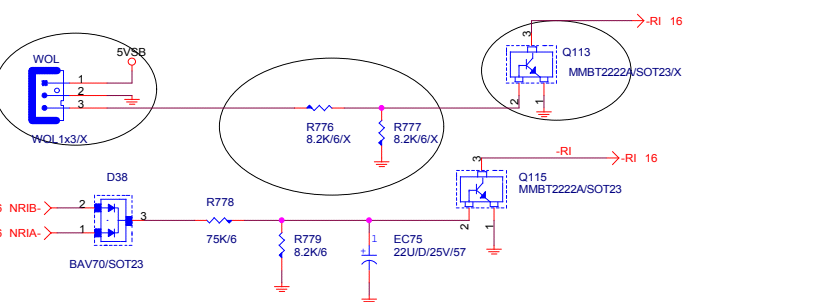
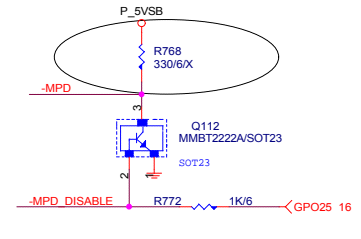
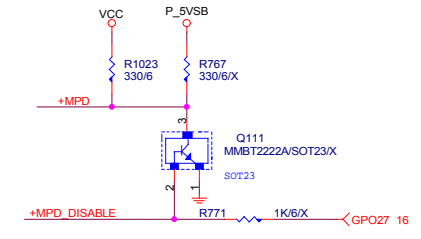
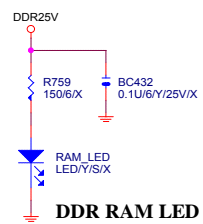
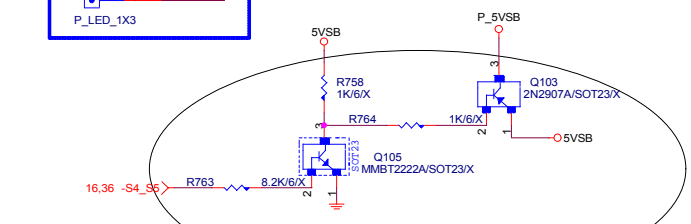
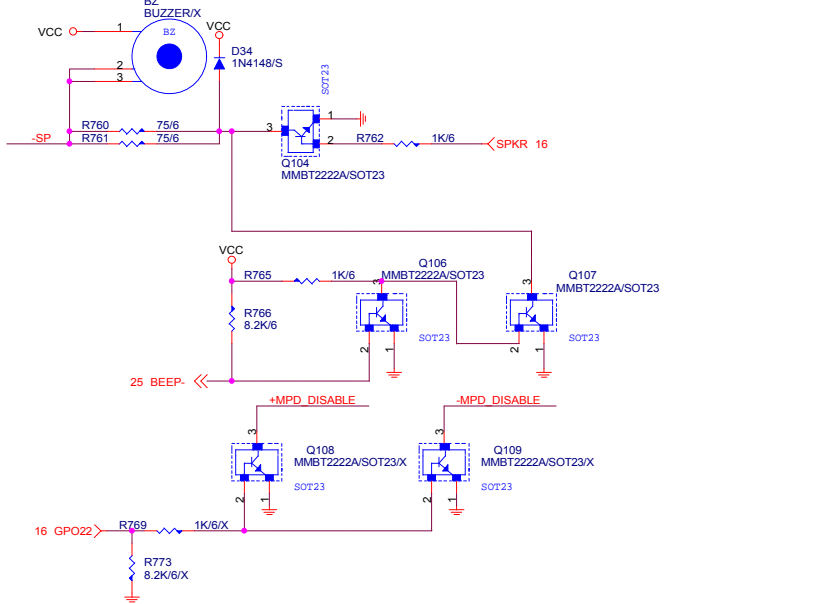
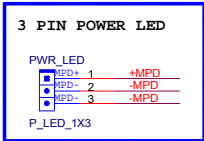
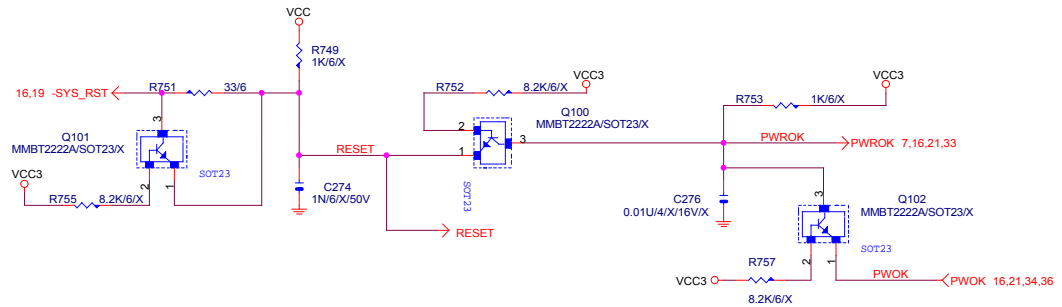
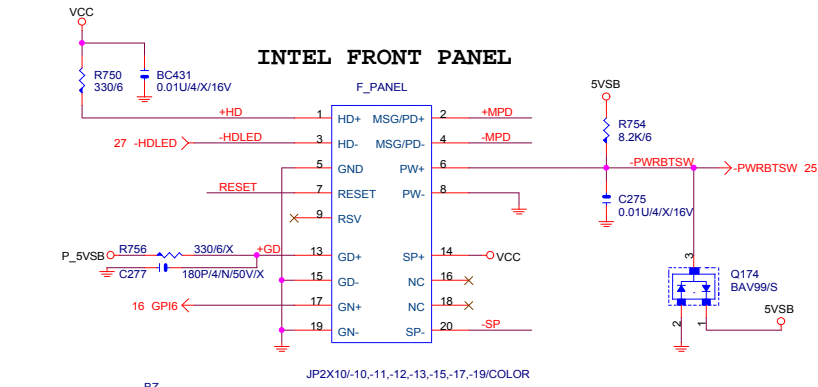


GAME_PORT



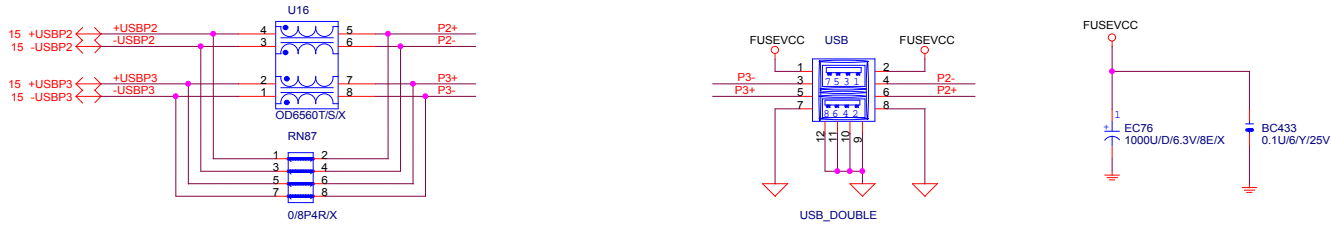
SIGABYTE CORP.		
Title		
KB & PS2 MOUSE & IR		
Size	Document Number	Rev
B	GA-8I848P-G	2.01
Date:	Sheet 29	of 38

INTEL FRONT PANEL

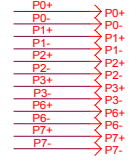
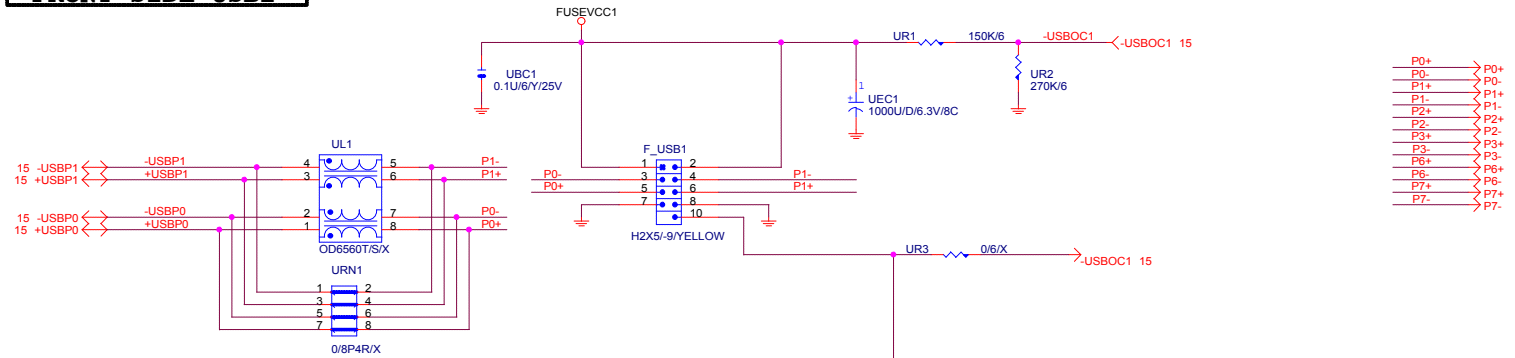


GIGABYTE CORP.		
Title		
PANEL & STR LED & RI		
Size B	Document Number	Rev
	GA-8I848P-G	2.01
Date:	Sheet 30 of 38	

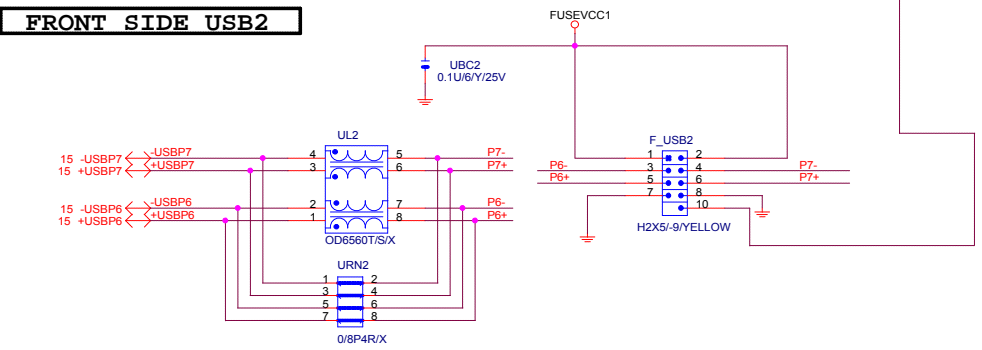
REAR USB



FRONT SIDE USB1

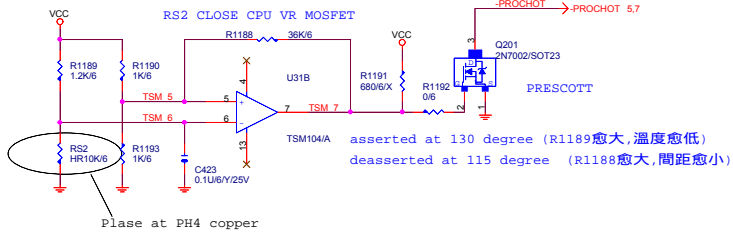


FRONT SIDE USB2



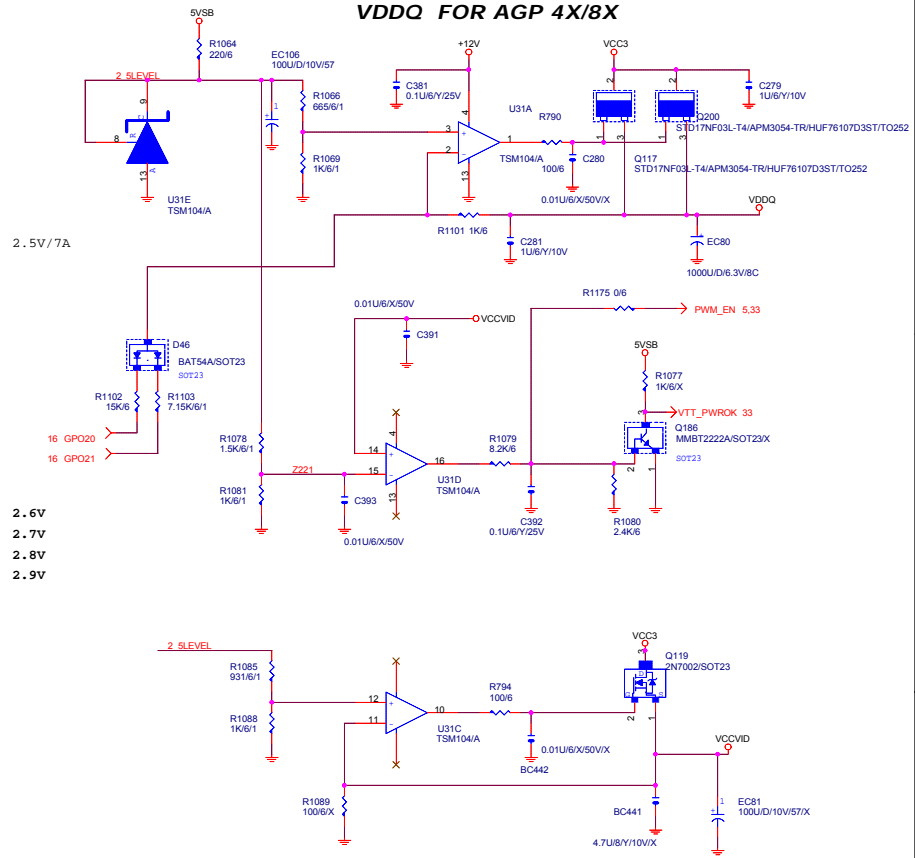
SIGABYTE CORP.		
Title: ICH USB PORT		
Size B	Document Number: GA-8I848P-G	Rev: 2.01
Date:	Sheet: 31	of 38

DDR25V FOR DDR DIMM & NB

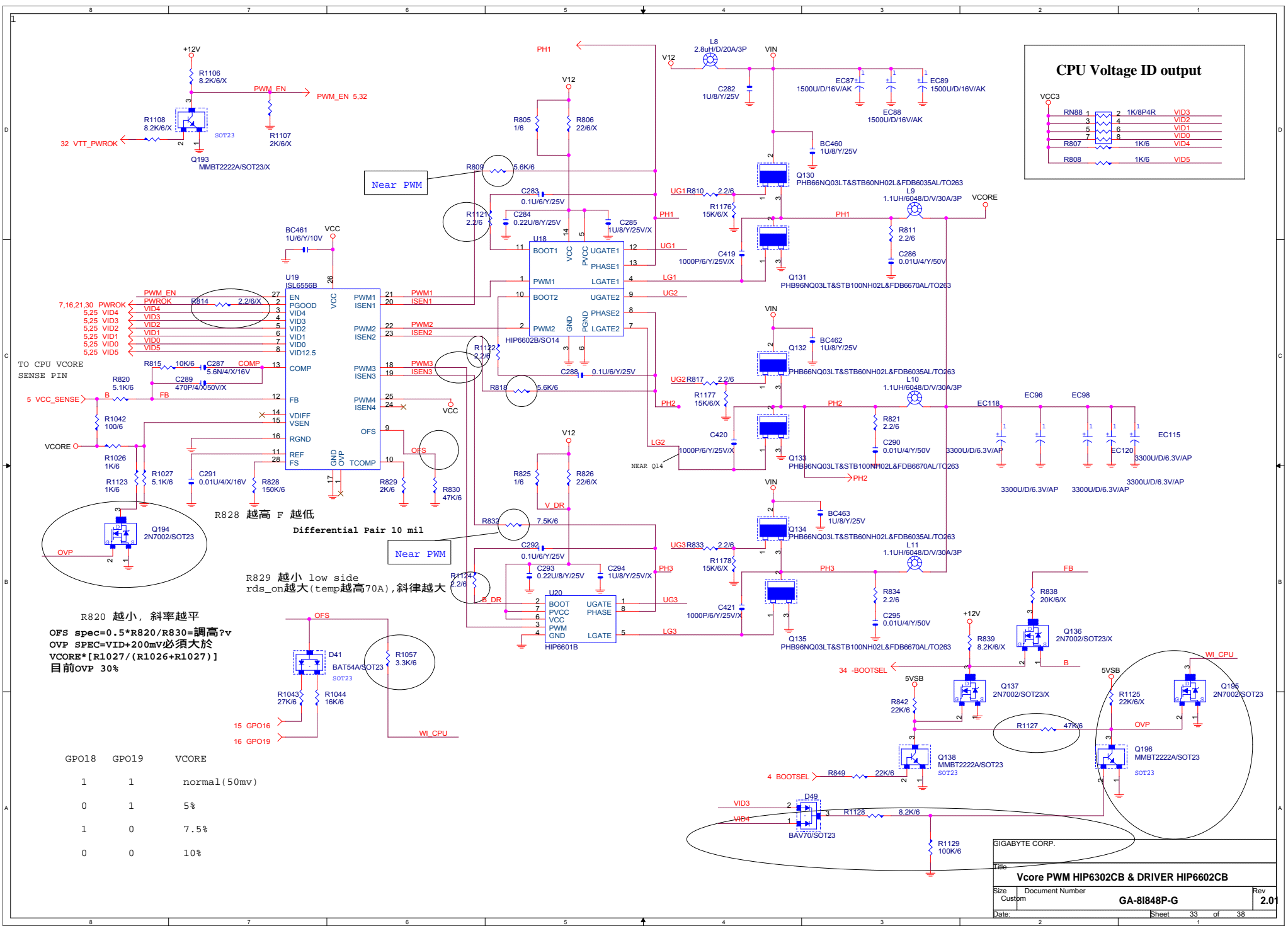
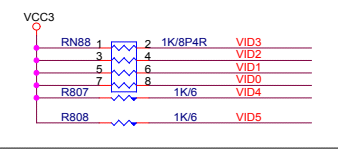


DDROVP1	DDROVP2	
1	1	2.6V
0	1	2.7V
1	0	2.8V
0	0	2.9V

VDDQ FOR AGP 4X/8X



CPU Voltage ID output



32 VTT_PWROK ← R1108 8.2K/6/X
 +12V → R1106 8.2K/6/X → PWM_EN → PWM_EN_5.32
 Q193 MMBT2222A/SOT23/X

Near PWM

7.16,21,30 PWROK → PWROK R814 2.2/6/X
 5.25 VID4 → VID4
 5.25 VID3 → VID3
 5.25 VID2 → VID2
 5.25 VID1 → VID1
 5.25 VID0 → VID0
 5.25 VID5 → VID5

TO CPU VCORE SENSE PIN

5 VCC_SENSE → B

R828 越高 F 越低

Differential Pair 10 mil

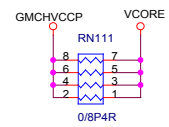
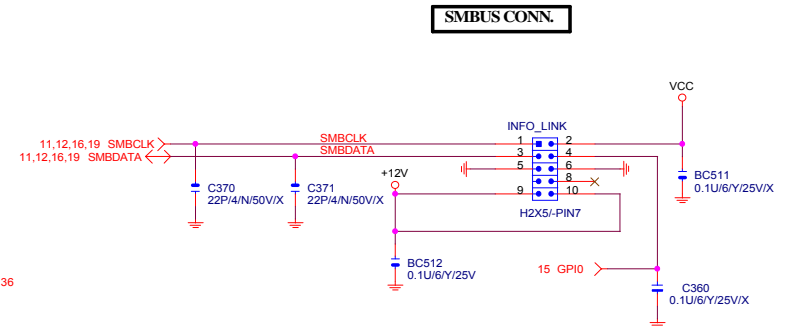
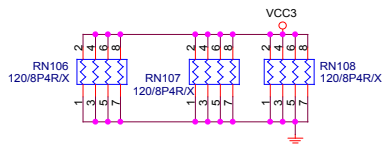
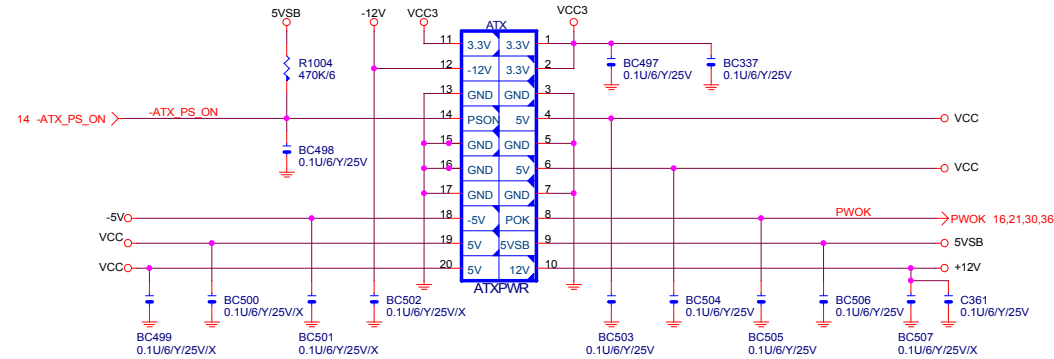
R829 越小 low side rds_on 越大 (temp 越高 70A), 斜律 越大

R820 越小, 斜率 越平

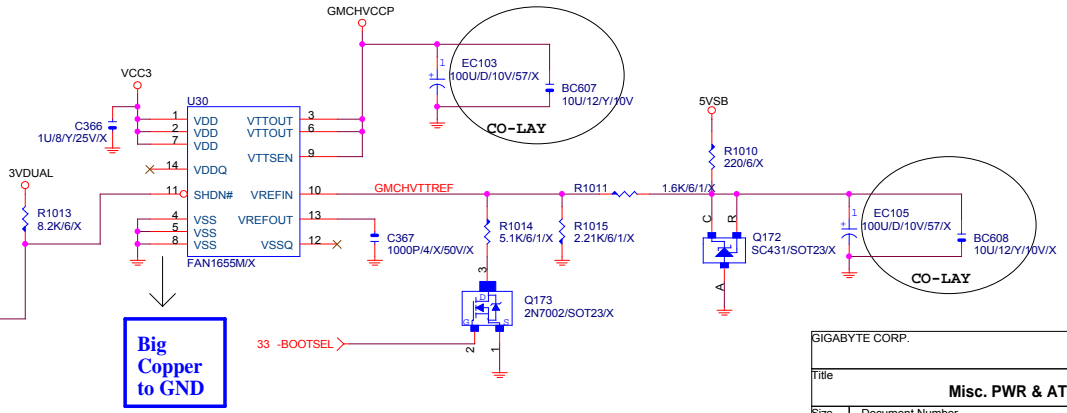
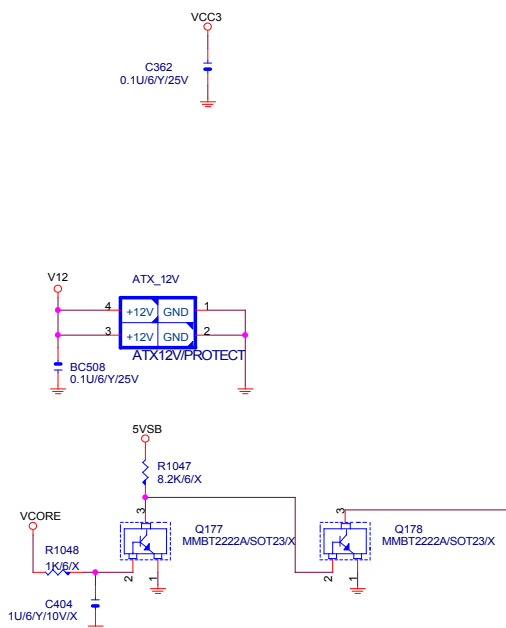
OFS spec = $0.5 * R820 / R830 = \text{調高 } \uparrow v$
 OVP SPEC = $VID + 200mV$ 必須大於 $V_{CORE} * [R1027 / (R1026 + R1027)]$
 目前 OVP 30%

GPO18	GPO19	VCORE
1	1	normal (50mv)
0	1	5%
1	0	7.5%
0	0	10%

ATX POWER CONNECTOR



Northwood:+1.45V
Prescott:+1.225V

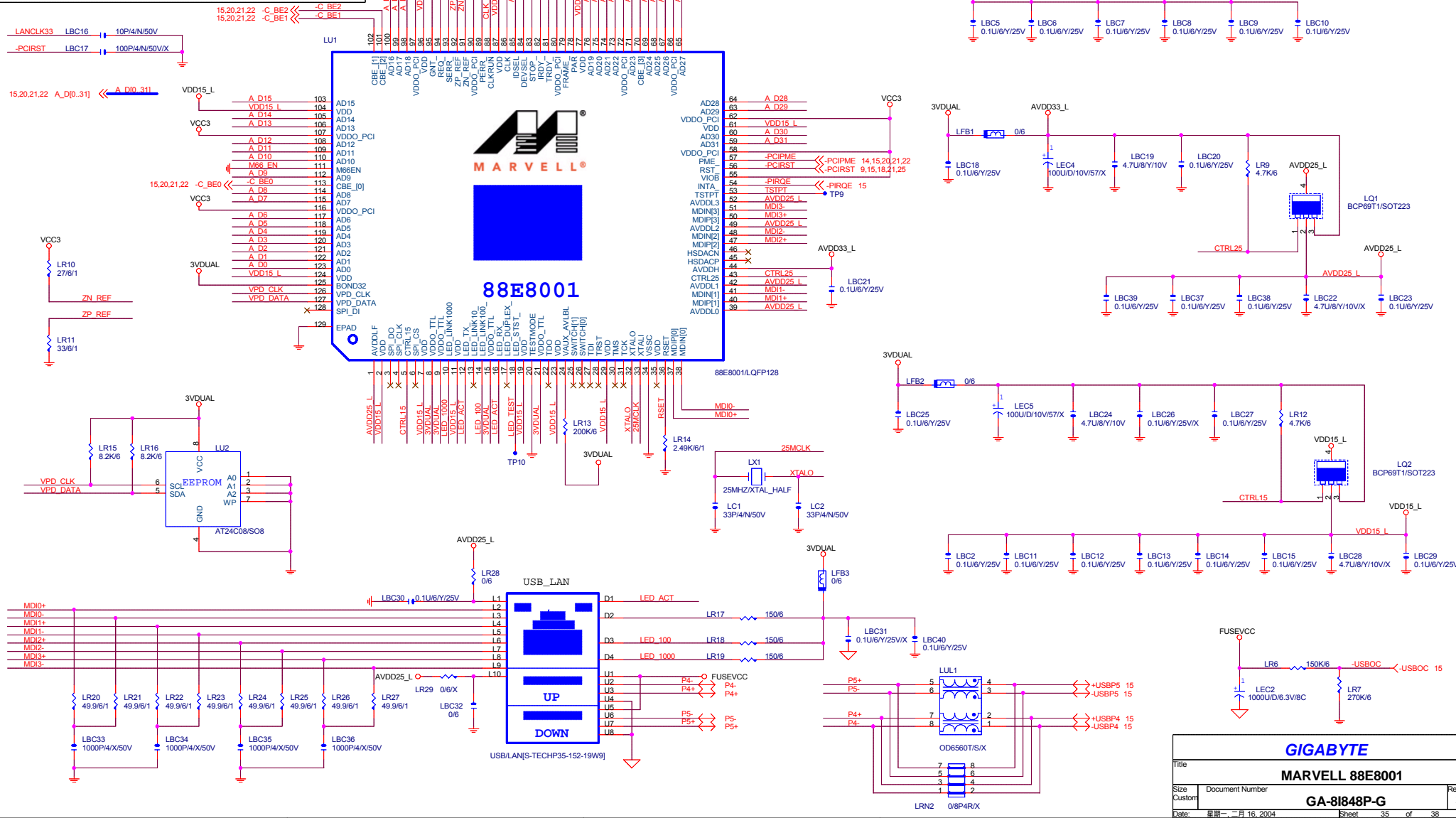


Big Copper to GND

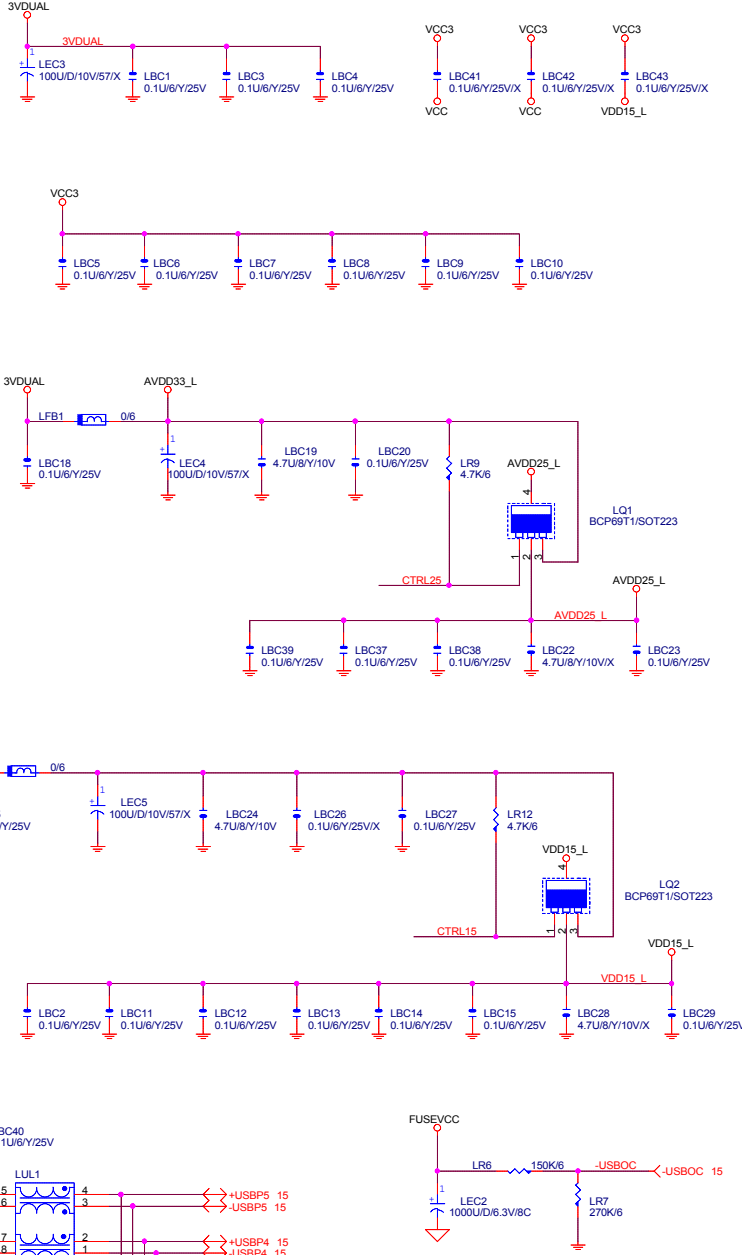
SIGABYTE CORP.		
Title		
Misc. PWR & ATX CONN.		
Size	Document Number	Rev
B	GA-8I848P-G	2.01
Date:	Sheet 34	of 38

Layout Check 注意事項

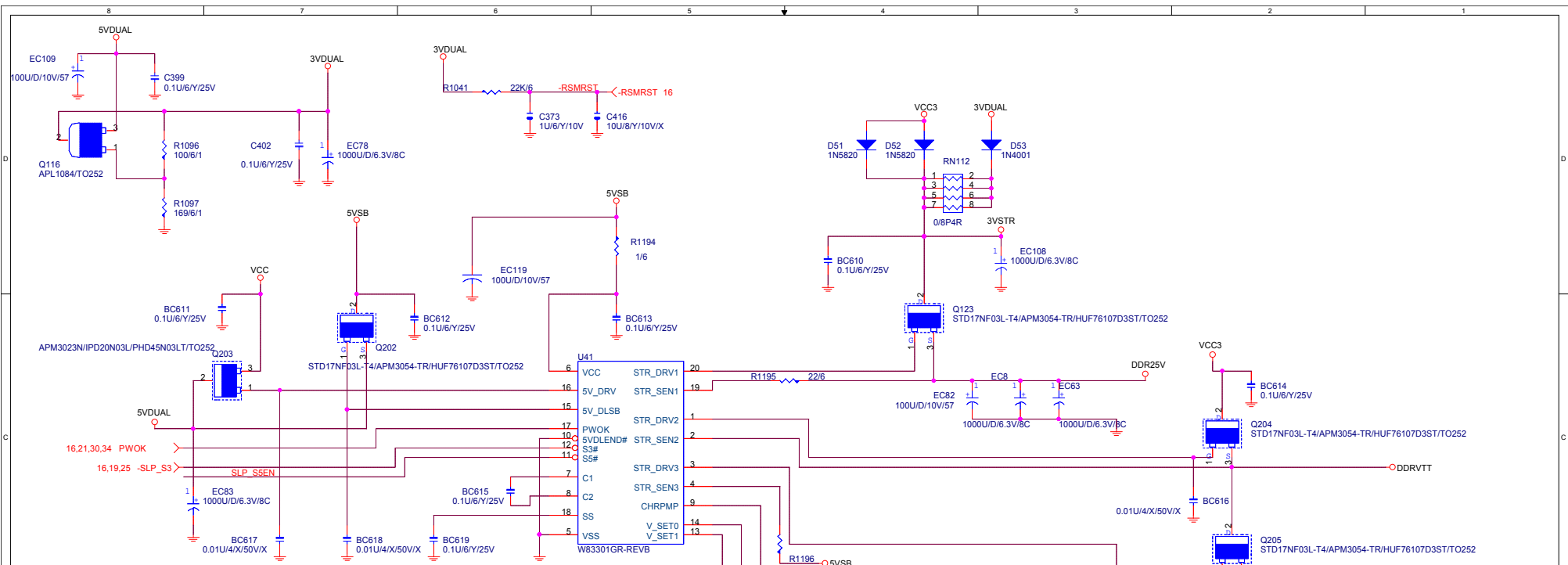
1. LU1 PIN129 需下內層GND,打 12 VIA
2. 3VDUAL, VCC3, VDD15_L, AVDD25_L 至少走20mil寬,並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線,TRACE 愈短愈好,線寬12mil
4. MDI正負0~3,TRACE 8:7:8, 每對之間保持 40mil



POWER DECOUPLING CAP.



Title		
MARVELL 88E8001		
Size	Document Number	Rev
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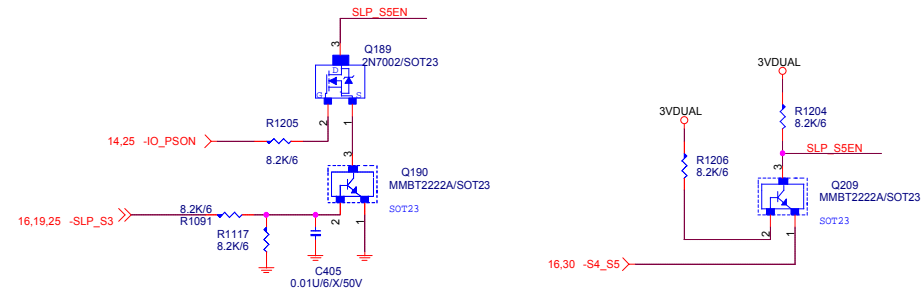


1.25V VTT_DDR LINEAR SOLUTION

DDROVP1, DDROVP2, DDROVP3 RESUME WELL DEFAULT HIGH

	DDROVP2	DDROVP1	DDROVP3	V_SET0	V_SET1
2.5V	HIGH	HIGH	HIGH	0V	0V
2.6V	LOW	HIGH	HIGH	0V	2.5V
2.7V	LOW	LOW	HIGH	0V	5V
2.8V	HIGH	HIGH	LOW	2.5V	0V

FOR 2.8V BIOS PROGRAMMING 時須先PROGRAMMING 2.5V後再PROGRAMMING 2.8V



GIGABYTE GA-8I848P-G PCI ROUNTING LIST

PCI DEVICE	IDSEL	INT	CLOCK	REQ	GNT	
PCI SLOT1	16	C,F,G,A	PCLK0	REQ0-	GNT0-	
PCI SLOT2	17	F,G,A,C	PCLK1	REQ1-	GNT1-	
PCI SLOT3	18	G,A,C,F	PCLK2	REQ2-	GNT2-	
PCI SLOT4	19	A,C,F,G	PCLK3	REQ3-	GNT3-	
PCI SLOT5	20	C,F,G,A	PCLK4	REQ4-	GNT4-	
LAN (Marvell)	25	E	LANCLK33	-REQ5 (REQB#)	-GNT5 (GNTB#)	

GIGABYTE GA-8I848P-G GPIO LIST

SHEET

TITLE

GPIIP	I/O	FUNCTION
GPI0/REQA-	I	PULL HIGH 8.2K to VCC3, SMB connector.
GPI1/REQ5-		PULL HIGH 8.2K to VCC, REQ5-.
GPI2/PIRQE-		PULL HIGH 8.2K to VCC3, PIRQE-.
GPI3/PIRQF-		PULL HIGH 8.2K to VCC3, PIRQF-.
GPI4/PIRQG-		PULL HIGH 8.2K to VCC, PIRQG-.
GPI5/PIRQH-	NA	PULL HIGH 8.2K to VCC
GPI6/AGPBUSY-	I	PULL 8.2K TO VCC3, PANEL GREEN_BUTTON
GPI7	I	DUAL BIOS FIRST BOOT SELECT.
GPI8	I	PULL 8.2K TO 3VDUAL, -CASPME.
GPI9/OC4-	NA	USB OC4-.
GPI10/OC5-	NA	USB OC5-.
GPI11/-SMBALRT	NA	PULL 8.2K TO 3VDUAL,-SMBALERT.
GPI12	I	PULL 8.2K TO VCC3,M/B REVERSION ID.
GPI13	I	LPC PME.
GPI14/OC6-	NA	USB OC6-.
GPI15/OC7-	NA	USB OC7-.
GPO16/GNTA-	NA	GPO16.
GPO17/GNT5-		GNT5-.
GPO18/STP_PCI-	NA	GPO18.
GPO19/SLP_S1-	O	DUAL BIOS.
GPO20/SLP_CPU-	O	DUAL BIOS.
GPO21/C3_SATA-	O	BLOCK TOP TABLE.
GPO22/CPUPERF-	O	PULL 8.2K TO VCC3,PANEL S3 POWER LED.

SHEET

TITLE

GPIIP	I/O	FUNCTION
GPO16		PULL 8.2K TO VCC3
GPO17		PULL 8.2K TO VCC3 (GNT5-)
GPO18		PULL 8.2K TO VCC3
GPO19		PULL 8.2K TO VCC3
GPO20		PULL 8.2K TO VCC3
GPO21		PULL 8.2K TO VCC3
GPO22		PULL 8.2K TO VCC3
GPO23		PULL 8.2K TO VCC3
GPO24		PULL 1K TO 3VDUAL (TOP BLOCK)
GPO25		PULL 4.7K TO 3VDUAL, LAN 100/10 DETECT.
GPO26		NOT IMPLEMENTED
GPO27		PULL 8.2K TO 3VDUAL, BIOS WRITE PROTECT.
GPO28		PULL 8.2K TO 3VDUAL