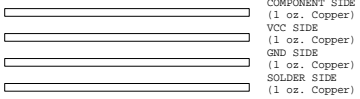


GIGABYTE GA-8I848E Schematics

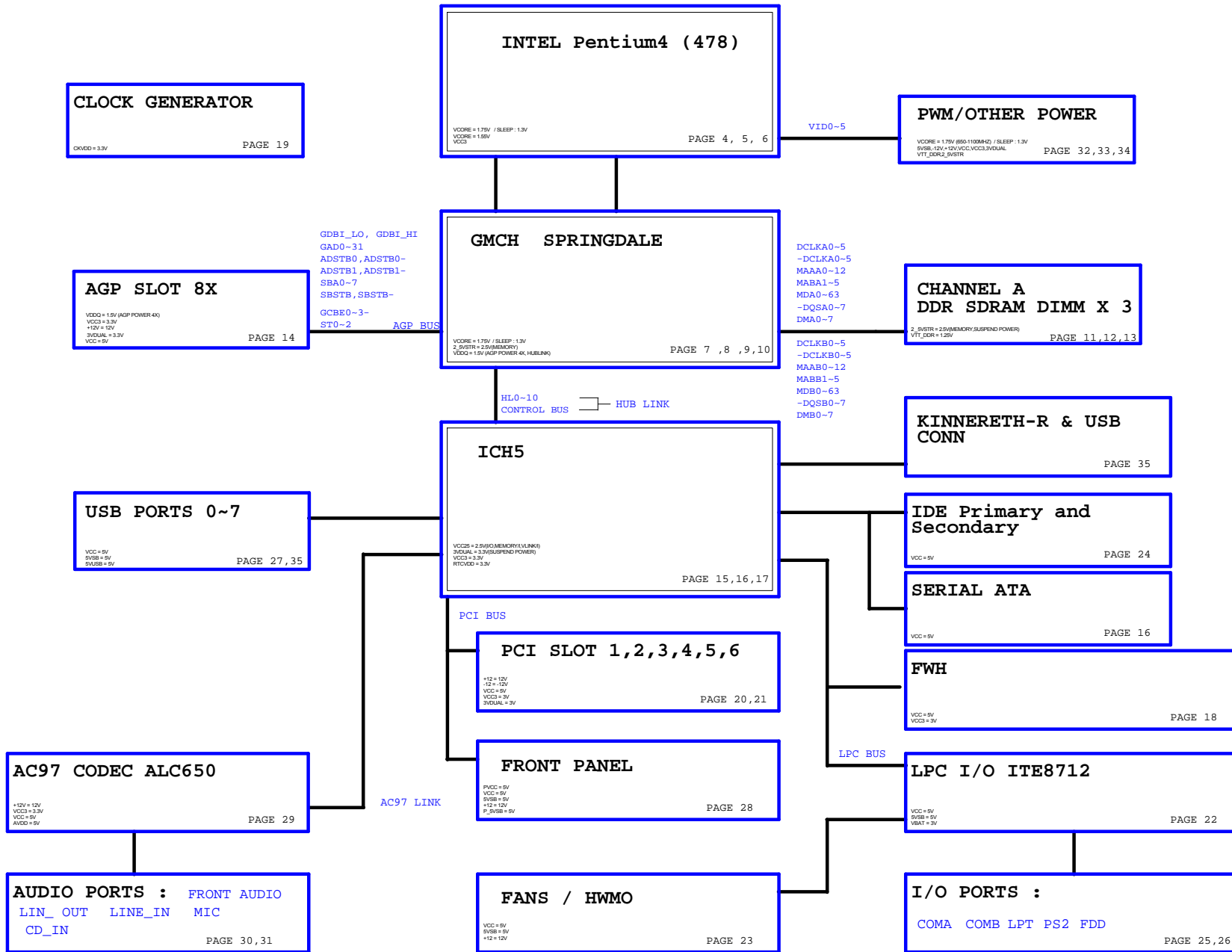
Revision
1.01

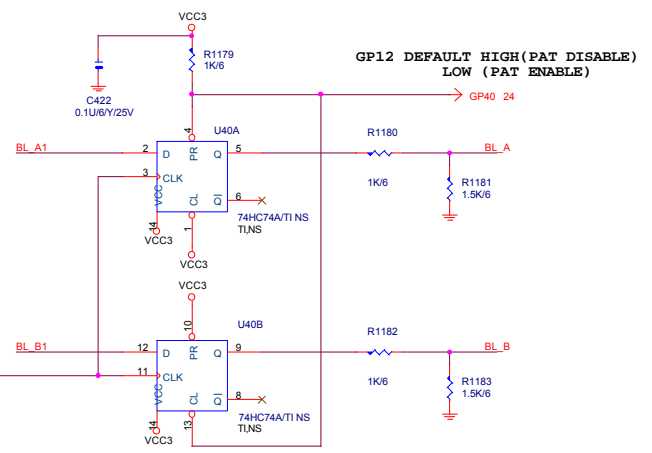
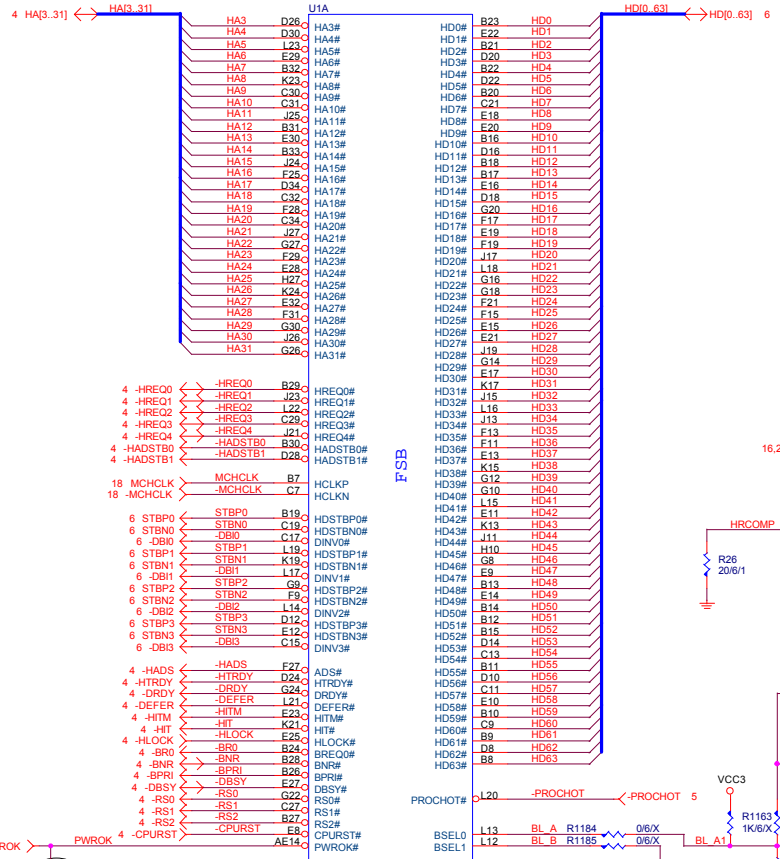
SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	P4_478A
05	P4_478B
06	P4_478C
07	SPRINGDALE HOST
08	SPRINGDALE DDR
09	SPRINGDALE AGP, HUB, CSA, VGA
10	SPRINGDALE PWR
11	DDR1,2 CHANNEL A
12	DDR3 CHANNEL A
13	DDR TERMINATION
14	AGP
15	ICH5 PCI, USB, HUB, LAN
16	ICH5 IDE, GPIO, SATA, CTRL
17	ICH5 VCC, GND
18	FWH
19	ICS952603 CLOCK GEN
20	PCI1_2
21	PCI3_4
22	PCI5_6

SHEET	TITLE
23	CODEC
24	AUDIO JACK, L_OUT, F_AUDIO
25	ITE 8712
26	COM_LPT
27	IDE
28	FAN/HWMO
29	KB_PS2
30	FPANEL
31	USB CONN
32	DDR POWER
33	VCORE POWER
34	ATX, OTHERS POWER
35	KINNERETH-R LNA(CSA-1)
36	KINNERETH-R LNA(CSA-2)
37	KINNERETH-R LNA(CSA-3)

		
GIGABYTE CORP.		
Title COVER SHEET		
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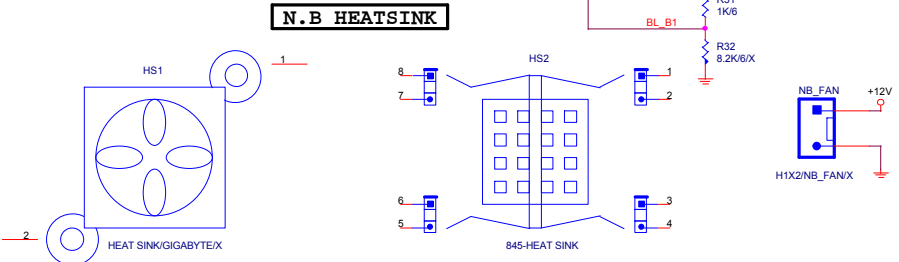
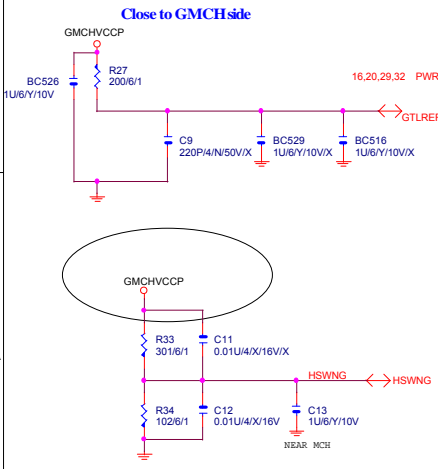
BLOCK DIAGRAM



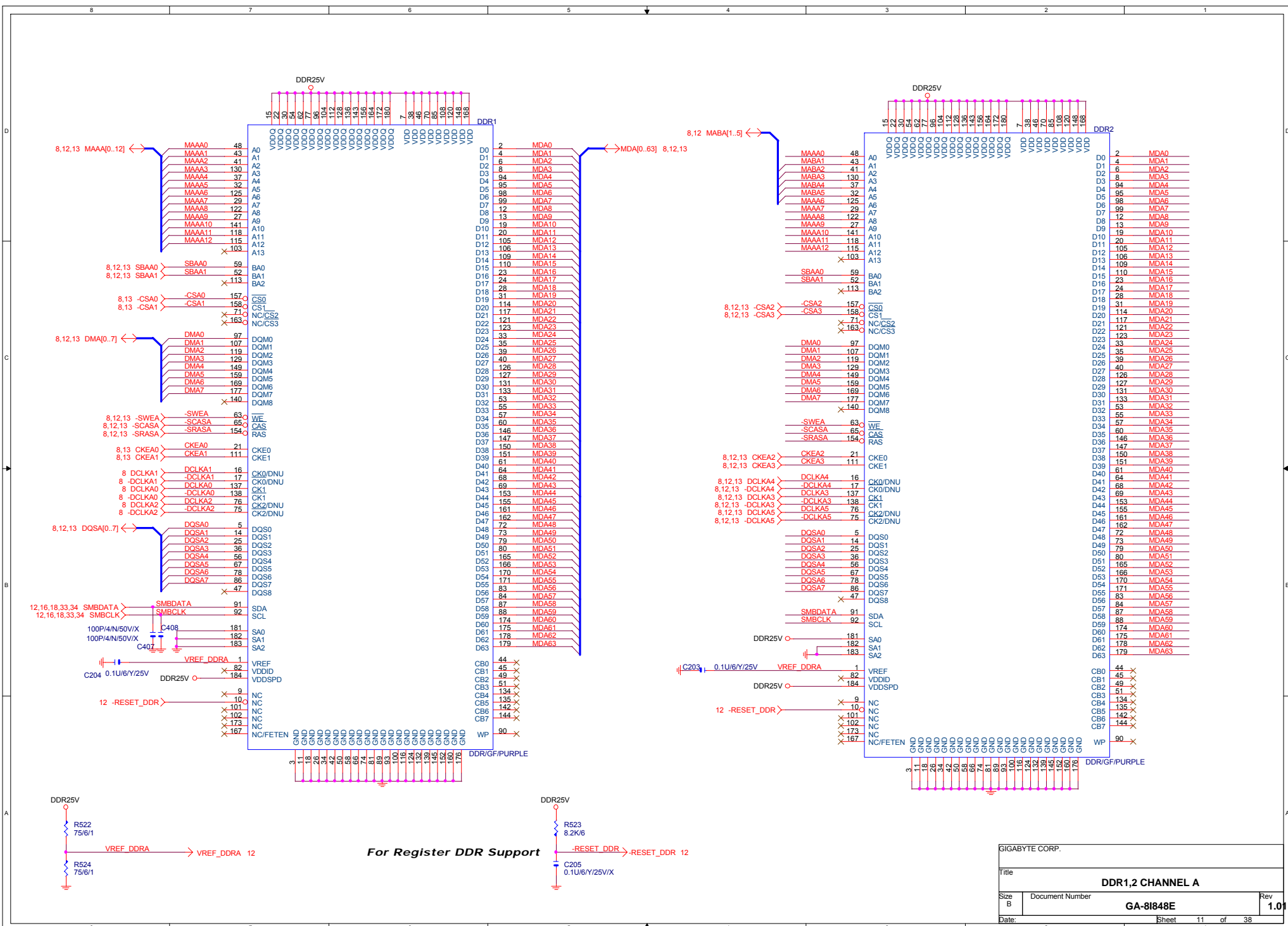


	100	133	200
FS_A	L	H	L
FS_B	L	L	H
X2 (NO)	X2		X1.33
X2.66	X2.5		X1.6
			X2

FOR SPD P (533MHZ)
REMOVE R28,R31
ADD R1163,U39,

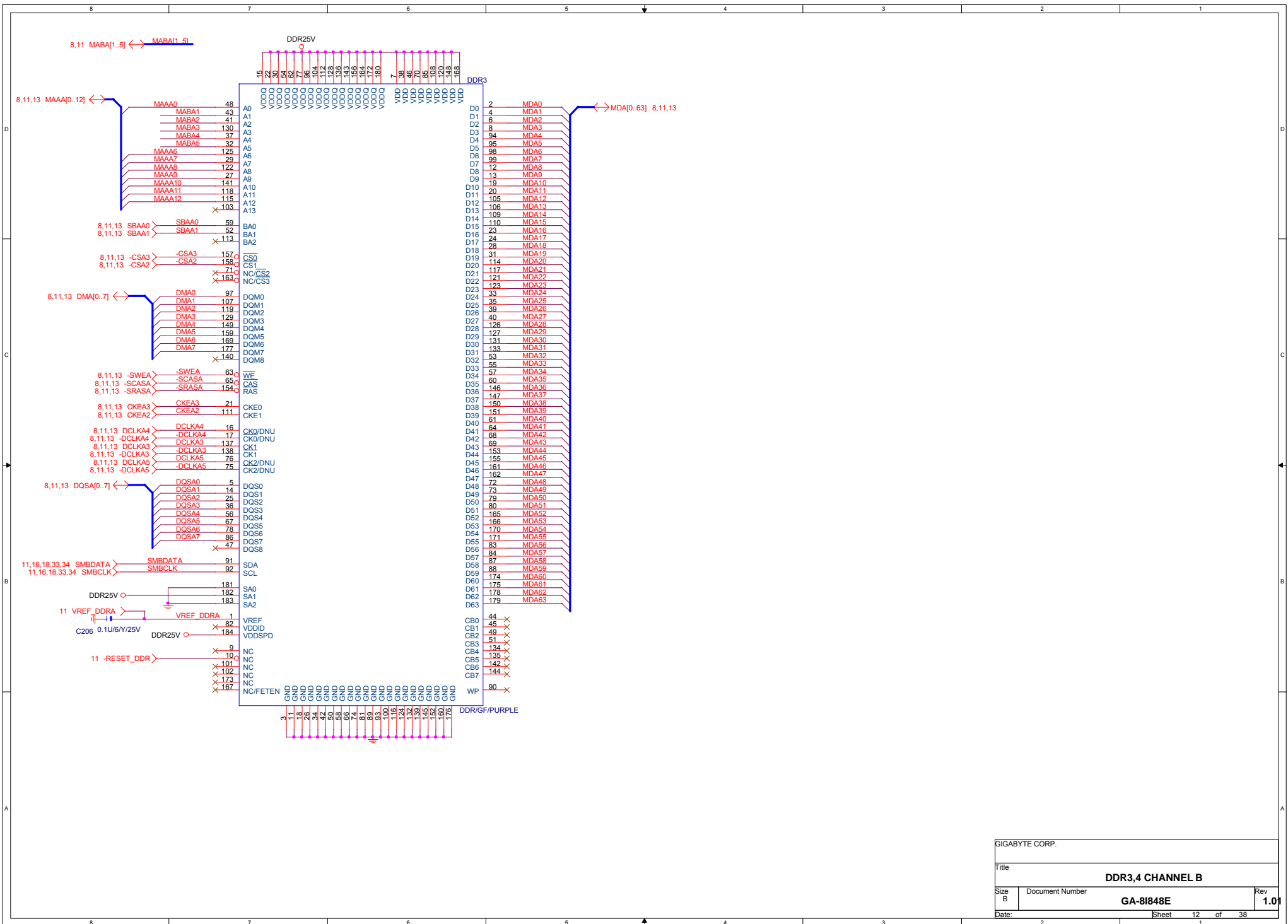


N.B HEATSINK



For Register DDR Support

GIGABYTE CORP.		
Title		
DDR1,2 CHANNEL A		
Size	Document Number	Rev
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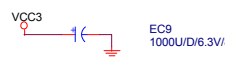
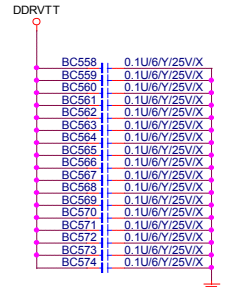
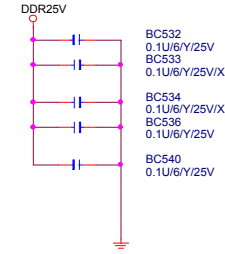
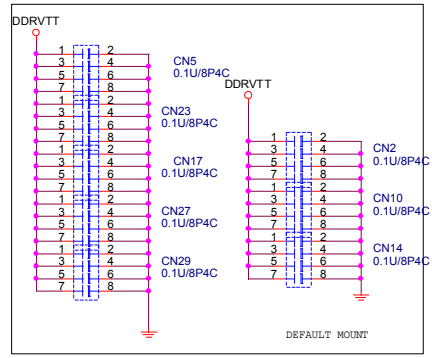
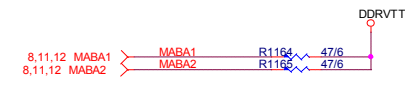
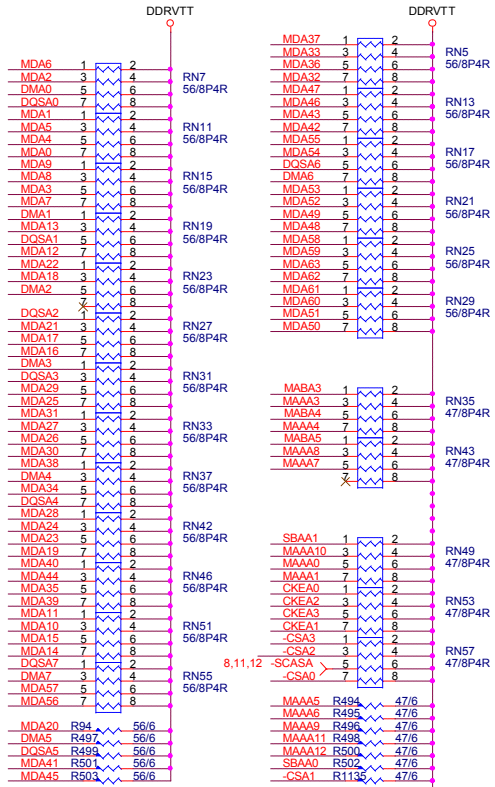
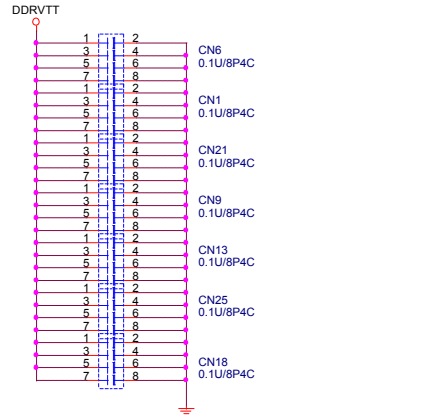


DDRVTT Decouple

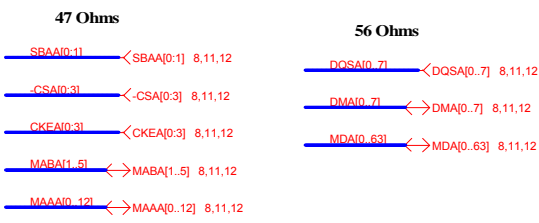
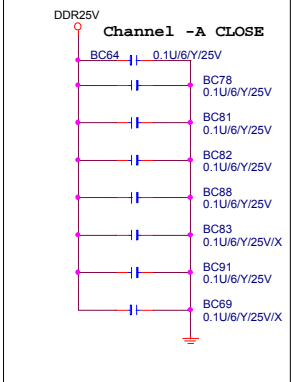
DDR TERMINATION CHANNEL A

DDRVTT Decouple

CHANNEL B

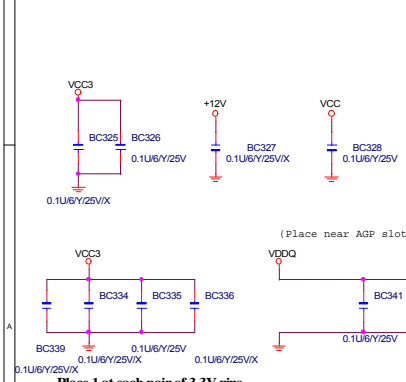
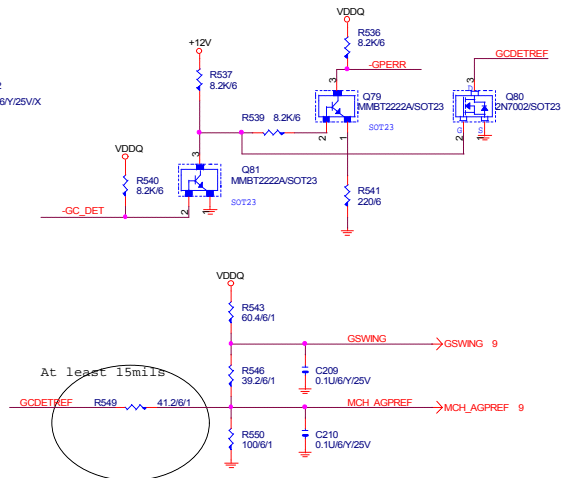
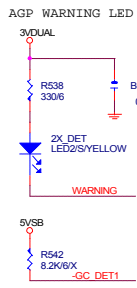
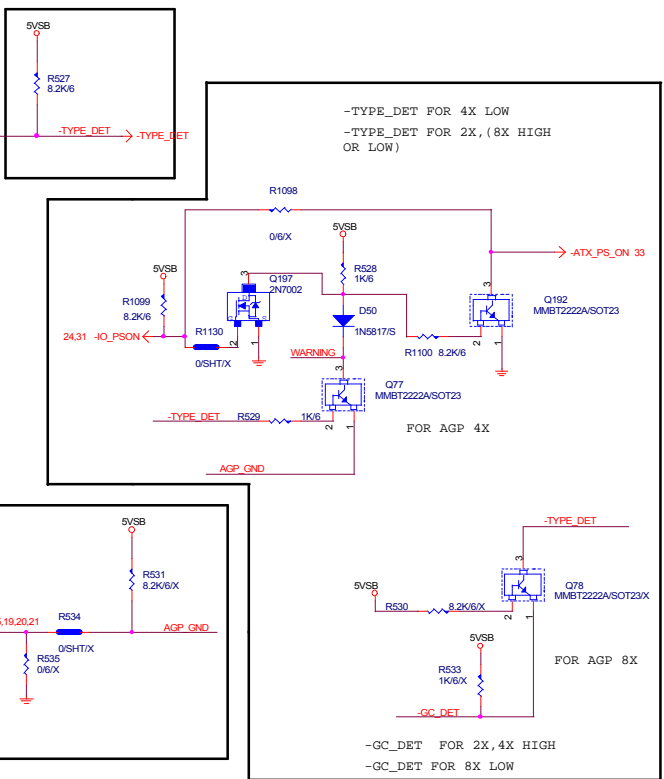
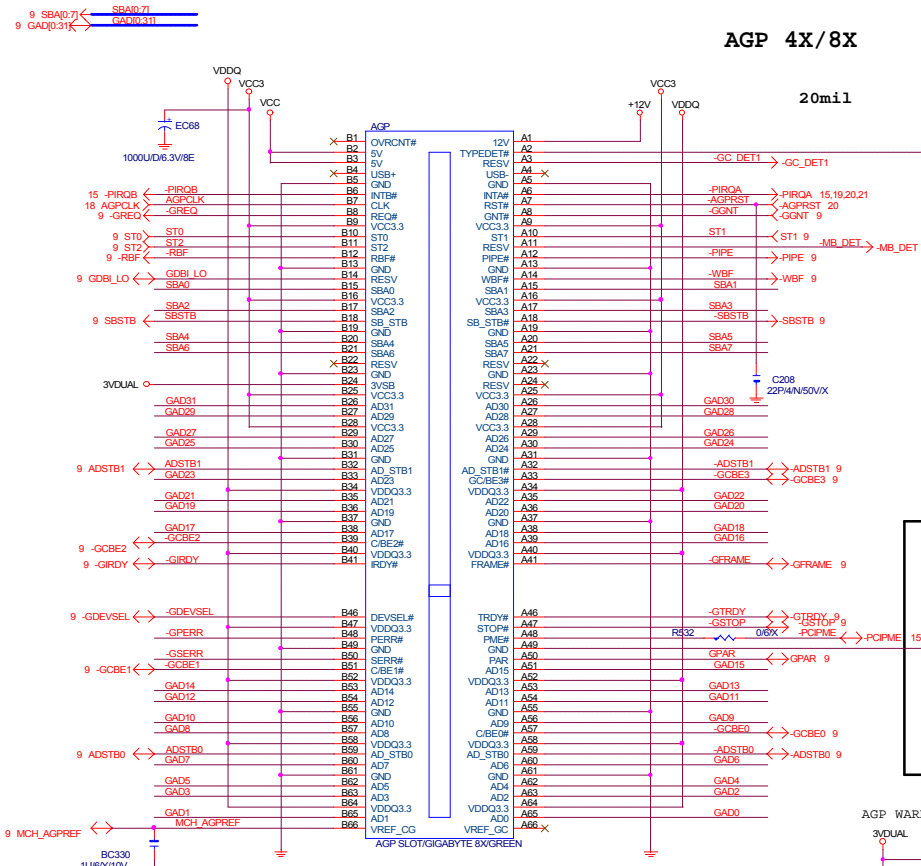


DDR25V Decouple



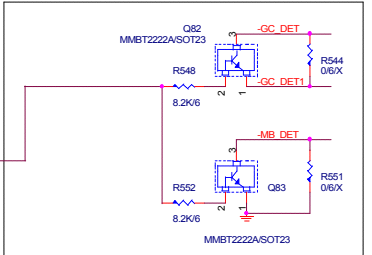
AGP 4X/8X

20mil



AGP_4X:

ON	AGP 4X
OFF	AGP 8X



Note: 1.GPO pin must power on default High

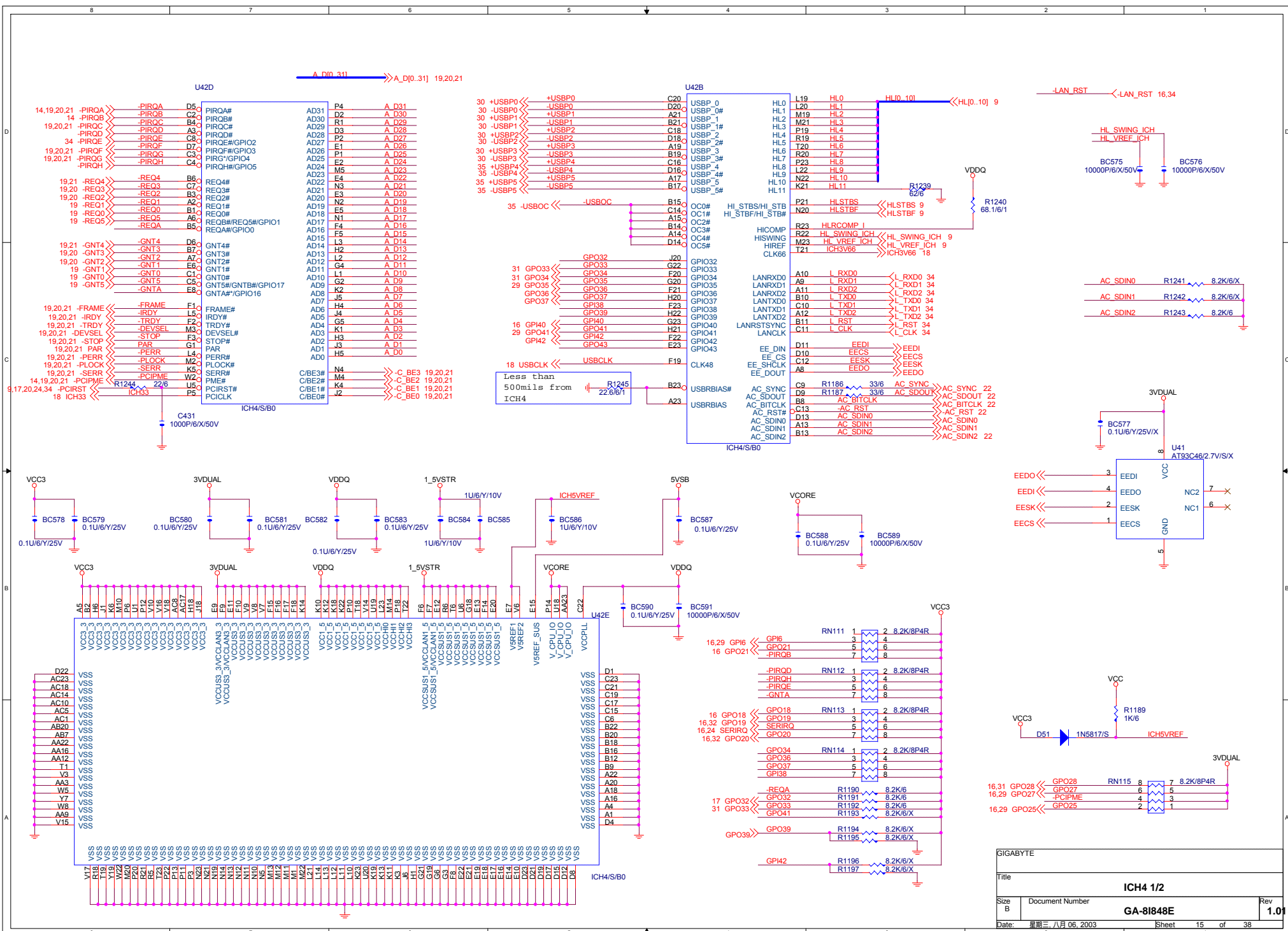
GIGABYTE CORP.

AGP SLOT

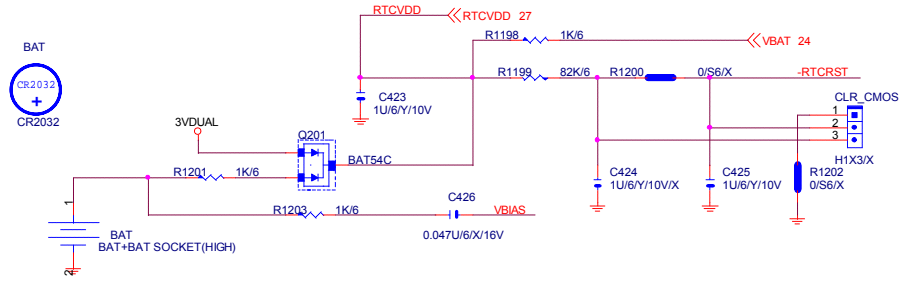
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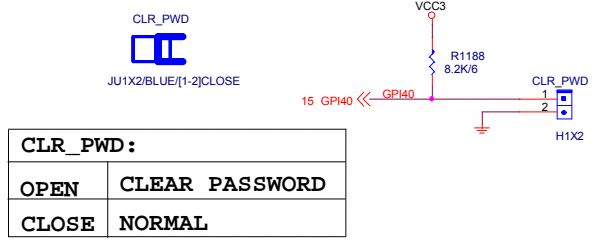


GIGABYTE		
Title		
ICH4 1/2		
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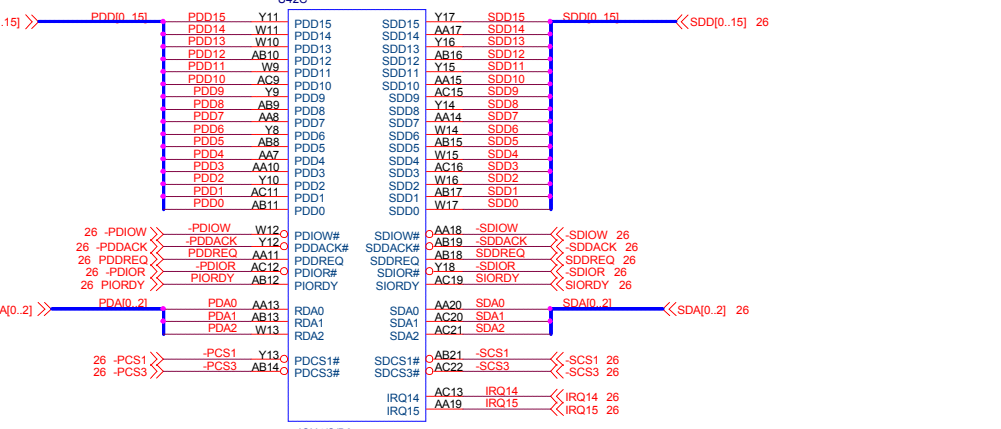
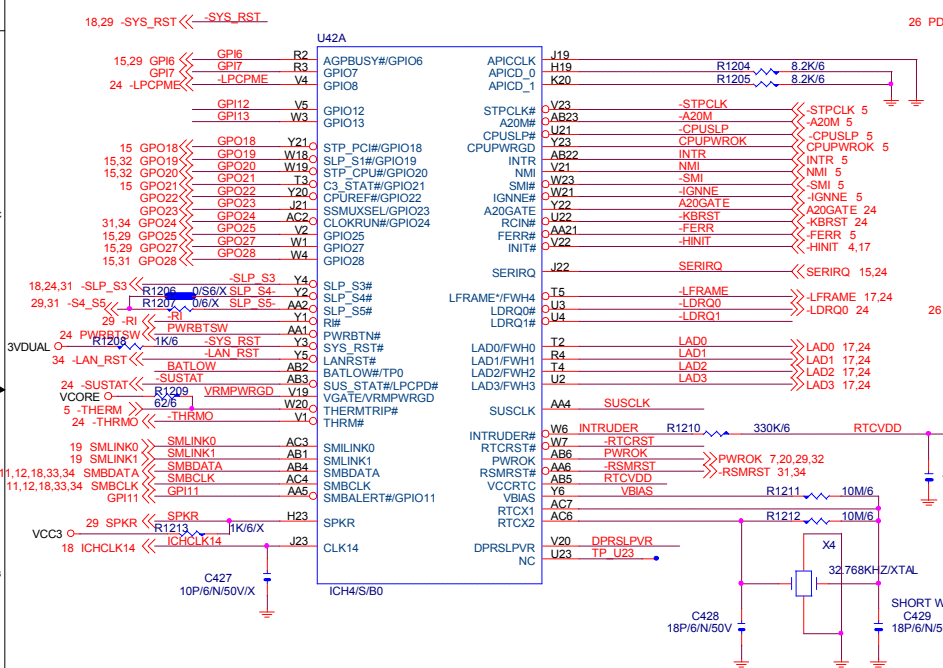
CLR_CMOS :

1-2	CLEAR CMOS
2-3	NORMAL

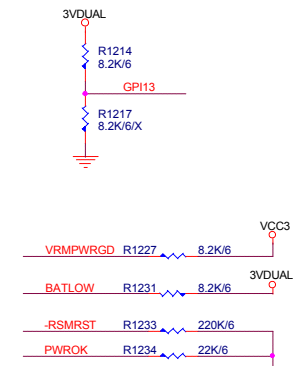
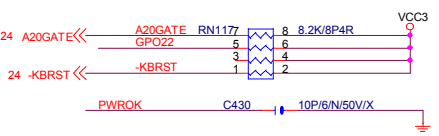
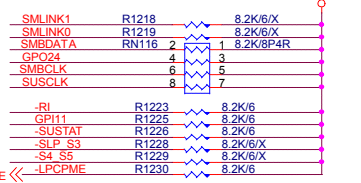


CLR_PWD :

OPEN	CLEAR PASSWORD
CLOSE	NORMAL

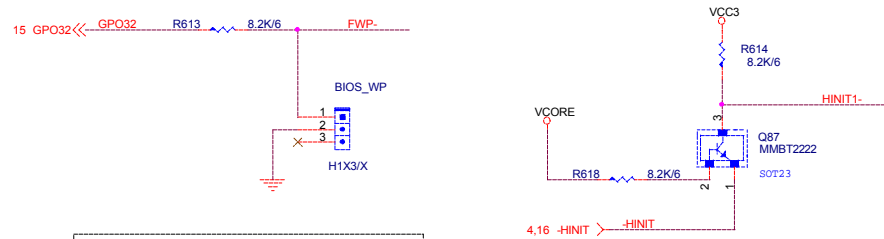


SMLINK0 R1215 0/S6/X SMBCLK
SMLINK1 R1216 0/S6/X SMBDATA

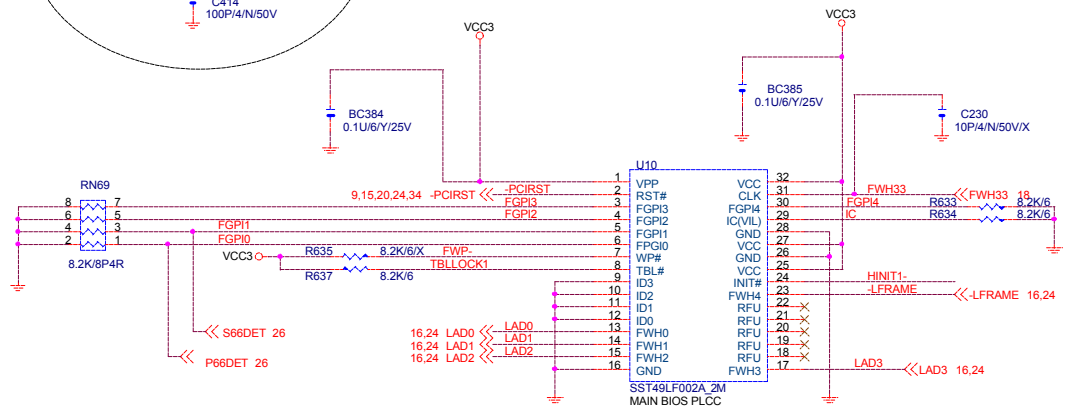
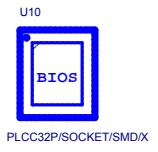
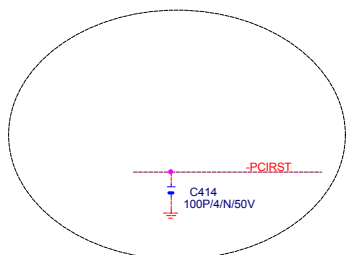


GIGABYTE

Title			ICH4 2/2		
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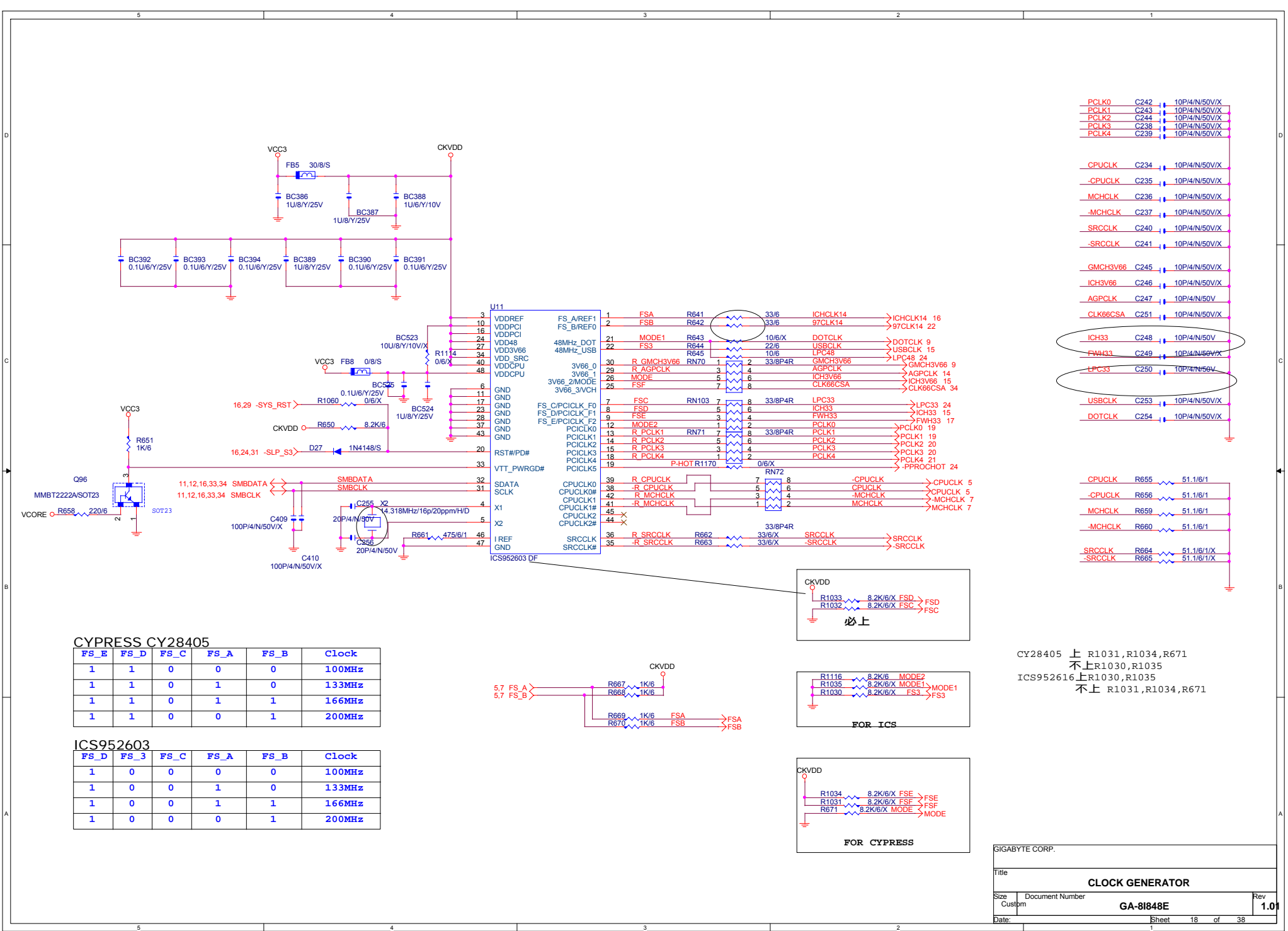


BIOS_WP:	
1-2	WRITE PROTECT
2-3	DISABLE



ADD WINBOUD FWH SEC. SOURCE

GIGABYTE CORP.		
Title		
FWH		
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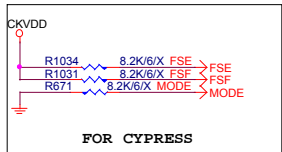
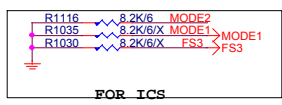
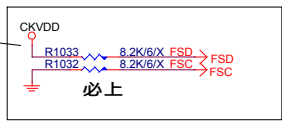
- PCLK0 C242 10P/4/N/50V/X
- PCLK1 C243 10P/4/N/50V/X
- PCLK2 C244 10P/4/N/50V/X
- PCLK3 C238 10P/4/N/50V/X
- PCLK4 C239 10P/4/N/50V/X
- CPUCLK C234 10P/4/N/50V/X
- GPUCLK C235 10P/4/N/50V/X
- MCHCLK C236 10P/4/N/50V/X
- MCHCLK C237 10P/4/N/50V/X
- SRCLK C240 10P/4/N/50V/X
- SRCLK C241 10P/4/N/50V/X
- GMCH3V66 C245 10P/4/N/50V/X
- ICH3V66 C246 10P/4/N/50V/X
- AGPCLK C247 10P/4/N/50V
- CLK66CSA C251 10P/4/N/50V/X
- ICH33 C248 10P/4/N/50V
- FWH33 C249 10P/4/N/50V/X
- LPC33 C250 10P/4/N/50V
- USCLK C253 10P/4/N/50V/X
- DOTCLK C254 10P/4/N/50V/X
- CPUCLK R655 51.1/6/1
- GPUCLK R656 51.1/6/1
- MCHCLK R659 51.1/6/1
- MCHCLK R660 51.1/6/1
- SRCLK R664 51.1/6/1/X
- SRCLK R665 51.1/6/1/X

CYPRESS CY28405

FS_E	FS_D	FS_C	FS_A	FS_B	Clock
1	1	0	0	0	100MHz
1	1	0	1	0	133MHz
1	1	0	1	1	166MHz
1	1	0	0	1	200MHz

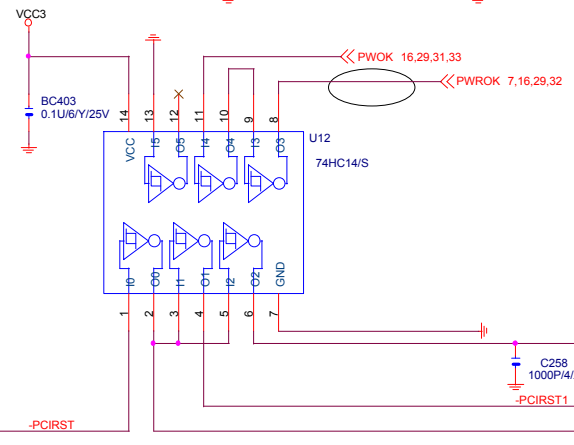
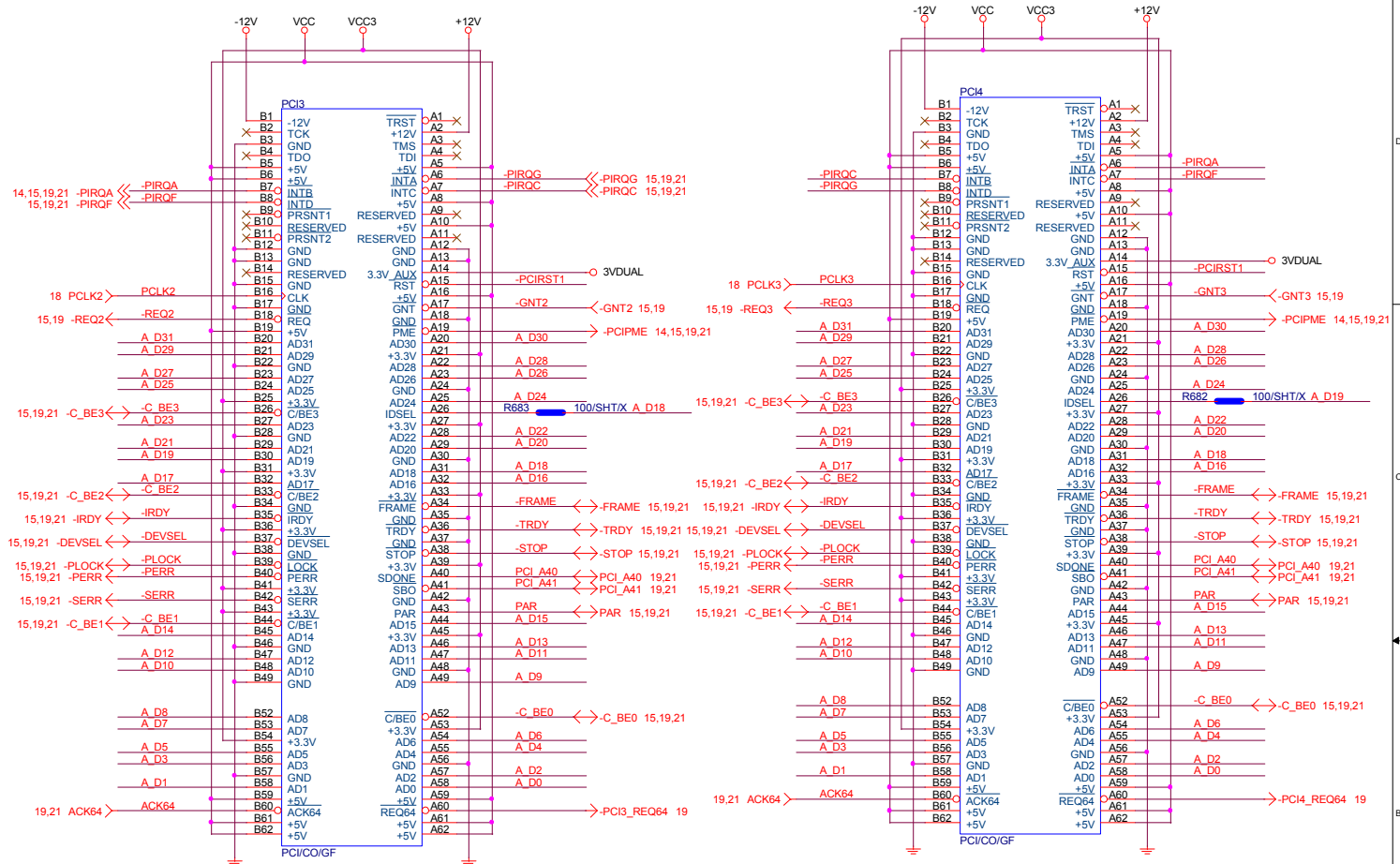
ICS952603

FS_D	FS_3	FS_C	FS_A	FS_B	Clock
1	0	0	0	0	100MHz
1	0	0	1	0	133MHz
1	0	0	1	1	166MHz
1	0	0	0	1	200MHz



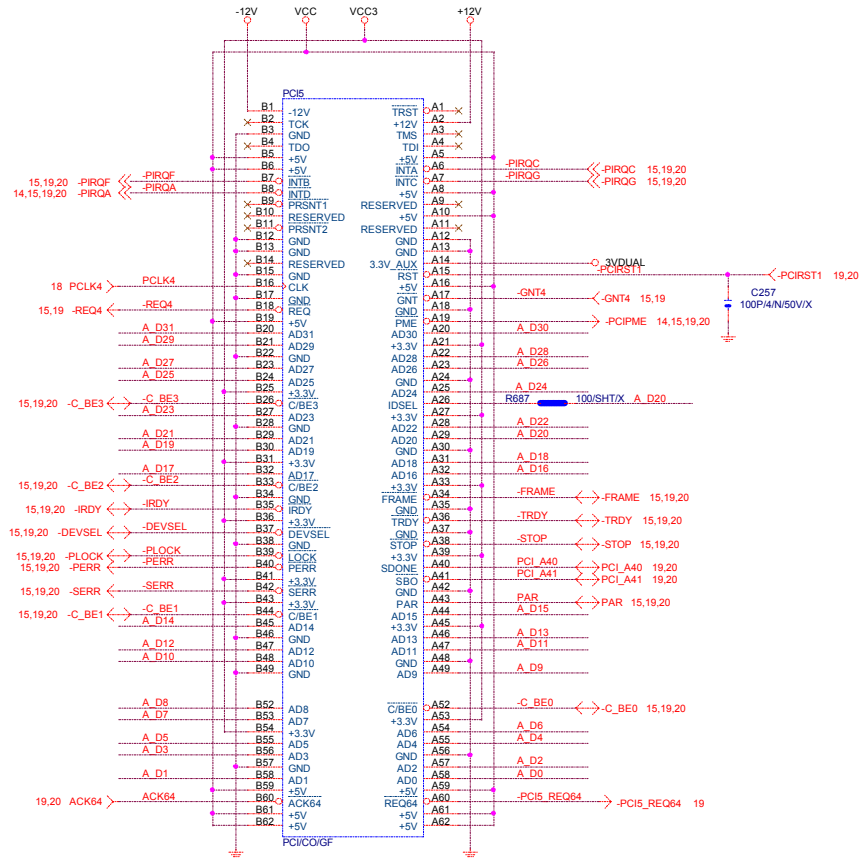
CY28405 上 R1031,R1034,R671
 不上 R1030,R1035
 ICS952616 上 R1030,R1035
 不上 R1031,R1034,R671

15,19,21 A_D[0..31] << A_D[0..31]



GIGABYTE CORP.		
Title PCI SLOT 3/4		
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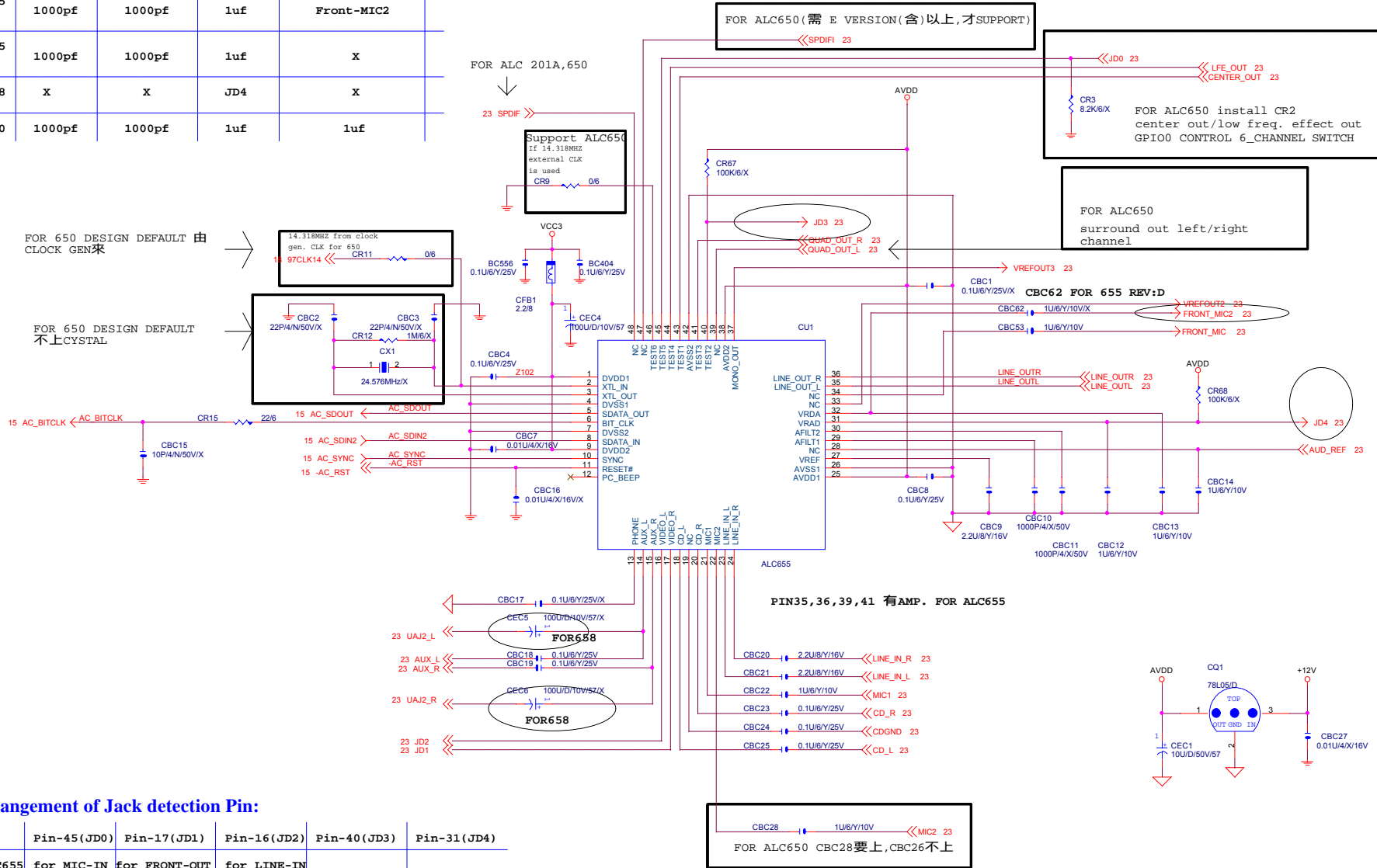
15,19,20_A_D[0..31] << A_D[0..31]



GIGABYTE CORP.			
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PCI SLOT 5/6			
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Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf

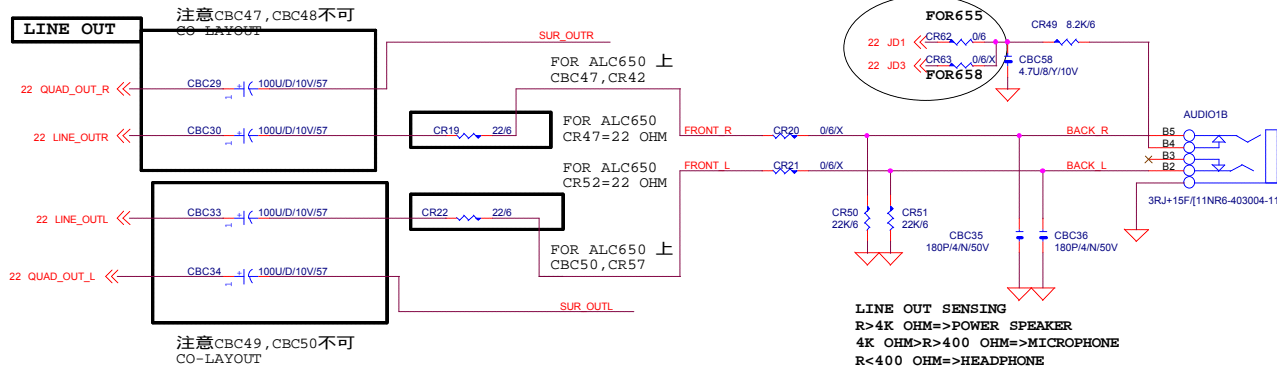


Arrangement of Jack detection Pin:

	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN		
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT	for LINE-IN External pull high is needed

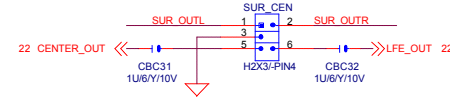
JDO,JD2,GPIO0 為偵測DEVICE INPUT 時由LOW TO HIGH Edge trigger(pop manual)

1/2(3.14)RC=1/2(3.14)8.2K*4.7U=4.3HZ以上AC 信號全部衰減 TO 0V 不會造成JDO 誤動作(無device 時play wav)



FOR SUPPORT 6 CHANNEL,
SURROUND OUT

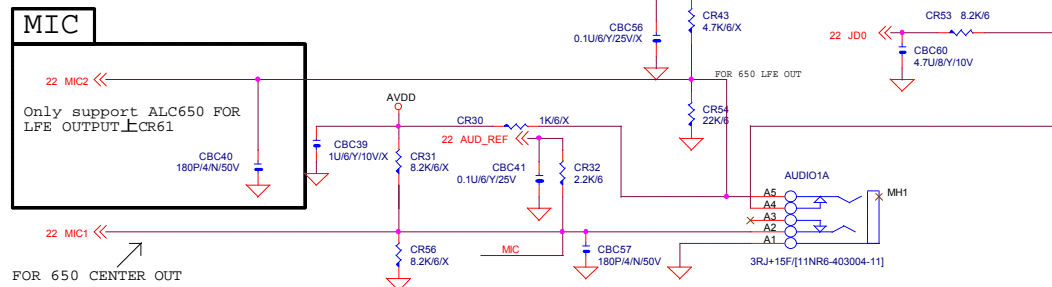
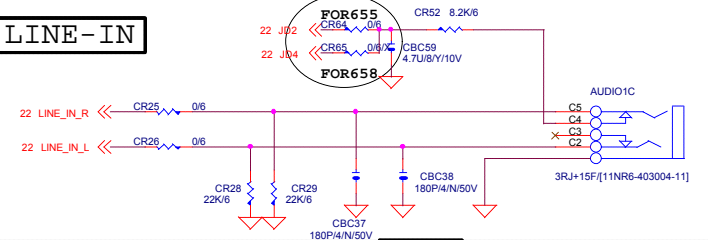
CENTER OUT, LOW
FREQUENCY EFFECT OUT



LINE IN SENSING(當OUTPUT)
R>4K OHM=>POWER SPEAKER
4K OHM>R>400 OHM=>MICROPHONE
R<400 OHM=>HEADPHONE

LINE IN SENSING(當INPUT)
swing of input signal>-40dbv(10mv)===>line in
device active
swing of input signal<-40dbv(10mv)===>unknown
line in device

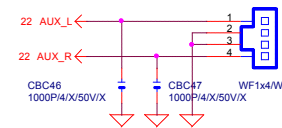
LINE-IN



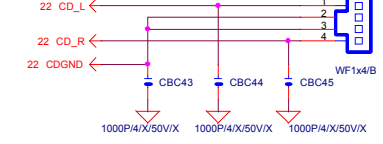
MICROPHONE IN SENSING(當INPUT)(利用vref 偏壓
與CR43,CR32 並聯求出阻抗)
7.1k ohm>R>2.3k ohm===>microphone in
R<2.3k ohm or R>7.1k ohm===>unknown device

MICROPHONE IN SENSING(當OUTPUT)
R>4K OHM=>POWER SPEAKER
4K OHM>R>400 OHM=>MICROPHONE
R<400 OHM=>HEADPHONE

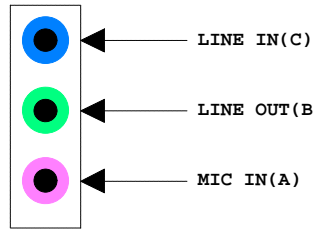
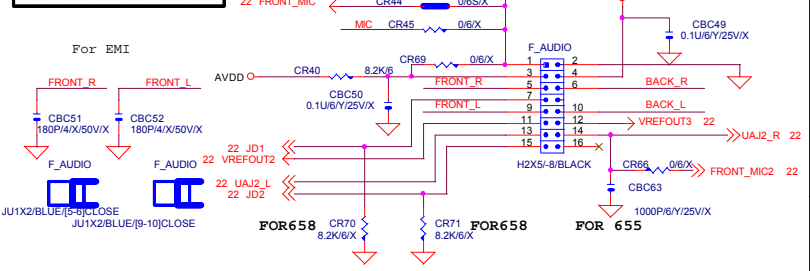
AUX IN DEFAULT NO POP



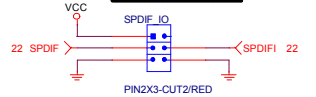
CD IN



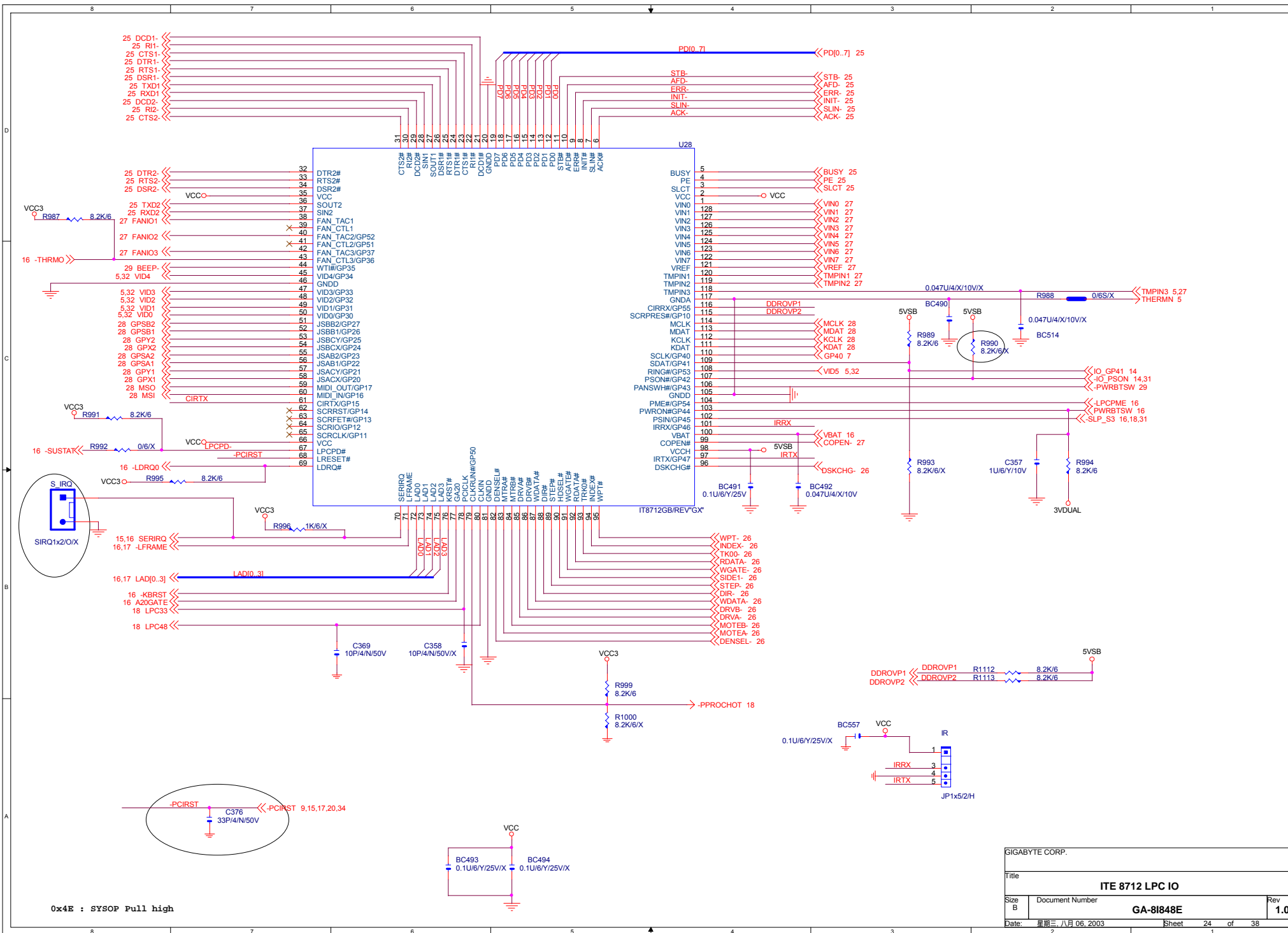
INTEL FRONT AUDIO



SPDIF IO

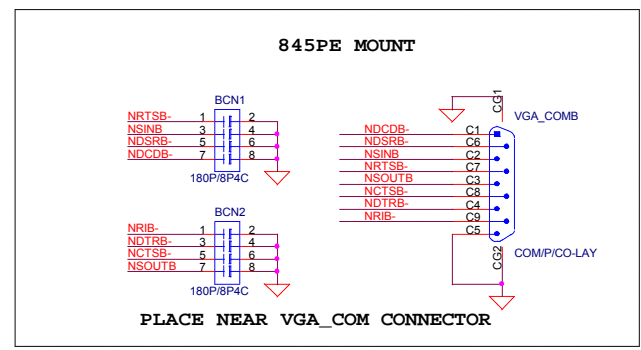
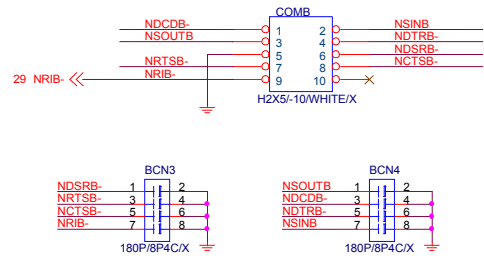
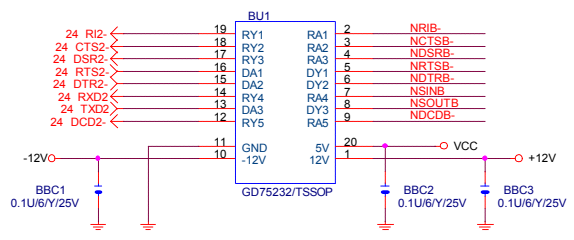
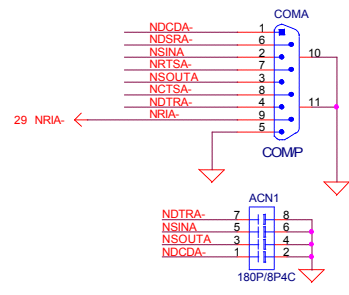
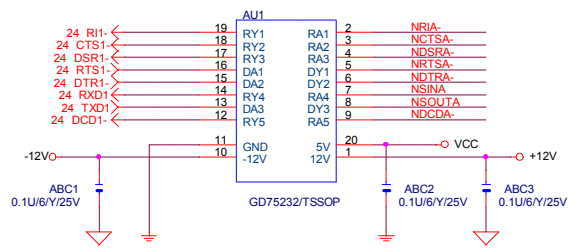


GIGABYTE CORP.			
AUDIO OUTPUT, GAME PORT			
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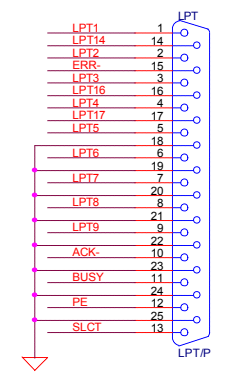
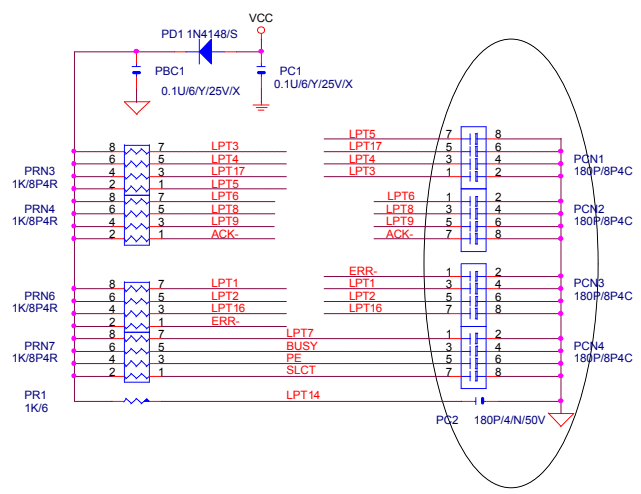
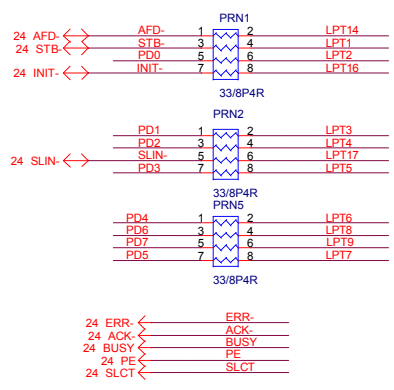


0x4E : SYSOP Pull high

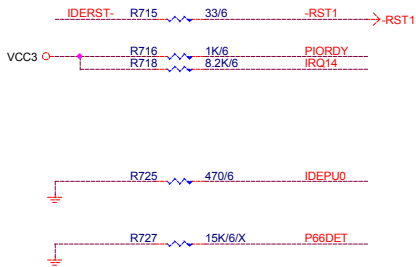
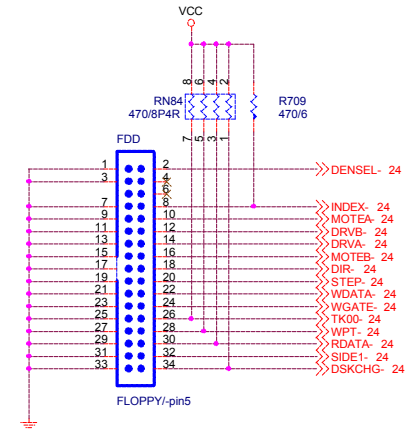
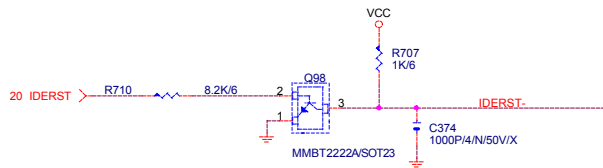
GIGABYTE CORP.		
Title		
ITE 8712 LPC IO		
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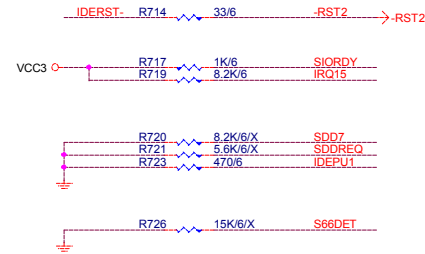
24 PD[0..7] ↔ PD[0..7]



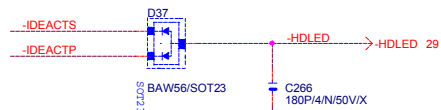
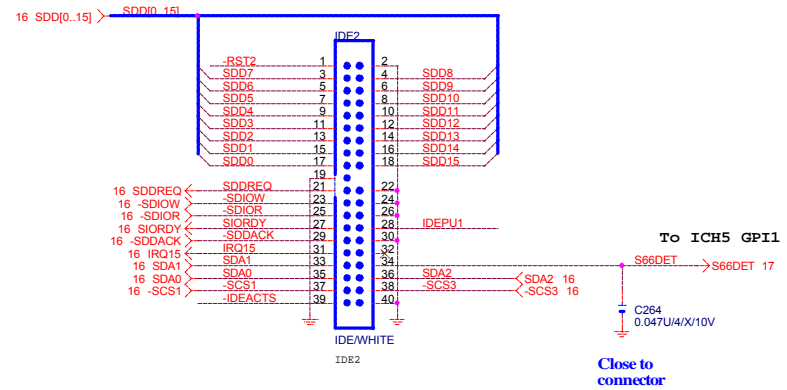
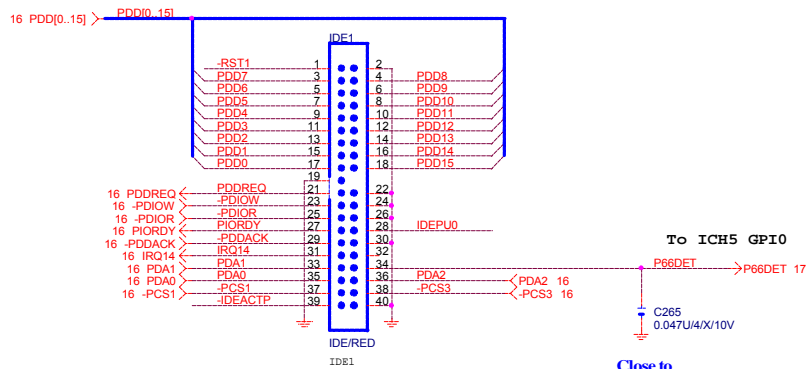
GIGABYTE CORP.		
Title		
COM & IR & LPT PORT & FLOOPY		
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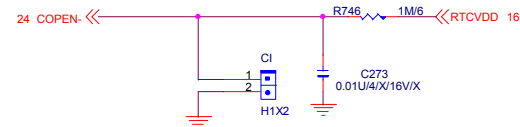
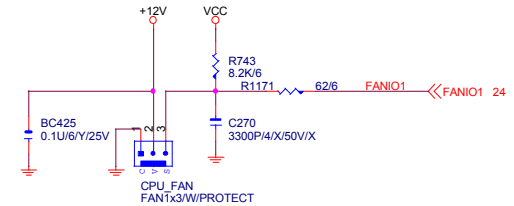
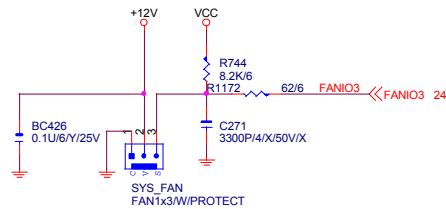
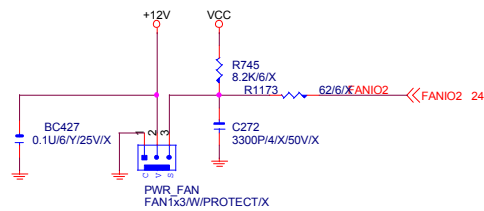
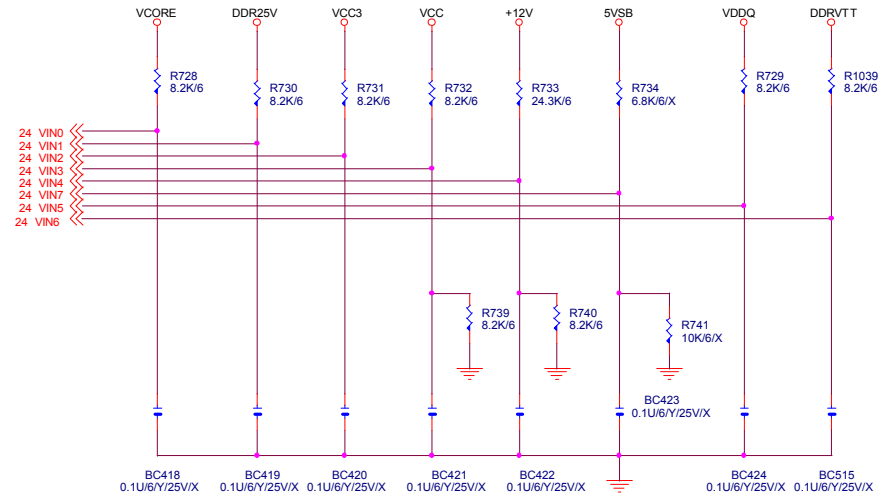
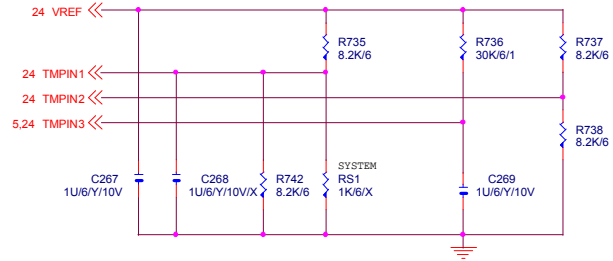
PRIMARY IDE CONNECTOR



SECONDARY IDE CONNECTOR

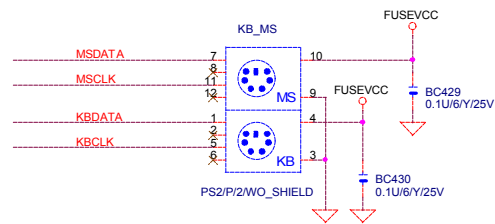
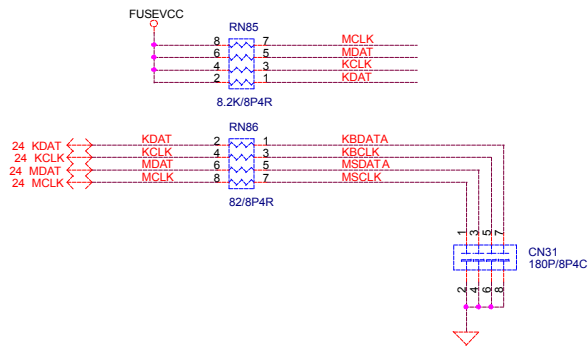
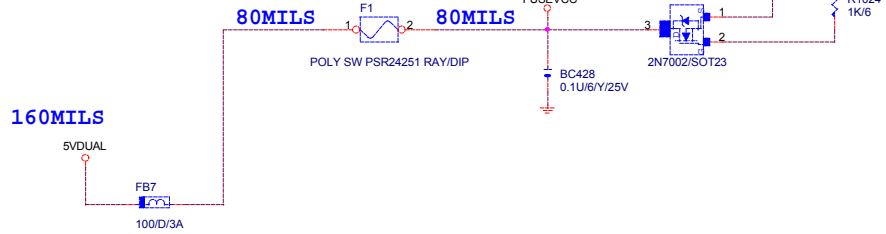
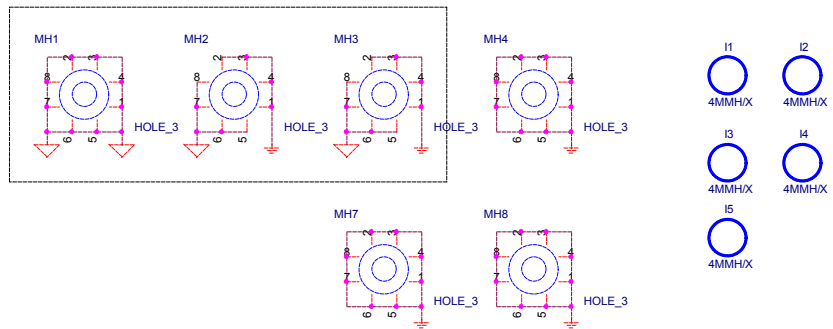


Hardware Monitor circuits

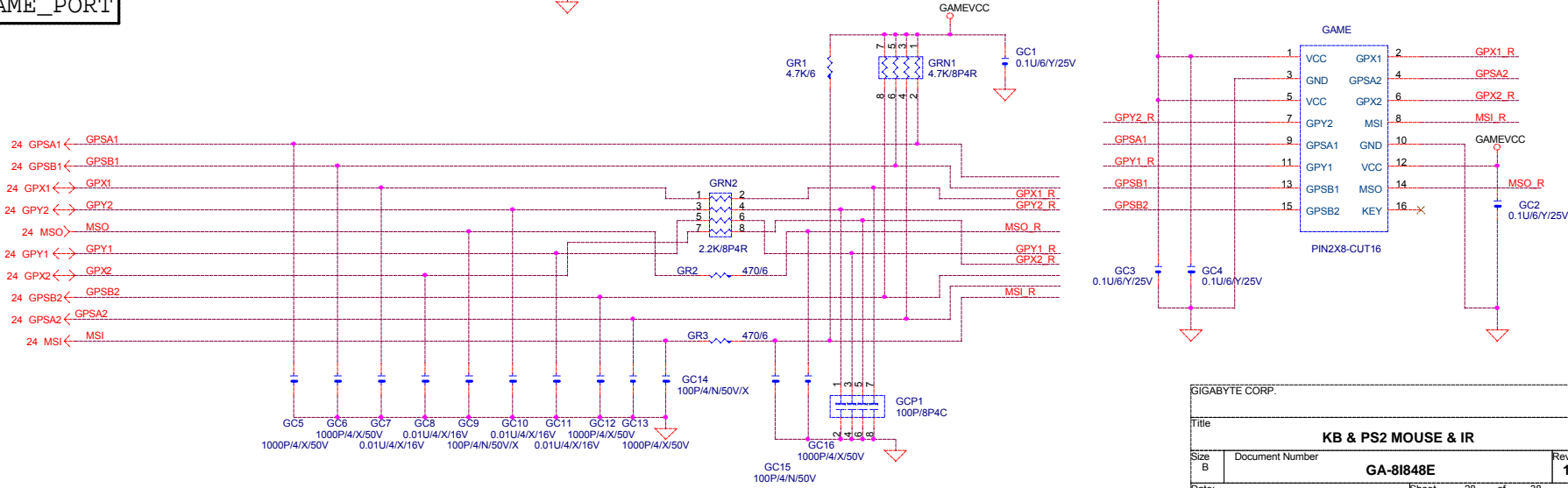


GIGABYTE CORP.			
Title			
FAN/HWMO			
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ATX AGND 與 GND 切割必須有三個

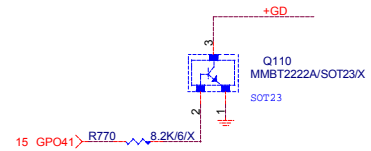
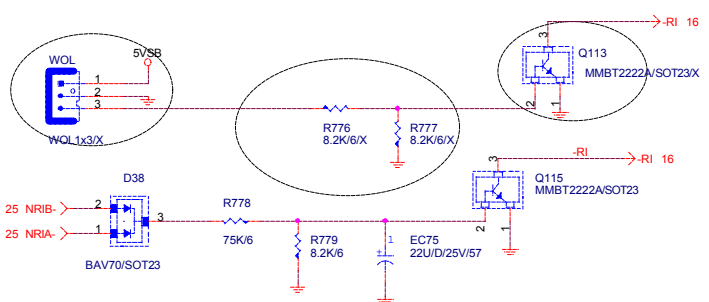
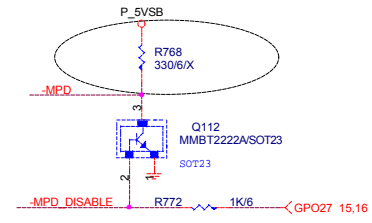
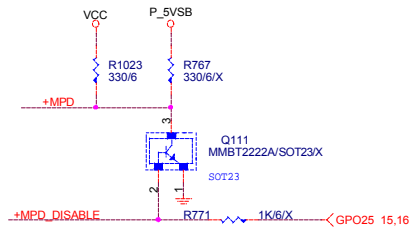
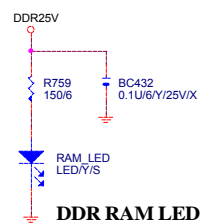
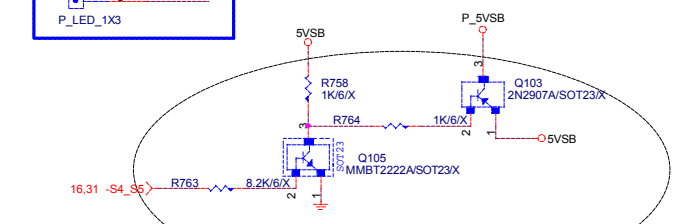
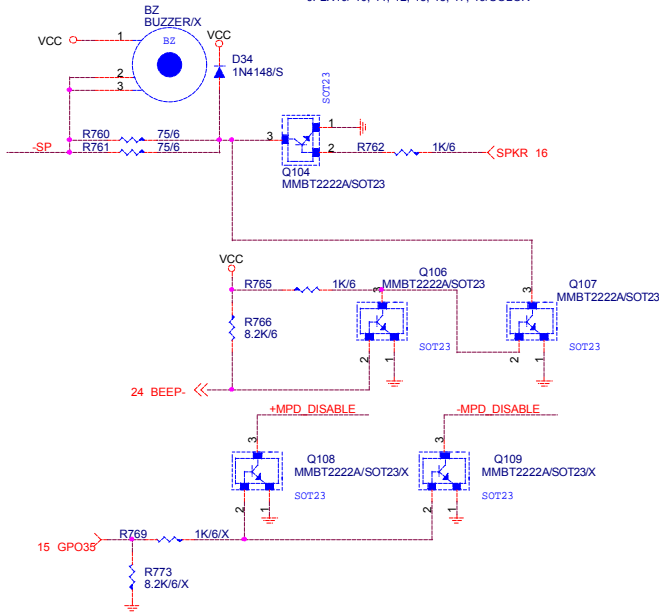
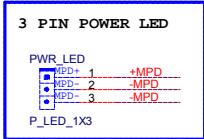
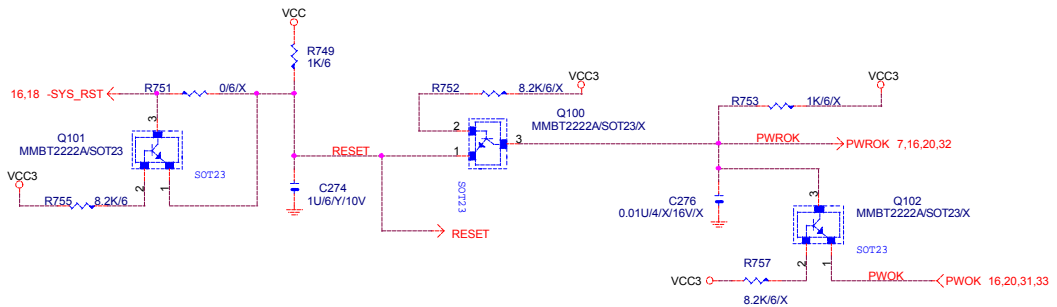
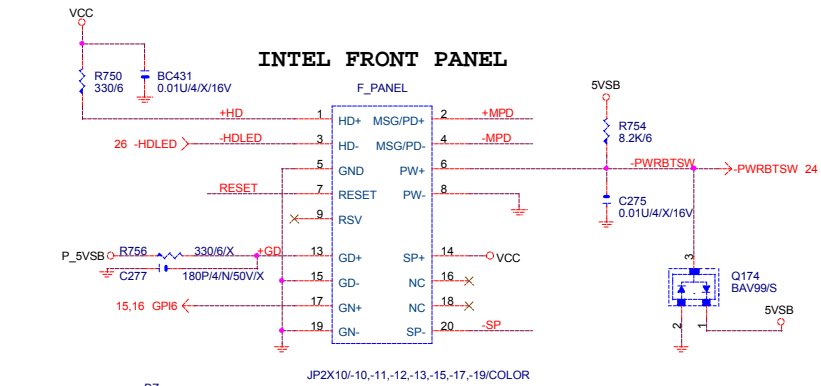


GAME_PORT

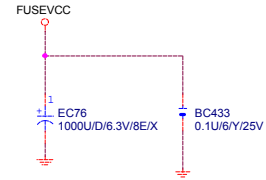


GIGABYTE CORP.		
Title		
KB & PS2 MOUSE & IR		
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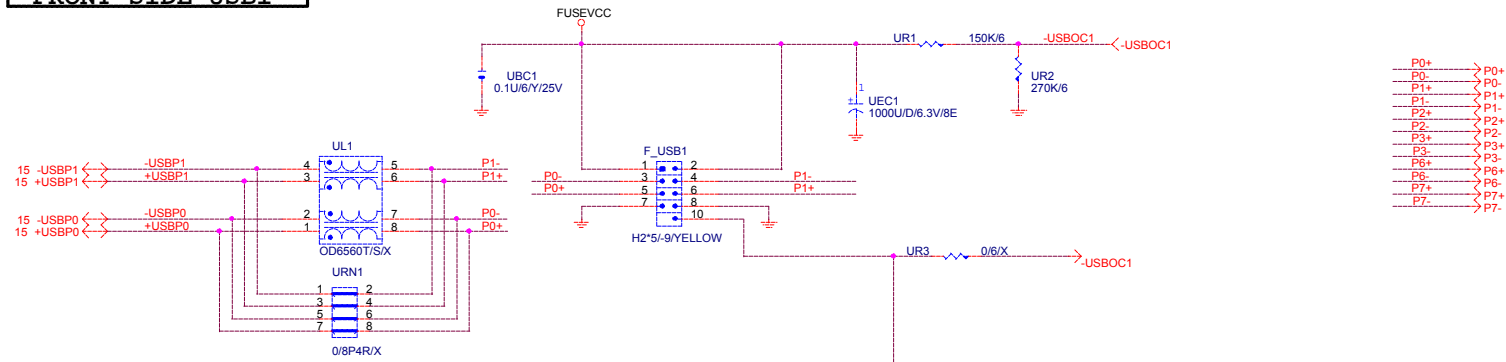
INTEL FRONT PANEL



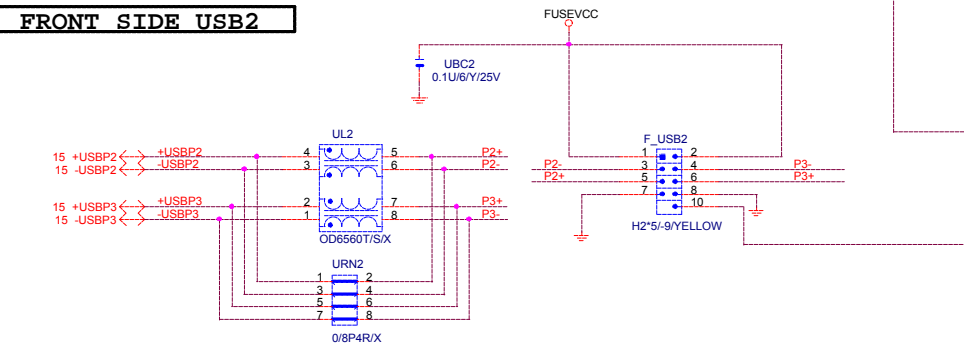
GIGABYTE CORP.		
Title		
PANEL & STR LED & RI		
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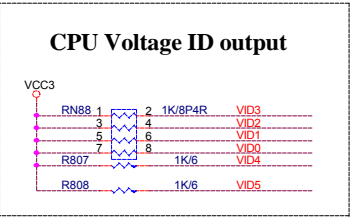
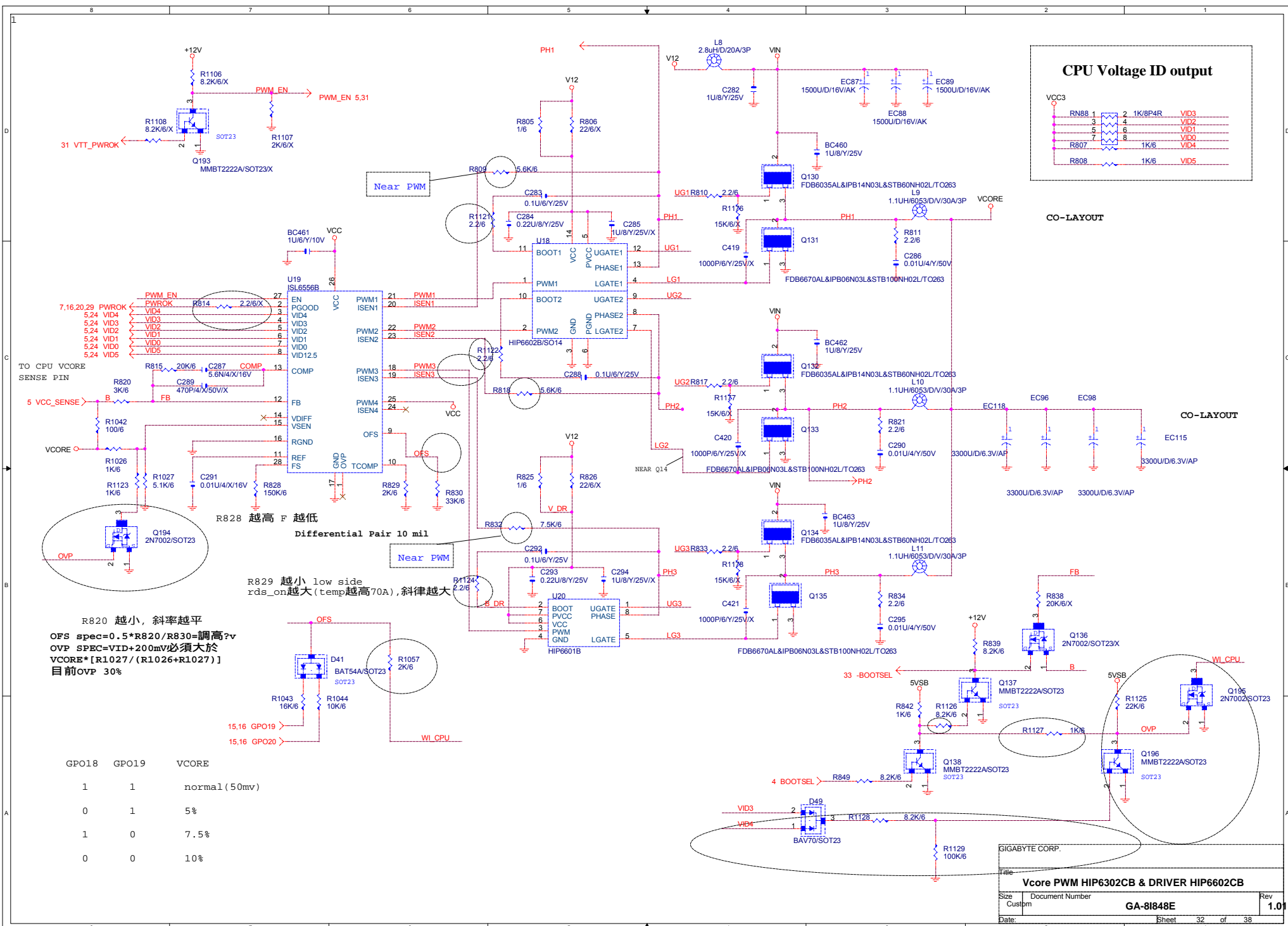


FRONT SIDE USB1



FRONT SIDE USB2





CO-LAYOUT

CO-LAYOUT

R828 越高 F 越低

Differential Pair 10 mil

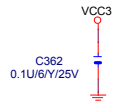
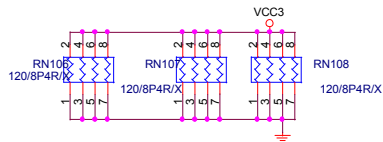
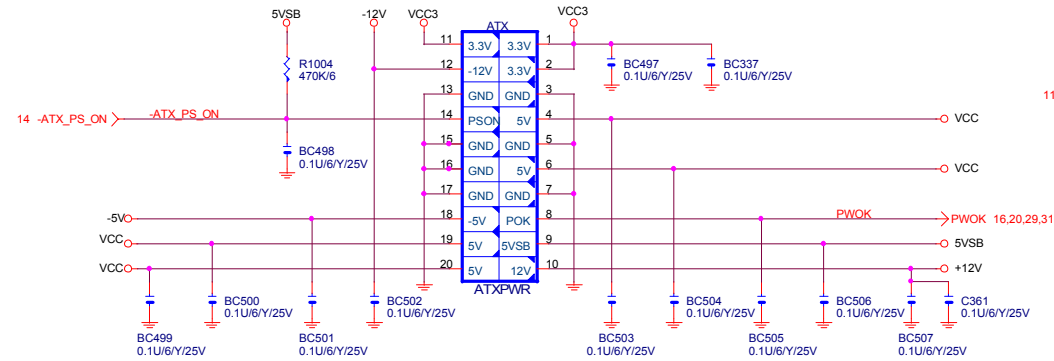
R829 越小 low side
rds_on 越大 (temp 越高 70A), 斜率 越大

R820 越小, 斜率 越平

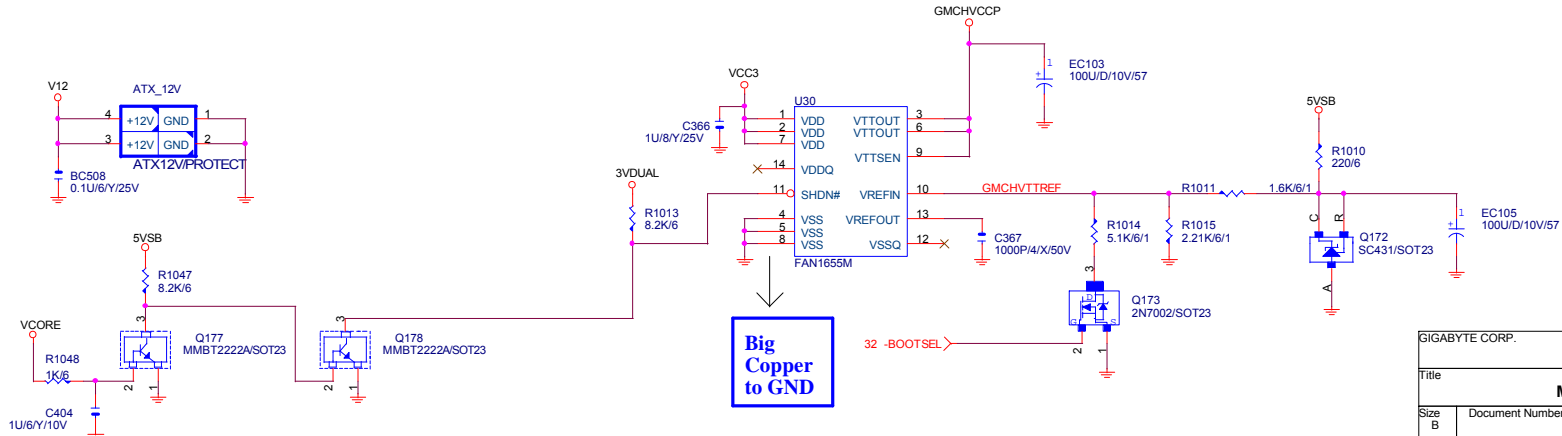
OFS spec = $0.5 * R820 / R830 = \text{調高?}$
 OVP spec = $\text{VID} + 200\text{mV}$ 必須大於
 $\text{VCORE} * [R1027 / (R1026 + R1027)]$
 目前 OVP 30%

GPO18	GPO19	VCORE
1	1	normal (50mv)
0	1	5%
1	0	7.5%
0	0	10%

ATX POWER CONNECTOR

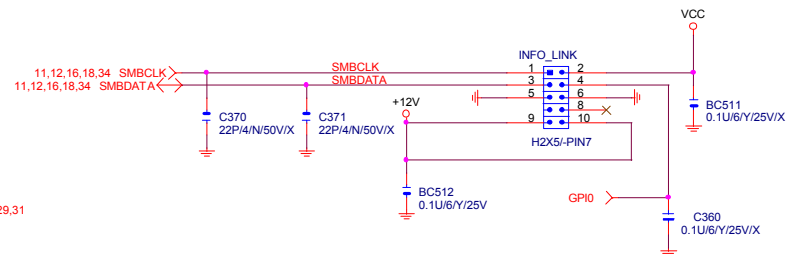


Northwood: +1.45V
 Prescott: +1.225V

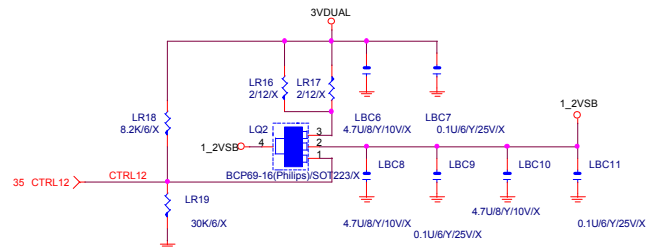


Big Copper to GND

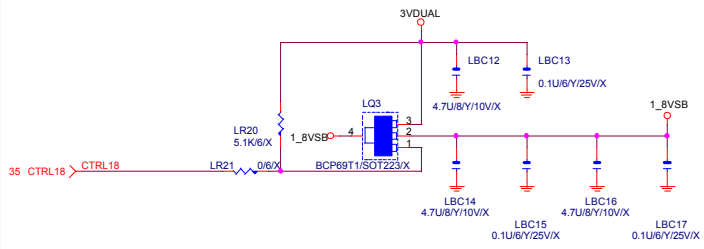
SMBUS CONN.



GIGABYTE CORP.		
Title		
Misc. PWR & ATX CONN.		
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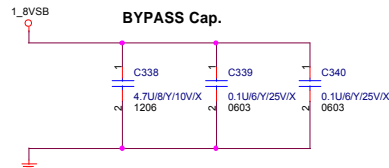
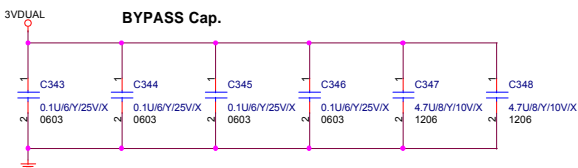
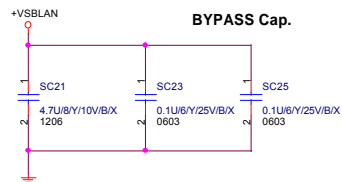
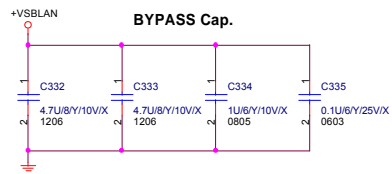


+1.2VSB
Max800mA
Typ500mA



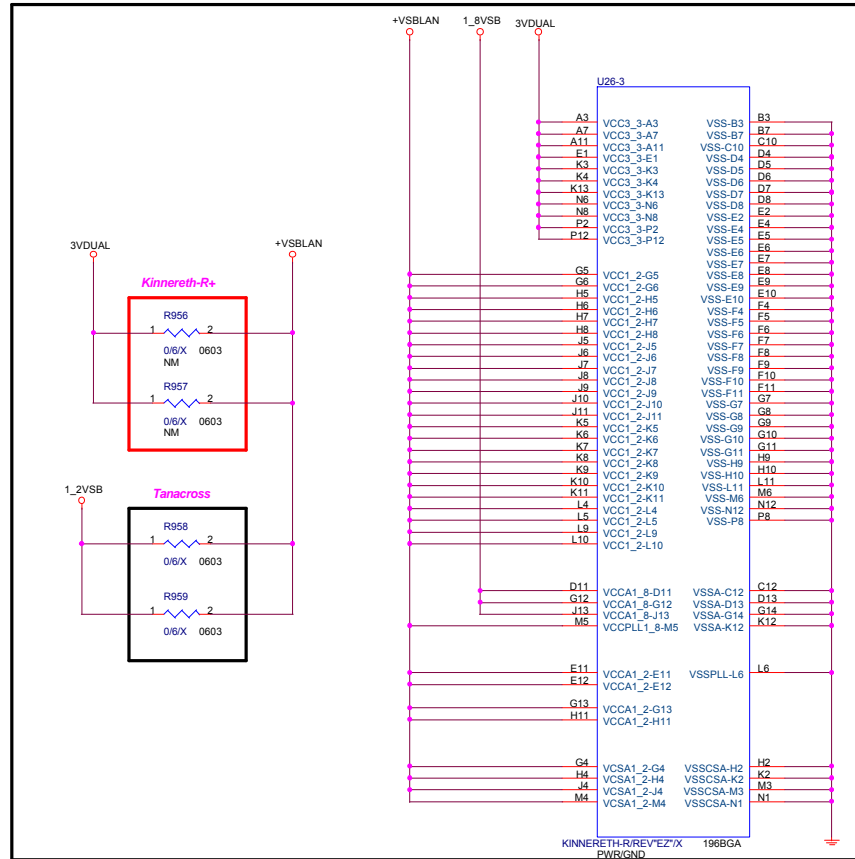
+1.8VSB
Max500mA
Typ250mA

Tanacross



Tanacross

Tanacross



SIGABYTE CORP.			
Title			
CSA TANACROSS_3			
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GIGABYTE GA-8I848E PCI ROUTING LIST

PCI DEVICE	IDSEL	INT	CLOCK	REQ	GNT	
PCI SLOT1	16	C,F,G,A	PCLK0	REQ0-	GNT0-	
PCI SLOT2	17	F,G,A,C	PCLK1	REQ1-	GNT1-	
PCI SLOT3	18	G,A,C,F	PCLK2	REQ2-	GNT2-	
PCI SLOT4	19	A,C,F,G	PCLK3	REQ3-	GNT3-	
PCI SLOT5	20	C,F,G,A	PCLK4	REQ4-	GNT4-	
VIA 1394	21	F	PCICLK1394	REQ5-	GNT5-	

GIGABYTE CORP.		
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PCI ROUNT LIST		
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GIGABYTE GA-8I848E GPIO LIST

SHEET

TITLE

GPIP	I/O	FUNCTION
GPI0/REQA-	I	PULL HIGH 8.2K to VCC3, SMB connector.
GPI1/REQ5-		PULL HIGH 8.2K to VCC, REQ5-.
GPI2/PIRQE-		PULL HIGH 8.2K to VCC3, PIRQE-.
GPI3/PIRQF-		PULL HIGH 8.2K to VCC3, PIRQF-.
GPI4/PIRQG-		PULL HIGH 8.2K to VCC, PIRQG-.
GPI5/PIRQH-	NA	PULL HIGH 8.2K to VCC
GPI6/AGPBUSY-	I	PULL 8.2K TO VCC3, PANEL GREEN_BUTTON
GPI7	I	DUAL BIOS FIRST BOOT SELECT.
GPI8	I	PULL 8.2K TO 3VDUAL, -CAS PME.
GPI9/OC4-	NA	USB OC4-.
GPI10/OC5-	NA	USB OC5-.
GPI11/-SMBALRT	NA	PULL 8.2K TO 3VDUAL, -SMBALERT.
GPI12	I	PULL 8.2K TO VCC3, M/B REVERSION ID.
GPI13	I	LPC PME.
GPI14/OC6-	NA	USB OC6-.
GPI15/OC7-	NA	USB OC7-.
GPO16/GNTA-	NA	GPO16.
GPO17/GNT5-		GNT5-.
GPO18/STP_PCI-	NA	GPO18.
GPO19/SLP_S1-	O	DUAL BIOS.
GPO20/SLP_CPU-	O	DUAL BIOS.
GPO21/C3_SATA-	O	BLOCK TOP TABLE.
GPO22/CPUPERF-	O	PULL 8.2K TO VCC3, PANEL S3 POWER LED.

SHEET

TITLE

GPIP	I/O	FUNCTION
GPO16		PULL 8.2K TO VCC3
GPO17		PULL 8.2K TO VCC3 (GNT5-)
GPO18		PULL 8.2K TO VCC3
GPO19		PULL 8.2K TO VCC3
GPO20		PULL 8.2K TO VCC3
GPO21		PULL 8.2K TO VCC3
GPO22		PULL 8.2K TO VCC3
GPO23		PULL 8.2K TO VCC3
GPO24		PULL 1K TO 3VDUAL (TOP BLOCK)
GPO25		PULL 4.7K TO 3VDUAL, LAN 100/10 DETECT.
GPO26		NOT IMPLEMENTED
GPO27		PULL 8.2K TO 3VDUAL, BIOS WRITE PROTECT.
GPO28		PULL 8.2K TO 3VDUAL

GIGABYTE CORP.

Title			GPIO LIST		
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