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05	Arrandale(DDR3)	0.1	
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Title: **Index**

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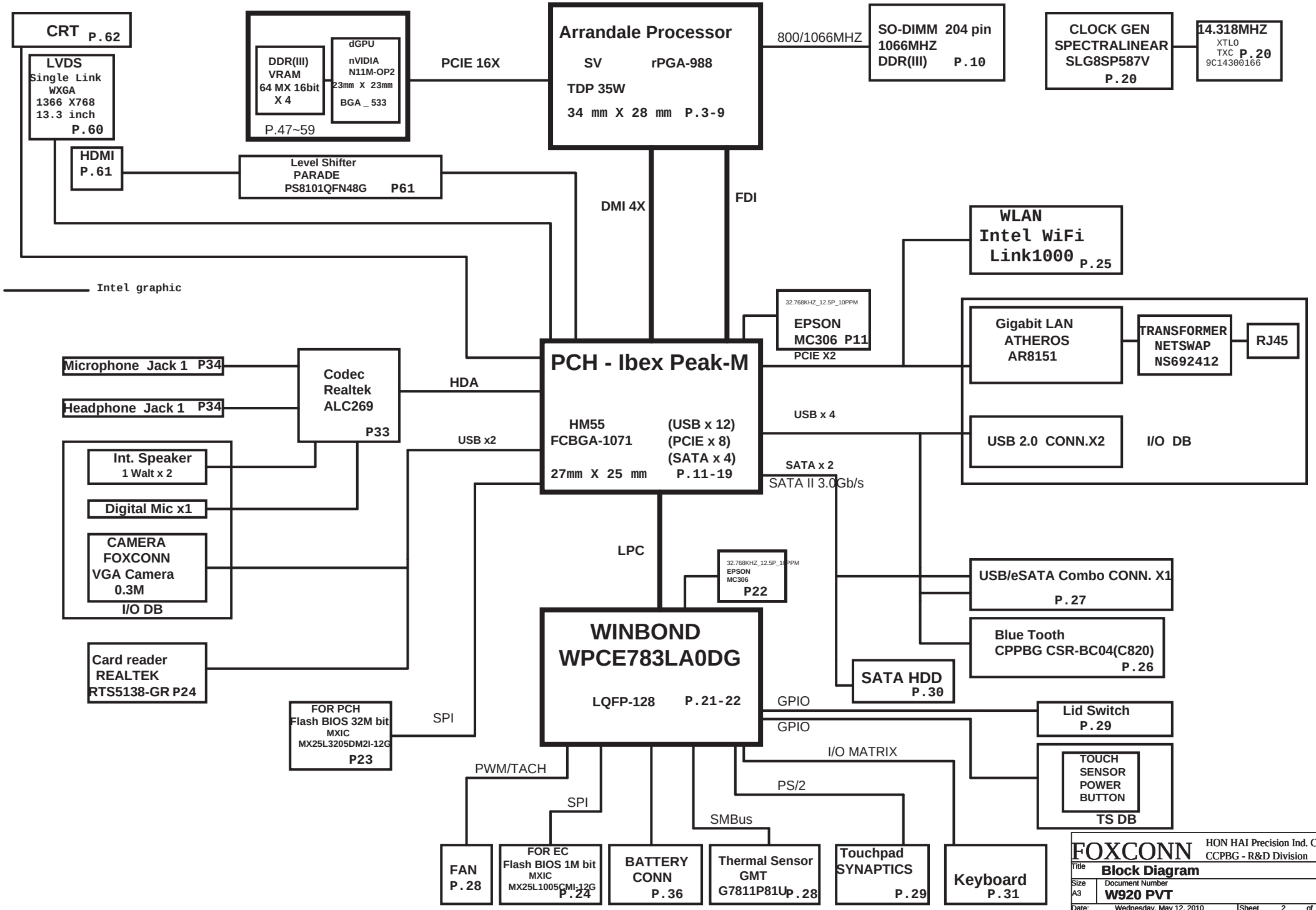
W920 Calpella Platform Block Diagram



FOXCONN — HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	Block Diagram	
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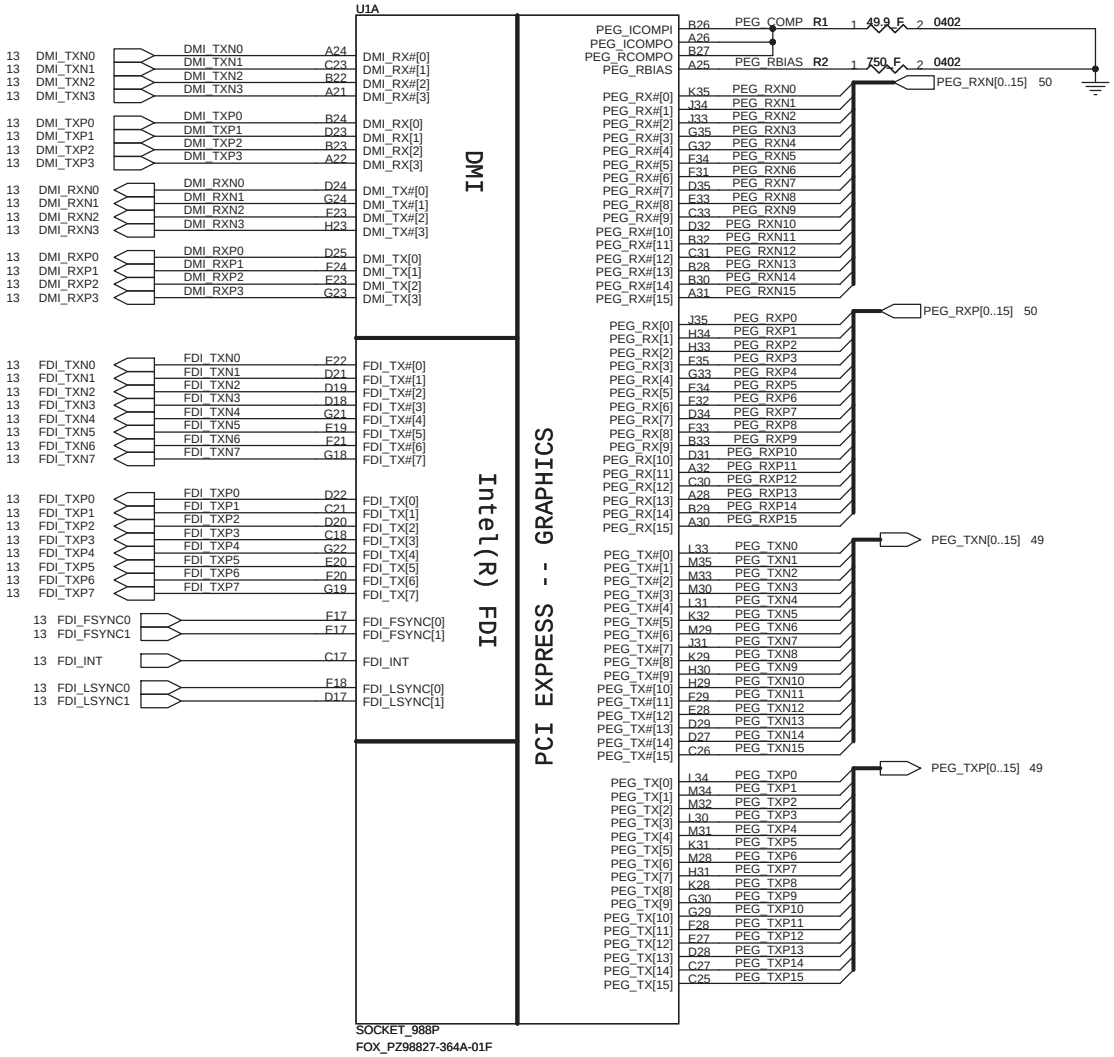
Date: Wednesday, May 12, 2010	Sheet 2 of 71	



Layout Note:
Comp0,1 connect with Zo=49.9 ohm,
Comp2,3 connect with Zo=20 ohm,
In order to minimize resistance,
use thick traces to route all
COMP signals, use 10-mils
(0.254-mm) wide trace for
routing less than 500 mils (12.7
mm), or 20-mils (0.508-mm)
wide trace for routing between
500 mils (12.7 mm) and
1000 mils (25.4 mm). Keep 20-mils
(0.508-mm) spacing to
any other signals in order to
minimize crosstalk.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Arrandale (DMI,PEG,FDI)		
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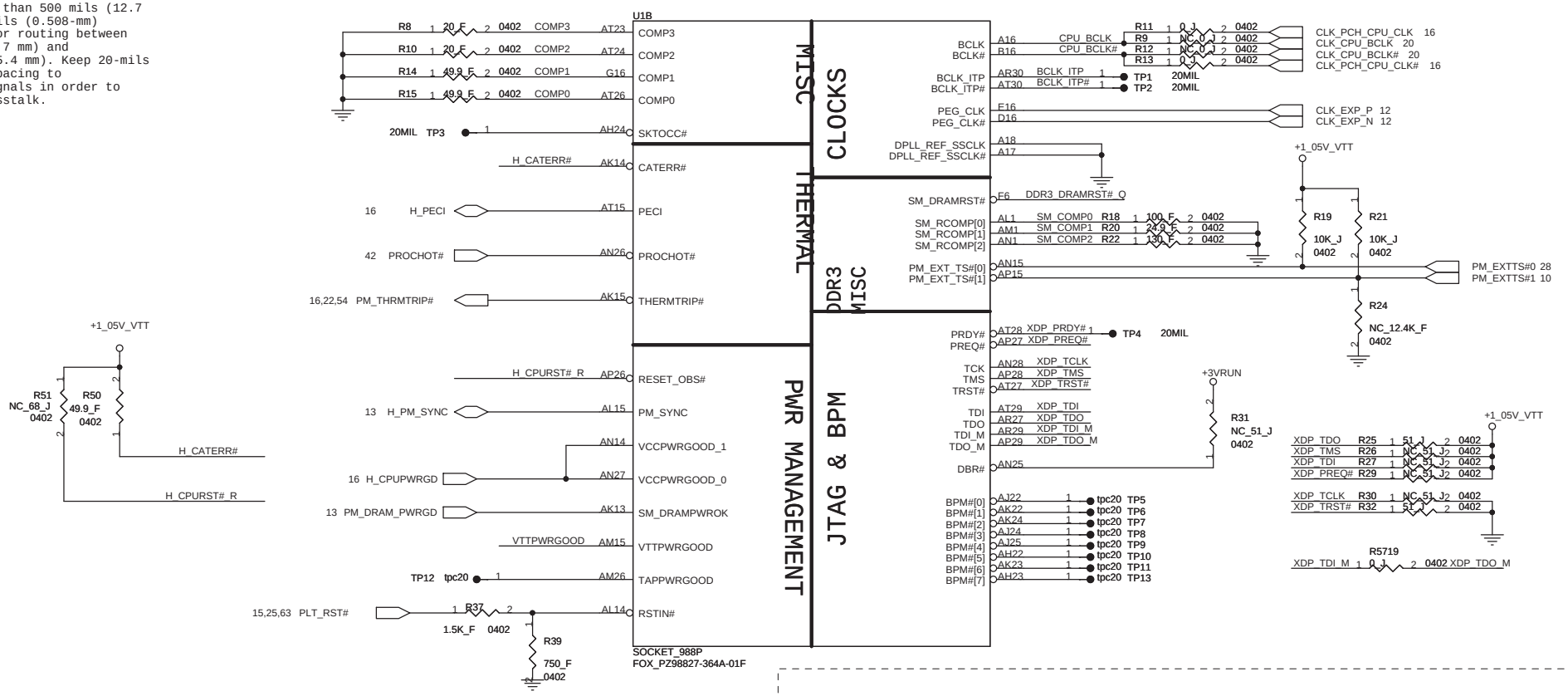
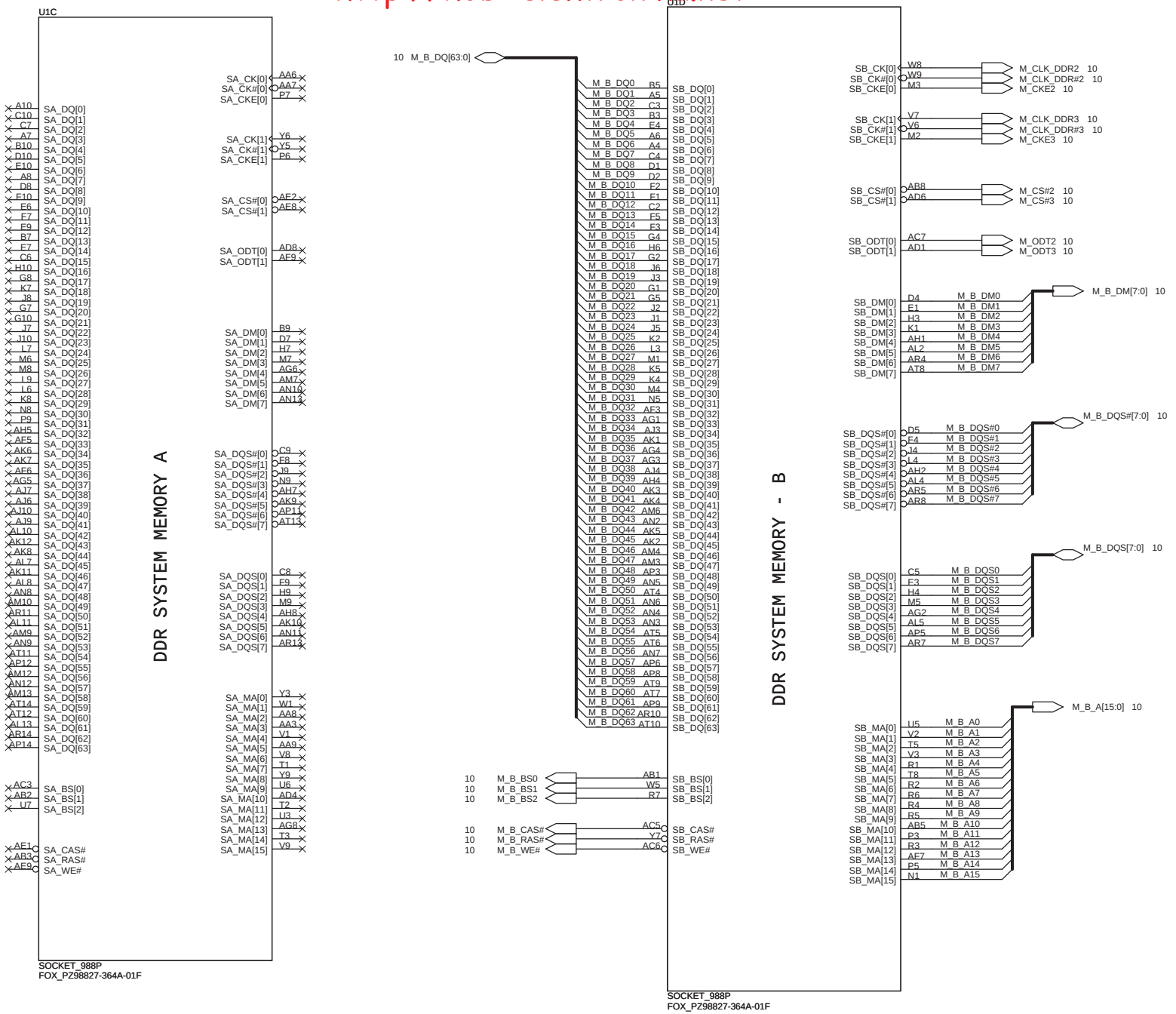
Layout Note:
Comp0,1 connect with Zo=49.9 ohm,
Comp2,3 connect with Zo=20 ohm,
In order to minimize resistance,
use thick traces to route all
COMP signals, use 10-mils
(0.254-mm) wide trace for
routing less than 500 mils (12.7
mm), or 20-mils (0.508-mm)
wide trace for routing between
500 mils (12.7 mm) and
1000 mils (25.4 mm). Keep 20-mils
(0.508-mm) spacing to
any other signals in order to
minimize crosstalk.



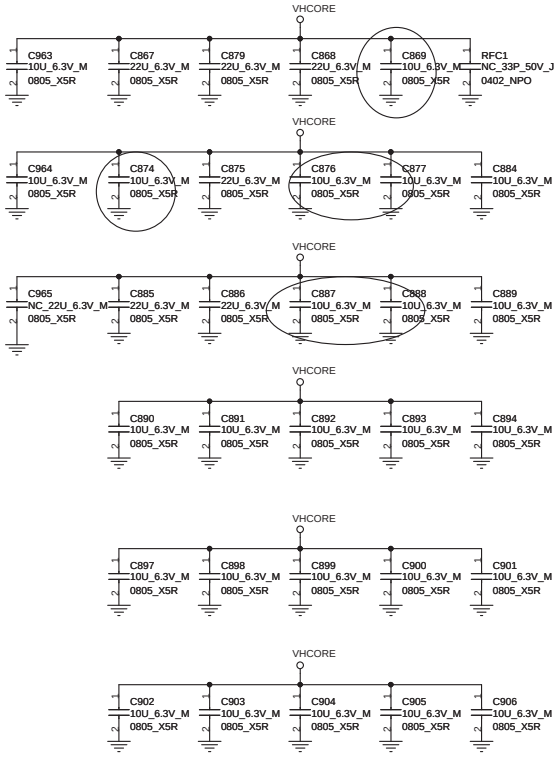
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Arrandale (CLK,MISC,JTAG)	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 4 of 71	



FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

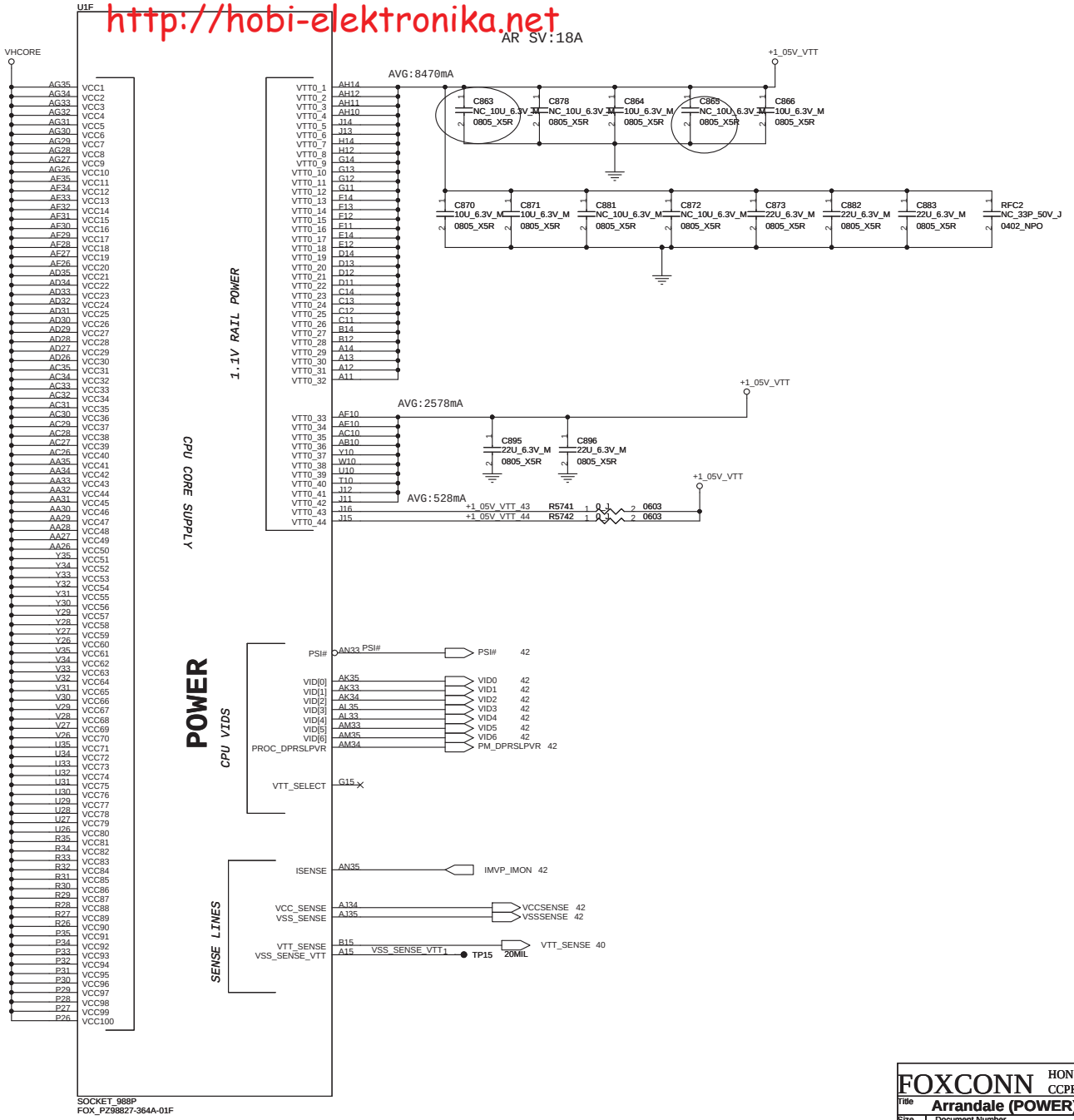
Title	Arrandale (DDR3)		
Size A3	Document Number W920 PVT		Rev 0.1
Date: Monday, May 17, 2010	Sheet 5 of 71		

AR SV:48A

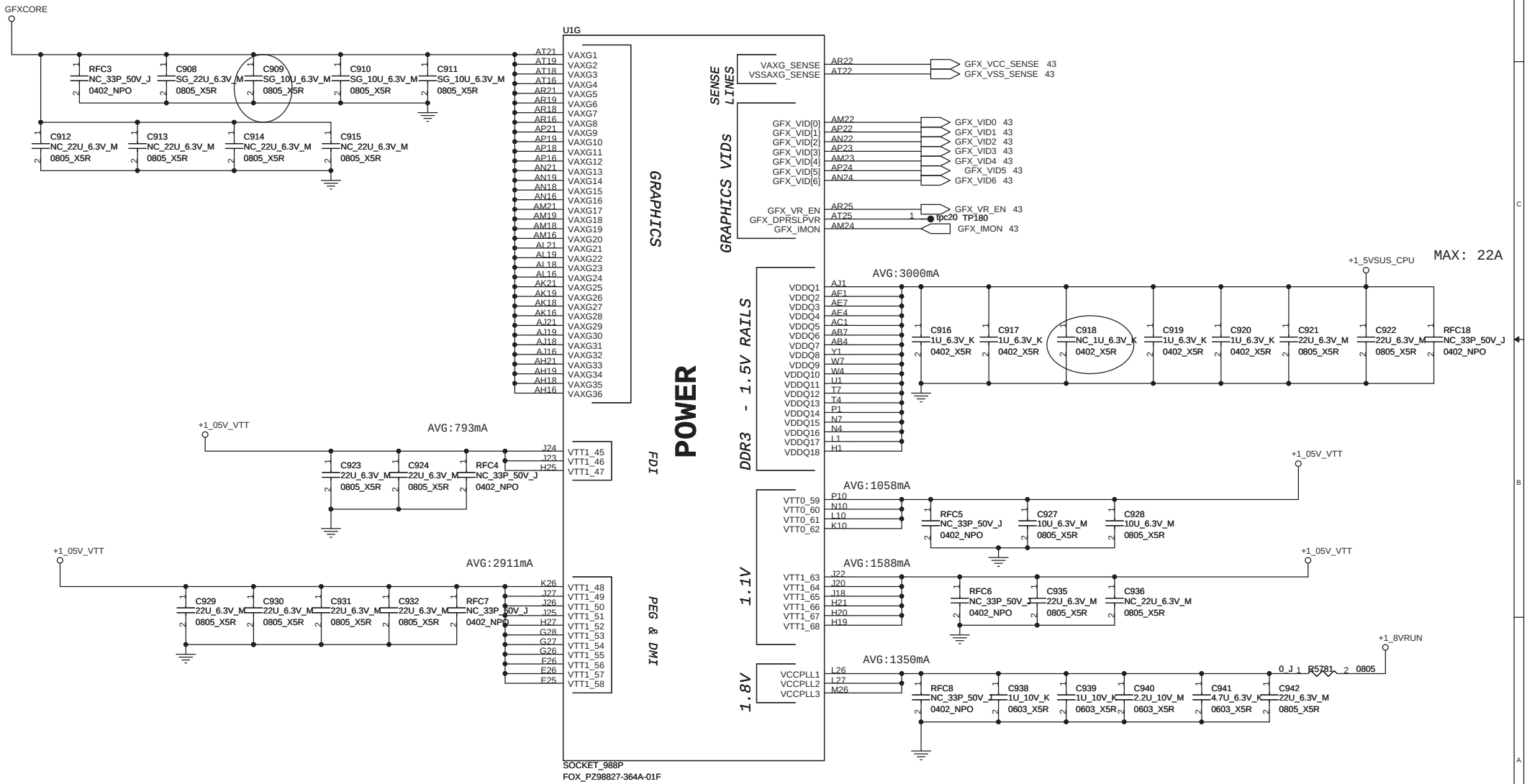


VCOREdecoupling
16 x 10uF
12 x 22uF

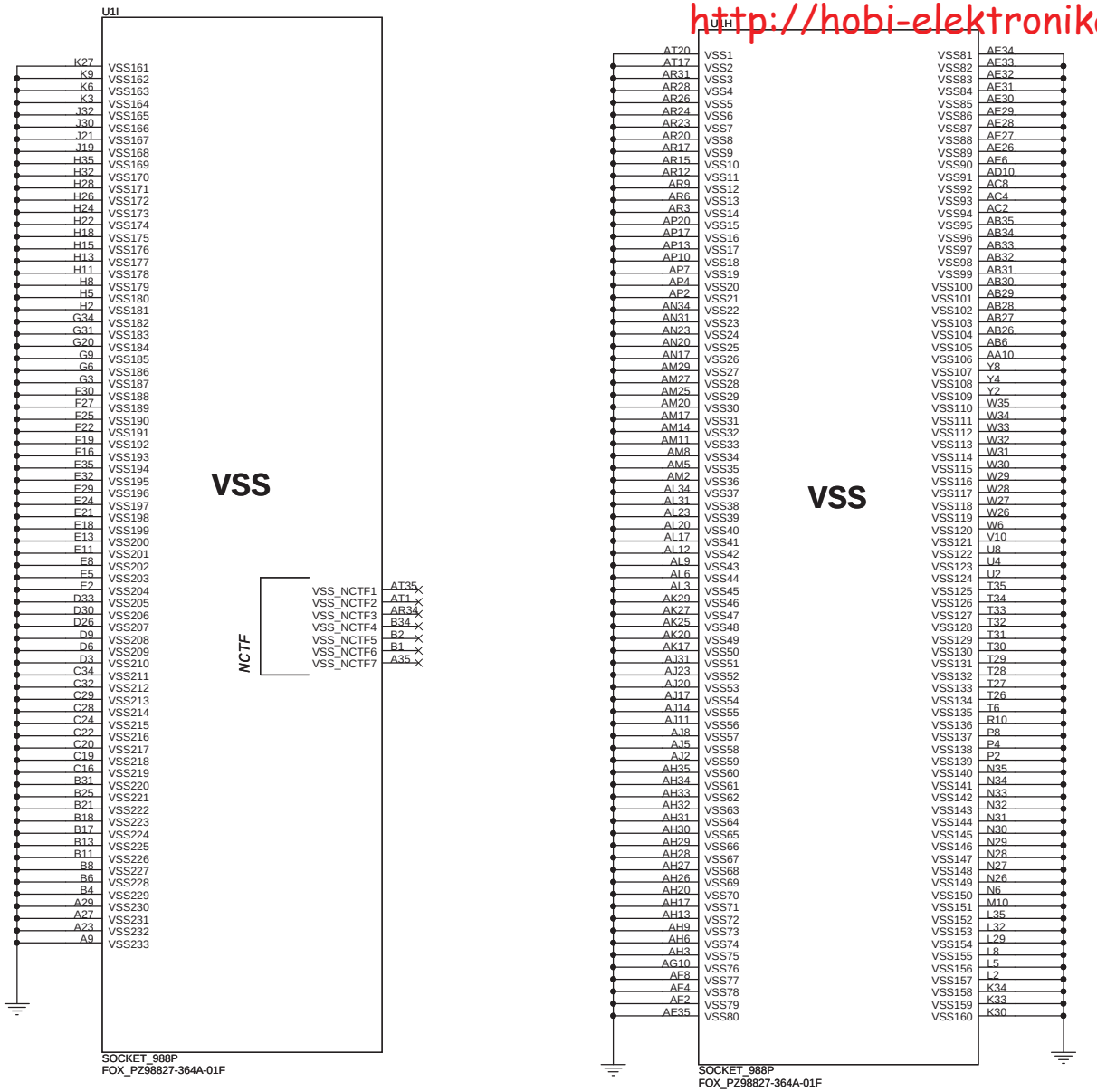
Intel Checklist Rev1.1 P54:
12x 0805 22uF inside cavity,
7x 0805 10uF under cavity and
9 x 0805 10uF between inductor
and socket on top layer



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Arrandale (POWER)	
Size: Custom	Document Number: W920 PVT	Rev: 0.1
Date: Monday, May 17, 2010	Sheet 6 of 71	

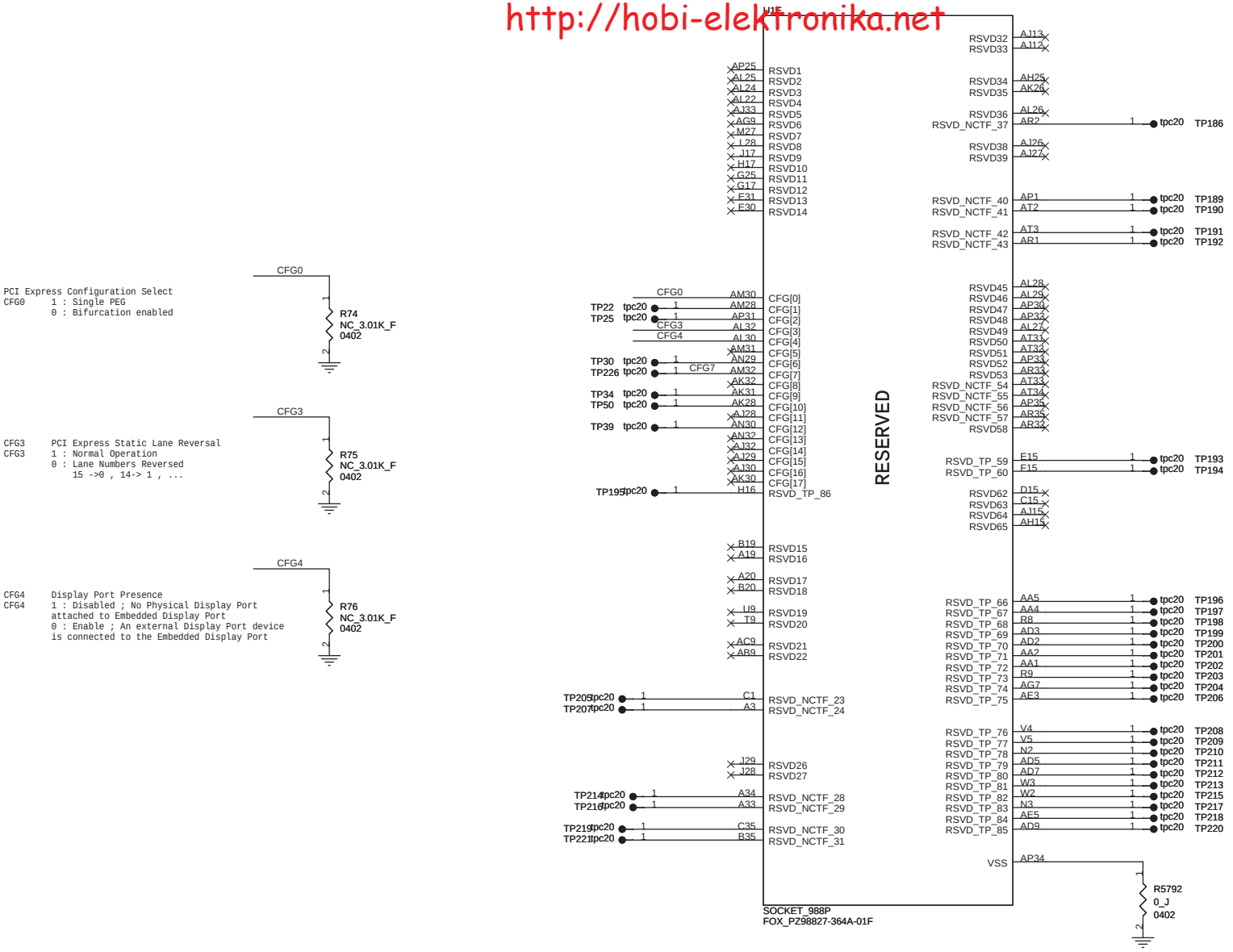


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Arrandale (GRAPHIC POWER)	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 7 of 71	

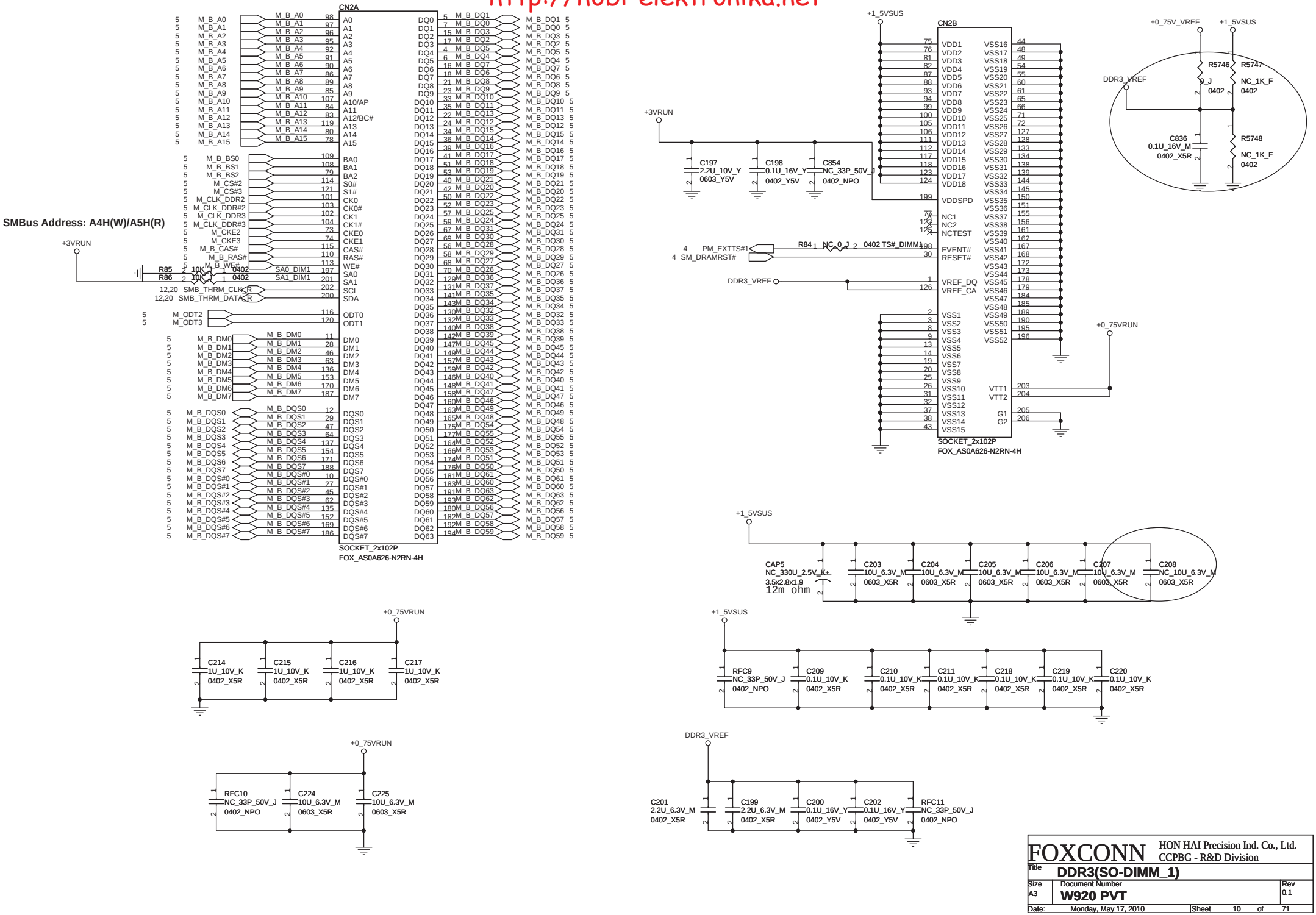


FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	Arrandale (GND)	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Wednesday, May 12, 2010	Sheet 8 of 71	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Arrandale (RESERVE)		
Size A3	Document Number W920 PVT		Rev 0.1
Date: Wednesday, May 12, 2010	Sheet 9 of 71		



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR3(SO-DIMM_1)	
Size A3	Document Number W920 PVT	Rev 0.1
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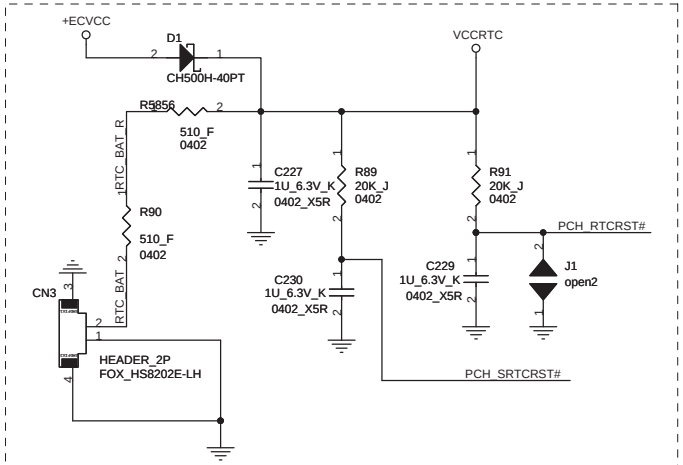
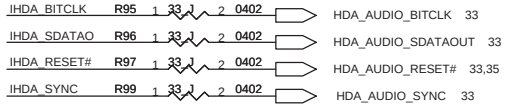
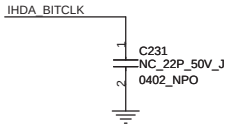
Delay time from VCCRTC high to RTCRST# inactive 18~25mS

http://hobi-elektronika.net

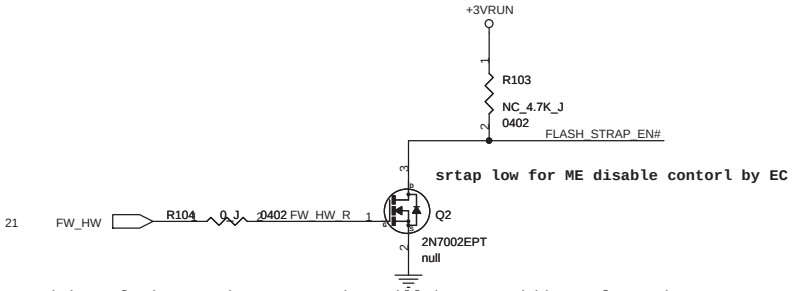
0223: Change Y1 from 1F-X32K768-1000 to 1F-X32K768-2006 for purchase difficult







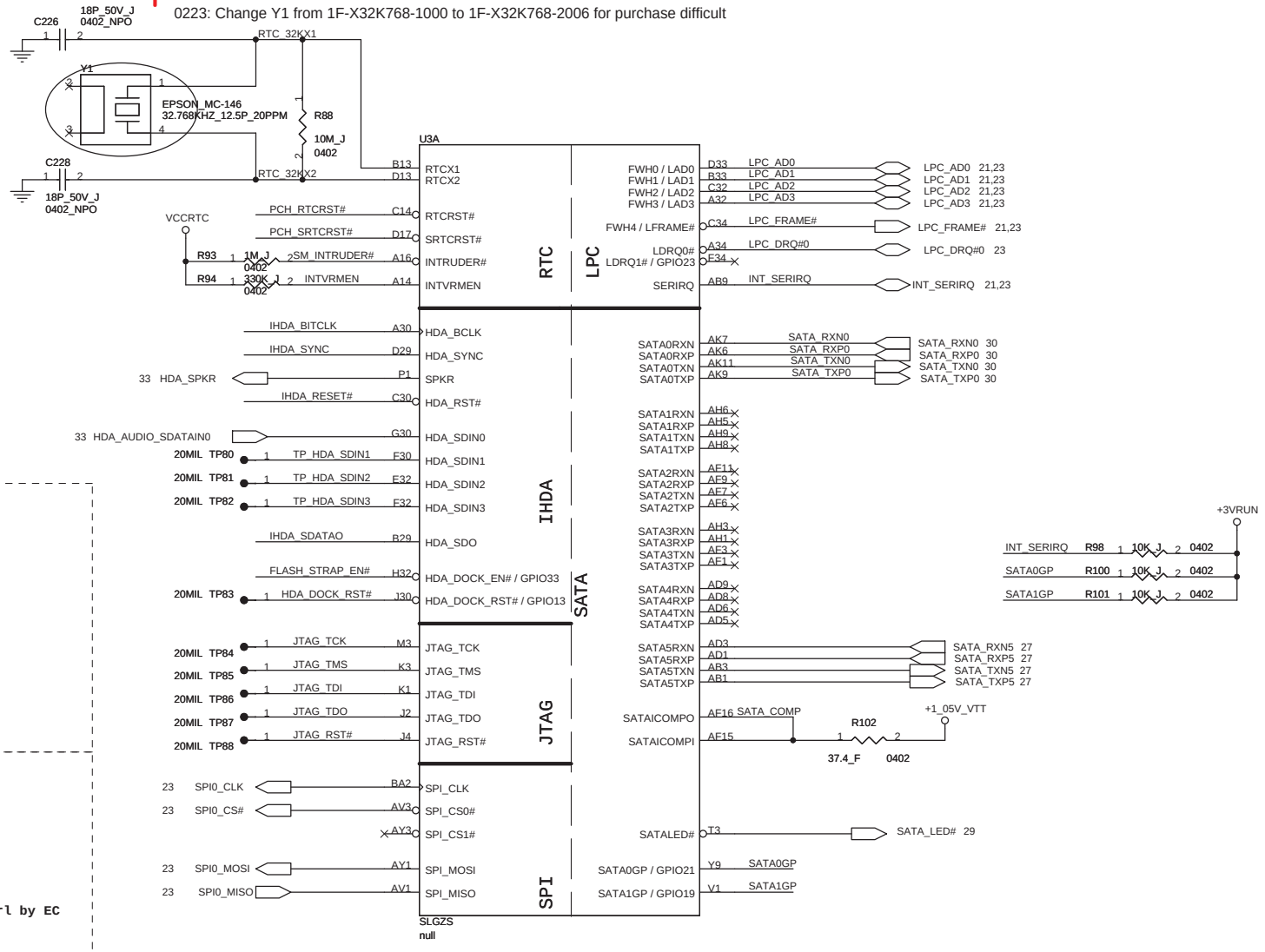
Audio



Low (0) – Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.
High (1) – Security measure defined in the Flash Descriptor will be enabled

HDA_SYNC internal Pull-D

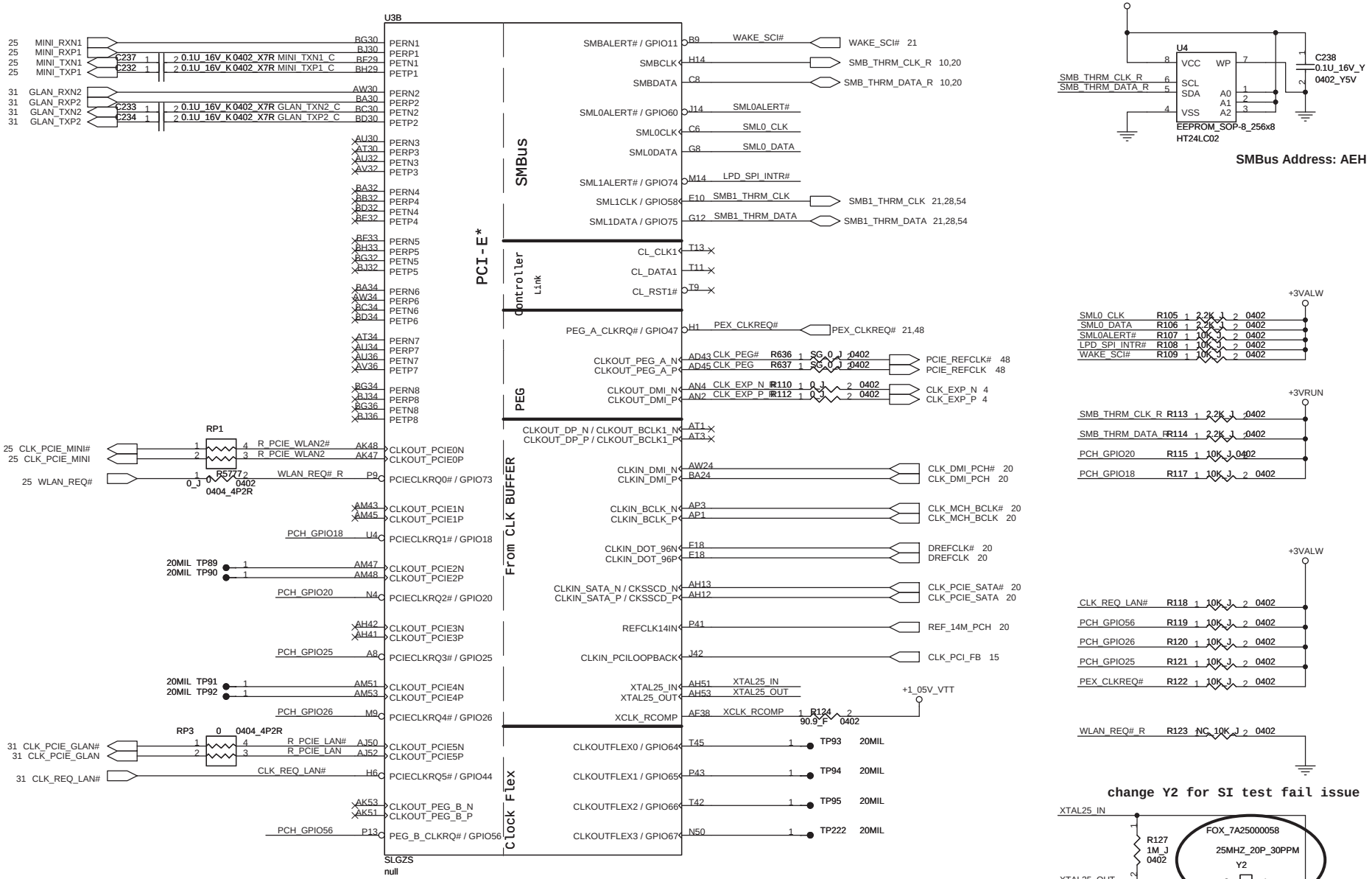
HIGH=Default On Die PLL VR is supplied by 1.5V
LOW= On Die PLL VR is supplied by 1.8V

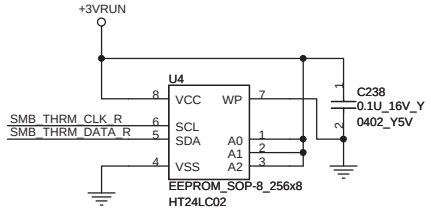


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	PCH (HDA,JTAG,SAT)		
Size A3	Document Number W920 PVT		Rev 0.1
Date: Monday, May 17, 2010	Sheet 11 of 71		

PCI-E Port Table

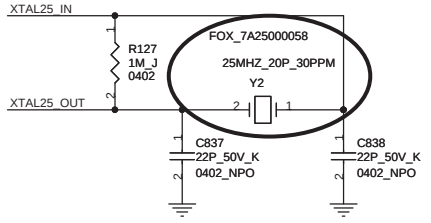
Port	Function
Port1	WLAN
Port2	Gigabit LAN
Port3	X
Port4	X
Port5	X
Port6	X
Port7	X
Port8	X



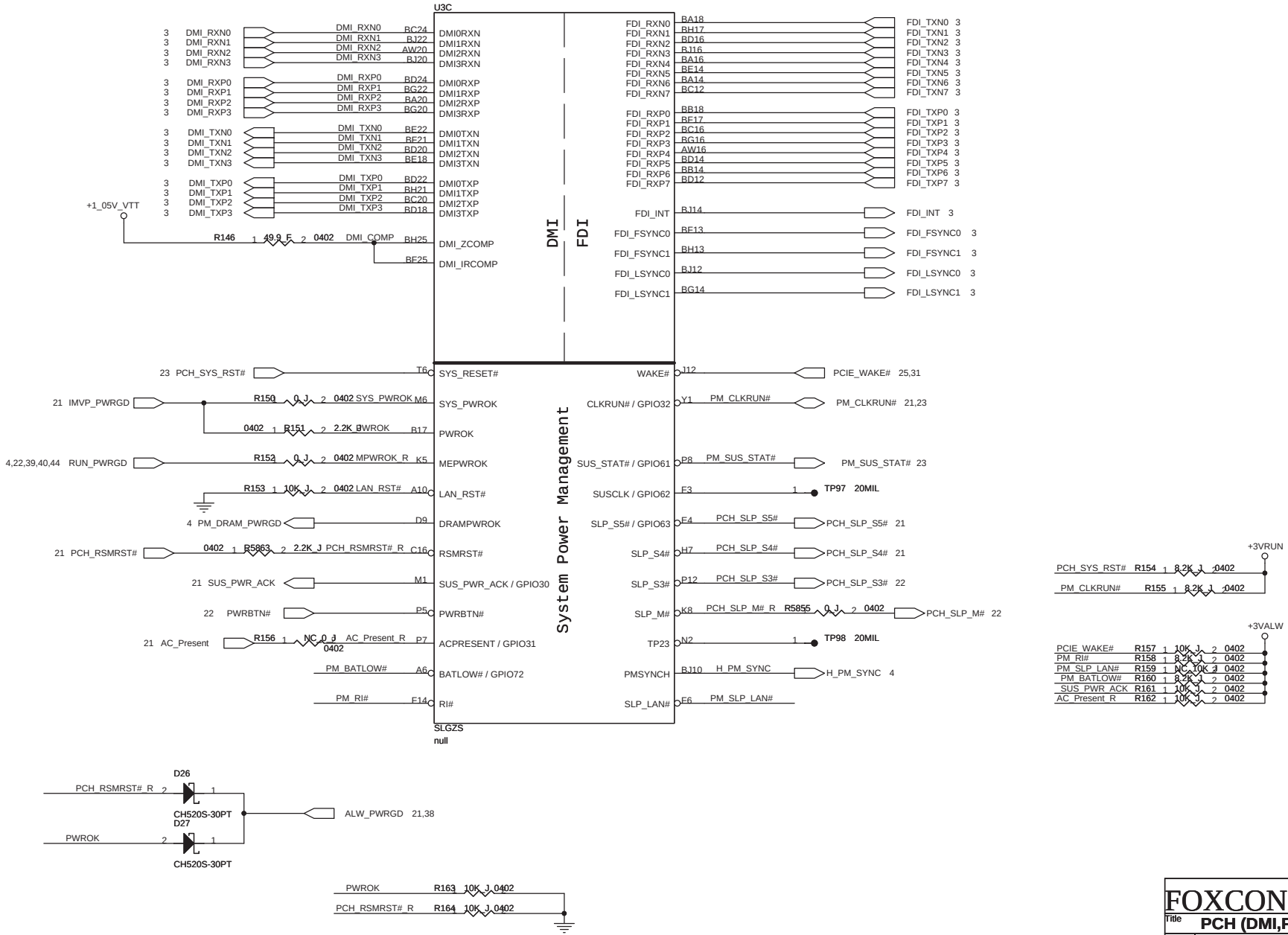


SMBus Address: AEH

change Y2 for SI test fail issue

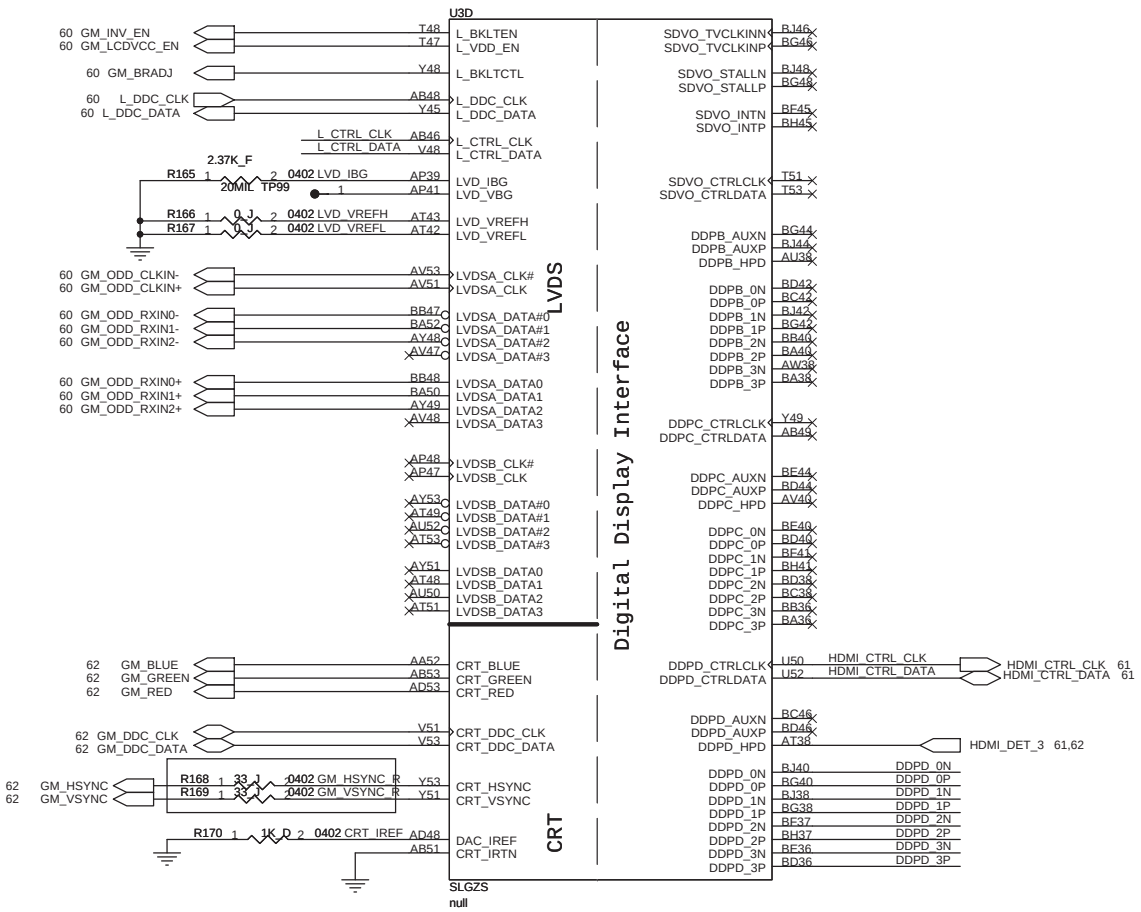


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (PCI-E,SMBUS,CLK)	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 12 of 71	

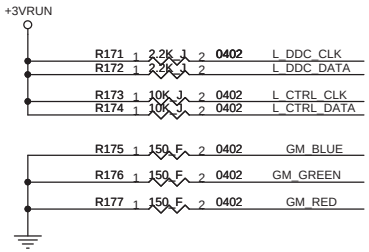


FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

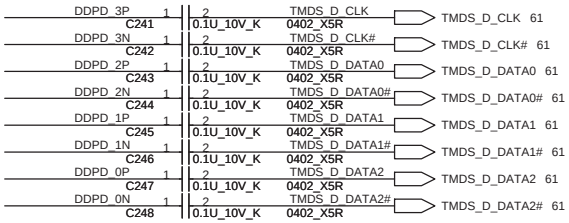
Title	PCH (DMI,FDI,GPIO,PM))	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 13 of 71	



04/15:Calpella Platform – Design Guide - Addendum / Update – Rev. 1.52 (Doc #414044).).



Place resistor close to PCH



FOXCONN — HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	PCH (LVDS,DDI)	
Size A3	Document Number W920 PVT	Rev 0.1
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DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Intel AT-d is capable of being enabled when sampled high.

USB PORT	Function
PORT-0	USB PORT1
PORT-1	USB PORT2
PORT-2	USB PORT3
PORT-3	Blue tooth
PORT-4	NC
PORT-5	CAMERA
PORT-6	NC
PORT-7	NC
PORT-8	Card reader
PORT-9	WLAN Change to NC
PORT-10	NC
PORT-11	NC
PORT-12	NC
PORT-13	NC

Strap for Boot-BIOS

	GNT1#	GNT0#
LPC	LOW	LOW
Reserved (NAND)	LOW	Hi
PCI	Hi	LOW
SPI(Default)	Hi	Hi

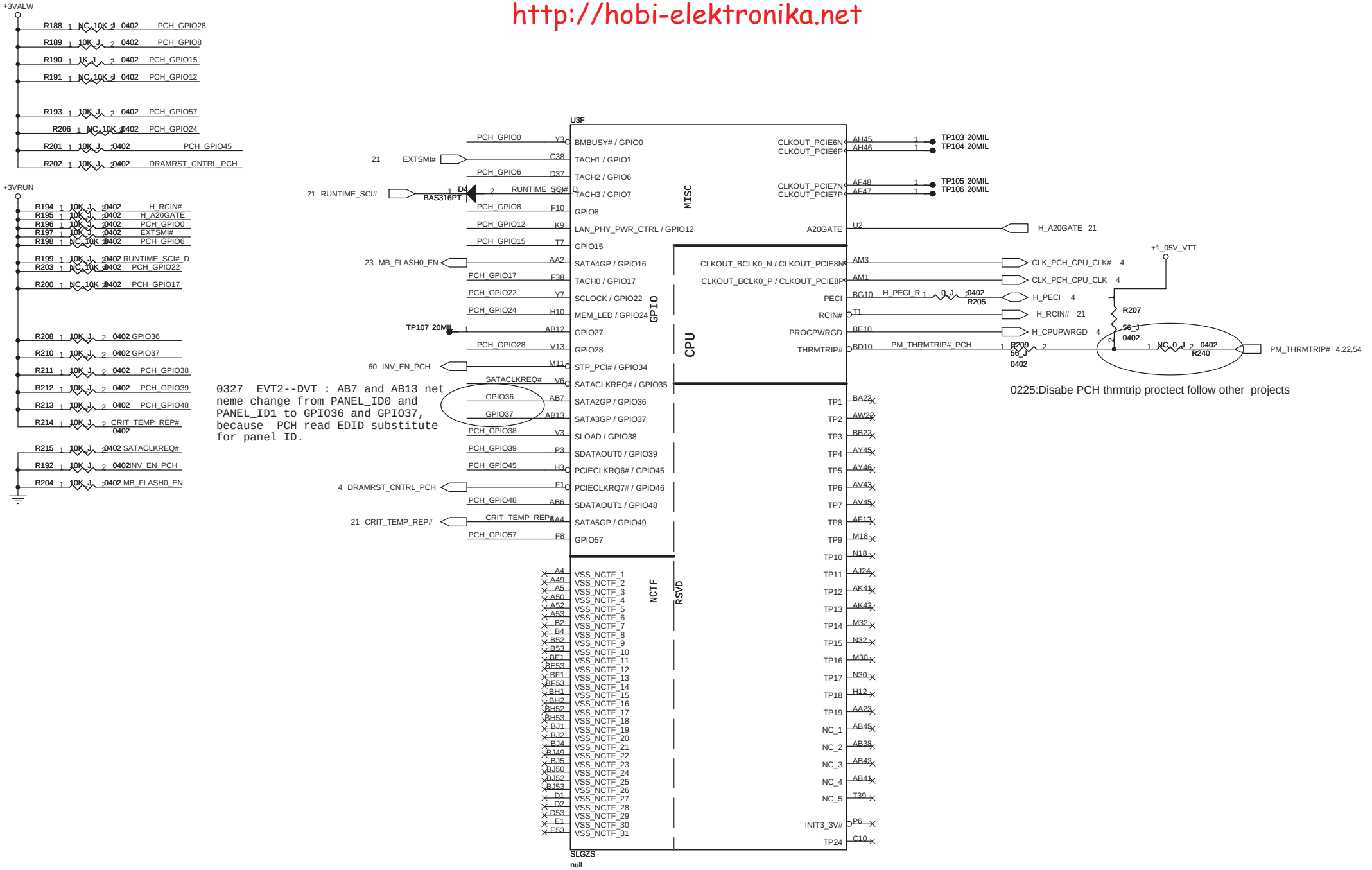
Internal pull-up 20K

In case of BIOS flash failed, the system may not boot OS.
Our BIOS will implement a feature, when short the pad,
BIOS will perform crisis recovery.
If possible, please put the pad near the DIMM door,
then end-user will be easily to recover their BIOS.

Reserve for BIOS Reset
Place close to DIMM door

Buffer to reduce loading on PLT_RST#.

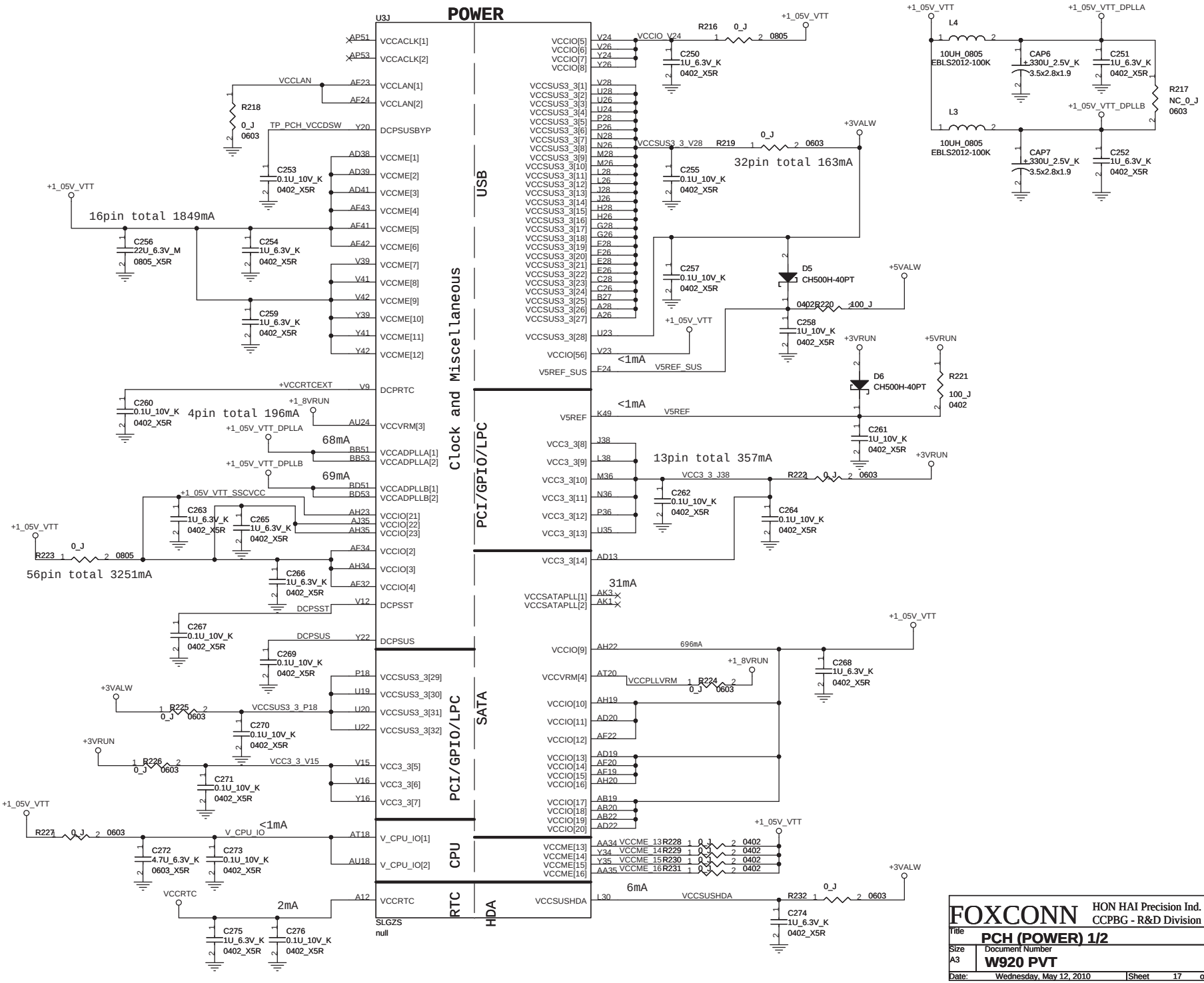
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	PCH (PCI,USB,NVRAM)		
Size A3	Document Number W920 PVT		Rev 0.1
Date: Monday, May 17, 2010		Sheet 15 of 71	



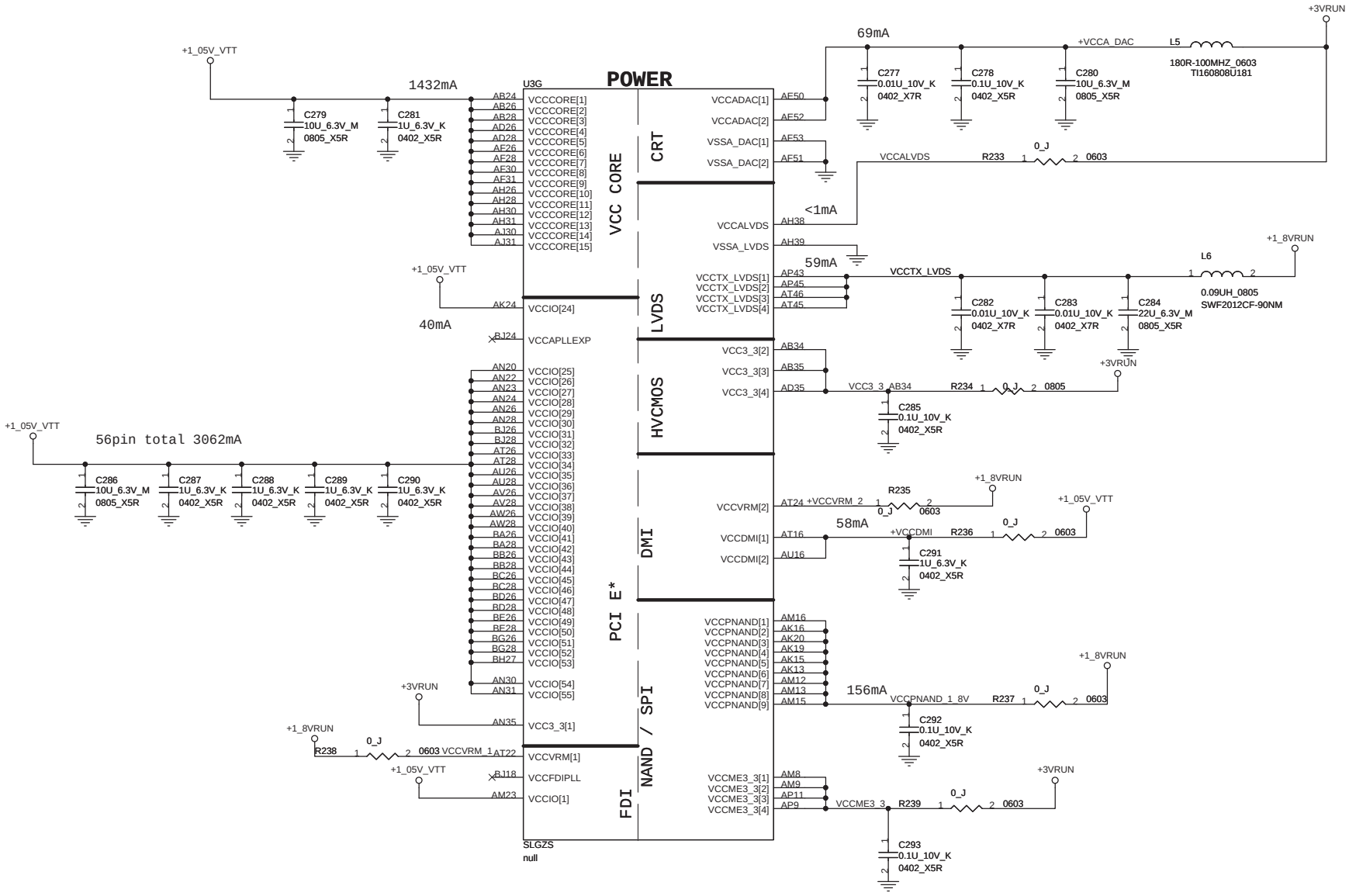
0327 EVT2--DVT : AB7 and AB13 net neme change from PANEL_ID0 and PANEL_ID1 to GPIO36 and GPIO37, because PCH read EDID substitute for panel ID.

0225:Disabe PCH thrmtrip proctect follow other projects

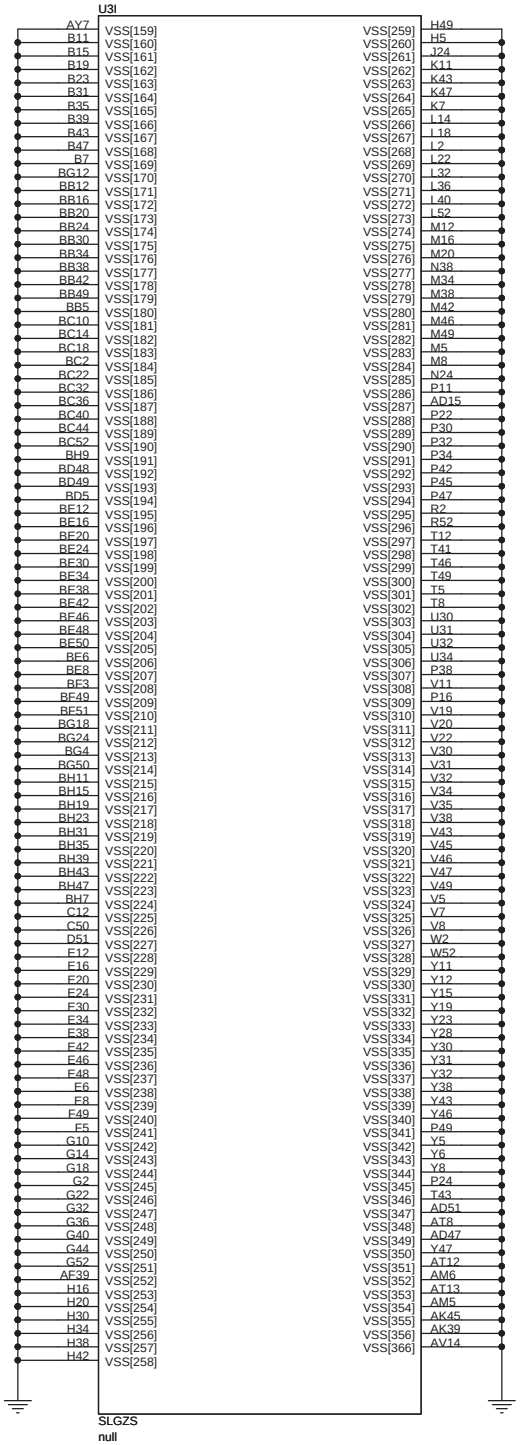
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (GPIO,VSS_NCTF,RSVD)	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 16 of 71	

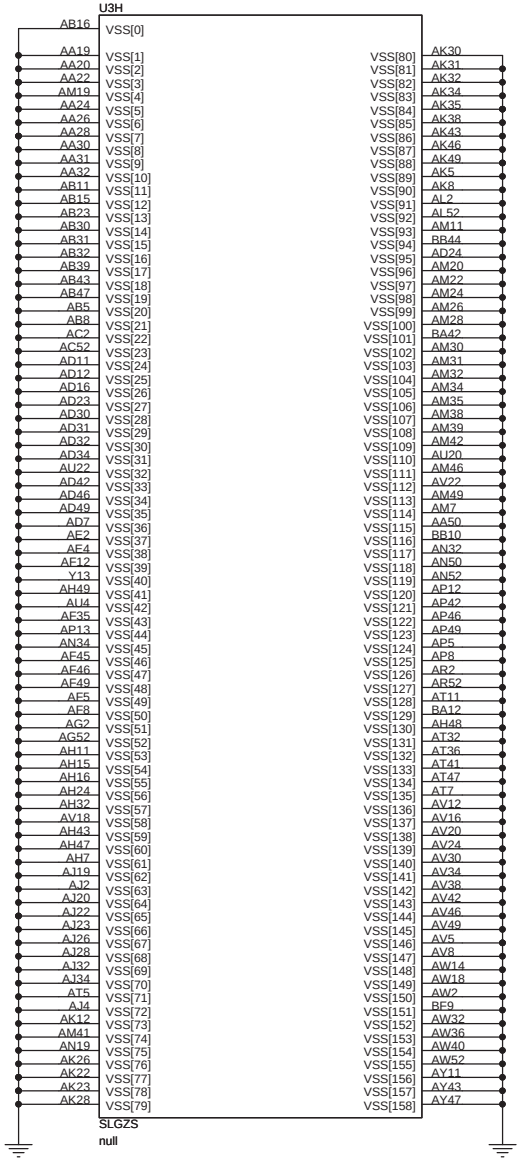


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (POWER) 1/2	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Wednesday, May 12, 2010	Sheet 17 of 71	



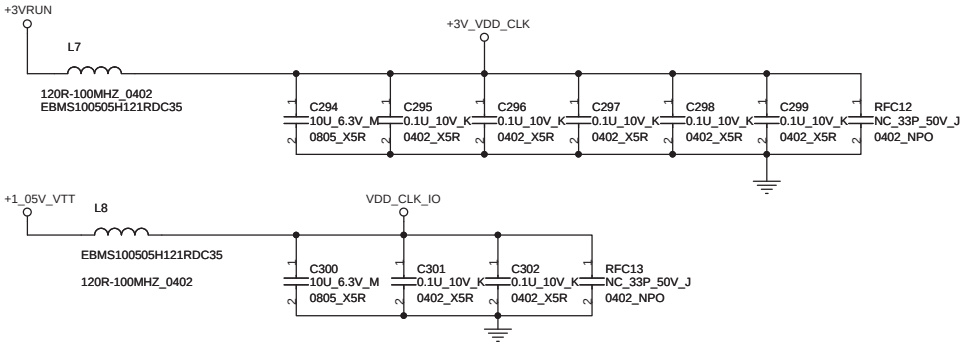
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (POWER) 2/2	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Friday, May 14, 2010	Sheet 18 of 71	

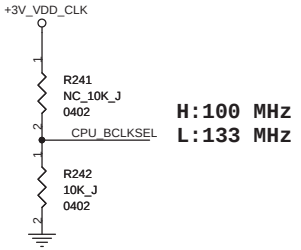


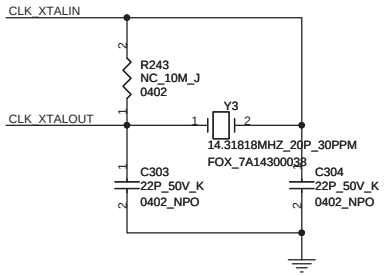


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	PCH (VSS)		
Size A3	Document Number W920 PVT		Rev SB
Date: Wednesday, May 12, 2010	Sheet 19 of 71		

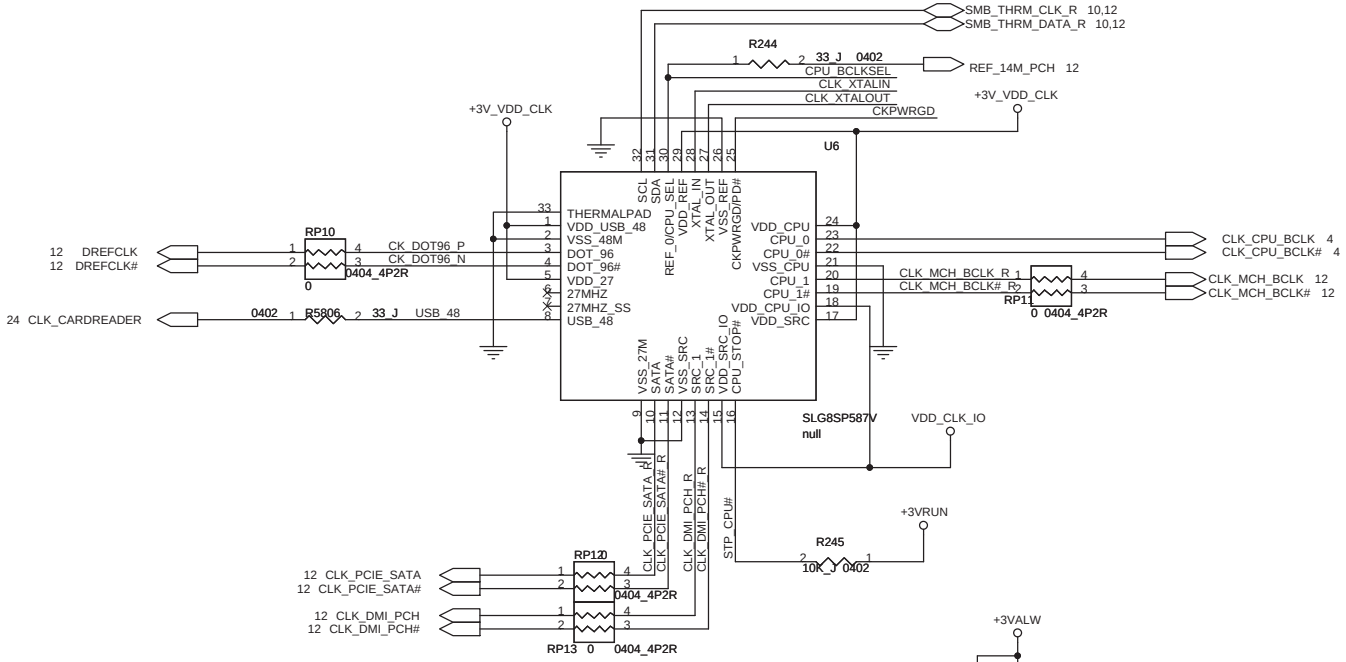
FS	CPU	Power On	SRC	SATA	DOT96	REF	GPU	Card reader
0	133MHz	Default	100MHz	100MHz	96MHz	14.318MHz	27 MHz	48 MHz
1	100MHz							

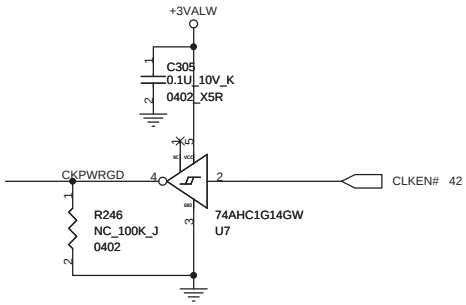






SMBUS Address:D2H





FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title: Clock Gen			
Size: A3	Document Number: W920 PVT		Rev: 0.1
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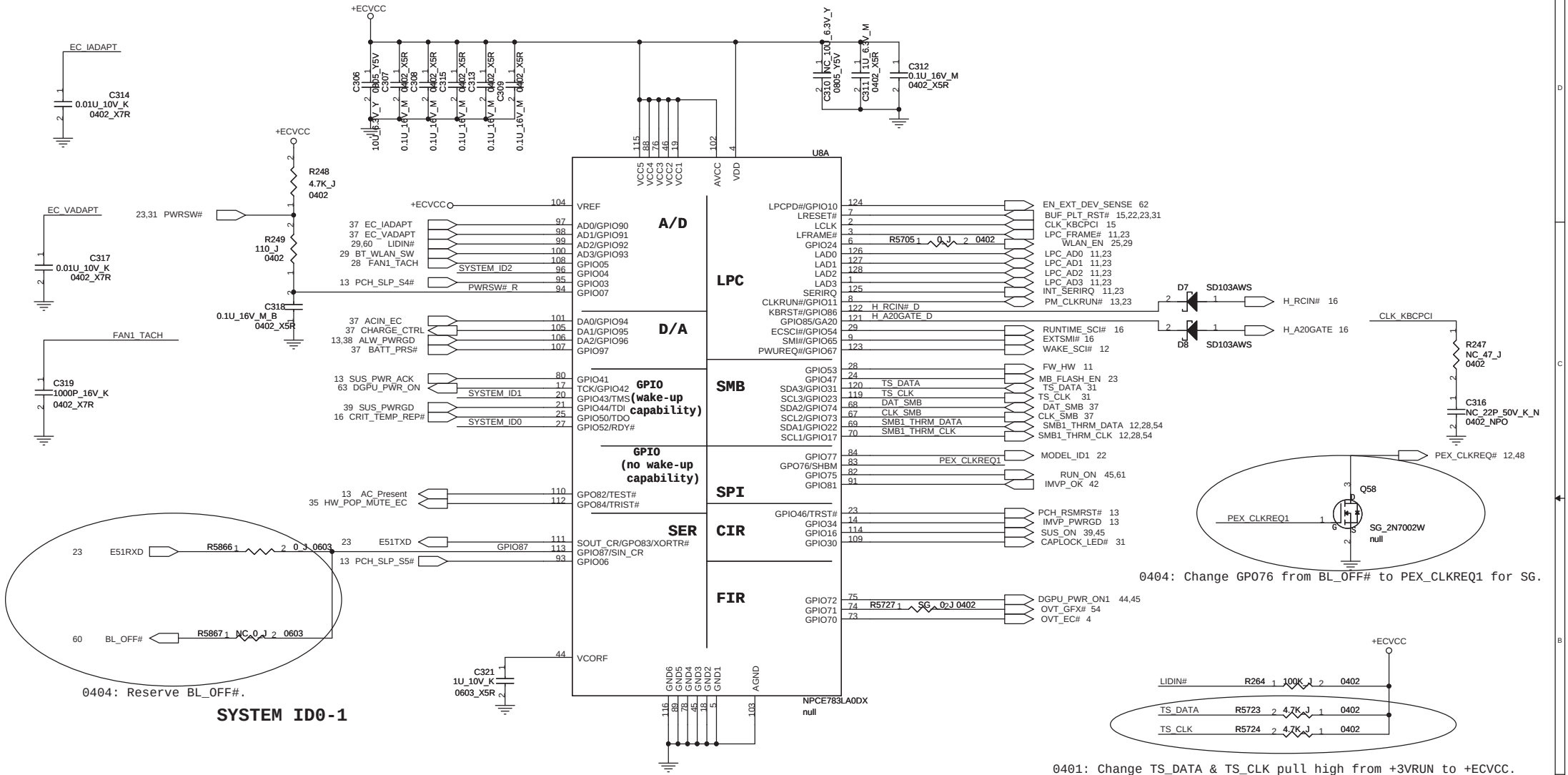

	SYSID0	SYSID1	SYSID2
W920	0	0	0
W930	1	0	0

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title: EC+KBC(WPCE775L) 1/2

Size: A3 | Document Number: W920 PVT | Rev: 0.1

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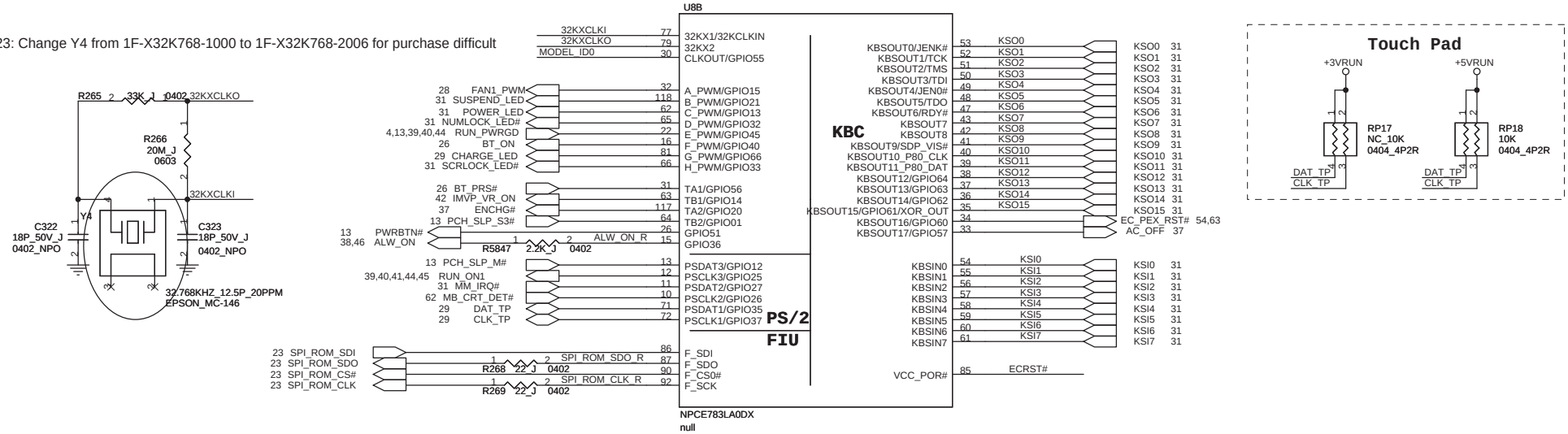
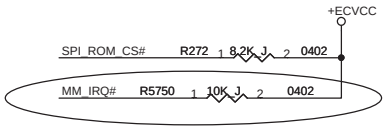
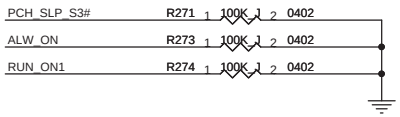
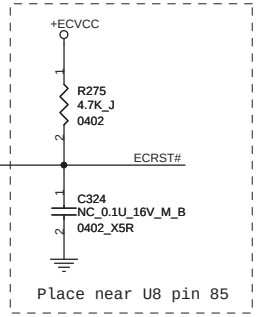
0223: Change Y4 from 1F-X32K768-1000 to 1F-X32K768-2006 for purchase difficult



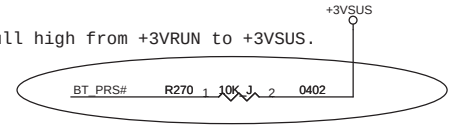


0401: Change MM_IRQ pull high from +3VRUN to +ECVCC.

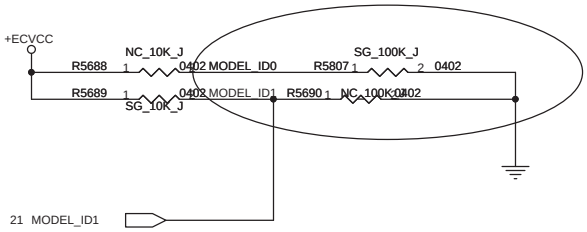


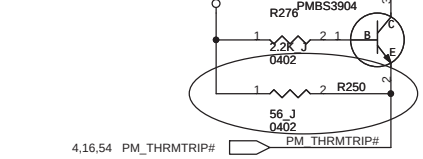


0406: Change BT_PRS# pull high from +3VRUN to +3VSUS.



0401: Cancel NC 100Kohm R5687 for SG.





0225:Add thrmtrip# pull up for disabe PCH thrmtrip proctect .

MODEL ID0-1

ID1	ID0	SKU
1	0	external GFX with SG
0	0	NC
1	1	NC

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	EC+KBC(WPCE775L) 2/2	
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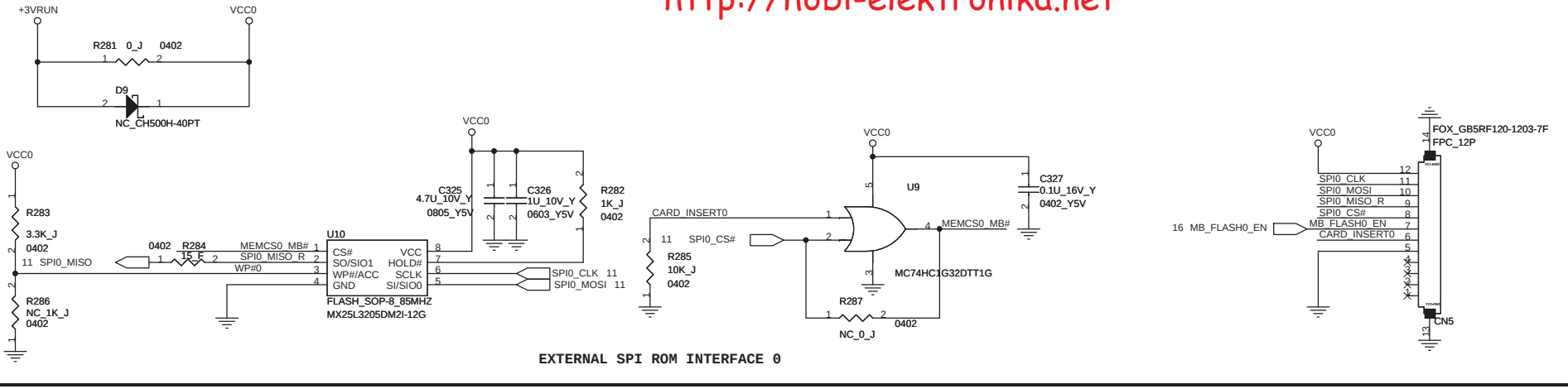
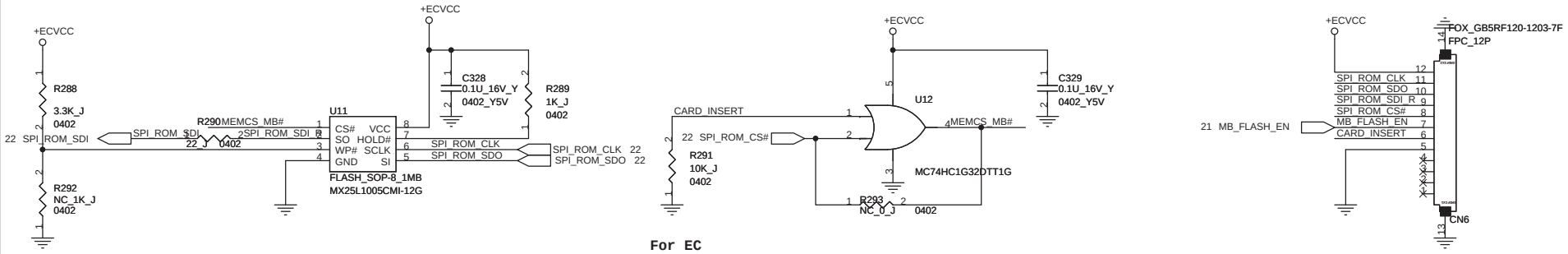
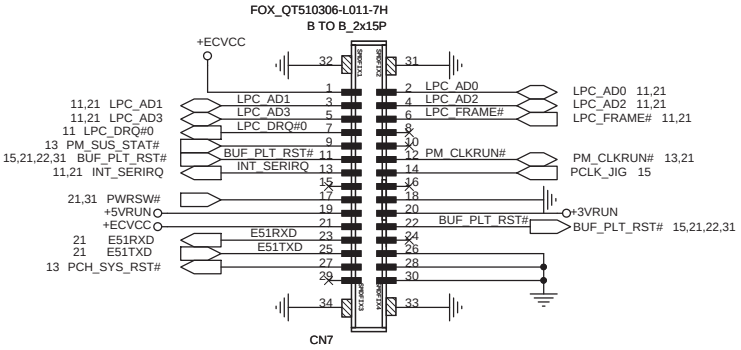


EXTERNAL SPI ROM INTERFACE 0

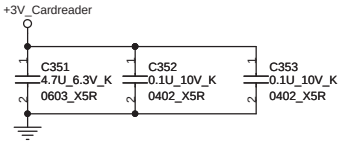


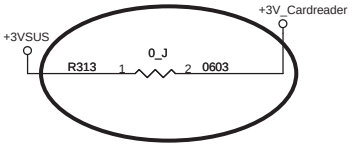
For EC

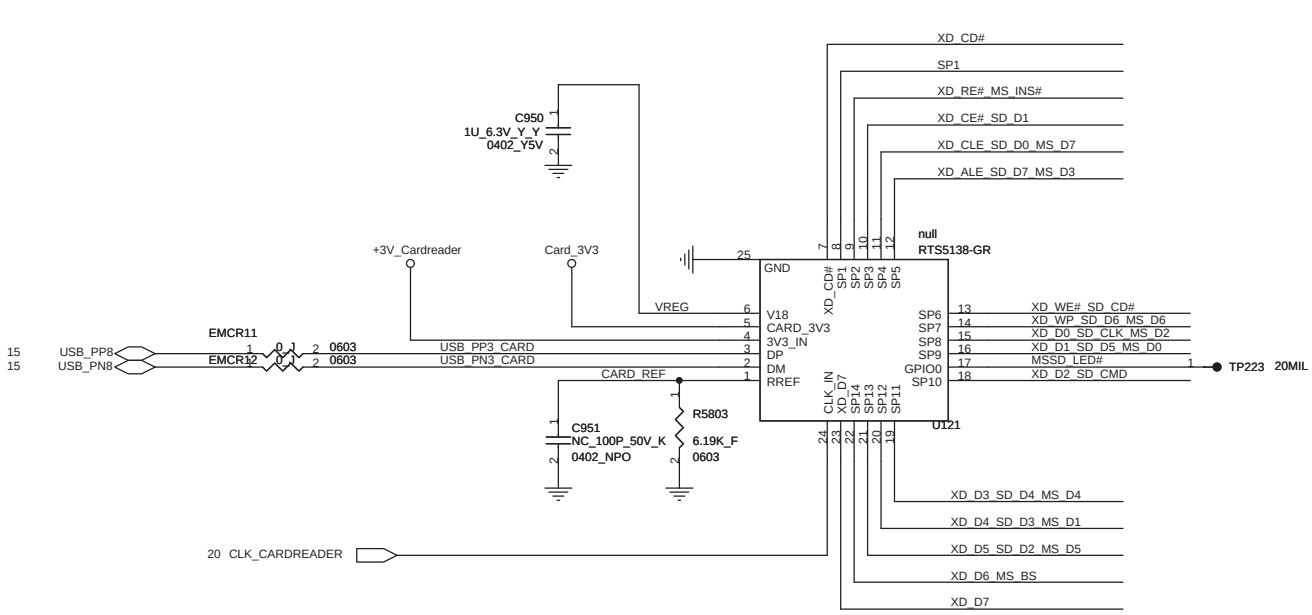


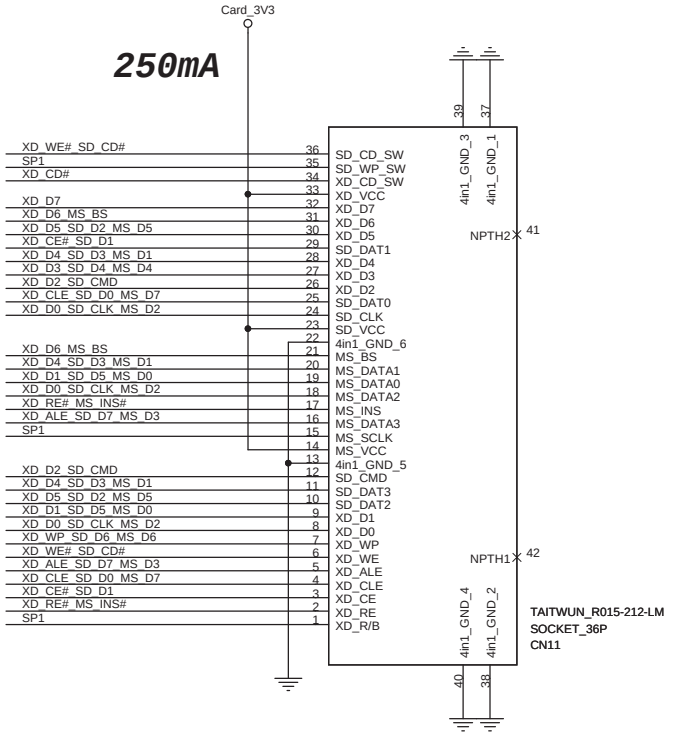
JIG-120

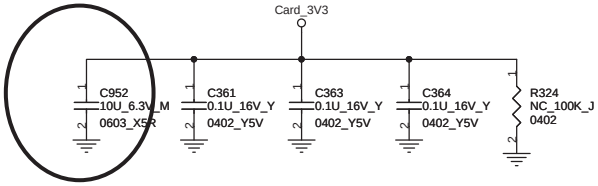
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	BIOS ROM/DEBUG PORT	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 23 of 71	





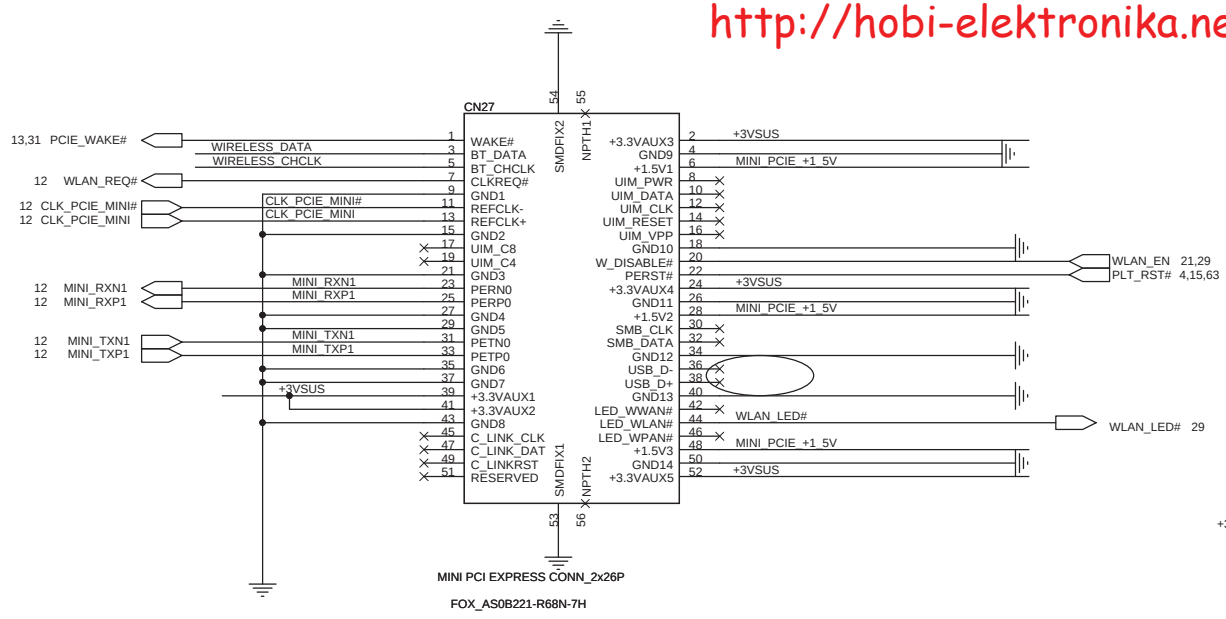






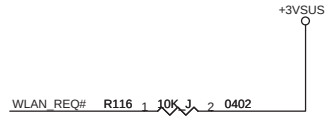
change form NC_4.7uF to 10uF on DVT

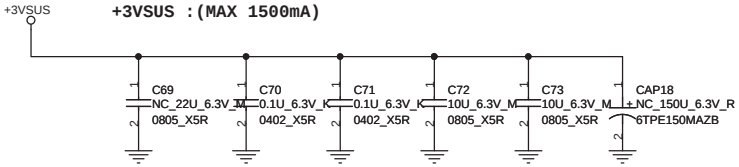
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Card reader (TRS5159-GR)	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 24 of 71	

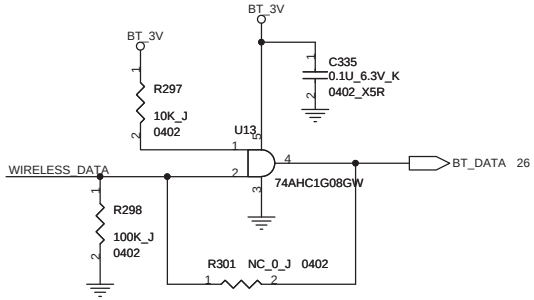


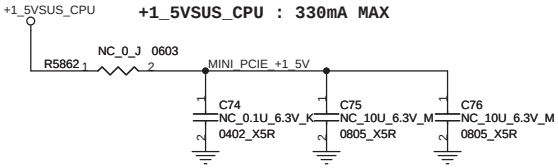
MINI PCI EXPRESS CONN_2x26P

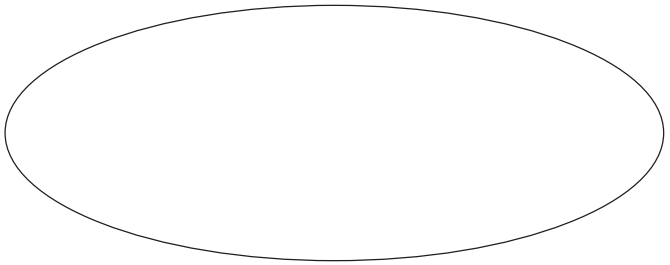
FOX_AS0B221-R68N-7H



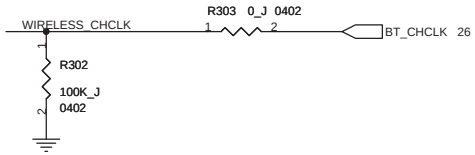




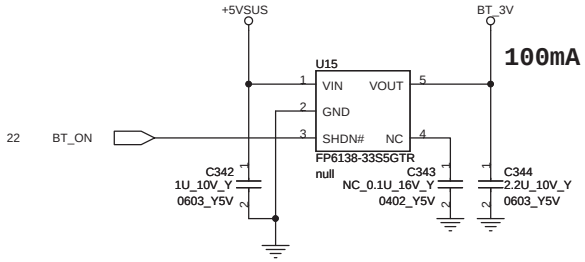




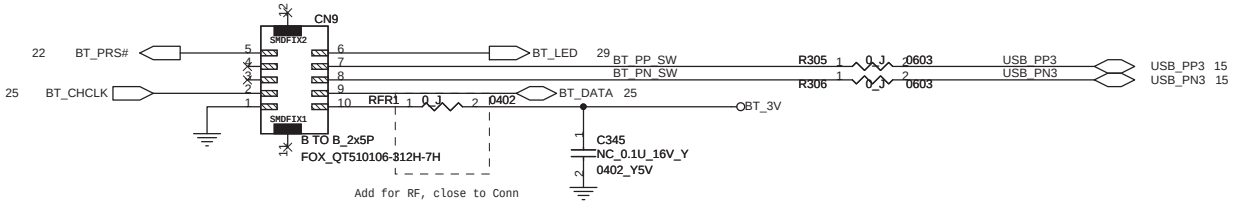
0408 EVT2--DVT: Delete U14 and C334 ,which were for Wlan usb interface!



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	WLAN	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 25 of 71	



Bluetooth CONN



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Bluetooth Connextor	
Size A3	Document Number W920 PVT	Rev 0.1
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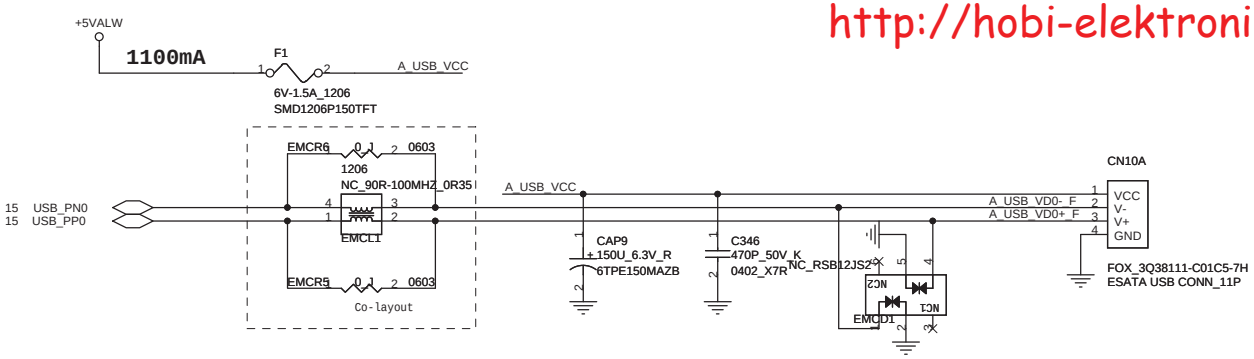
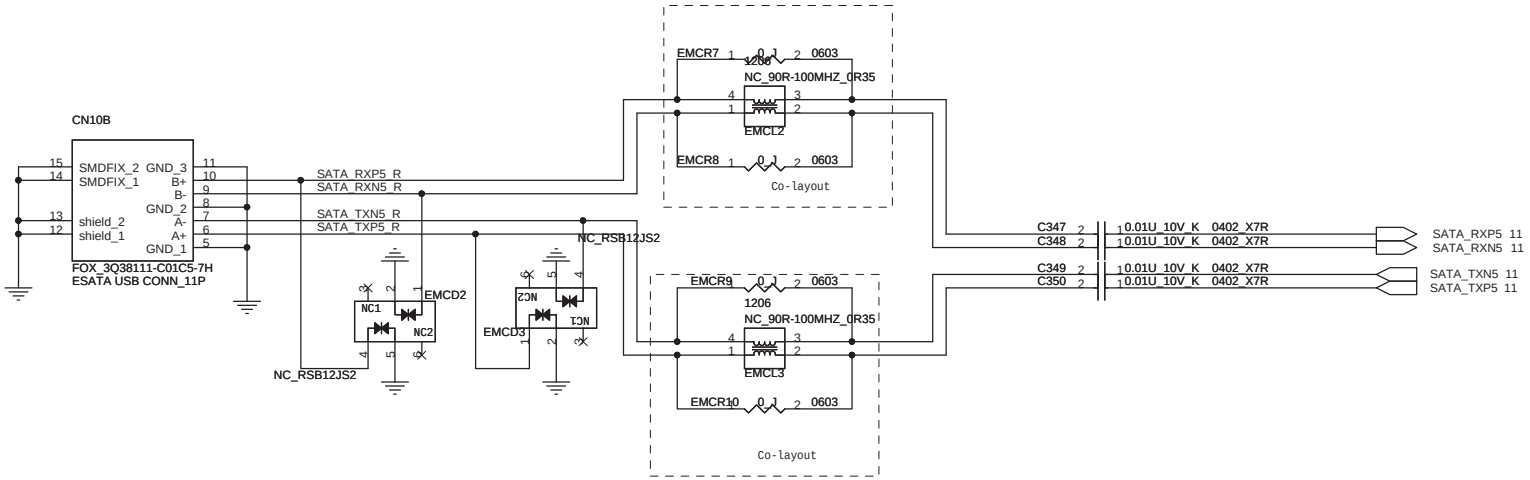


USB/eSATA Combo



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	USB/eSATA Combo	
Size A3	Document Number W920 PVT	Rev 0.1
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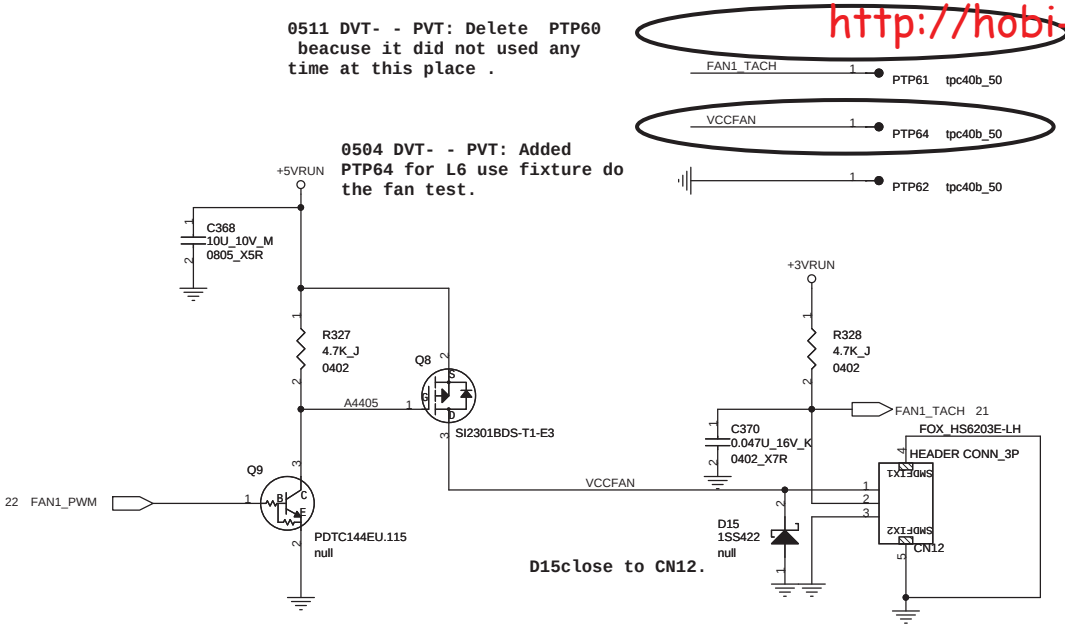
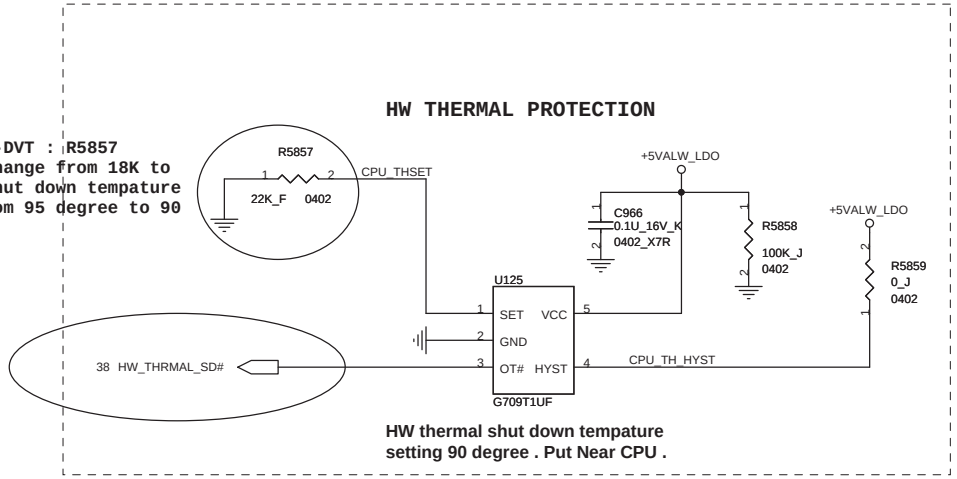
0511 DVT- - PVT: Delete PTP60 beacuse it did not used any time at this place .

0504 DVT- - PVT: Added PTP64 for L6 use fixture do the fan test.

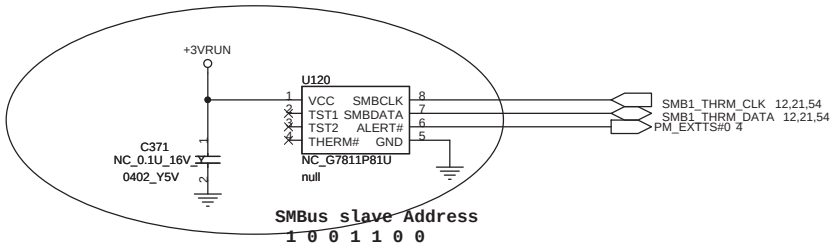


FAN

0401 EVT2--DVT : R5857 resister Change from 18K to 22K, for shut down tempature setting from 95 degree to 90 degree.



0323 EVT2--DVT Change: U125 pull low HW_THRMAL_SD# from pull low ALW_ON, for Sequence issue when this function action at EC hang up.



0312 EVT2--DVT Change: NC U120 and NC C371 which are for DDR thermal senser.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: FAN/THERMAL SENSOR		
Size: A3	Document Number: W920 PVT	Rev: 0.1
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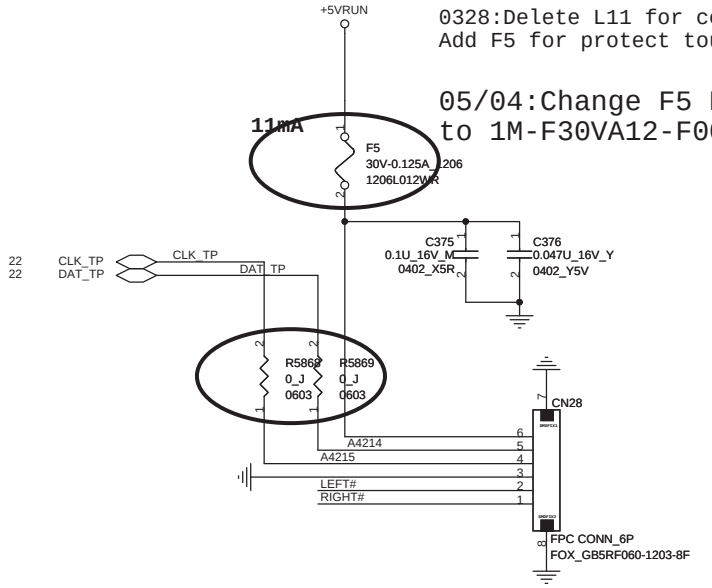
Touch Pad CONN.

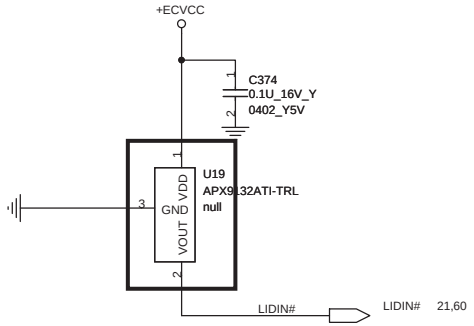
0328:Delete L11 for cost down.
Add F5 for protect touch pad

05/04:Change F5 HH PN from 1M-F10V0A1-F000
to 1M-F30VA12-F000 for vendor PN change

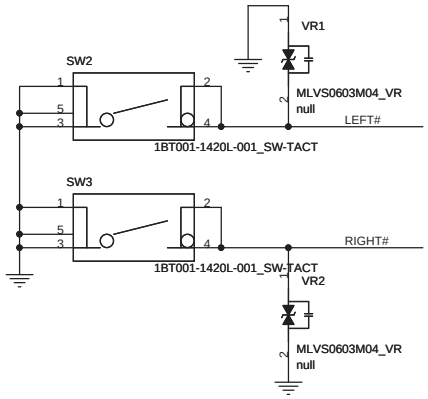


0328: Delete L9,L10&L10 for cost down and add R5868 &R5869 .

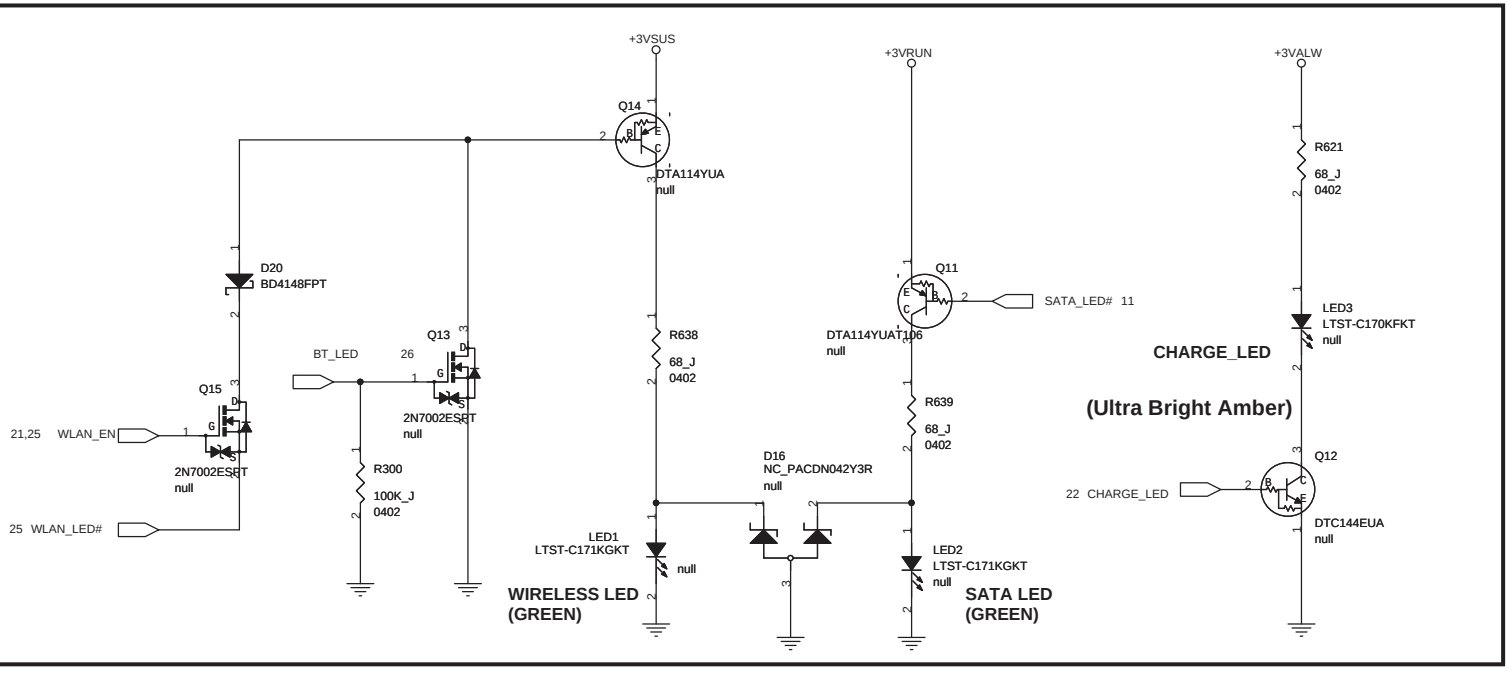
LID Switch



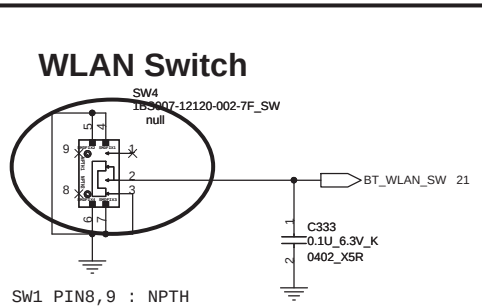
TP_LEFT Button



TP_Right Button



WLAN Switch



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	TOUCHPAD&LID and LED	
Size A3	Document Number W920 PVT	Rev 0.1
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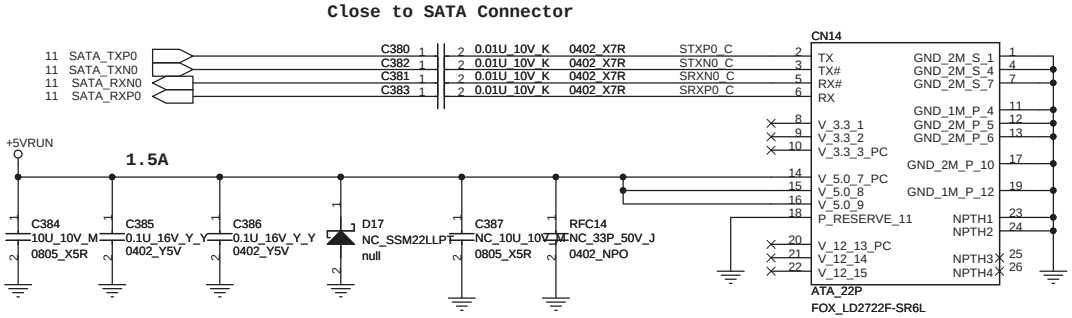
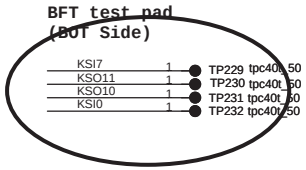
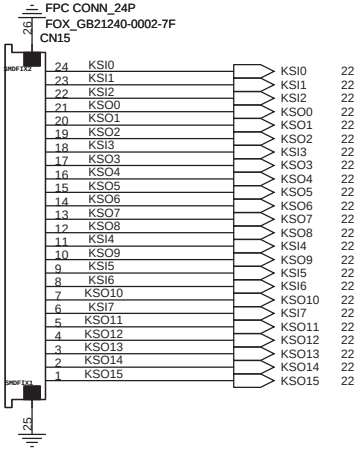
SATA HDD CONN



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: SATA HDD CONN		
Size: A3	Document Number: W920 PVT	Rev: 0.1
Date: Monday, May 17, 2010	Sheet 30 of 71	

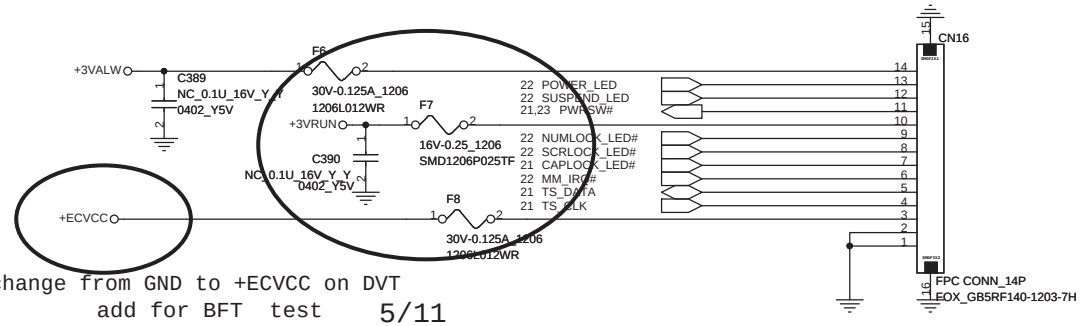
K/B CONN





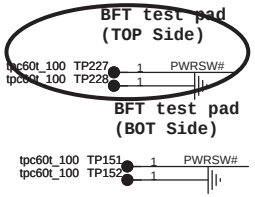
5/11
Change KB test piont for TE request

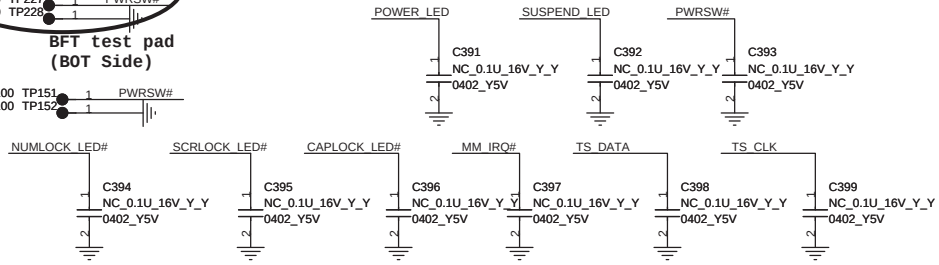
CONN TO Touch Sensor daughter board



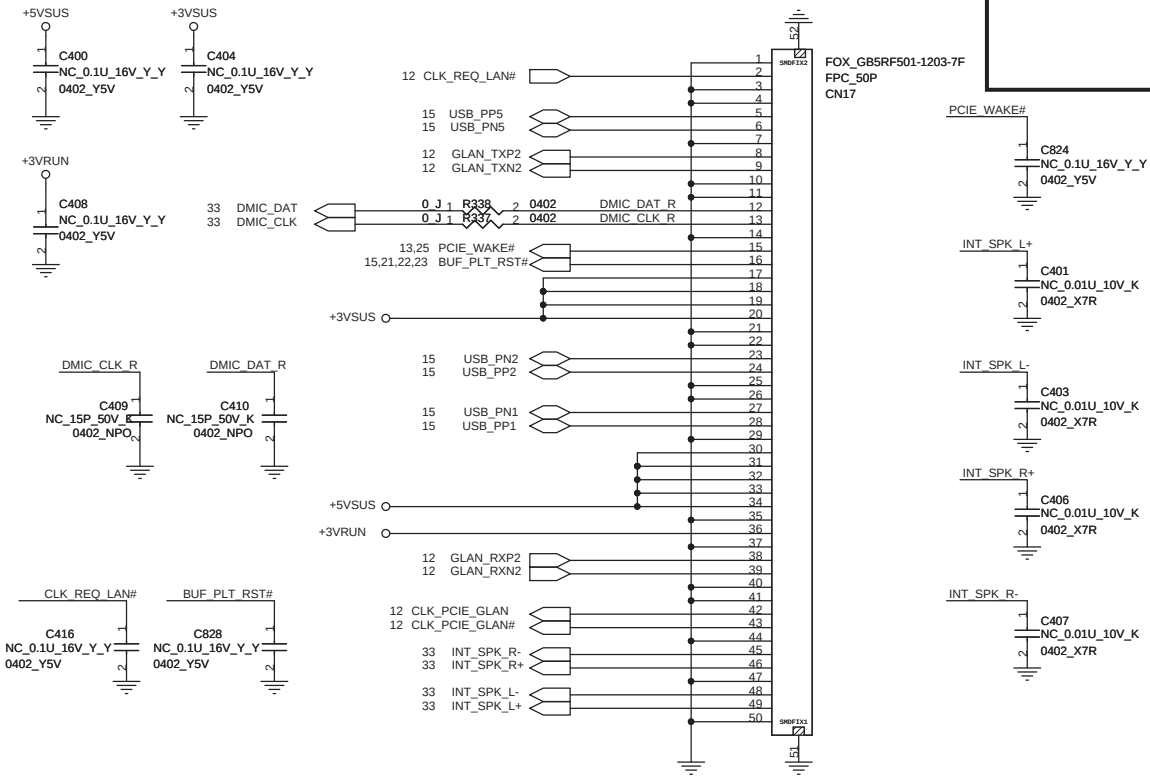
change from GND to +ECVCC on DVT
add for BFT test

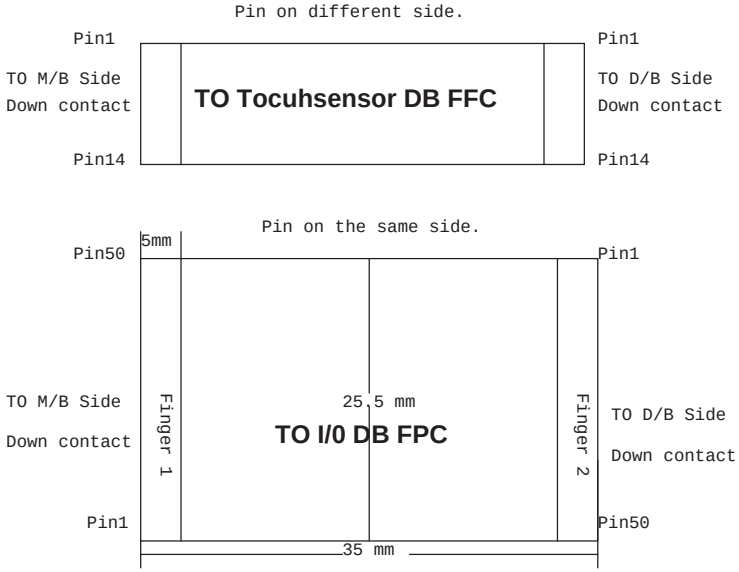
5/11
Add F6,F7&F8for system safety





CONN to I/O daughter board





FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	KB/DB CONNECTOER	
Size A3	Document Number W920 PVT	Rev 0.1
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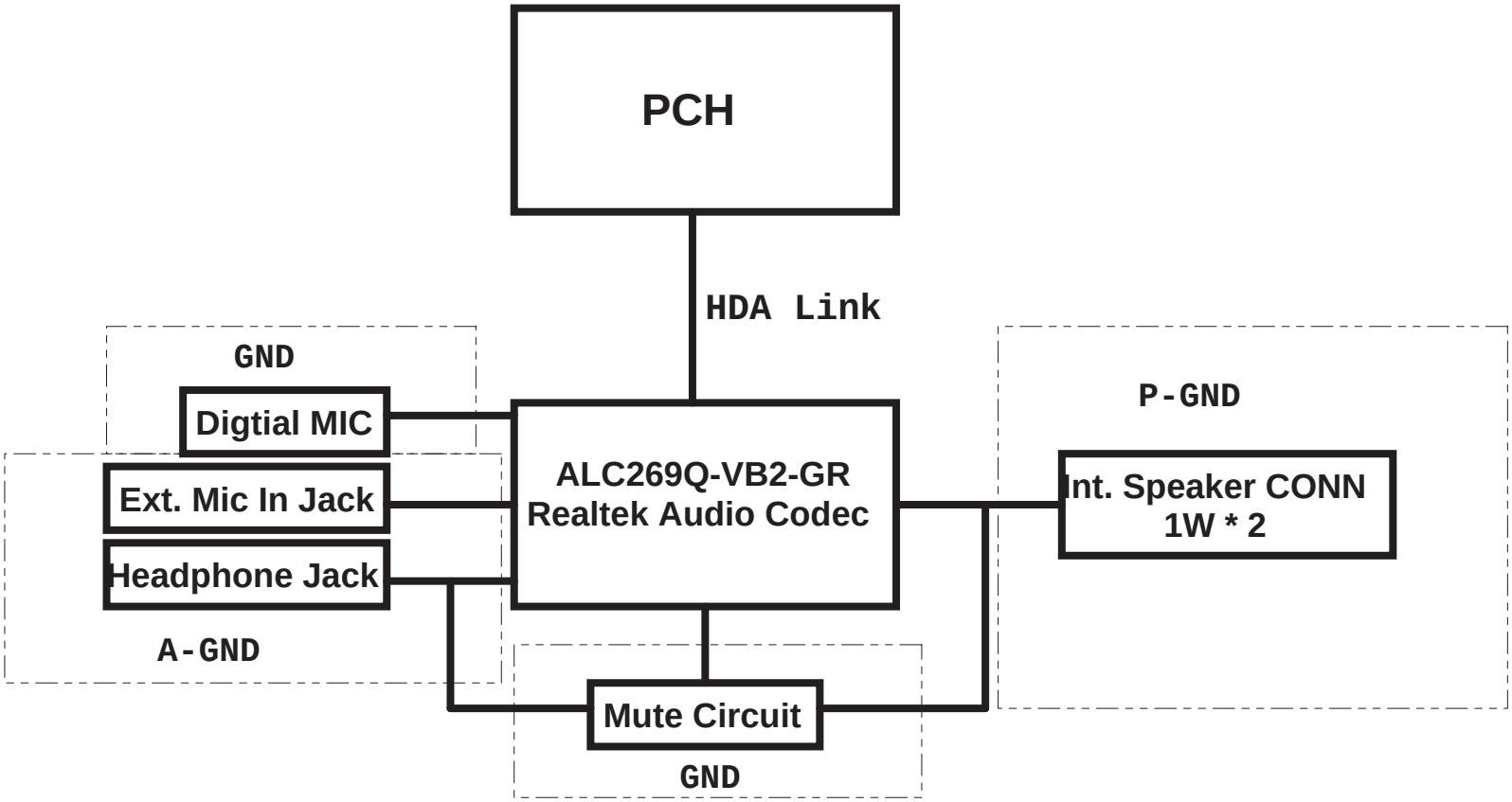
Audio Block Diagram



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: Audio Block Diagram		
Size: A3	Document Number: W920 PVT	Rev: 0.1
Date: Wednesday, May 12, 2010	Sheet 32 of 71	

C758 place close to Pin1, C762 place close to Pin 9

C756 place close to Pin35, C754 place close to Pin 38

C765&CAP11 place close to pin 39

C767&CAP13 place close to pin 46

0407: Reserve RC filter for EMC.

C806,C807 place close to pin 27

R577,C783,C822 place close to pin 12

Add Bead for ALC269Q-VB2-GR colay

AUDIO POWER(4.75V/200mA)

Place together

Place together

Place together

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	Codec
Size A3	Document Number W920 PVT
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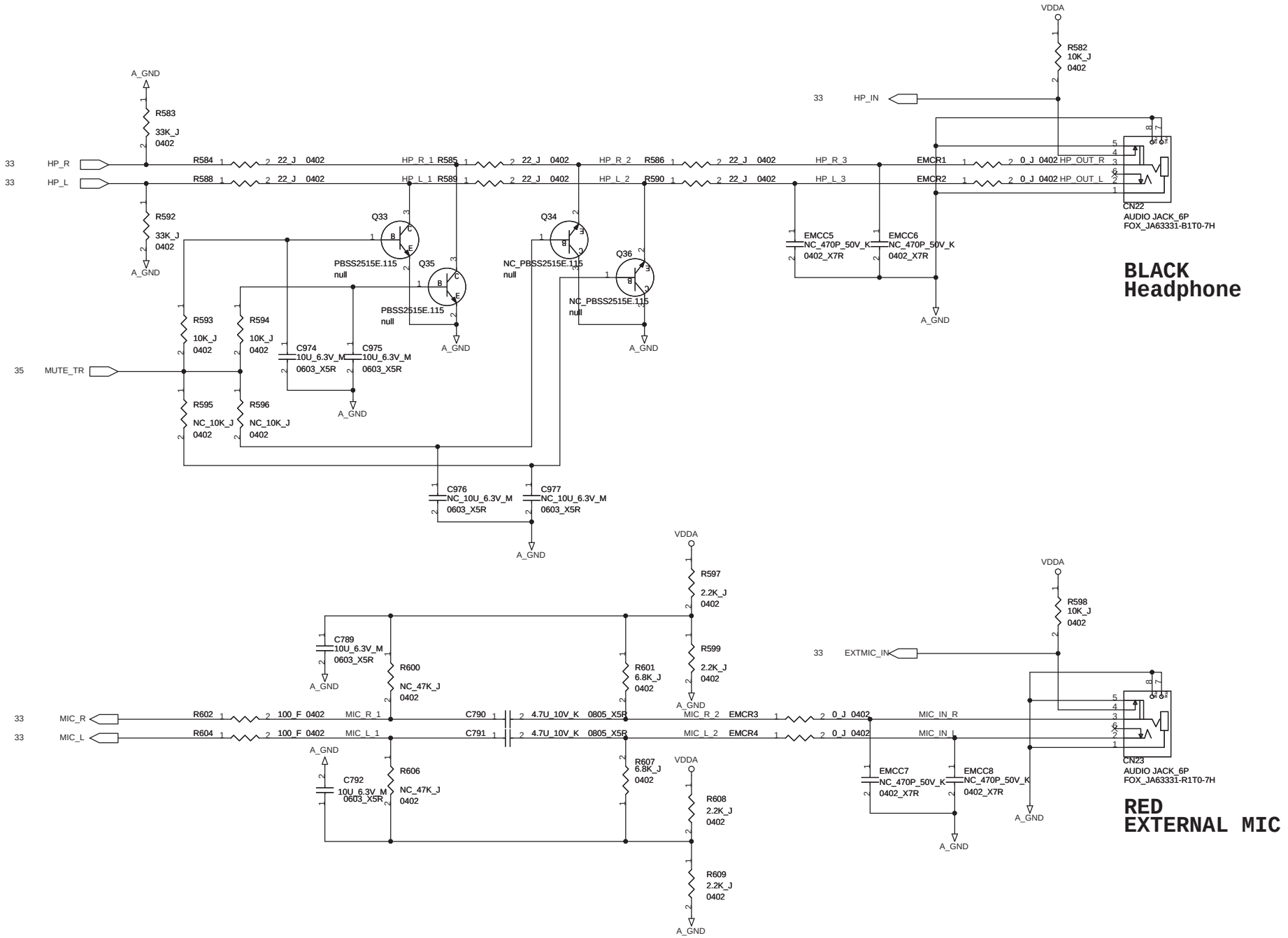
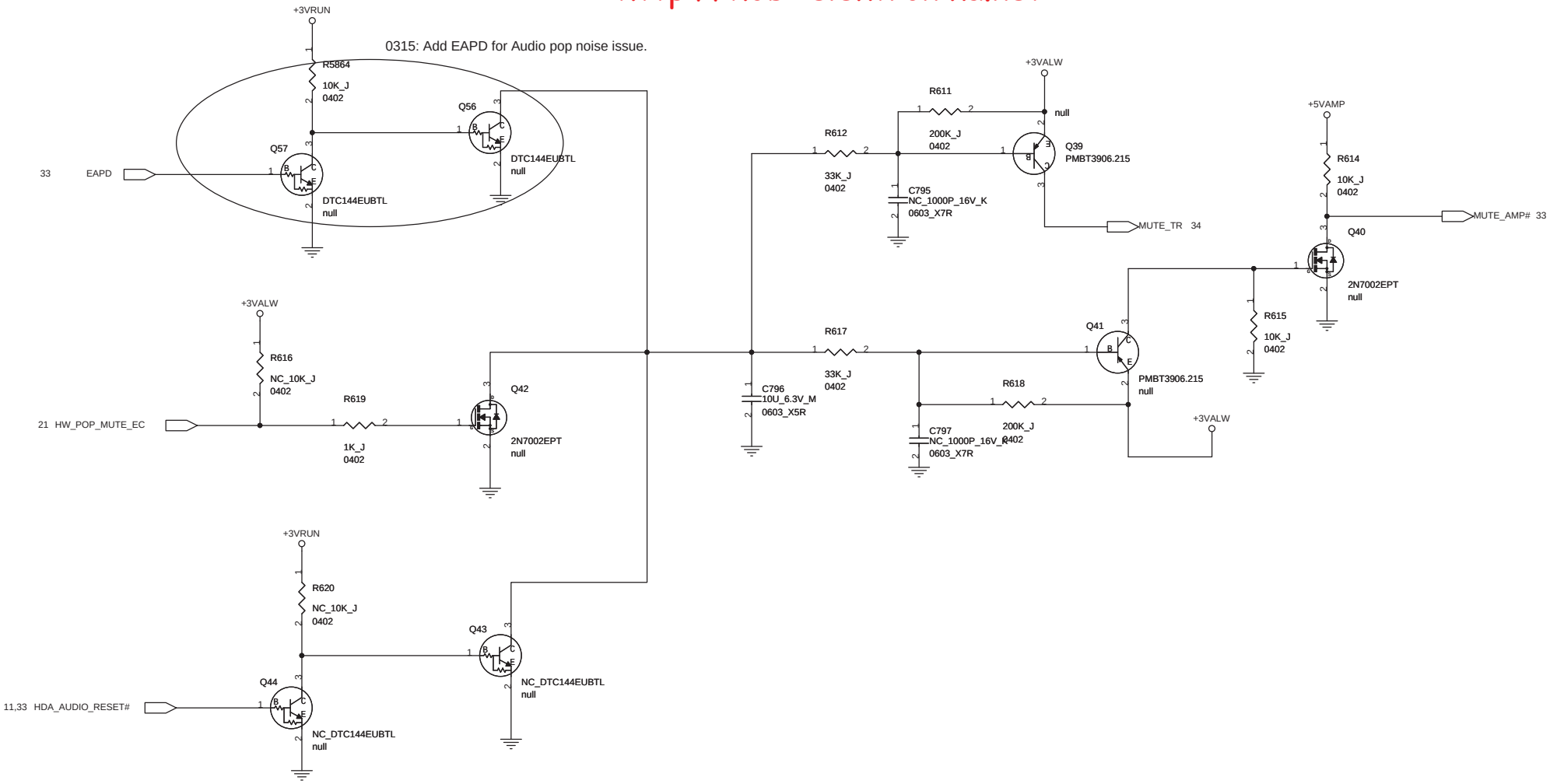
Date: Monday, May 17, 2010	Sheet 33 of 71

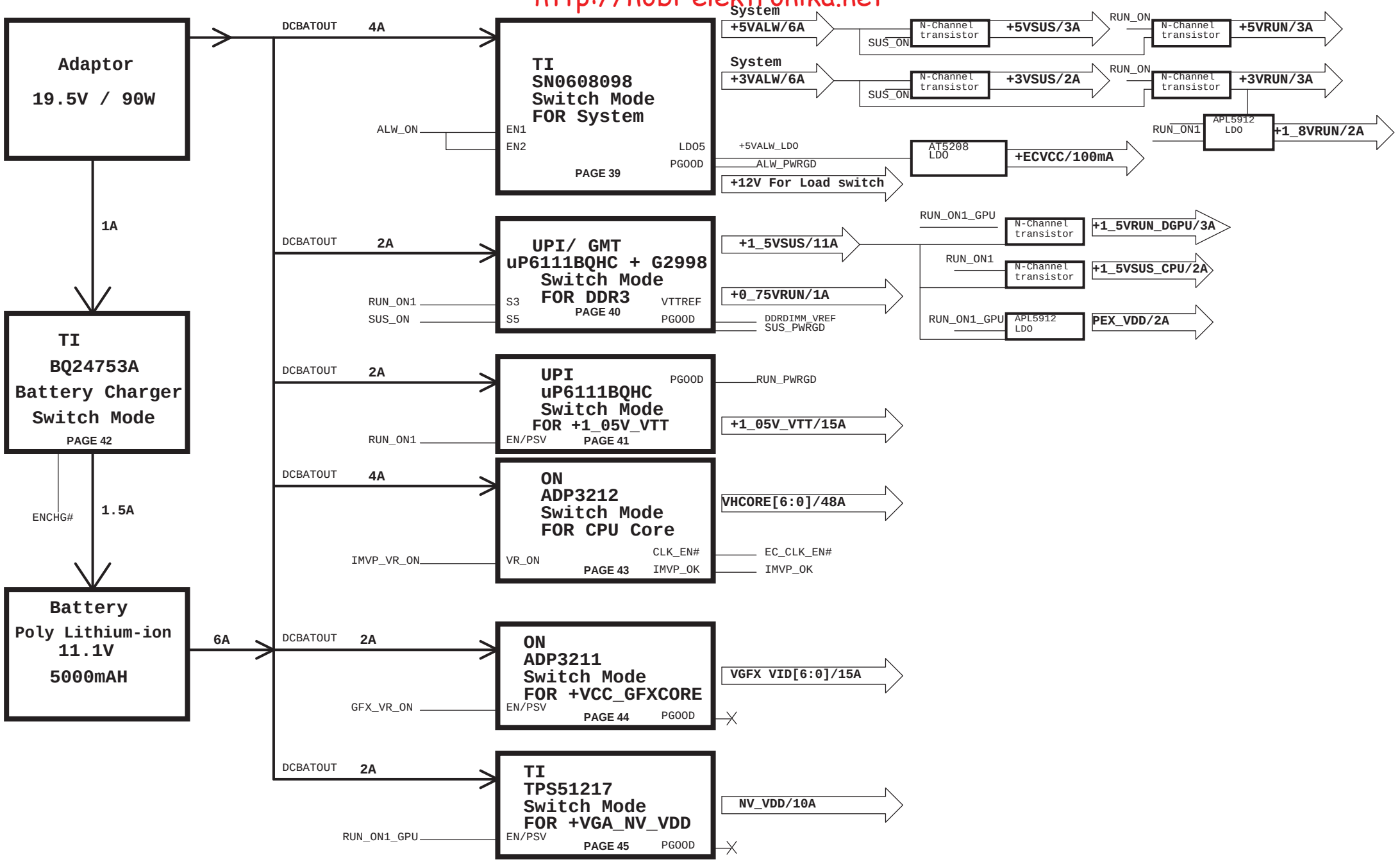


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HP,EXT MIC	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 34 of 71	

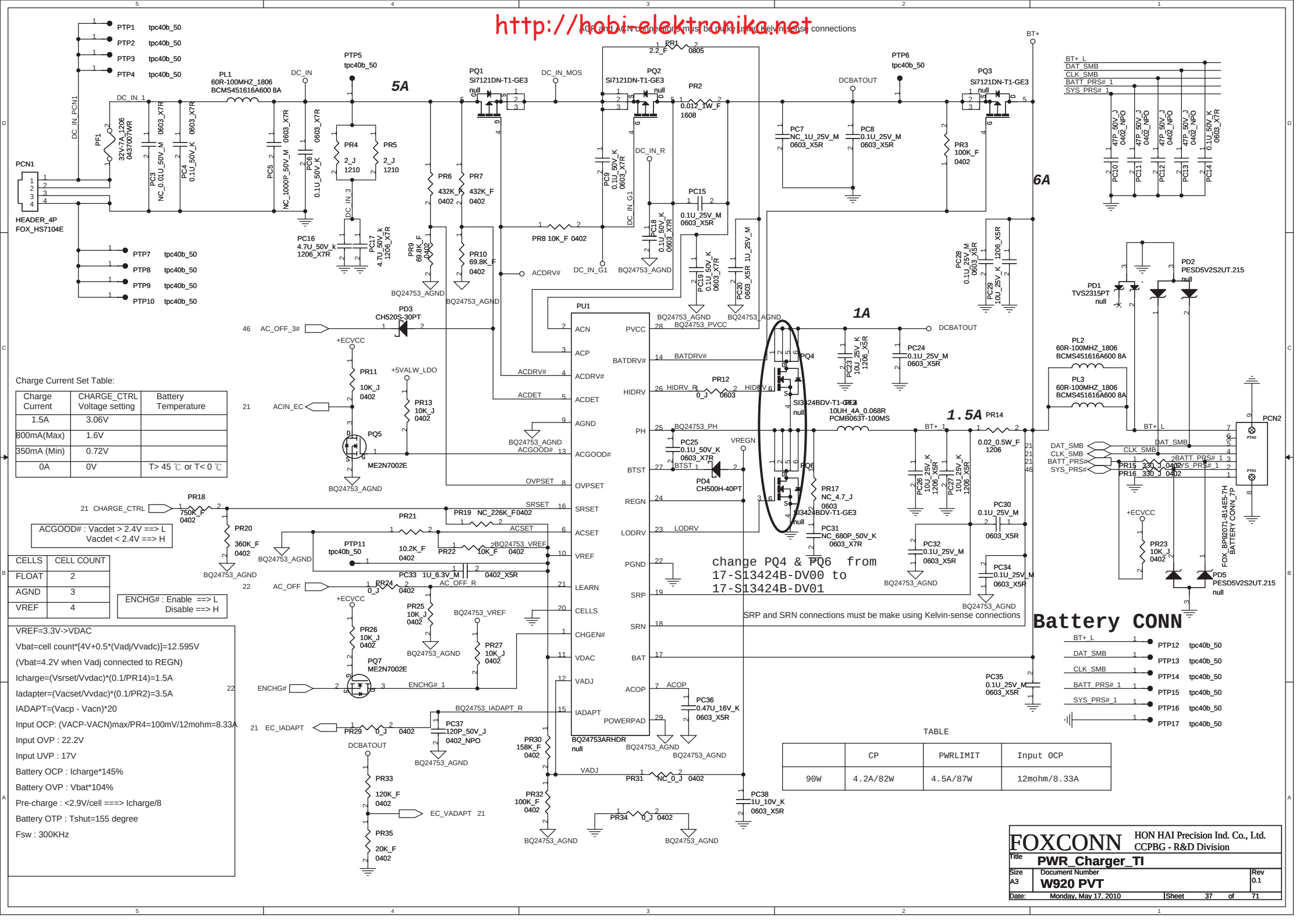
0315: Add EAPD for Audio pop noise issue.

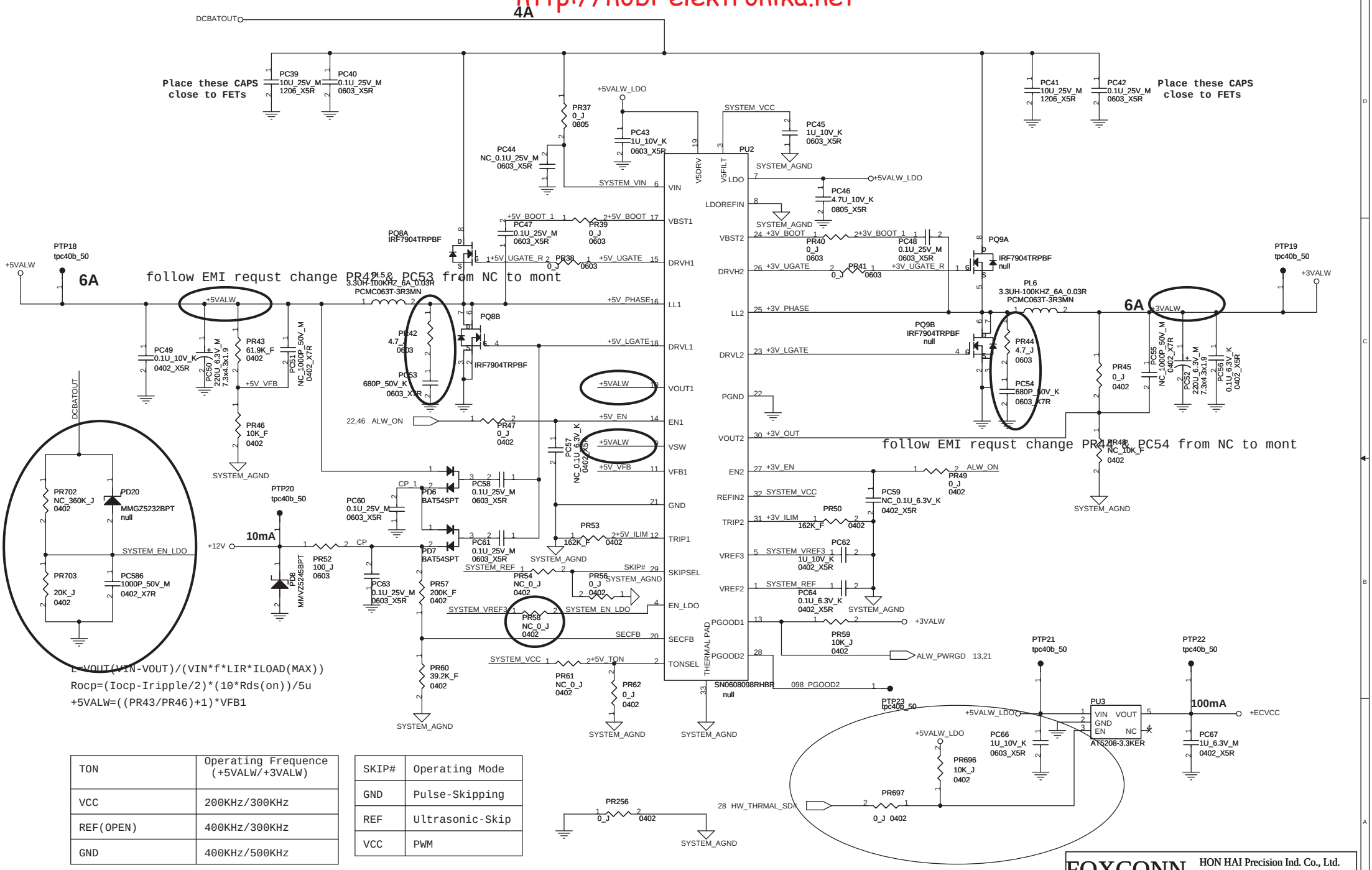


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	MUTE	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 35 of 71	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PWR_Power Design Diagram	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Wednesday, May 12, 2010	Sheet 36 of 71	





TON	Operating Frequence (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF(OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	PWR_+5V/+3V_TI
Size A3	Document Number W920 PVT
Rev	0.1
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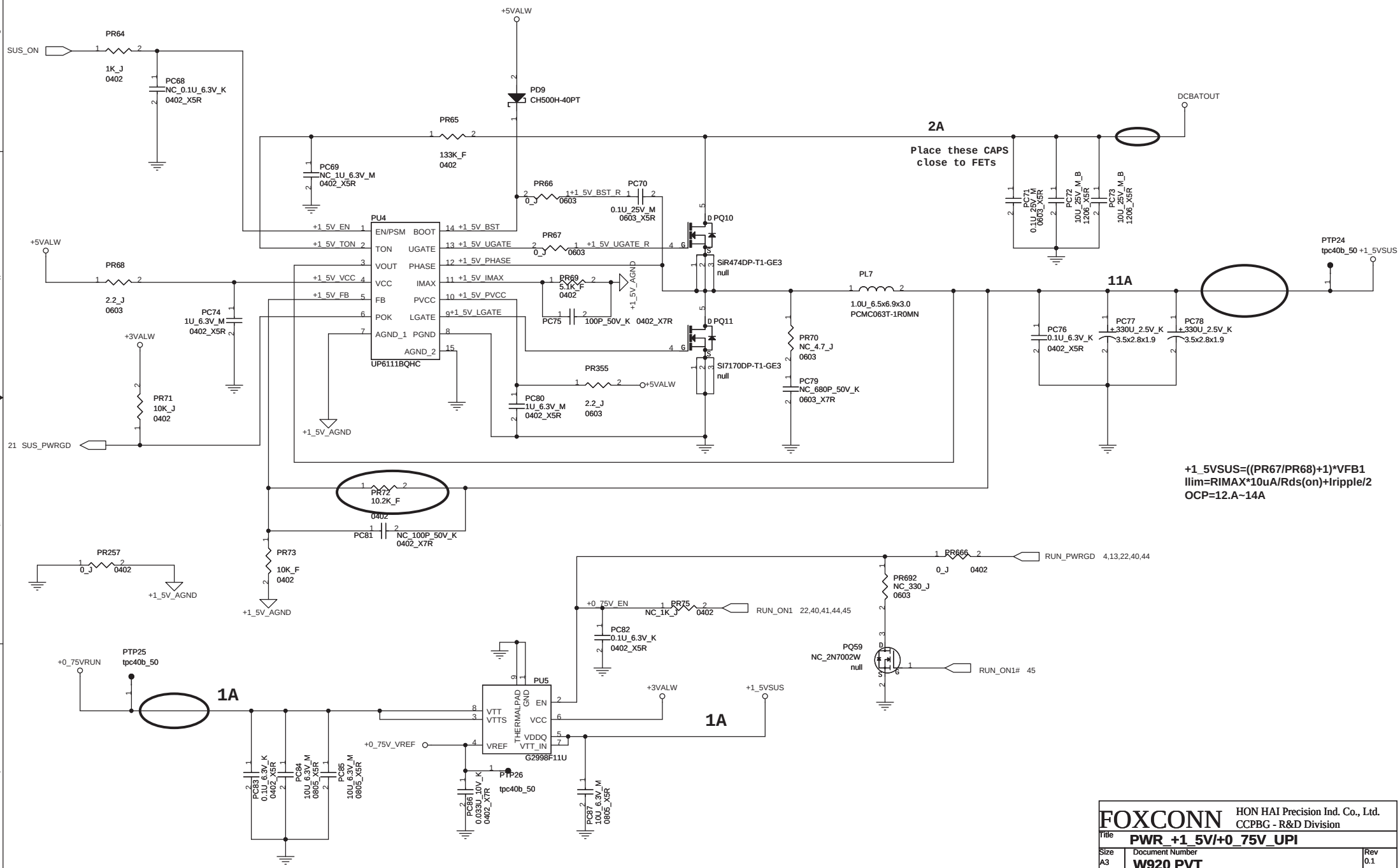
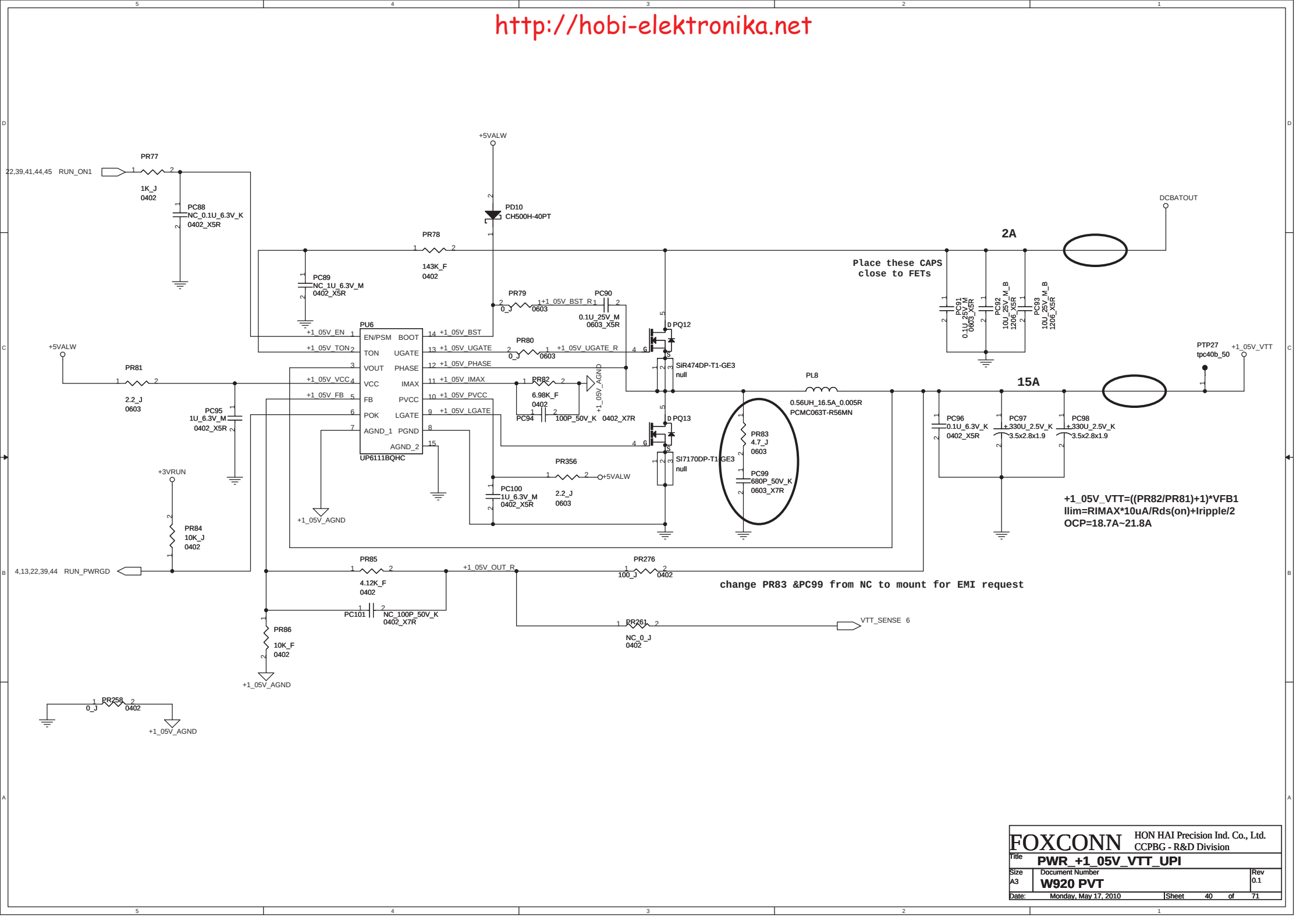
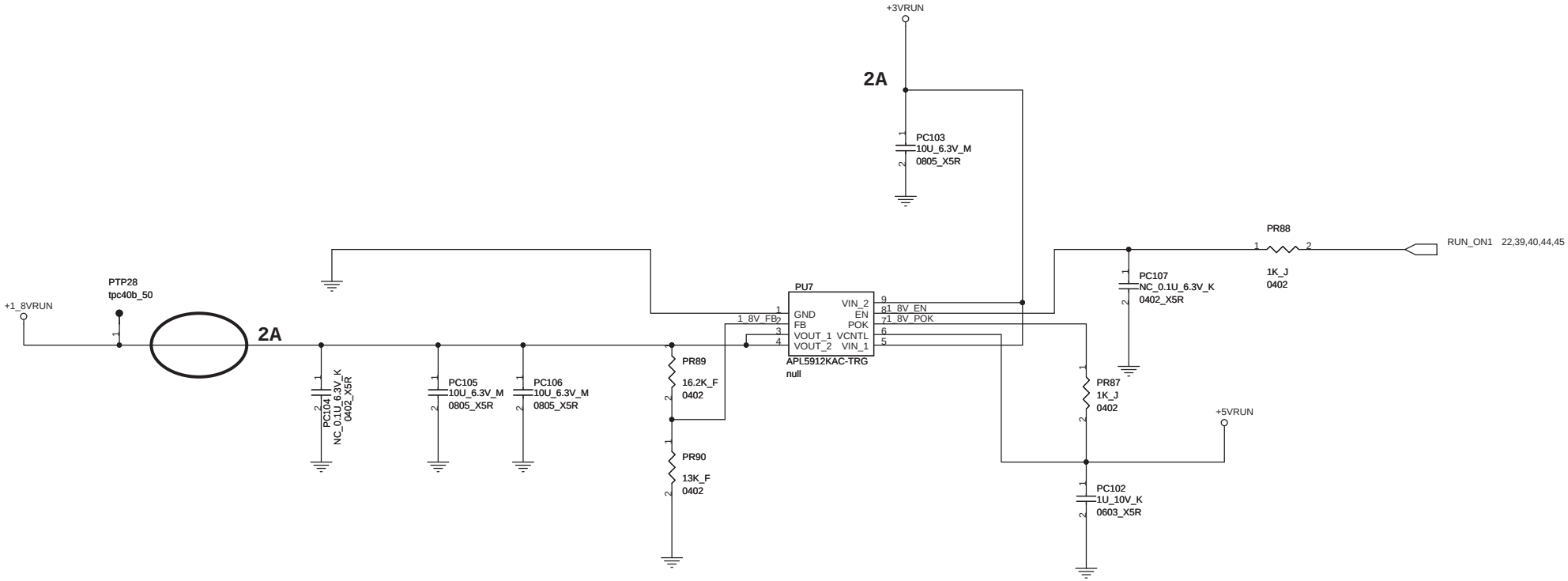


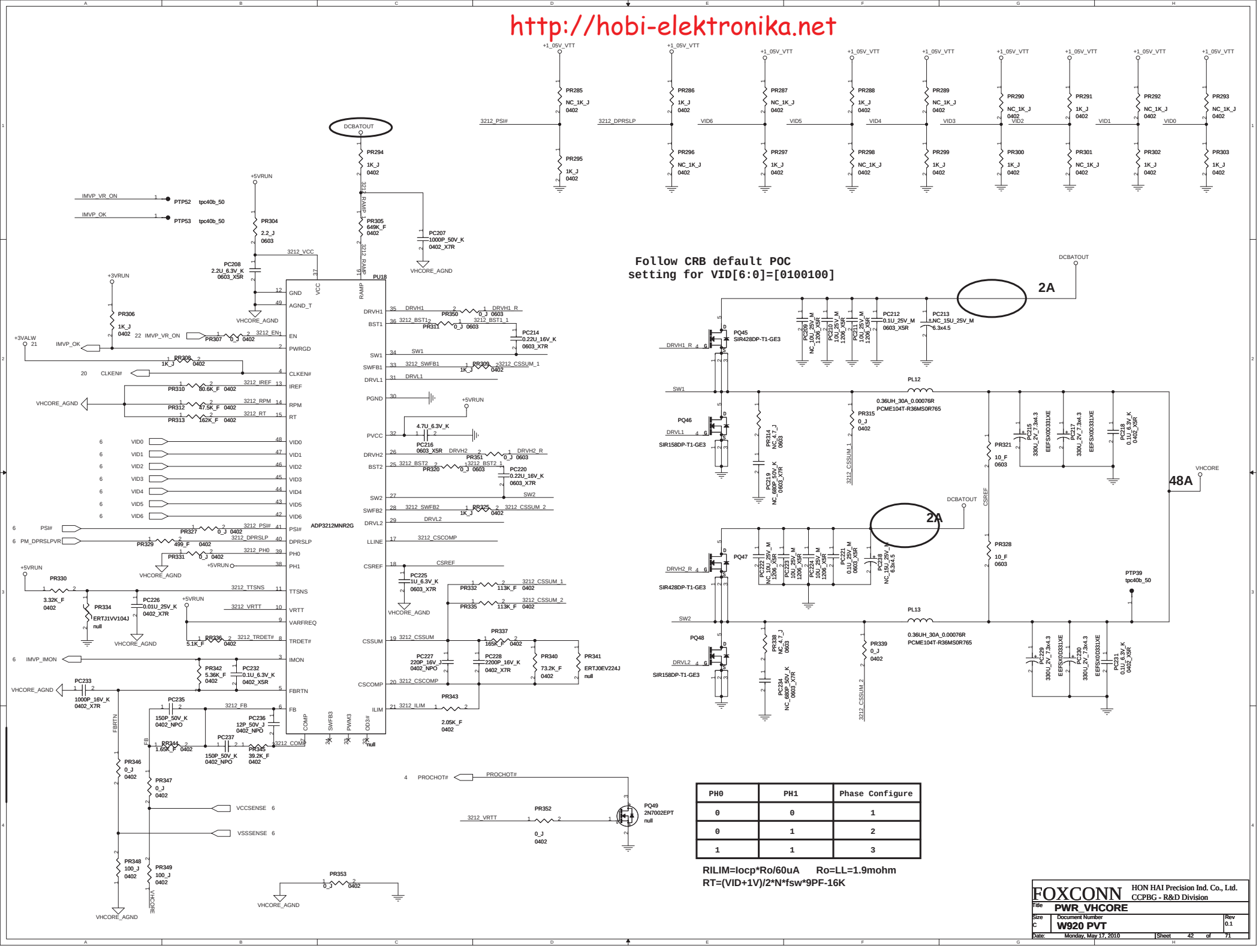
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PWR_+1_5V/+0_75V_UPI	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 39 of 71	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PWR_+1_05V_VTT_UPI	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 40 of 71	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PWR_1_8V_GMT	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 41 of 71	



PH0	PH1	Phase Configure
0	0	1
0	1	2
1	1	3

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	PWR_VHCORE
Size: C	Document Number: W920 PVT
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Date:	Monday, May 17, 2010
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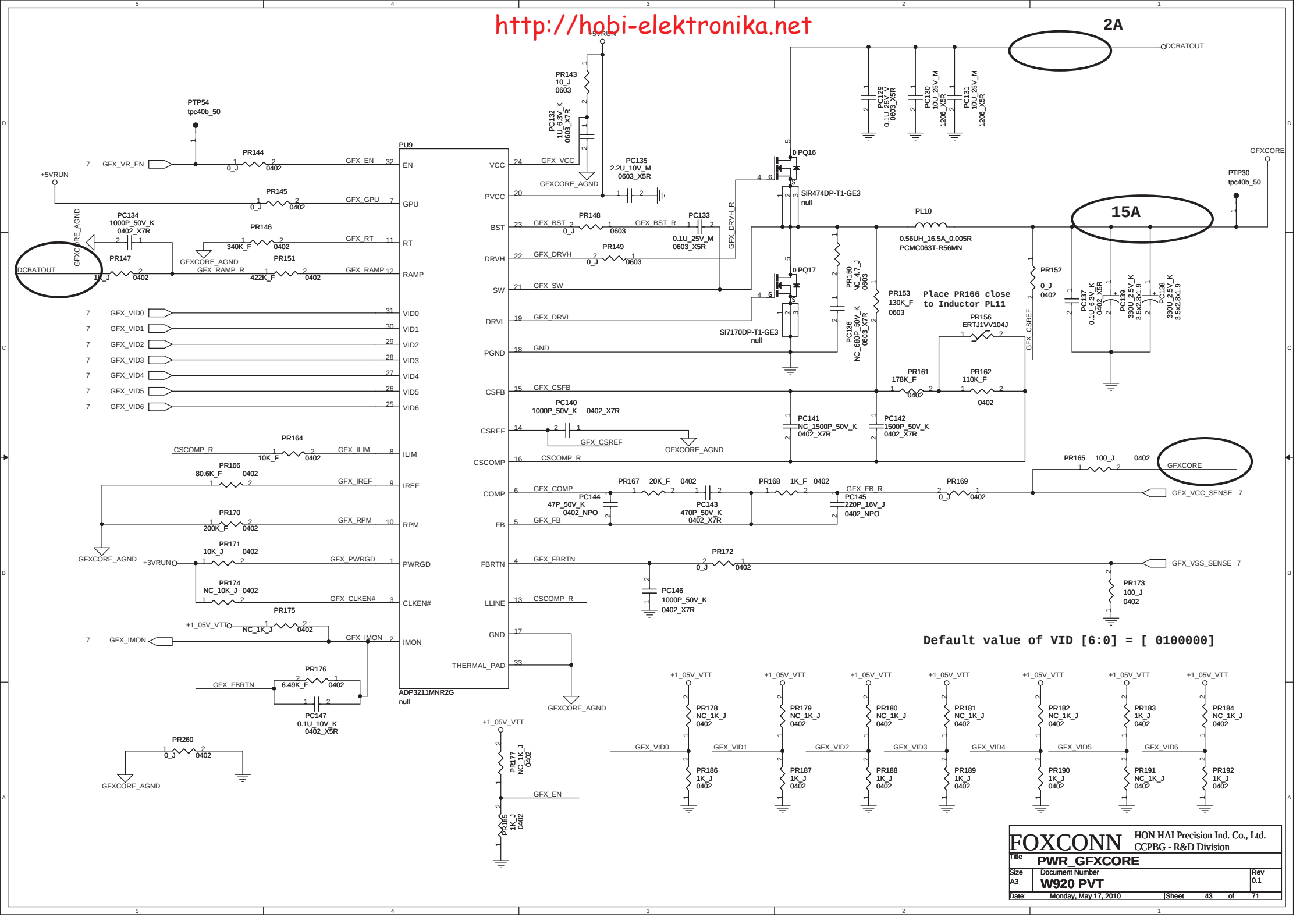
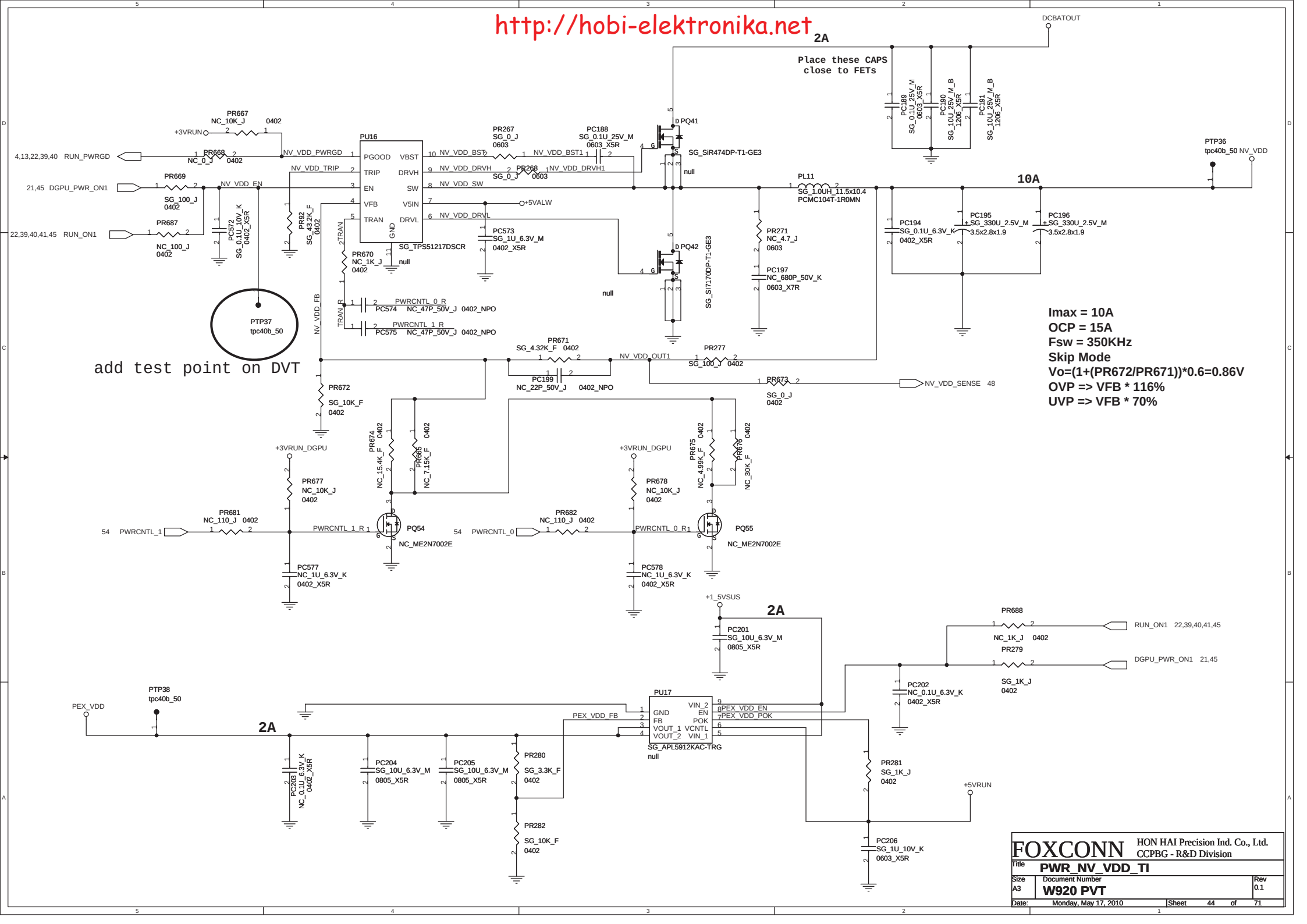
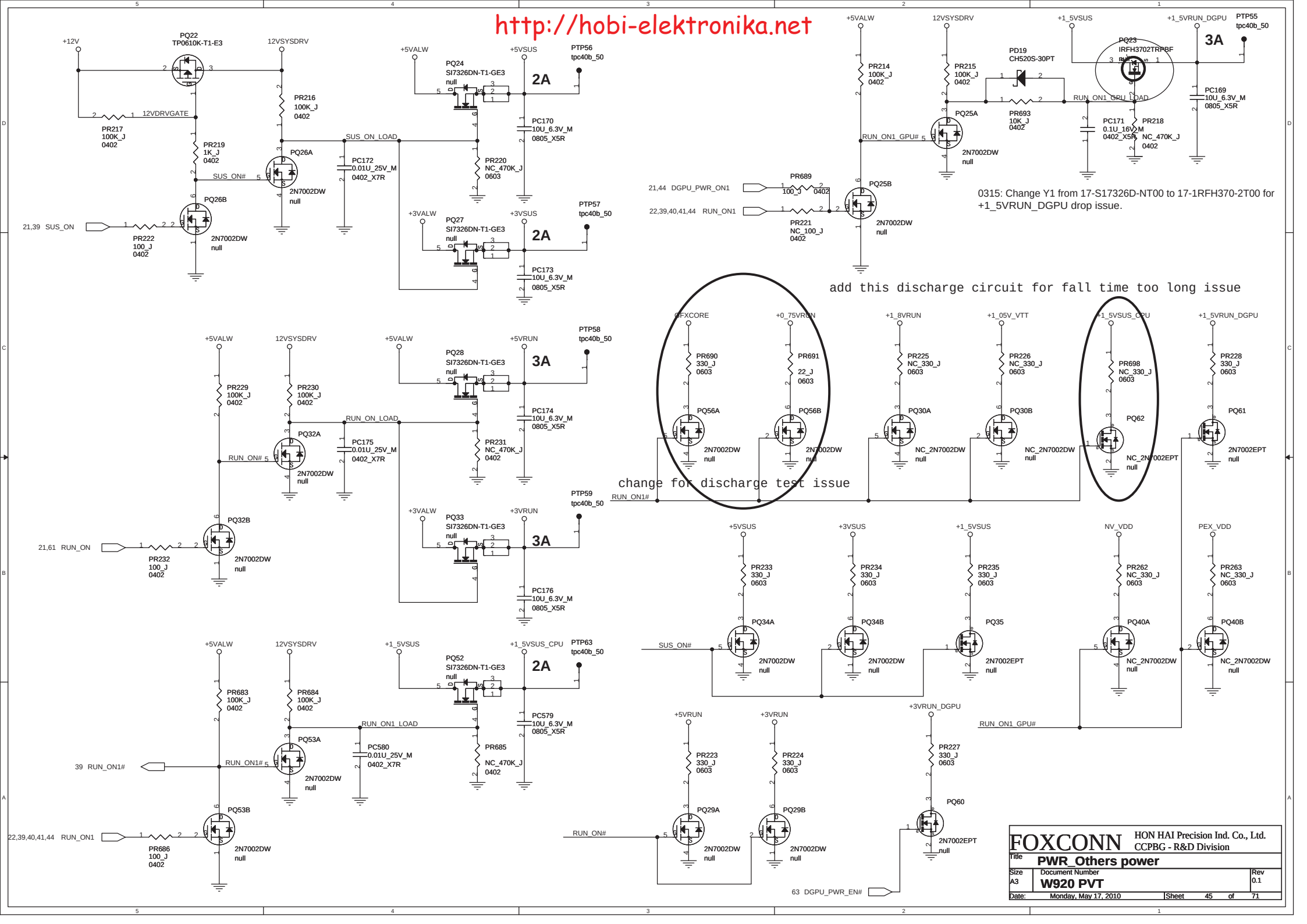
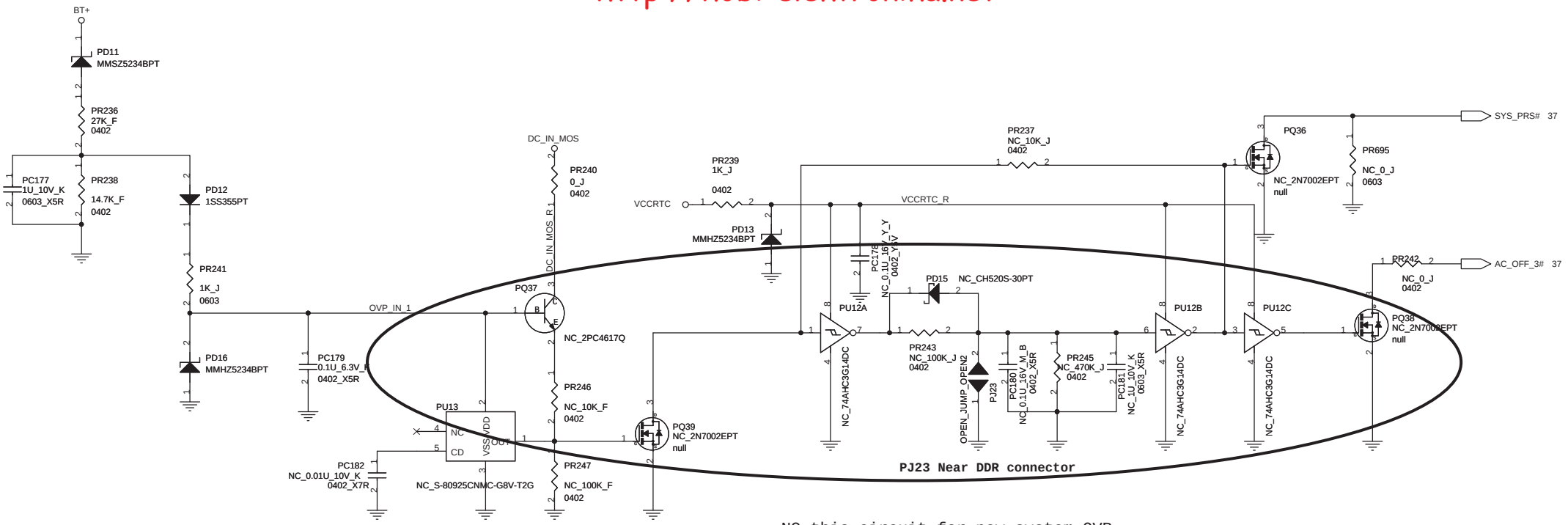




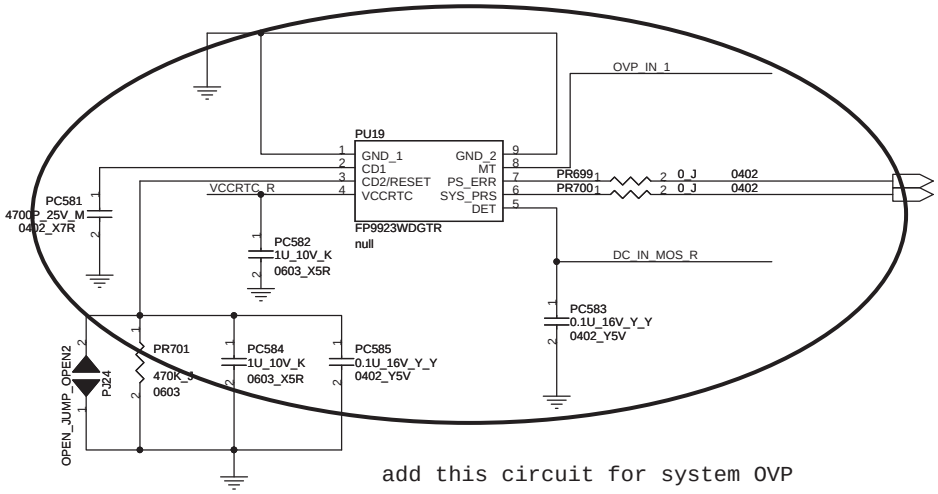
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PWR_NV_VDD_TI	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 44 of 71	



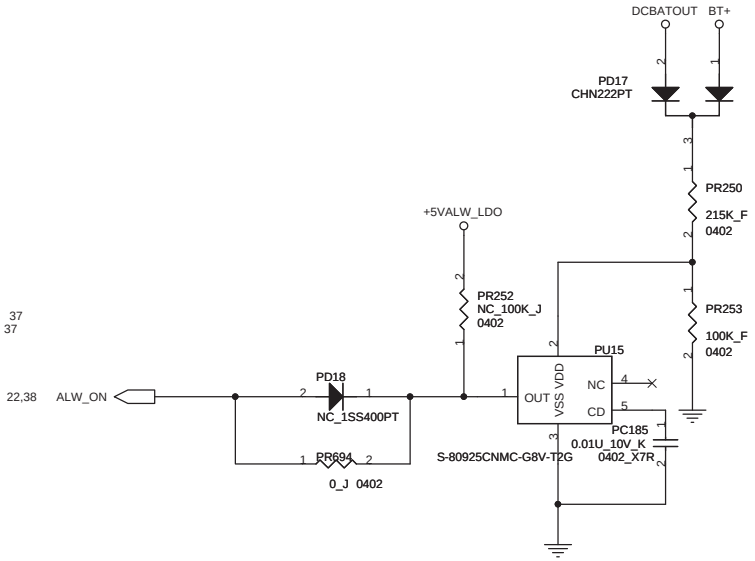
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PWR_Others power	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 45 of 71	



NC this circuit for new system OVP



add this circuit for system OVP



Battery UVP

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PWR_OVP function	
Size A3	Document Number W920 PVT	Rev 0.1
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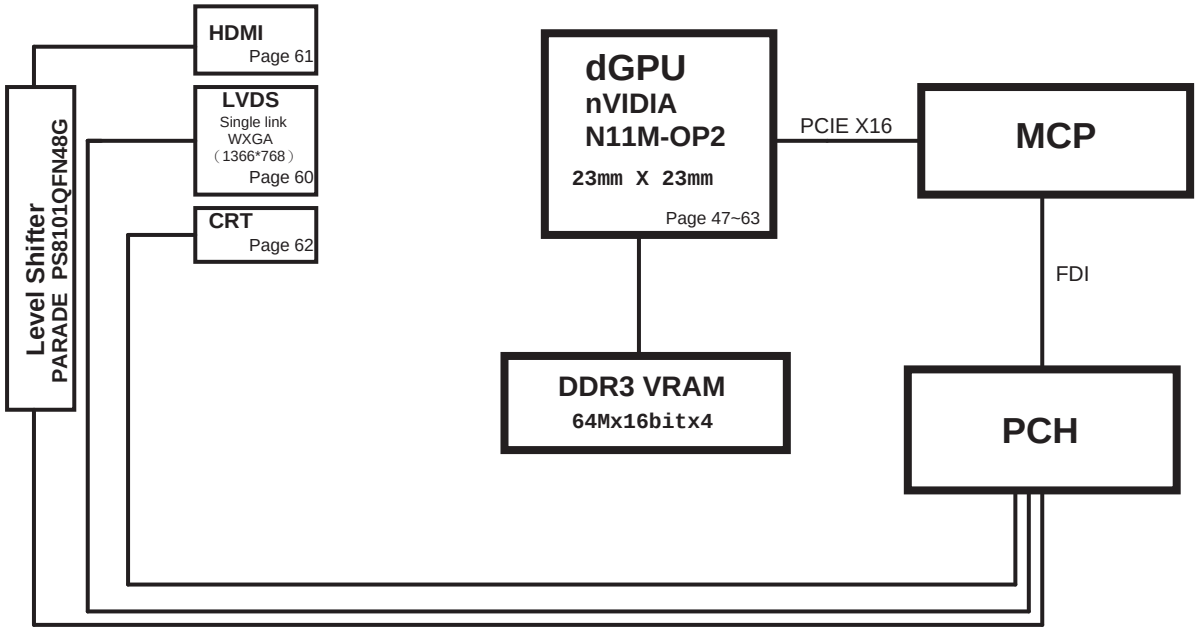
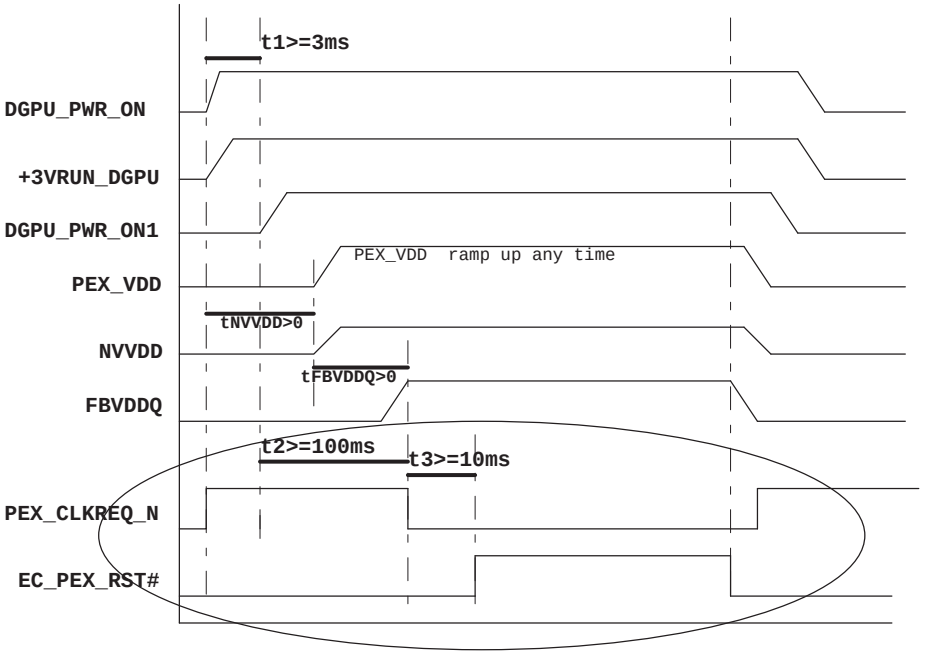
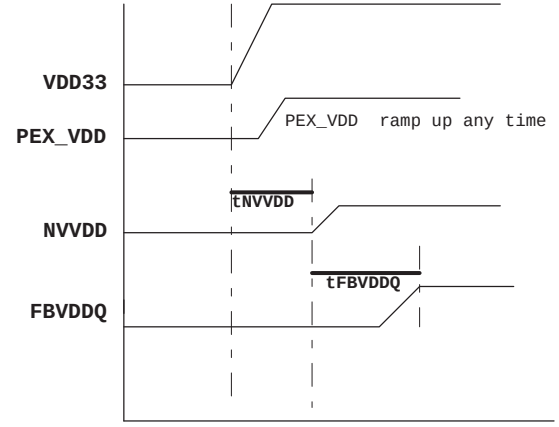
For SG SKU

For L SKU and SG SKU both





0404 Redefine the dGPU power timing



Recommended Power sequencing timing

note:
VDD33 =+3VRUN_DGPU
NVVDD=NV_VDD
FBVDDQ=FBVDD=+1_5VRUN_DGPU

tNVVDD>0
tFBVDDQ>0

The ramp time for any rail must be more than 40 us

At any time
NVVDD<=VDD33+0.5V
FBVDDQ<=VDD33+0.5V

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: VGA Block Diagram		
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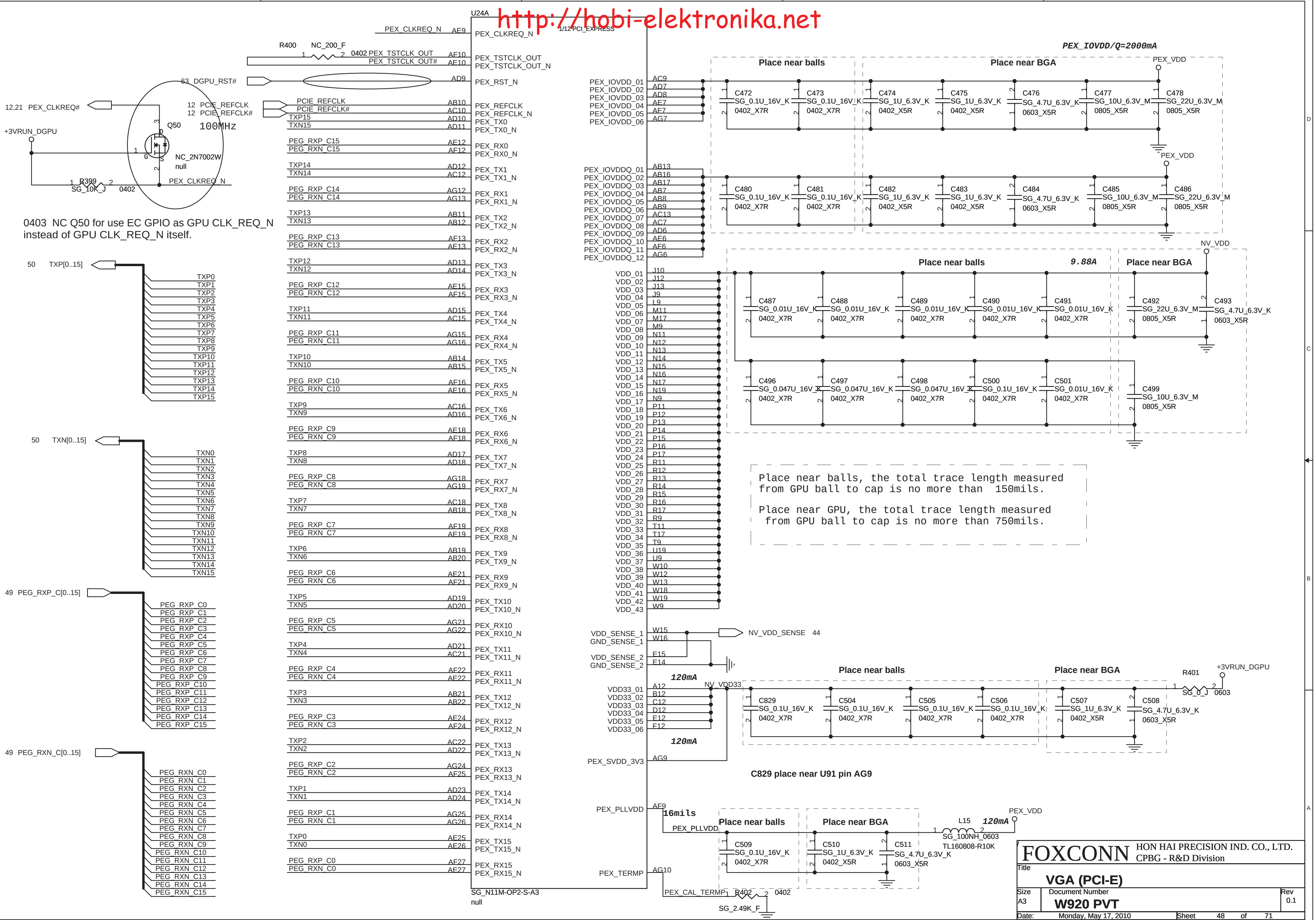

http://hobi-elektronika.net
U24A
1/12 PCI_EXPRESS
SG_N11M-OP2-S-A3
null
PEX_IOVDD/Q=2000mA
Place near balls
Place near BGA
PEX_VDD
NV_VDD
9.88A
0403 NC Q50 for use EC GPIO as GPU CLK_REQ_N
instead of GPU CLK_REQ_N itself.
Q50
NC_2N7002W
100MHz
R399
SG_10K_J
0402
R400
NC_200_F
+3VRUN_DGPU
PEX_CLKREQ#
DGPU_RST#
PCIE_REFCLK
PCIE_REFCLK#
TXP[0..15]
TXN[0..15]
PEG_RXP_C[0..15]
PEG_RXN_C[0..15]
Place near balls, the total trace length measured
from GPU ball to cap is no more than 150mils.
Place near GPU, the total trace length measured
from GPU ball to cap is no more than 750mils.
NV_VDD_SENSE 44
120mA
NV_VDD33
C829 place near U91 pin AG9
R401
SG_0_J
0603
16mils
PEX_PLLVDD
L15
SG_100NH_0603
TL160808-R10K
PEX_CAL_TERM
R402
SG_2.49K_F
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
VGA (PCI-E)
Size A3
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3 PEG_TXP[0..15]

PEG_TXP0
PEG_TXP1
PEG_TXP2
PEG_TXP3
PEG_TXP4
PEG_TXP5
PEG_TXP6
PEG_TXP7
PEG_TXP8
PEG_TXP9
PEG_TXP10
PEG_TXP11
PEG_TXP12
PEG_TXP13
PEG_TXP14
PEG_TXP15

3 PEG_TXN[0..15]

PEG_TXN0
PEG_TXN1
PEG_TXN2
PEG_TXN3
PEG_TXN4
PEG_TXN5
PEG_TXN6
PEG_TXN7
PEG_TXN8
PEG_TXN9
PEG_TXN10
PEG_TXN11
PEG_TXN12
PEG_TXN13
PEG_TXN14
PEG_TXN15

PEG_TXP0	2	C512	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C0
PEG_TXN0	2	C513	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C0
PEG_TXP1	2	C514	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C1
PEG_TXN1	2	C515	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C1
PEG_TXP2	2	C516	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C2
PEG_TXN2	2	C517	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C2
PEG_TXP3	2	C518	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C3
PEG_TXN3	2	C519	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C3
PEG_TXP4	2	C520	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C4
PEG_TXN4	2	C521	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C4
PEG_TXP5	2	C522	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C5
PEG_TXN5	2	C523	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C5
PEG_TXP6	2	C524	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C6
PEG_TXN6	2	C525	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C6
PEG_TXP7	2	C526	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C7
PEG_TXN7	2	C527	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C7
PEG_TXP8	2	C528	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C8
PEG_TXN8	2	C529	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C8
PEG_TXP9	2	C530	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C9
PEG_TXN9	2	C531	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C9
PEG_TXP10	2	C532	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C10
PEG_TXN10	2	C533	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C10
PEG_TXP11	2	C534	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C11
PEG_TXN11	2	C535	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C11
PEG_TXP12	2	C536	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C12
PEG_TXN12	2	C537	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C12
PEG_TXP13	2	C538	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C13
PEG_TXN13	2	C539	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C13
PEG_TXP14	2	C540	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C14
PEG_TXN14	2	C541	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C14
PEG_TXP15	2	C542	0402_X7R	1	SG_0.1U_16V_K	PEG_RXP_C15
PEG_TXN15	2	C543	0402_X7R	1	SG_0.1U_16V_K	PEG_RXN_C15

close to MCP

PEG_RXP_C[0..15] 48

PEG_RXP_C0
PEG_RXP_C1
PEG_RXP_C2
PEG_RXP_C3
PEG_RXP_C4
PEG_RXP_C5
PEG_RXP_C6
PEG_RXP_C7
PEG_RXP_C8
PEG_RXP_C9
PEG_RXP_C10
PEG_RXP_C11
PEG_RXP_C12
PEG_RXP_C13
PEG_RXP_C14
PEG_RXP_C15

PEG_RXN_C[0..15] 48

PEG_RXN_C0
PEG_RXN_C1
PEG_RXN_C2
PEG_RXN_C3
PEG_RXN_C4
PEG_RXN_C5
PEG_RXN_C6
PEG_RXN_C7
PEG_RXN_C8
PEG_RXN_C9
PEG_RXN_C10
PEG_RXN_C11
PEG_RXN_C12
PEG_RXN_C13
PEG_RXN_C14
PEG_RXN_C15

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (PCI-E TX)

Size: A3 | Document Number: W920 PVT | Rev: 0.1

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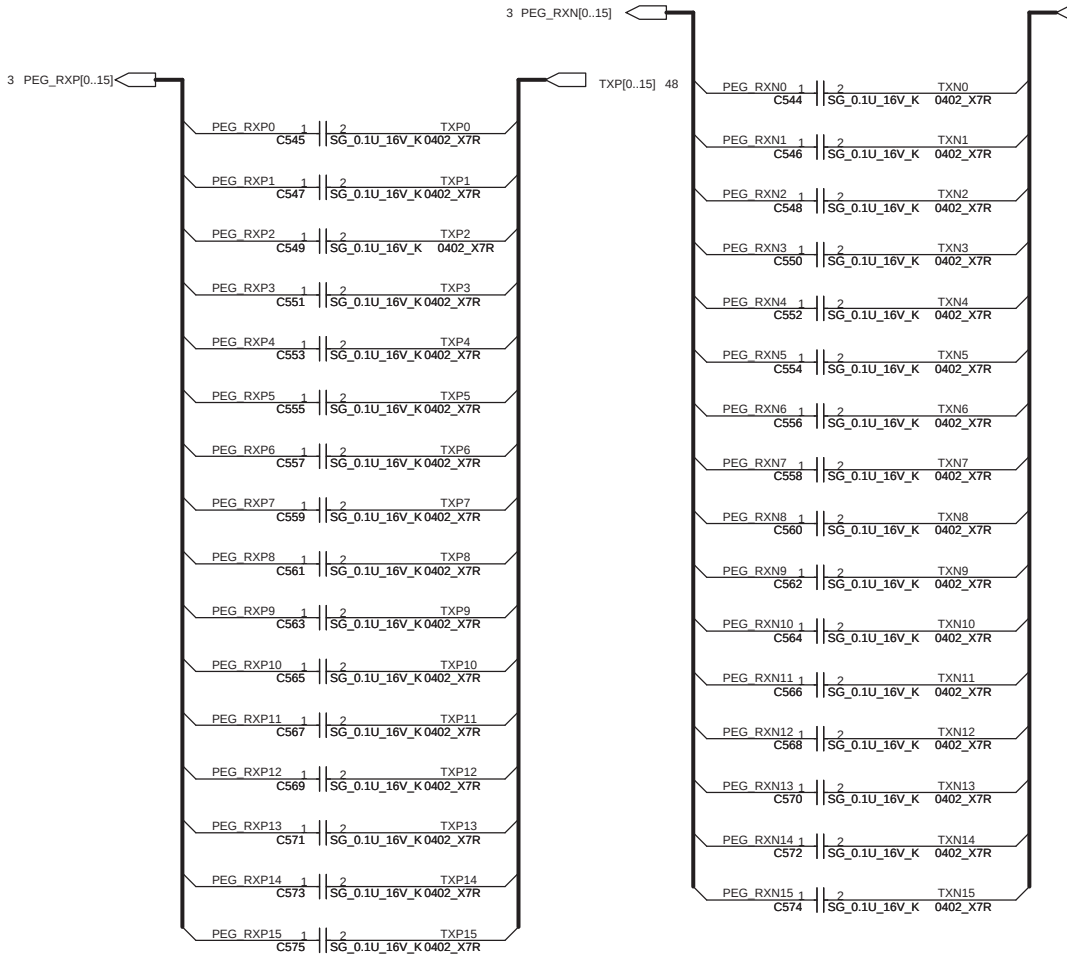


XCLK_417 : 0
1 (Reserved) 0 (277M Hz Default)
FB_0_BAR_SIZE 0 256MB(Default)
SMB_ALT_ADDR: 0(0X9E)
VGA_DEVICE: 1(VGA Device)

ROM_SO (0001)

PCI_DEVID[4]: 1
SUB_VENDOR: 0

ROM_SCLK (1010)

0 (No vedio BIOS ROM)
1 (BIOS ROM is present)

SLOT_CLK_CFG: 1

0 (GPU and MCH not share a common reference clk)
1 (GPU and MCH share a common reference clk)

PEX_PLL_EN_TERM: 0

0 Disable(Default)
1 Enable

Panel strap
USER[3:0]: EDID is used 1111

STRAP0 (1111)

PCI Express strap
N113GIO_PADCFG[3:0]
1110 (NOTEBOOK)

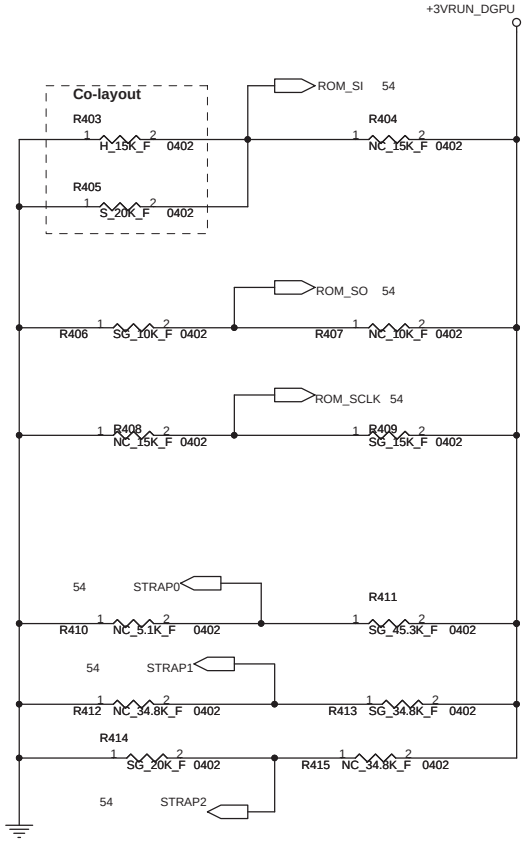
STRAP1 (1110)

N11X PCI_DEVID[3:0]:PUN
N11M-OP2 0X0A73

STRAP2 (0011)

ROM_SI

0010 64Mx16 DDR3 - 96 ball - monolithic 64-bit Hynix
0011 64Mx16 DDR3 - 96 ball - monolithic 64-bit Samsung



close to GPU

Logical Strap bit Mapping

Resister values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

Strap Options

Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SO	+3VRUN	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

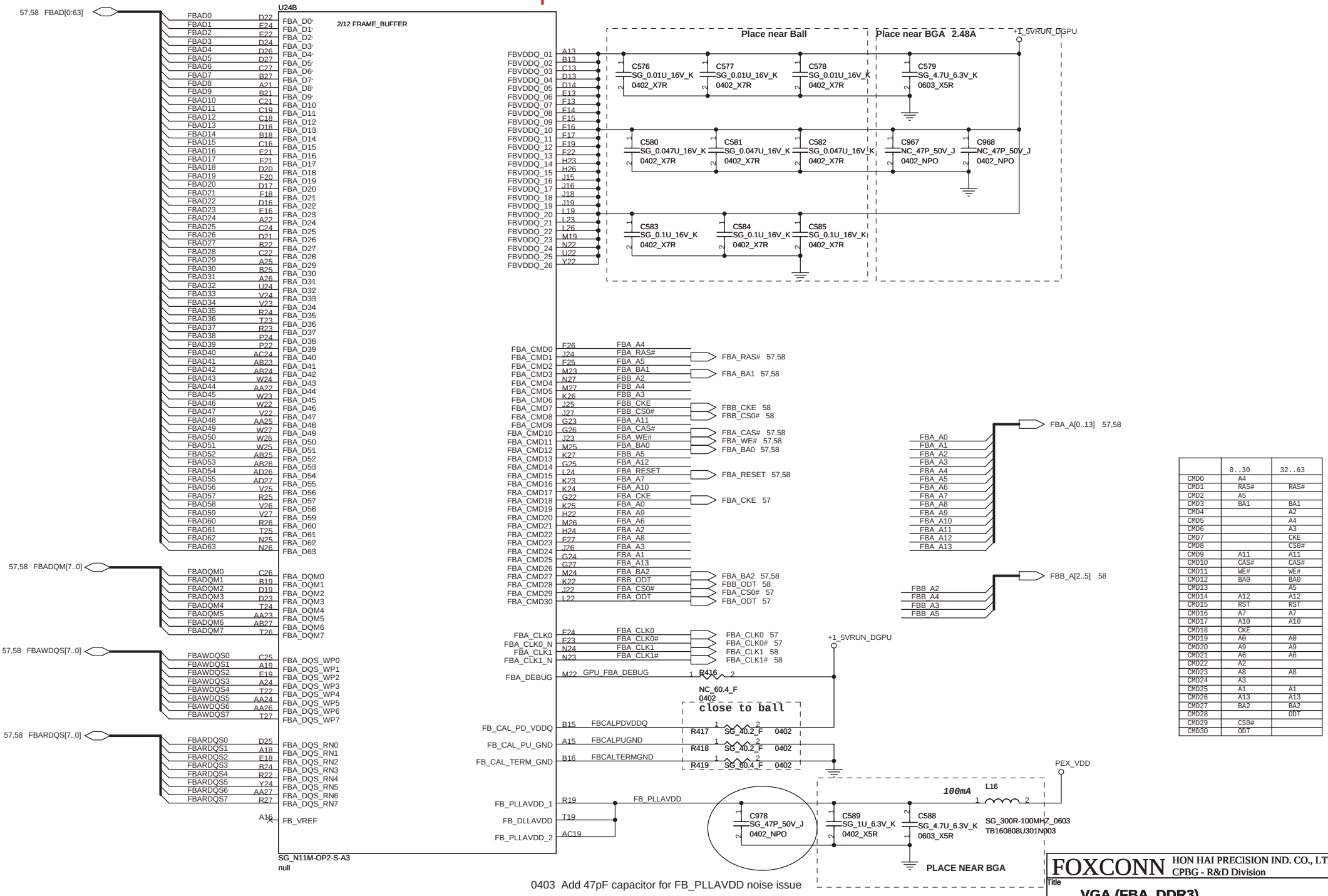
Refer to <GB1 Family Design Guide DG-04642-001_v01_secured>

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **VGA (PCIE RX&STRAP)**

Size: A3 | Document Number: **W920 PVT** | Rev: 0.1

Date: Monday, May 17, 2010 | Sheet 50 of 71



	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	

0403 Add 47pF capacitor for FB_PLLAVDD noise issue

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (FBA_DDR3)

Size: A3 | Document Number: W920 PVT | Rev: 0.1

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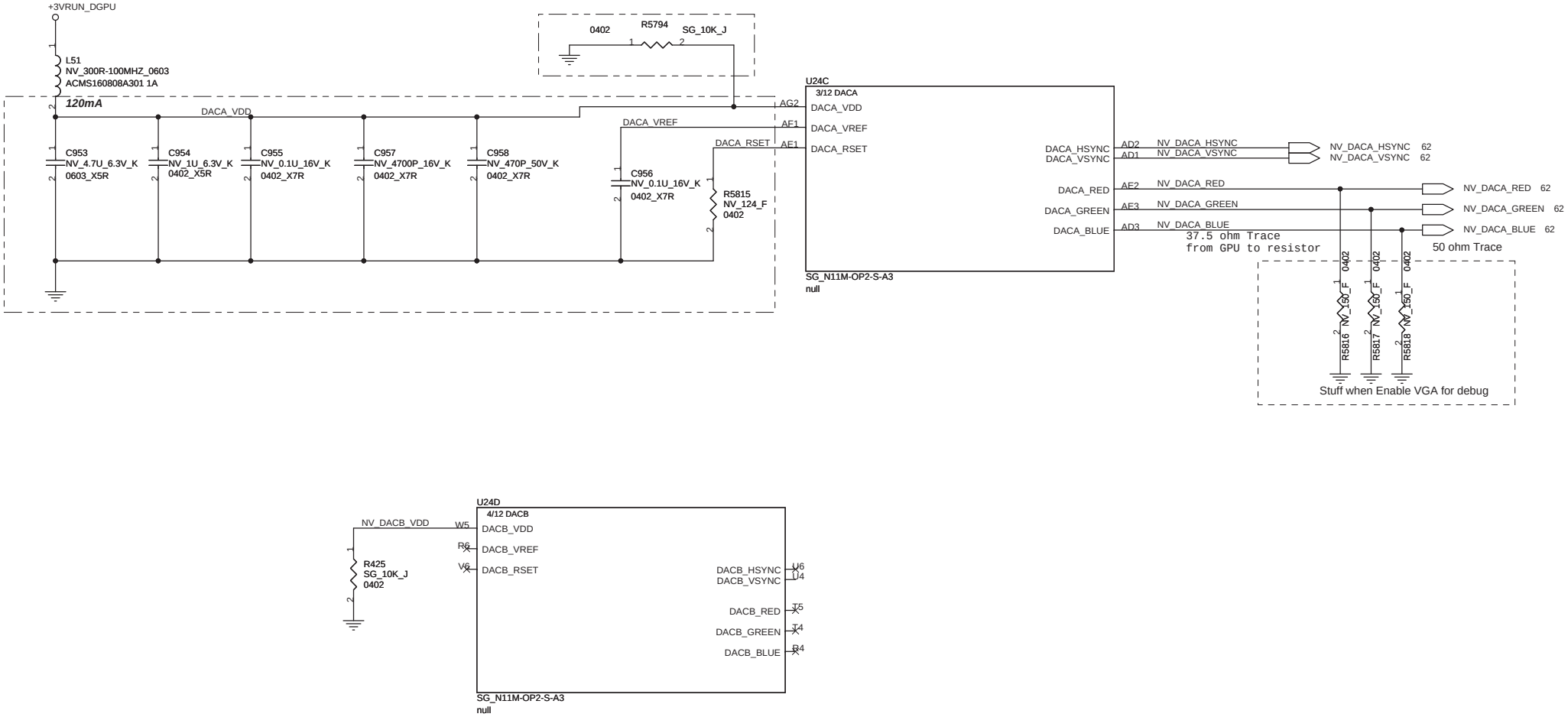
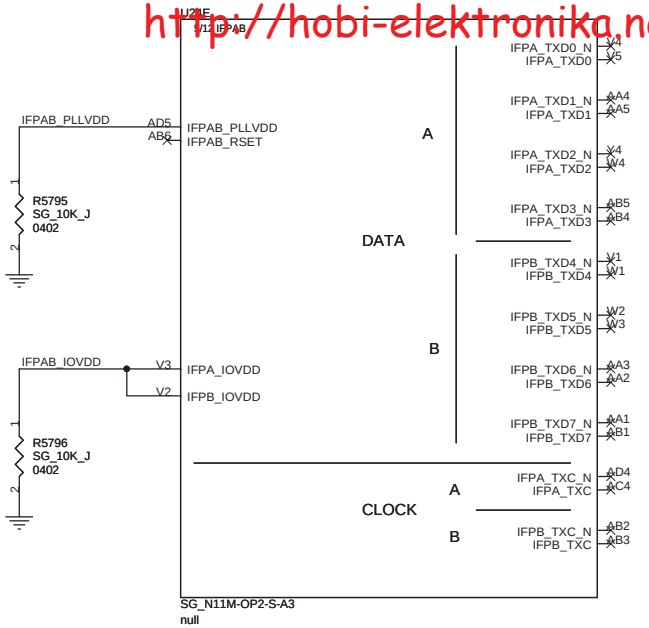
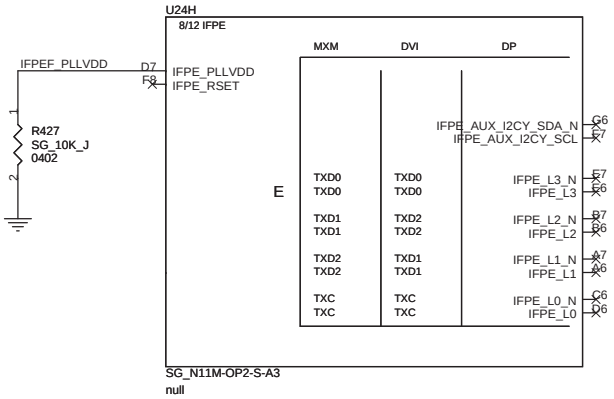
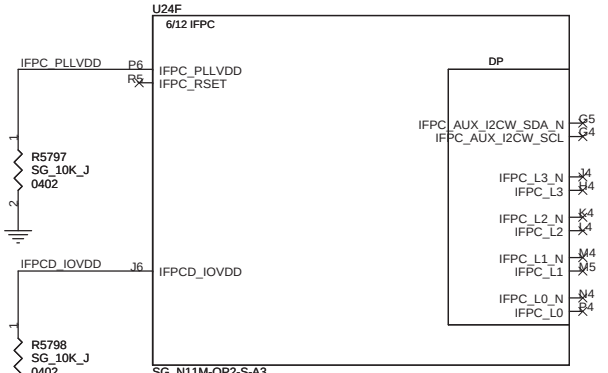
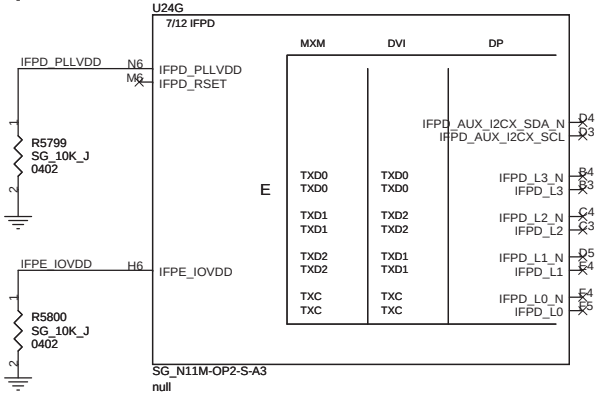


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: VGA (DACAB)		
Size: A3	Document Number: W920 PVT	Rev: 0.1
Date: Monday, May 17, 2010	Sheet 52 of 71	

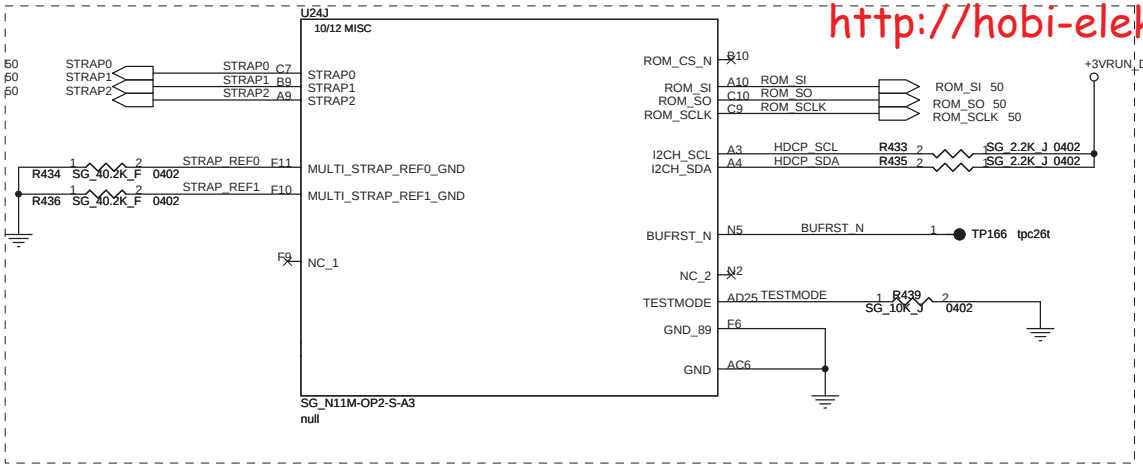


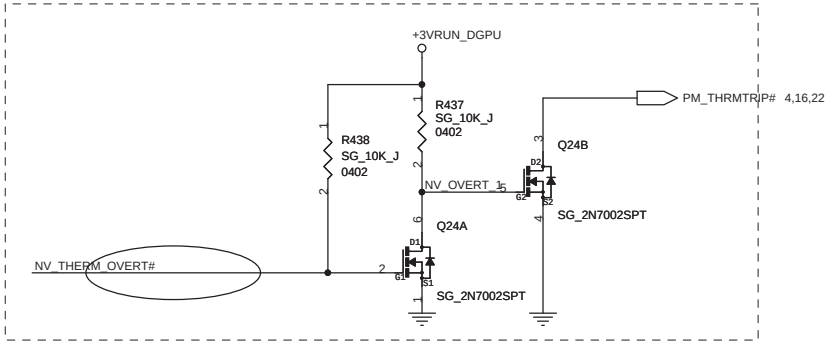


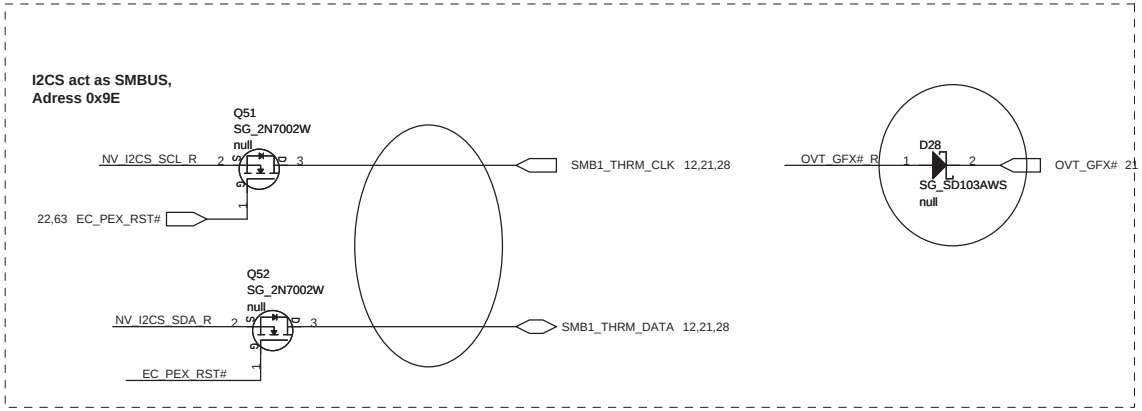


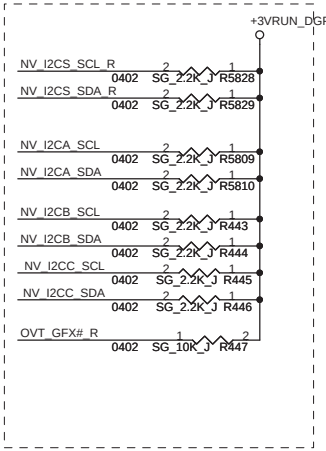


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA (IFP_ABCDEF)	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Wednesday, May 12, 2010	Sheet 53 of 71	



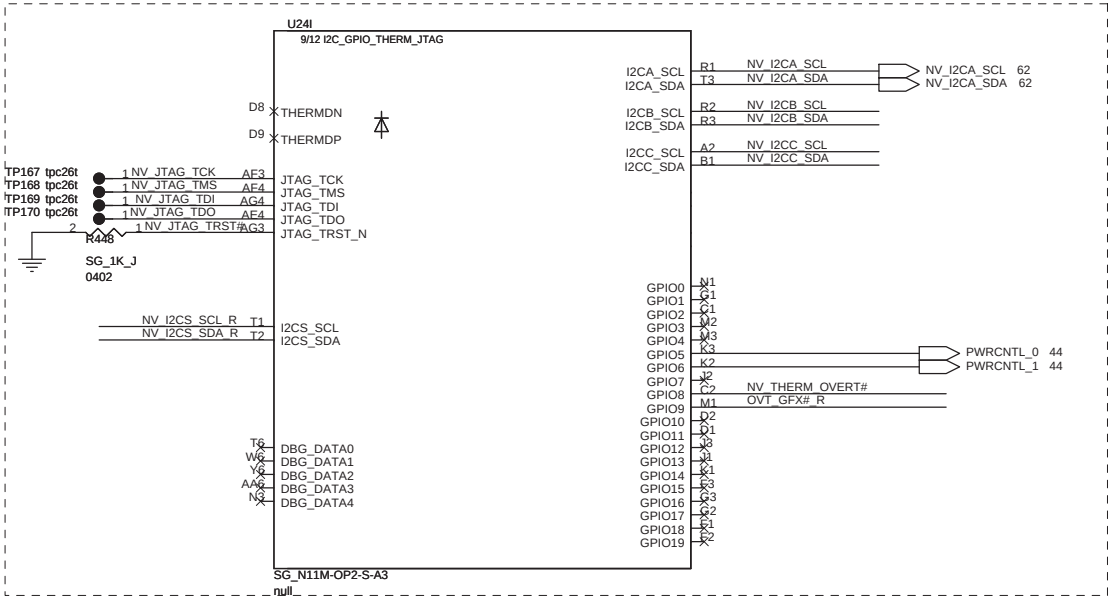


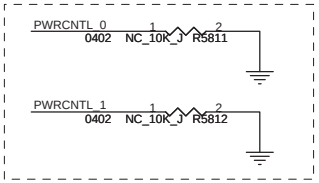




SIGNAL	Application	Type	USED
I2CA_SCL I2CA_SDA	DAC A CRT display interface DDC	Master	NO
I2CB_SCL I2CB_SDA	None use		NO
I2CC_SCL I2CC_SDA	None use		NO
I2CS_SCL I2CS_SDA	SMBUS for internal thermal sensor interface	Slave Add:0X9E	YES
I2CH_SCL I2CH_SDA	None use		NO
I2CW_SCL I2CW_SDA	AUX/DDC		NO
I2CX_SCL I2CX_SDA	AUX/DDC		NO
I2CY_SCL I2CY_SDA	AUX/DDC		NO
I2CZ_SCL I2CZ_SDA	AUX/DDC		NO

GPIO	I/O	Internal pull	External pull	GPIO FUNCTION	Active	USED
GPIO0	n/a			gerneral purpose	n/a	NO
GPIO1	I			HDMI_DET	-	NO
GPIO2	O		PD	LCD0_BL_PWM	HIGH	NO
GPIO3	O		PD	LCD0_VDD	HIGH	NO
GPIO4	O		PD	LCD0_BL_EN	HIGH	NO
GPIO5	O		PD	GPU_VID0	-	NO
GPIO6	O		PD	GPU_VID1	-	NO
GPIO7	O			GPU_VID2	-	NO
GPIO8	O		PU	NV_THERM_OVERT#	LOW	YES
GPIO9	I		PU	NV_THERM_ALERT#	LOW	YES
GPIO10	O				-	NO
External pull-ups and pull-downs, when needed,must be 5-10Kohm						



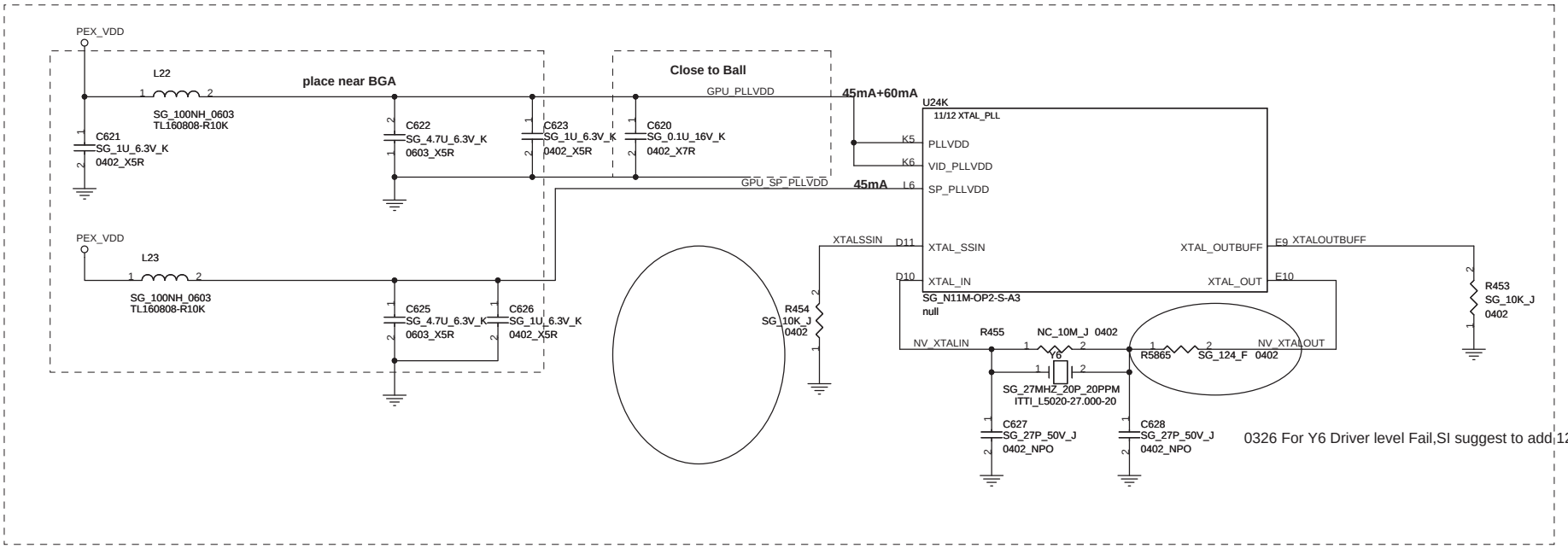


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (GPIO)

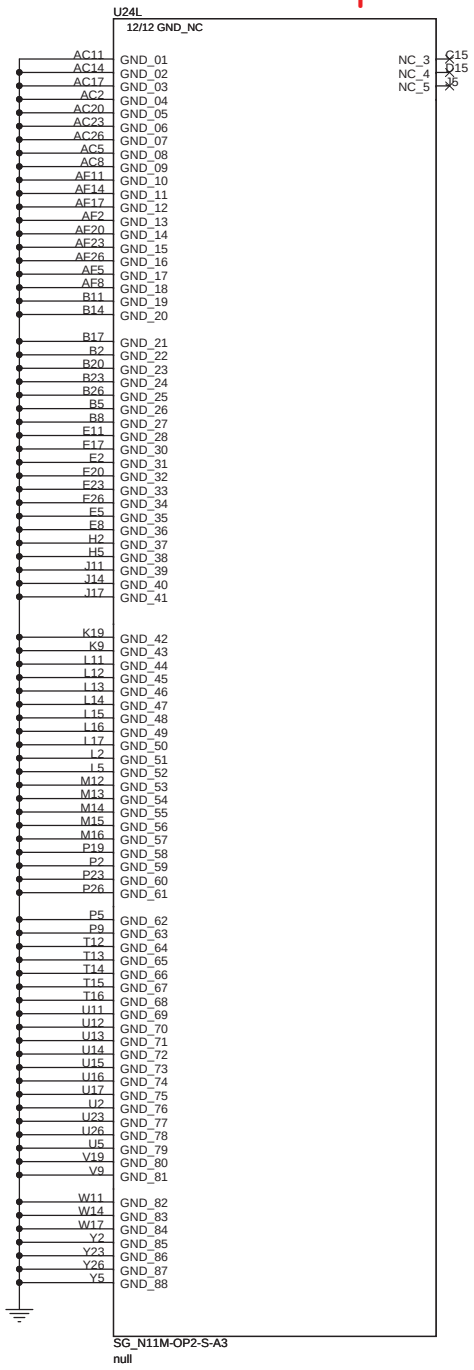
Size: A3 | Document Number: W920 PVT | Rev: 0.1

Date: Monday, May 17, 2010 | Sheet 54 of 71

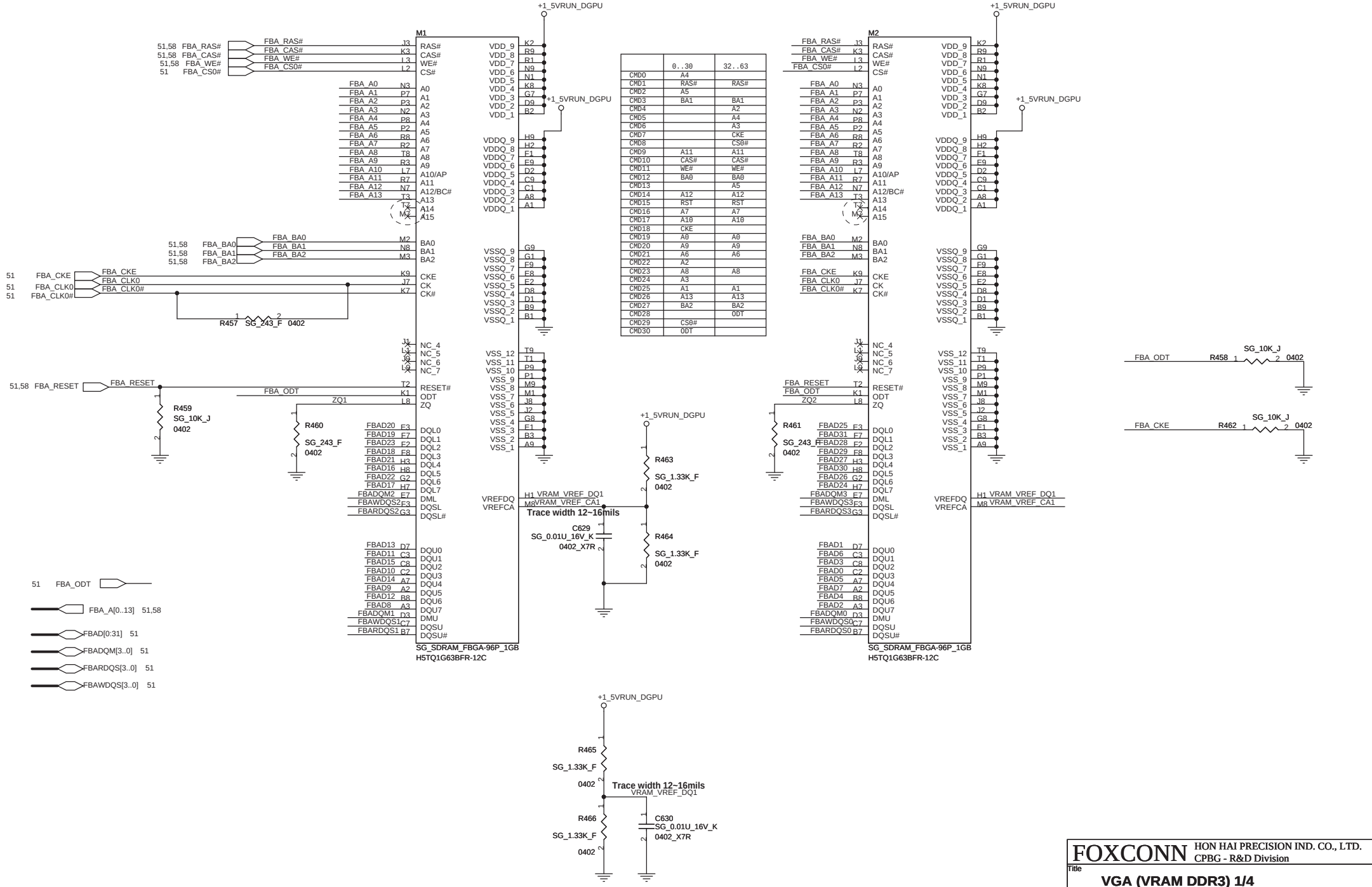


0326 For Y6 Driver level Fail,SI suggest to add 124 ohm resistor.

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: VGA (CRYSTAL)		
Size: A3	Document Number: W920 PVT	Rev: 0.1
Date: Wednesday, May 12, 2010	Sheet 55 of 71	

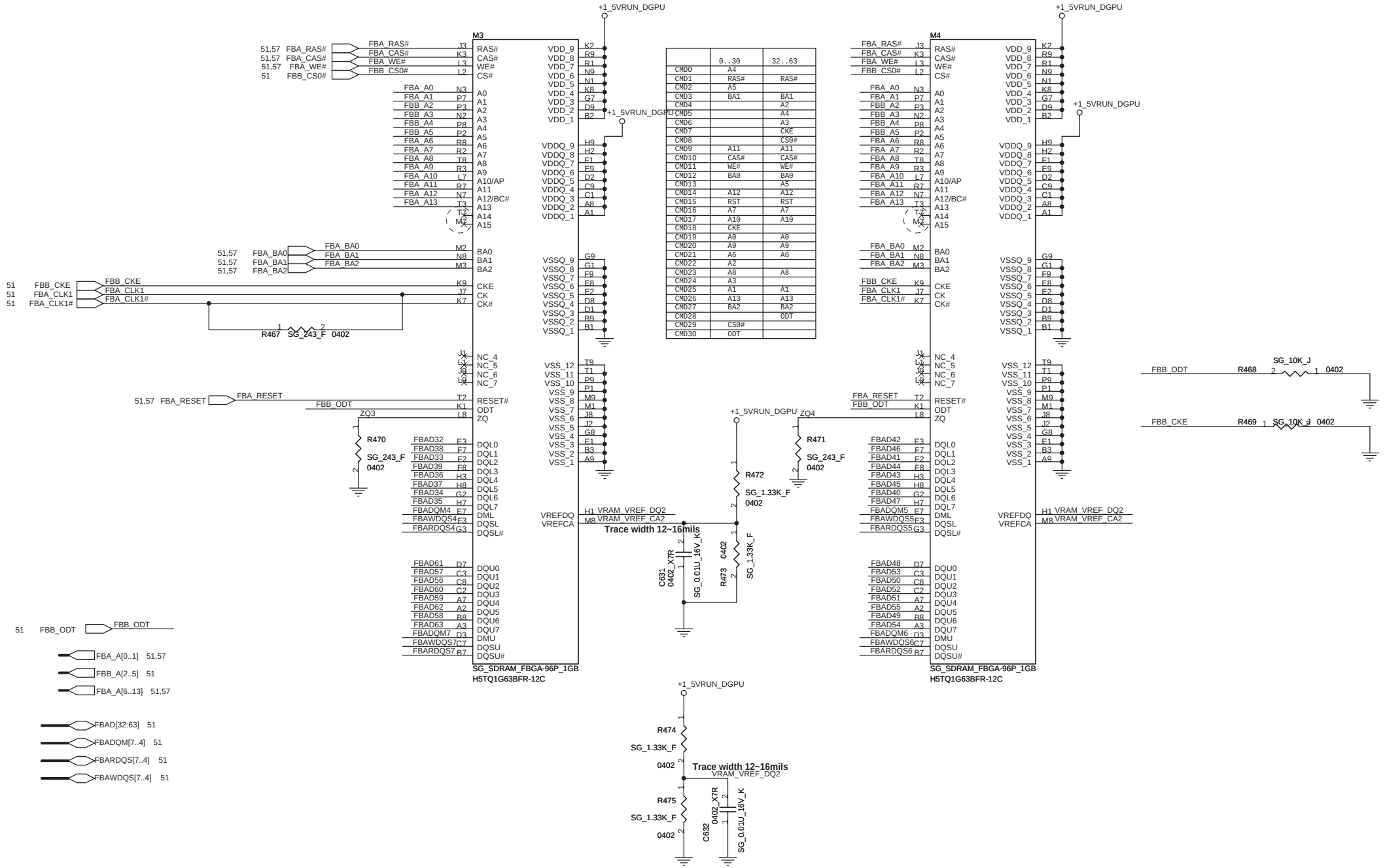


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA (PWR&GND)	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Wednesday, May 12, 2010	Sheet 56 of 71	



	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA (VRAM DDR3) 1/4	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 57 of 71	



	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA (VRAM DDR3) 2/4	
Size A3	Document Number W920 PVT	Rev 0.1
Date: Monday, May 17, 2010	Sheet 58 of 71	

for Back to Back VRAM Layout

Place around the VRAM M1

+1_5VRUN_DGPU

500mA

C633 SG_0.1U_16V_K 0402_X7R
C634 SG_0.1U_16V_K 0402_X7R
C635 SG_0.1U_16V_K 0402_X7R
C969 NC_47P_50V_J 0402_NPO
C644 22U_6.3V_M 0805_X5R

Place around the VRAM M1

+1_5VRUN_DGPU

C646 SG_0.1U_16V_K 0402_X7R
C647 SG_1U_6.3V_K 0402_X5R
C648 SG_1U_6.3V_K 0402_X5R
C650 SG_1U_6.3V_K 0402_X5R

Place around the VRAM M2

+1_5VRUN_DGPU

500mA

C656 SG_0.1U_16V_K 0402_X7R
C657 SG_0.1U_16V_K 0402_X7R
C658 SG_0.1U_16V_K 0402_X7R
C970 NC_47P_50V_J 0402_NPO

Place around the VRAM M2

+1_5VRUN_DGPU

C651 SG_0.1U_16V_K 0402_X7R
C652 SG_1U_6.3V_K 0402_X5R
C653 SG_1U_6.3V_K 0402_X5R
C655 SG_1U_6.3V_K 0402_X5R

Place around the VRAM M3

+1_5VRUN_DGPU

500mA

C670 SG_0.1U_16V_K 0402_X7R
C671 SG_0.1U_16V_K 0402_X7R
C672 SG_0.1U_16V_K 0402_X7R
C971 NC_47P_50V_J 0402_NPO
C685 22U_6.3V_M 0805_X5R

Place around the VRAM M3

+1_5VRUN_DGPU

C669 SG_0.1U_16V_K 0402_X7R
C675 SG_1U_6.3V_K 0402_X5R
C676 SG_1U_6.3V_K 0402_X5R
C678 SG_1U_6.3V_K 0402_X5R

change C685 from NC to mount for SI test fail issue

Place around the VRAM M4

+1_5VRUN_DGPU

500mA

C687 SG_0.1U_16V_K 0402_X7R
C688 SG_0.1U_16V_K 0402_X7R
C689 SG_0.1U_16V_K 0402_X7R
C972 NC_47P_50V_J 0402_NPO

PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.

Place around the VRAM M4

+1_5VRUN_DGPU

C696 SG_0.1U_16V_K 0402_X7R
C697 SG_1U_6.3V_K 0402_X5R
C698 SG_1U_6.3V_K 0402_X5R
C704 SG_1U_6.3V_K 0402_X5R

PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA VRAM BYPASS

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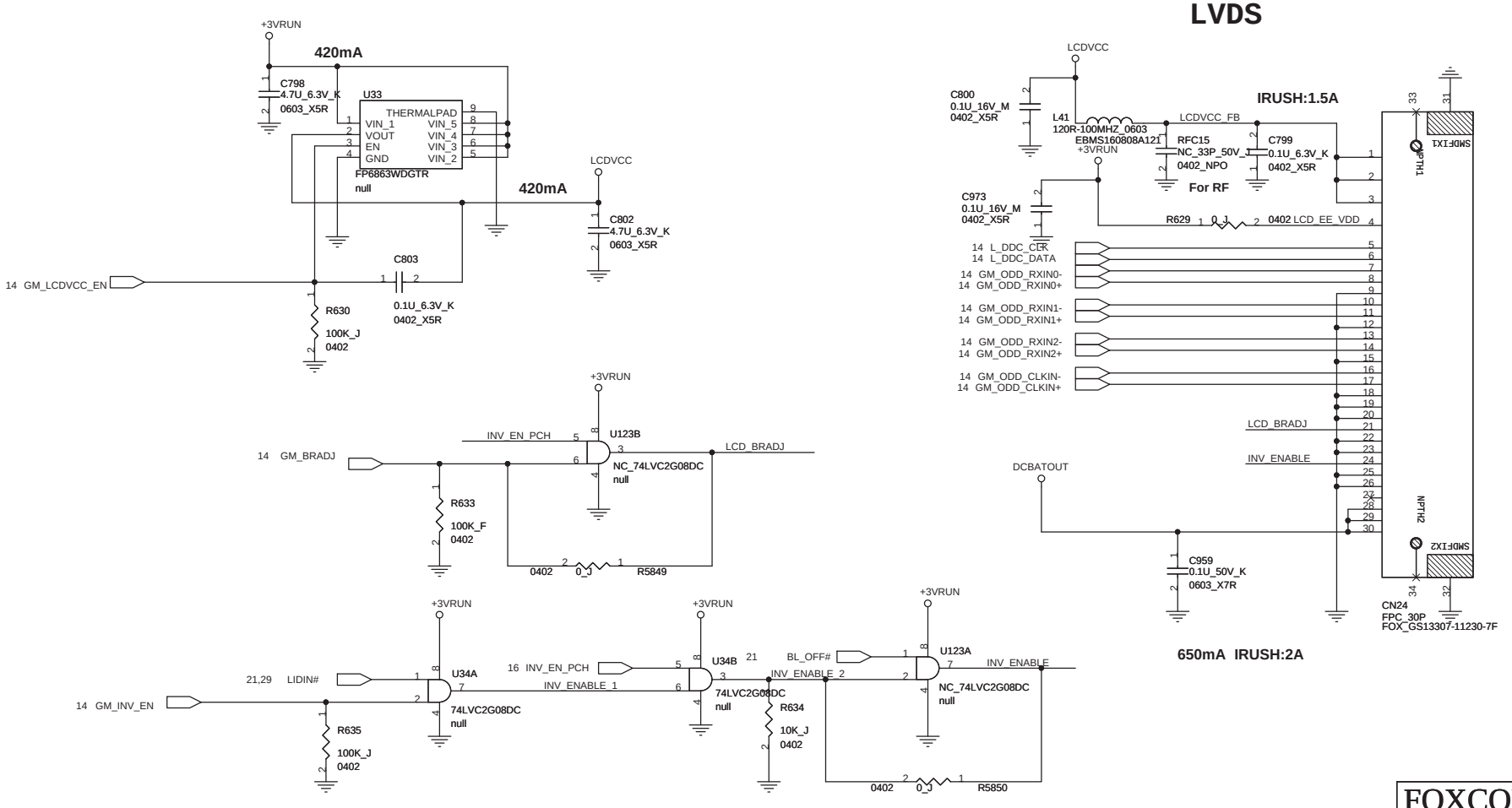

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: LVDS		
Size: A3	Document Number: W920 PVT	Rev: 0.1
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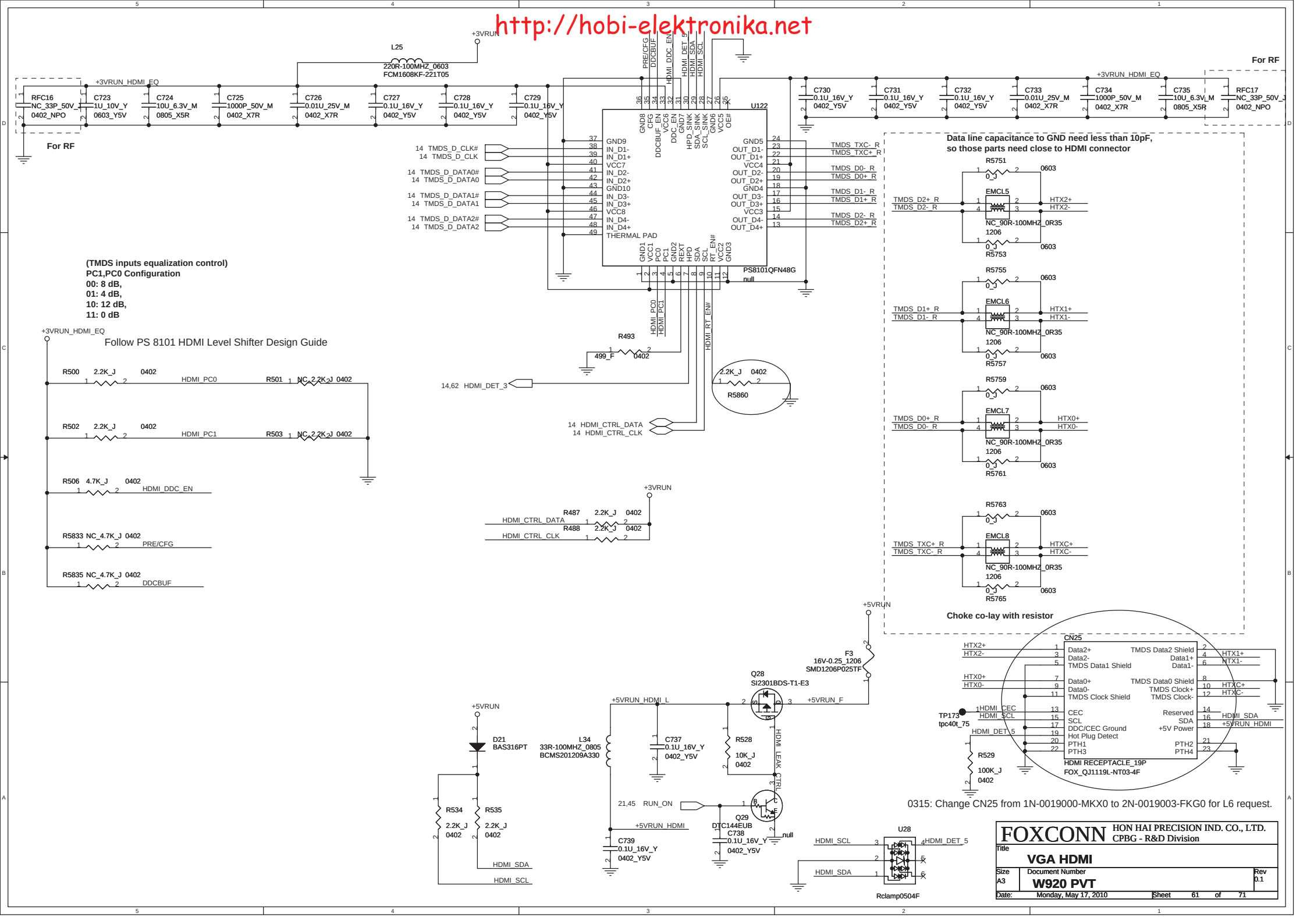

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VGA HDMI
Size	A3
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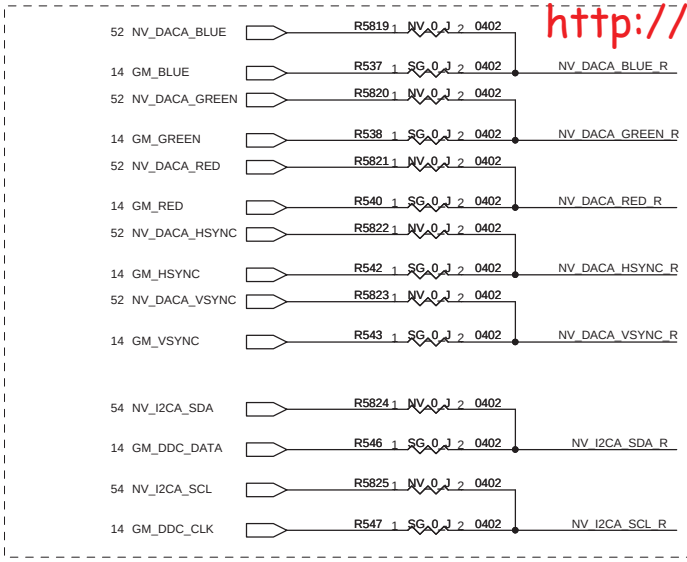
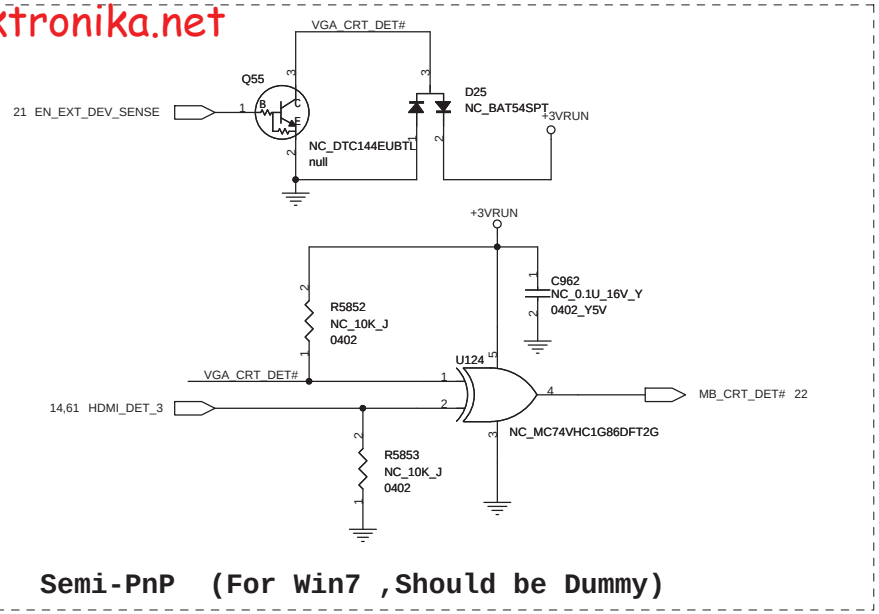
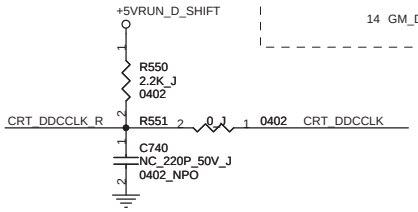
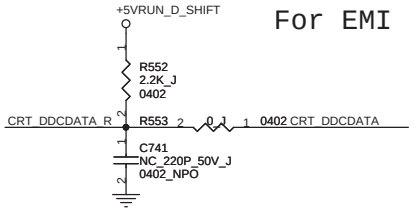
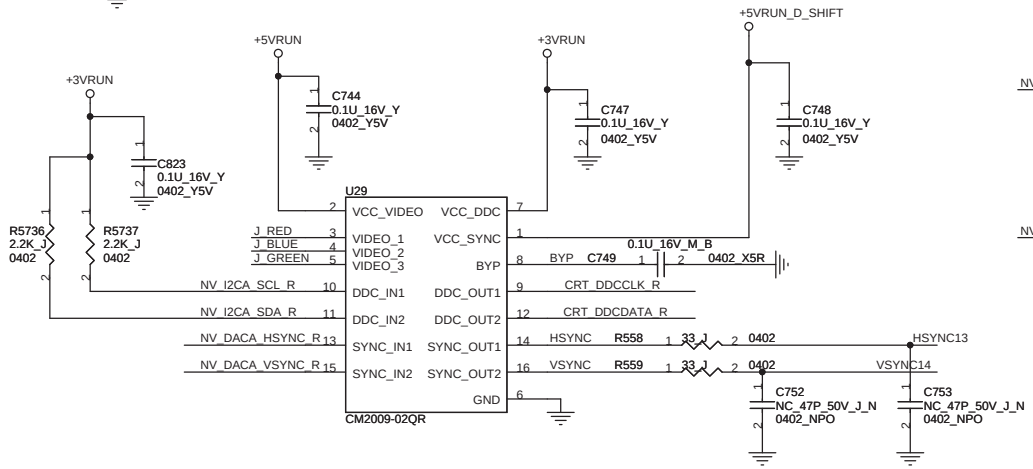


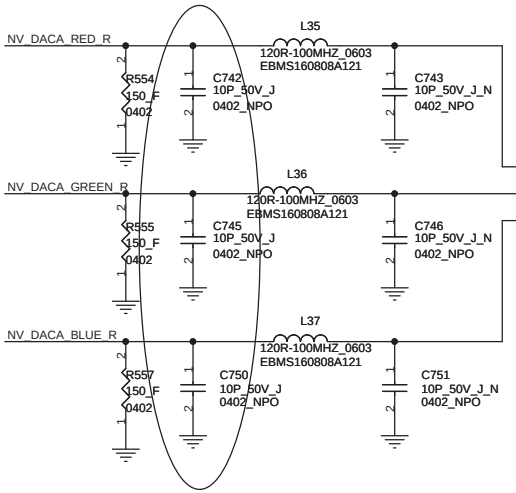




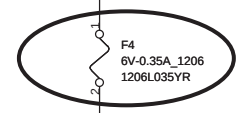


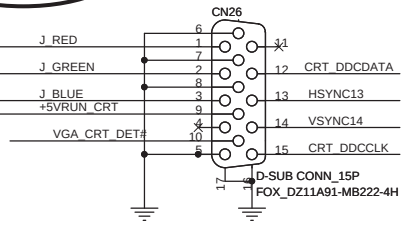


0315: Change C742, C745, C750 from NC to mount for CRT noise issue.



Change F4 HH PN from 1M-F006A35-F000
to 1M-F6V0A35-F000 for vendor PN change





CRT CONNECTOR

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: VGA CRT		
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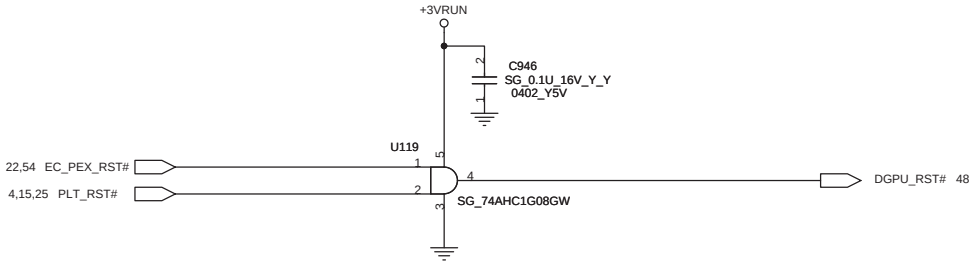
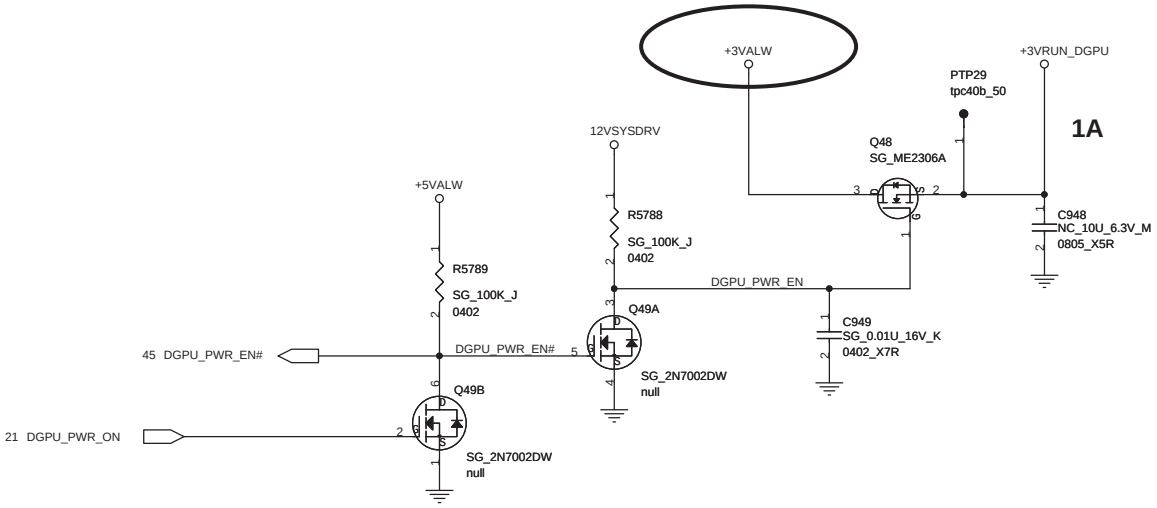
0322 Remove U118,C944 for there is no necessary to use this AND gate.



change from +3VRUN to +3VALW on DVT



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: VGA Optimus		
Size: A3	Document Number: W920 PVT	Rev: 0.1
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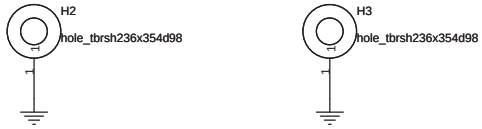
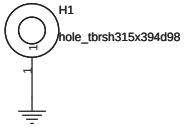
Type A



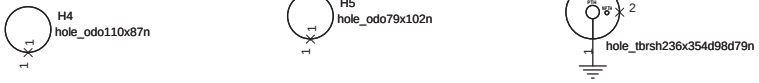
For M/B

Type H



For M/B

Type E,F,G



Type E

Type F

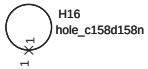
Type G for M/B

Type B

For Bluetooth

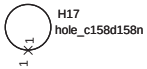
For M/B

Type J



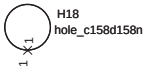
FOR CPU Bracket

Type L

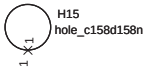


FOR CPU Bracket

Type I



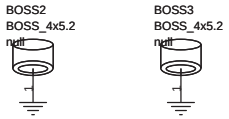
FOR CPU Bracket



FOR CPU Bracket

For Thermal module

Type B



For Mini-Card

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: HOLE&BOSS		
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(2010/02/23)

P. 11 {PCH (HDA,JTAG,SAT)} Change Y12 from 1F-X32K768-1000 to 1F-X32K768-2006 for purchase difficult.
P. 22 {EC+KBC(NPCE783L) 2/2} Change Y12 from 1F-X32K768-1000 to 1F-X32K768-2006 for purchase difficult.

(2010/02/25)

P. 16 {PCH (GPIO,VSS_NCTF,RSVD)} Disabe PCH thrmtrip proctect follow other projects.
P. 22 {EC+KBC(NPCE783L) 2/2} Add thrmtrip# pull up for disabe PCH thrmtrip proctect .
P. 29 {TOUCHPAD&LID&LED} Change R333 from NC to mount for ALPS Touchpad.
P. 62 {CRT} Change C742, C745, C750 from NC to mount for CRT noise issue.

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **EVT history**

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(2010/03/15)

P. 45 {PWR_Others power plane} Change Y1 from 17-S17326D-NT00 to 17-1RFH370-2T00 for +1_5VRUN_DGPU drop issue.

P. 28 {FAN/THERMAL SENSOR} Change U120 and C371 from mount to NC for DDR thermal sensor.

P. 61 {HDMI} Change CN25 from 1N-0019000-MKX0 to 2N-0019003-FKG0 for L6 request.

P. 35 {MUTE} Add EAPD for Audio pop noise issue.

(2010/03/23)

P. 37 {PWR_Charger_TI} Change PR21 from 1R-0007321-F200 to 1R-0001022-F200 for CP point setting

P. 38 {PWR_+5V/+3V_TI} Change PU3 enable pin setting

P. 45 {PWR_Others power plane} Change PQ24/PQ27/PQ28/PQ33/PQ52 from 17-S17326D-NT00 to 17-S17326D-NT01 for Vendor EOL

P. 63 {Optimus} Remove U118,C944 for there is no necessary to use this AND gate.

P. 28 {FAN/THERMAL SENSOR} U125 pull low HW_THRMAL_SD# from pull low ALW_ON, for Sequence issue when this function action at EC hang up.

(2010/03/26)

P. 25 {CRYSTAL}For Y6 Driver level Fail,SI suggest to add 124 ohm resistor.

P. 24 {card reader}for SI test system voltage card 3.3v fail，change c952 from NC_4.7uF to 10uF

(2010/03/27)

P. 16 {PCH} Change AB7 and AB13 net neme.

P. 11-- P19 {PCH} Change U3 from 12-1BEXPEA-0000 to 12-1BEXPEA-B301.

P. 29 -- {TOUCHPAD&LID&LED} Delete L11 for cost down.
Add F5 for protect touch pad .

(2010/03/29)

P .63 --{ Optimus} change +3VRUN_DGPU power from +3VRUN to +3VALW

(2010/04/01)

P .22 --Cancel NC 100Kohm R5687 for SG.
P .22 --Change MM_IRQ pull high from +3VRUN to +ECVCC.
P .21 --Change TS_DATA & TS_CLK pull high from +3VRUN to +ECVCC.
P .28 --{ FAN/THERMAL SENSOR} R5857 resister Change from 18K to 22K.

(2010/04/03)

P .37 --Change PQ4 & PQ6 from 17-S13424B-DV00 to 17-S13424B-DV01
P .38 --follow EMI requst change PR42 & PC53 from NC to mont
P .38 --follow EMI requst change PR44 & PC54 from NC to mont

(2010/04/04)

P .48 --NC Q50 for use EC GPIO as GPU CLK_REQ_N instead of GPU CLK_REQ_N itself
P .51 --Add 47pF capacitor C978 for FB_PLLAVDD noise issue
P .21 --Reserve BL_OFF#.
P .21 --Change GPO76 from BL_OFF# to PEX_CLKREQ1 for SG.
P .31 --Change CN16 pin3 from GND to +ECVCC for TS DB change request

(2010/04/06)

P .45 --Add discharge circuit PR698 & PQ62 for fall time too long issue
P .29--add reserve resister R5868 & R5869 for debug
P .22--Change BT_PRS# pull high from +3VRUN to +3VSUS.
P .45 --change PR691 from NC_330 to 22 & PR690 from NC to mount & PQ56 from NC to mount for discharge issue

(2010/04/07)

P .33--Reserve RC filter for EMC.

(2010/04/08)

P. 25 { WLAN} Delete U14 and C334.

P. 31 ---- add TP227,TP228 on top side for PWR test

P. 46 ---- reserve new OVP function circuit for colay

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: DVT history		
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(2010/05/04)

1.P. 28 ---{ FAN/THERMAL SENSOR} Added test point PTP64.

2. P29 ---Change F5 HH PN from 1M-F10V0A1-F000
to 1M-F30VA12-F000 for vendor PN change

3. P29 ---Change F5 HH PN from 1M-F10V0A1-F000
to 1M-F30VA12-F000 for vendor PN change

(2010/05/05)

1. P. 38 {PWR_+5V/+3V_TI} delete test jump PJ3/PJ4
2. P. 39 {PWR_+1_5V/+0_75V_UPI} delete test jump PJ5/PJ6/PJ7/PJ8
3. P. 40 {PWR_+1_05V_VTT_UPI} delete test jump PJ9/PJ10/PJ11
4. P. 41 {PWR_1_8V_GMT} delete test jump PJ12
5. P. 42 {PWR_VHCORE -- ON} delete test jump PJ28/PJ29
6. P. 43 {PWR_+GFXCORE_ON} delete test jump PJ16/PJ17/PJ18
7. P. 44 {PWR_NV_VDD_TI} delete test jump PJ24/PJ25/PJ26/PJ27
8. P. 46 {PWR_OVP function} add PJ24 and mount PU19/PC582/PC581/PR701/PC584/PC585/PR699/PR700/PC583 for new OVP circuit .
9. P. 46 {PWR_OVP function} NC PU13/PC182/PQ37/PR246/PR247/PQ39/PU12/PC178/PD15/PR243/PC180/PR245/ PC181/PR237/PQ36/PQ38/PR242 for old OVP circuit

(2010/05/11)

1. P. 31 {KB/DB CONNECTOER}add 3 fuse on TS DB for DVT burn cable issue
2. P 54 VGA (GPIO) Change Q54 to D28 to correct the naming mistake.
3. P. 38 {PWR_+5V/+3V_TI} NC PR58 and add PC586/PD20/PR702/PR703 For 5VALW_LDO enable more smooth

(2010/05/12)

1. P. 31 {KB/DB CONNECTOER}Change KB test piont for TE request

(2010/05/13)

1. P. 29 -- {TOUCHPAD&LID&LED}Change for wlan swith change

(2010/05/14)

1. 40 -- {PWR_+1_05V_VTT_UPI} change PR83 &PC99 from NC to mount for EMI request

(2010/05/15)

1. 12 -- PCH (PCI-E,SMBUS,CLK) change Y2 from 1F-X00025M-3000 to 1F-X00025M-3001 for SI test fail issue

(2010/05/17)

1. 59 -- VGA (VRAM BYPASS) change C685 from NC to mount for SI test fail issue

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