

RS485M-M

BASED ON RES485-M VER:A
PCB : 244mm*244mm

Rev : 1.0 L2:PWR
L3:GND

1	Cover Page
2	Block Diagram
3	Clock Generator
4	Power (CPU Vcore) Intersil 6566(DCR Sense)
5	Power A(DC to DC)
6	Power B(DC to DC),PWR sequence&good
7	K8 - M2 CPU (HT) D
8	K8 - M2 CPU (MEM) A
9	K8 - M2 CPU (CTRL) B,C
10	K8 - M2 CPU (POWER,GND) E,F,G,H
11	NB - RS485(HT LINK0 IF) A
12	NB - RS485 (PCI-E LINK I/F) B
13	NB - RS485 (SYSTEM I/F) C
14	NB - RS485 (POWER & GND) D,E
15	DIMM1 & DIMM2(Dual Channel)
16	DIMM3 & DIMM4(Dual Channel)
17	DDR2 DIMMS POWER
18	DDR2 TERMINATION
19	PCI Express Slot x16 & x1
20	SB - ATI SB460/600(PCI, CPU, LPC)
21	SB - ATI SB460/600(APIC, GPIO, AUDIO, USB)
22	SB - ATI SB460/600(SATA, IDE,HWM,SPI)
23	SB - ATI SB460/600(STRAPS, PWR, DECOUPLING)
24	LPC SIO-ITE8712F/IX, LPC ROM
25	PCI 1, PCI2
26	PCI Extender & VGA
27	USB, IDE
28	COM, LPT
29	Front Panel, FAN
30	LAN (RTL8100SB/8100C)
31	1394:VT6307/6308
32	AUDIO ALC883/655 (CHIP)
33	AUDIO ALC883/655 (PANEL)
34	POWER DELIVERY CHART
35	CLOCK DISTRIBUTION

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VER:B ->C
1. FIX V_DIMM & GND SHORT BY THERMAL PAD IN LAYER3.
2. ADD D22.....P6
3. ADD C525.....P24

VER:C ->D
1. ADD R609,R610, CHANGE R554/R555 value.....P3
2. DEL U8,R586-R590. ADD R653-R655.....P7
3. CHANGE CODEC CIRCUIT TO STANDARD 655/883 CO LAY.....P21,P32
4. ADD TBM CIRCUIT.....P21,P24,P26
5. ADD IR1 & R556.....P24
6. CHANGE CPU & SYS FAN TO 3/4 pin CO LAY.....P24,P29
7. ADD Q62 FOR MSG LED.....P29
8. ADD 6307/6308P CO LAY CIRCUIT.....P31
9. ADD 655/833 CO LAY CIRCUIT.....P32,P33

RS485-M940 VER:D ->RS485M-M VER:1.0
1. CHANGE AC97_OSCIN TO U6 PIN 54.....P3
2. ADD C550 FOR EMI.....P3
3. ADD Q67 & R678 FOR PWM UPDATE.....P4
4. ADD C547.....P6
5. ADD R668-R673 FOR ATI UPDATE.....P7
6. ADD C552 FOR EMI.....P14
7. ADD C554-C556 FOR EMI.....P20
8. ADD SR4 & SR5 FOR ATI UPDATE.....P21
9. ADD C553 FOR EMI & IR1.....P24
10. DEL C546 & FB11.....P27
11. ADD F8.....P27
12. DEL 6308'S PME PIN FOR VIA UPDATE.....P31
13. ADD AUXIN.....P32
    
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IDE Cable detect

-P66DET	SB: GPIO9
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Voltage Adjustment

VCC18	SIO_GPIO20
	SIO_GPIO21

LED Blinking


G_LED1	SIO:GP10 (PIN84)
G_LED2	SIO:GP53 (PIN77)

Other

BIOS_WP	SIO:GP41 (PIN28)
WT_BEEP	SIO:GP16 (PIN29)
SIO_S4S5	SIO:GP40 (PIN79)
GPO_1394	SIO:GP31
GPO_LAN	SIO:GP30

PCI Bus Resource

PCI1	AD16	INT E, FGH	REQ0
PCI2	AD17	INT F, GHE	REQ1
LAN	AD21	INT G	REQ3
1394	AD24	INT H	REQ4

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Title			
Cover Page			
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High Side*2 TO-252
Low Side*2 TO-252

**PWM Intersil
SL6566CR(DCR sense)**

**Clock Generator
ICS 951416**

PCIE X 16

**AMD-K8
M2
mPGA-940**

HyperTransport
LINK0
OUT
IN
16x16

NB:ATI RS485
HT LINK0 CPU I/F
Integrated Graphics
1 16X PCIE VIDEO I/F
1 2X PCIE I/F with SB
4 1X PCIE I/F

2X/4X ALINK

SB:ATI SB460/600
USB2.0*10
SATA*4
AC97 2.3 & Azalia
ATA 66/100/133
ACPI 2.0
LPC 1.1
MII
PCI/PCI Bridge

460 : *8
600 : *10
USB 2.0

IDE*1
ATA66/100/133

AUDIO CODEC
ALC883
HD I/F

SATA*4
Serial ATA
RAID 0, 1, 0+1

**1394
VT6307**
2 Port

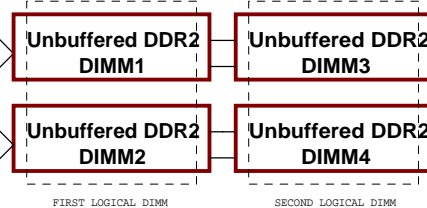
**LAN
RTL8110S/
RTL8100C**
RJ45

PCI*2

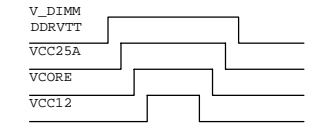
ITE SIO 8712F/IX
KB/
MOUSE
FLOPPY

BIOS
M

TPM



K8 POWER UP SEQUENCE	
RX480	AMD DESIGN GUIDE
1. -PS_ON	1. -PS_ON
2. V_DIMM DDRVT	2. VDDIO(V_DIMM) VTT (DDRVT)
3. VCC25A	3. VDDA (VCC25A)
4. VCORE	4. VDD (VCORE)
5. VCC12	5. VLDT (VCC12)
	6. PWROK

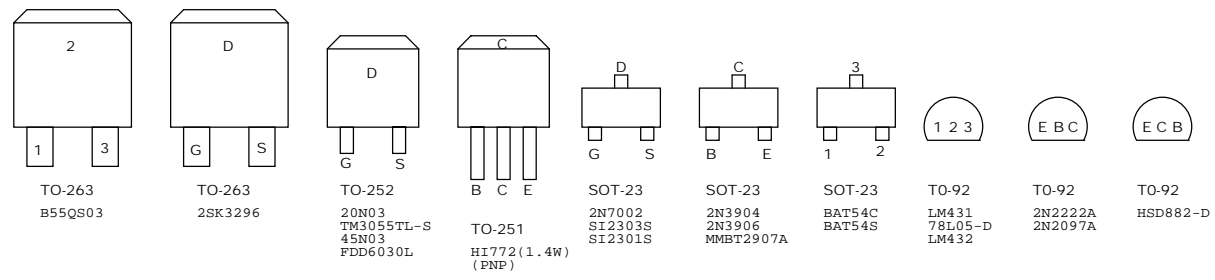


Layout width/space		PCB 2116	
USB(45/90)	20/8/8/8/20 20/8/8/8/20	(47/87) layout (47/87)	
LAN(50/100)	20/8/12/8/20 20/8/10/8/20	(47/91) layout (47/90)	
SATA(50/100)	20/6/6/6/20 20/5/7/5/20	(57/98) layout (62/111)	
PCI-E(50/100)	20/6/6/6/20 20/5/7/5/20	(57/98) layout (62/111)	
1394(55/110)	20/6/9/6/20 20/6/9/6/20	(56/105) layout (56/105)	
R.G.B (37.5)	20/9/18/9/18/9/20 25/5/25/5/25/5/25	ATI DEMO layout	
		Put 75 ohm on NB (Impedance=37.5 ohm)	

NB RX480

VDDHT	VCC1.2	0.5A
PCI-E CORE&VCO	VCC1.2	2.25A
NB CORE	NBCORE_1.2V	5A
DAC Main Power	VCC3	0.2A
DAC-Q&PLL	VCC1.8	0.1A
DAC Digital Power	VDD_1.8A	0.3A
LVDS	VDD_1.8A	0.1A

22U/25DE	5*7 mm
100U/16DE	6.3*11 mm
220U/10DE	6.3*11 mm
470U/16DE	8*11 mm
1000U/10DE	8*14 mm
1500U/16DE	10*25 mm
3300U/25DE	10*25 mm



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Block Diagram

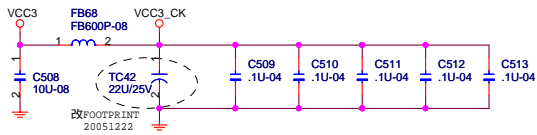
Size: Document Number
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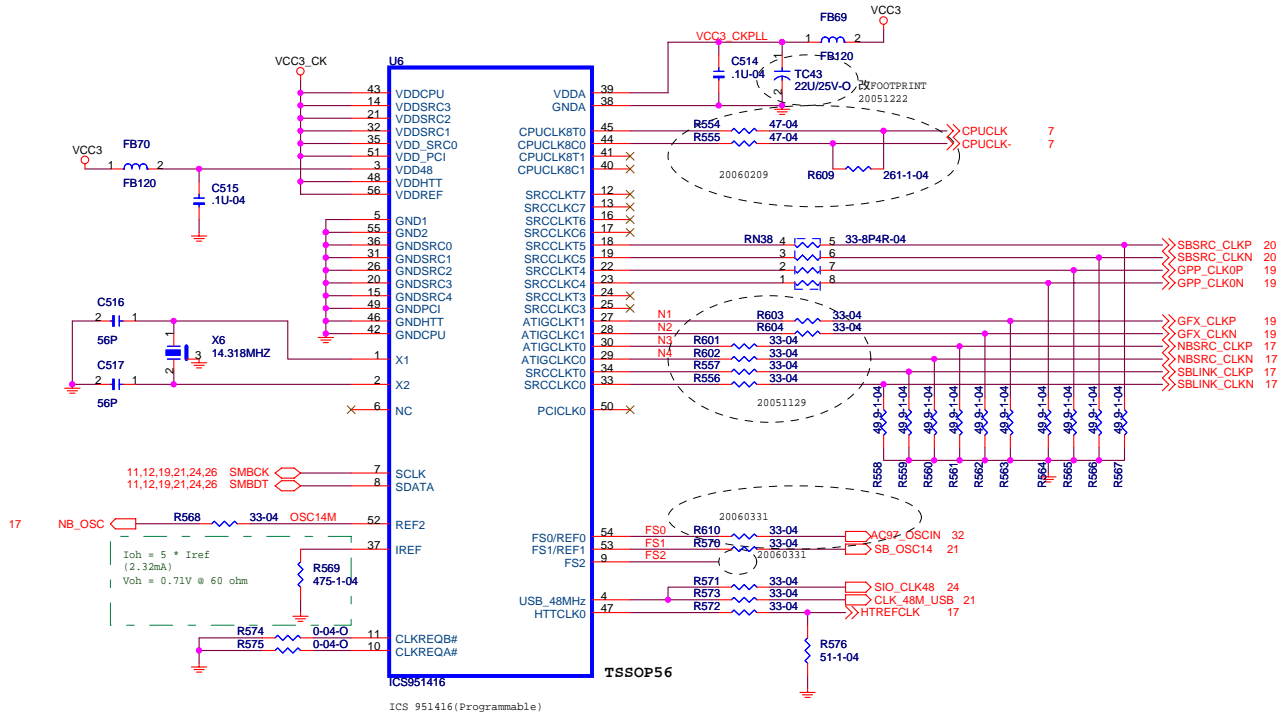
Rev 1.0

ATIGCLK Divider Selection

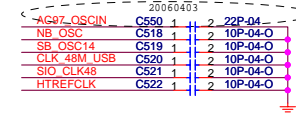
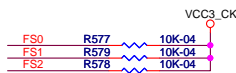
ATIG_Div(3:0)	ATIG_Div(3:0) (MHz)
1000	100.00
0011	114.29
TBD	133.33
0010	160.00



- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO CLOCK GEN
- 2- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



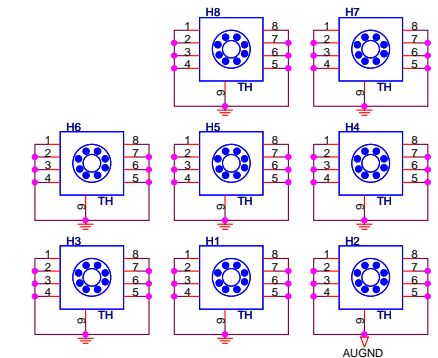
CUSTOMER CAN ALSO USE CY28RS480 CLOCK GENERATOR TO REPLACE ICS951412 WITHOUT HARDWARE CHANGE. BOTH CHIPS HAVE THE SAME FOOTPRINT.



EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

* FS0,1,2 internal pull low(120K ohm)

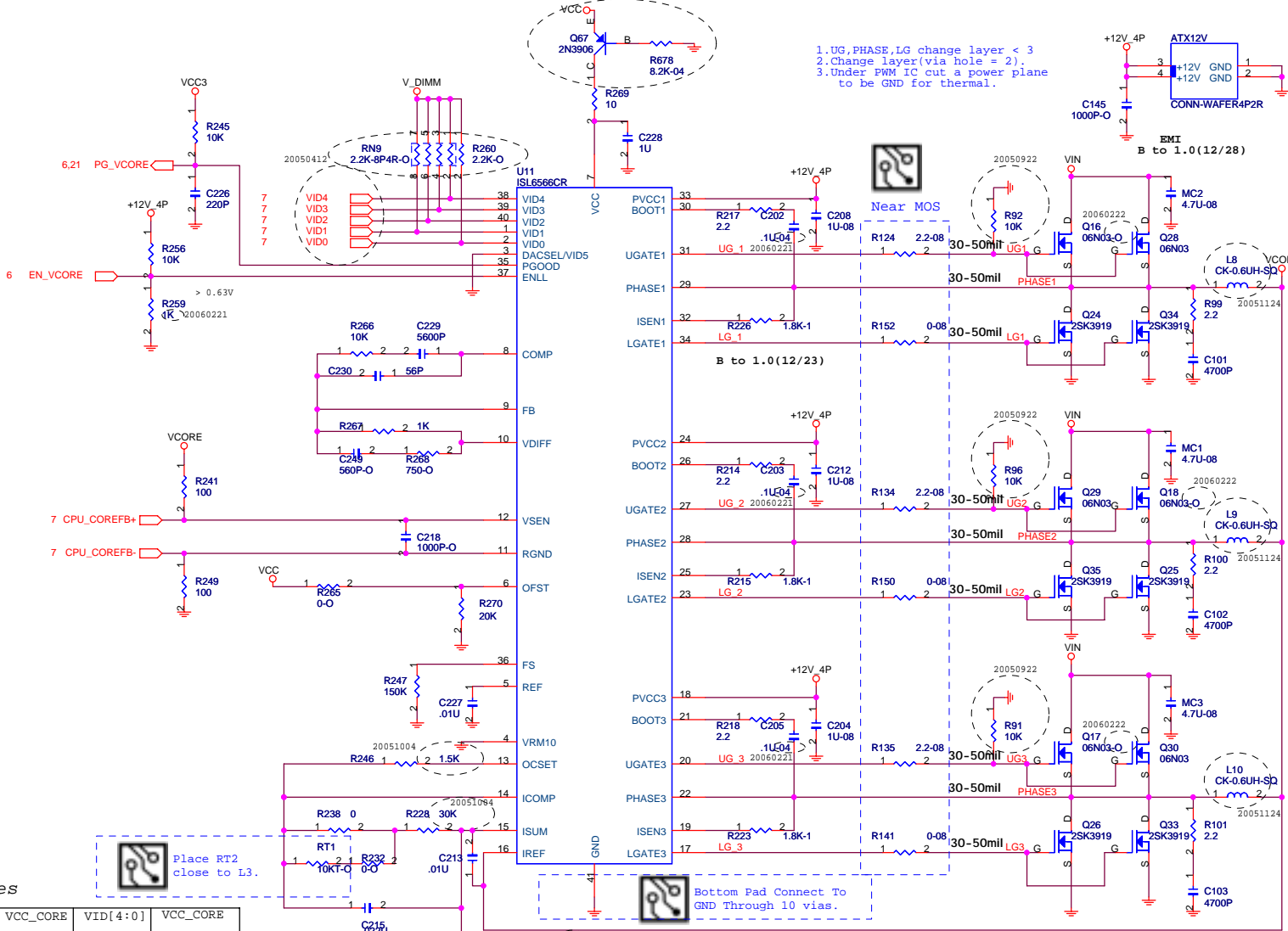


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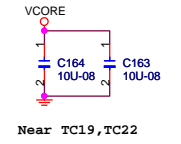
Title: **Clock Generator**

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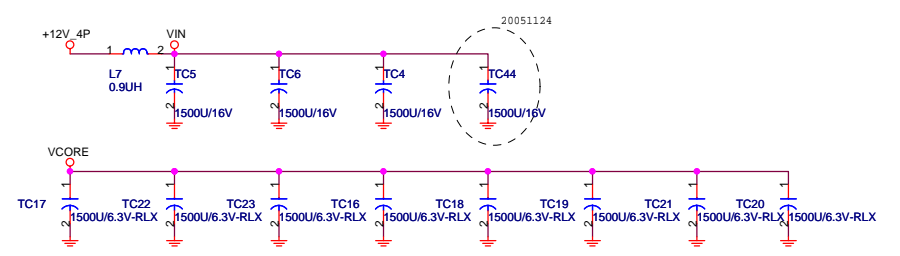
- 1.UG, PHASE, LG change layer < 3
- 2.Change layer(via hole = 2).
- 3.Under PWM IC cut a power plane to be GND for thermal.



0.8V-1.55V/80A

VID Codes

VID[4:0]	VCC_CORE	VID[4:0]	VCC_CORE
00000	1.550	10000	1.150
00001	1.525	10001	1.125
00010	1.500	10010	1.100
00011	1.475	10011	1.075
00100	1.450	10100	1.050
00101	1.425	10101	1.025
00110	1.400	10110	1.000
00111	1.375	10111	0.975
01000	1.350	11000	0.950
01001	1.325	11001	0.925
01010	1.300	11010	0.900
01011	1.275	11011	0.875
01100	1.250	11100	0.850
01101	1.225	11101	0.825
01110	1.200	11110	0.800
01111	1.175	11111	No CPU



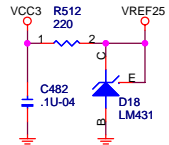
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Title: **Power (CPU Vcore)**

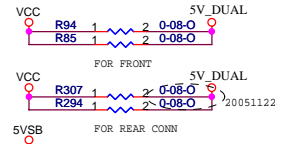
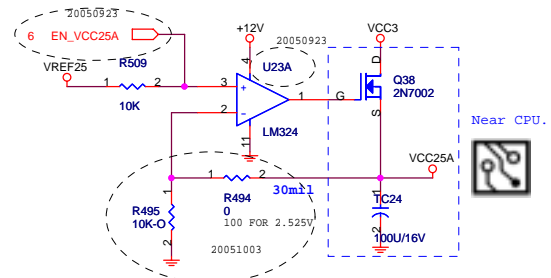
Size: Custom Document Number: **RS485M-M** Rev: **1.0**

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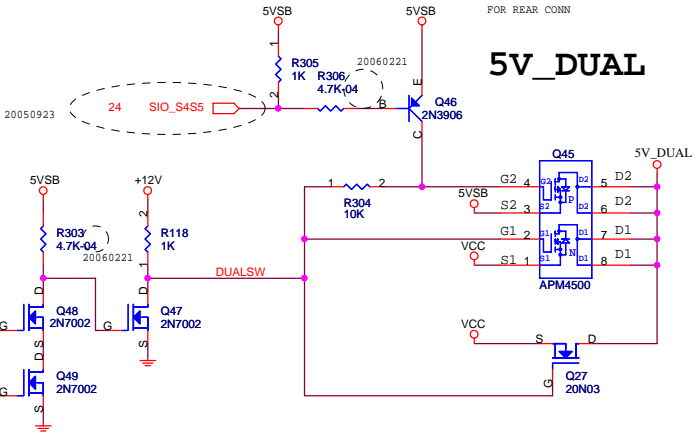
Status	Target	Super I/O F/GXS
	5V_DUAL=VCC	SIO_S4S5=0, D=1
S0, S1	5V_DUAL=VCC	SIO_S4S5=1
S3	5V_DUAL=5VSB	SIO_S4S5=0
S4, S5	5V_DUAL=5VSB	SIO_S4S5=0
S4, S5	5V_DUAL=0	SIO_S4S5=1



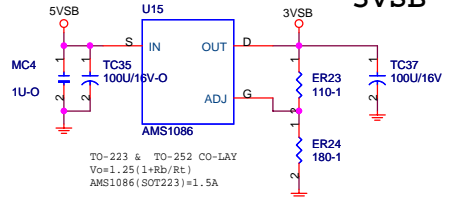
VCC25A



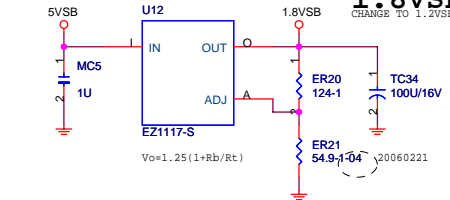
5V_DUAL



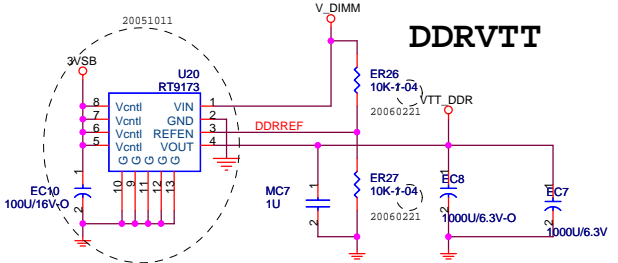
3V3SB



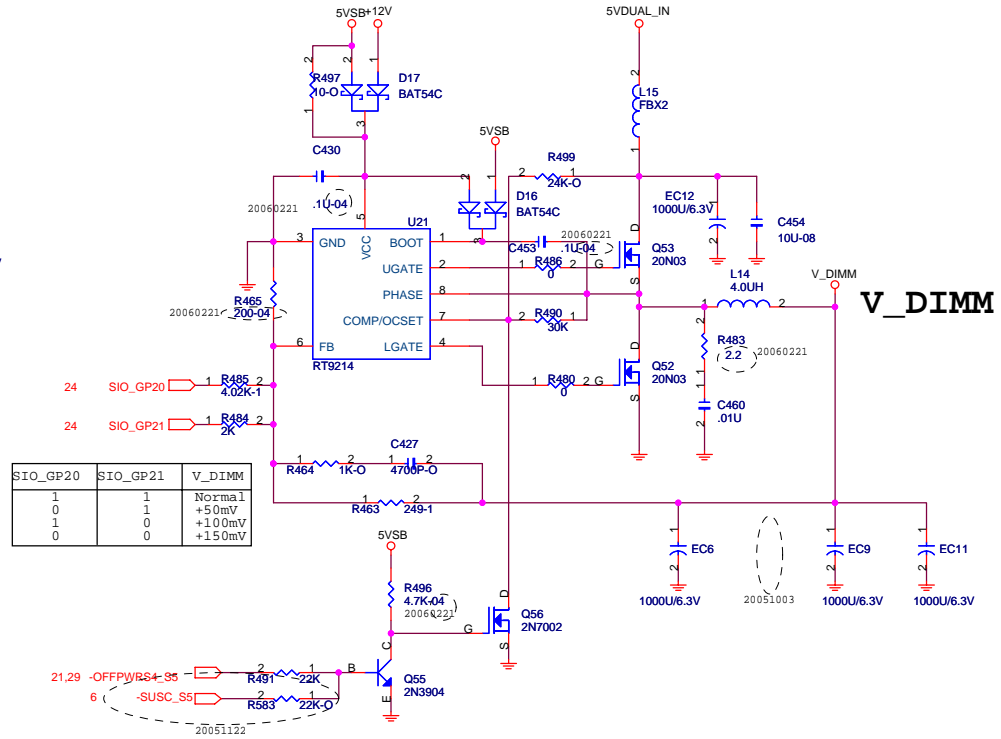
1.8V3SB



DDRVTT



V_DIMM



SIO_GP20	SIO_GP21	V_DIMM
1	1	Normal
0	1	+50mV
1	0	+100mV
0	0	+150mV

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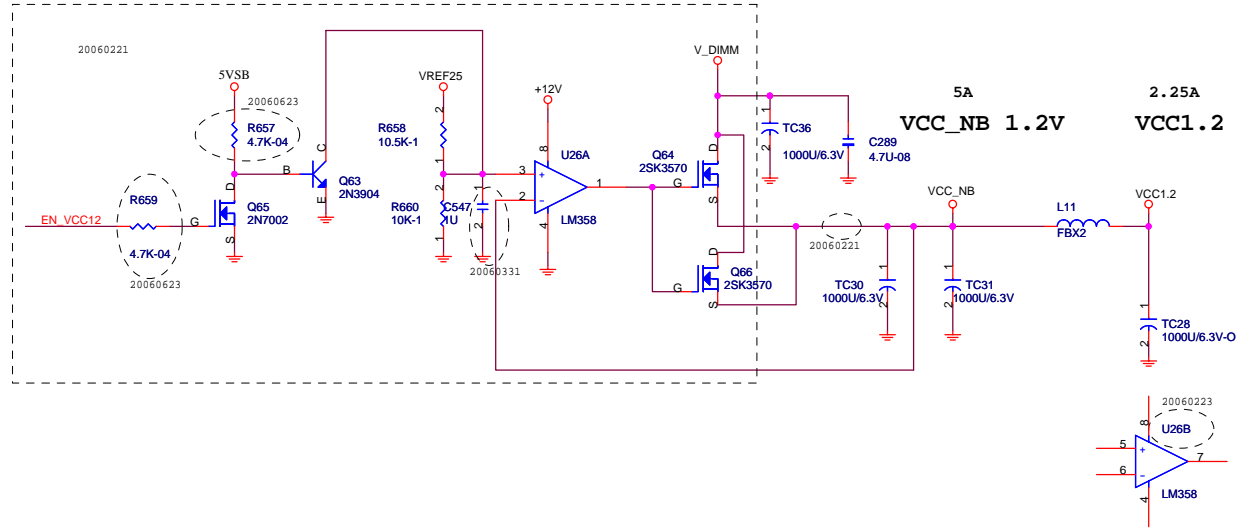
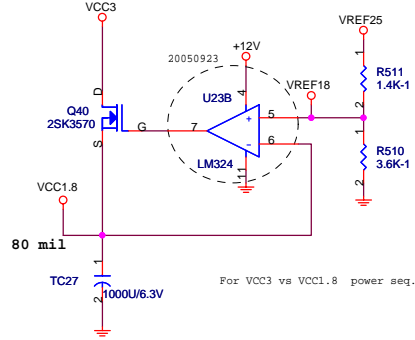
Title: **Power A(DC to DC)**

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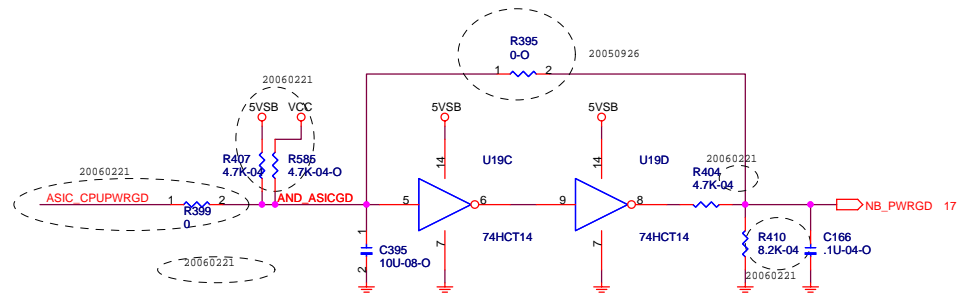
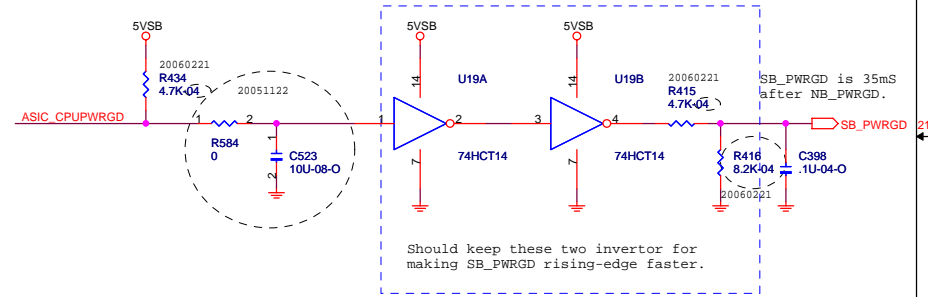
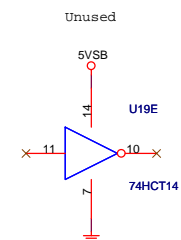
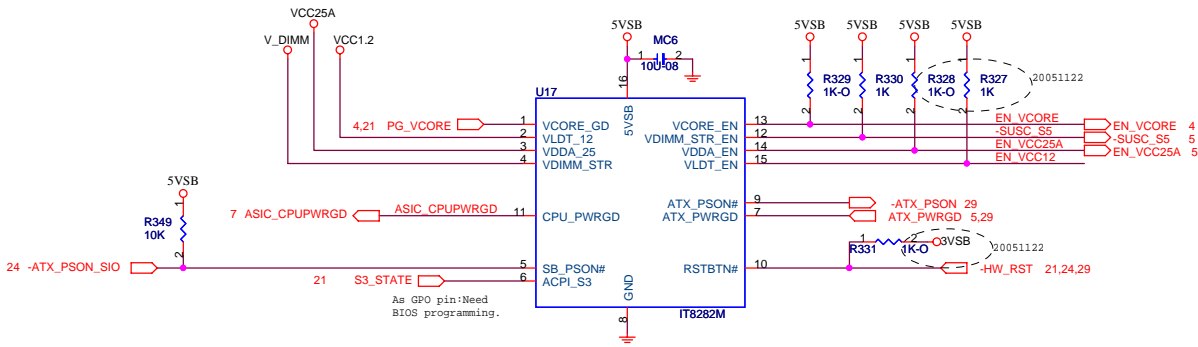
Custom: **RS485M-M**

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VCC1.8



K8 Power Sequence



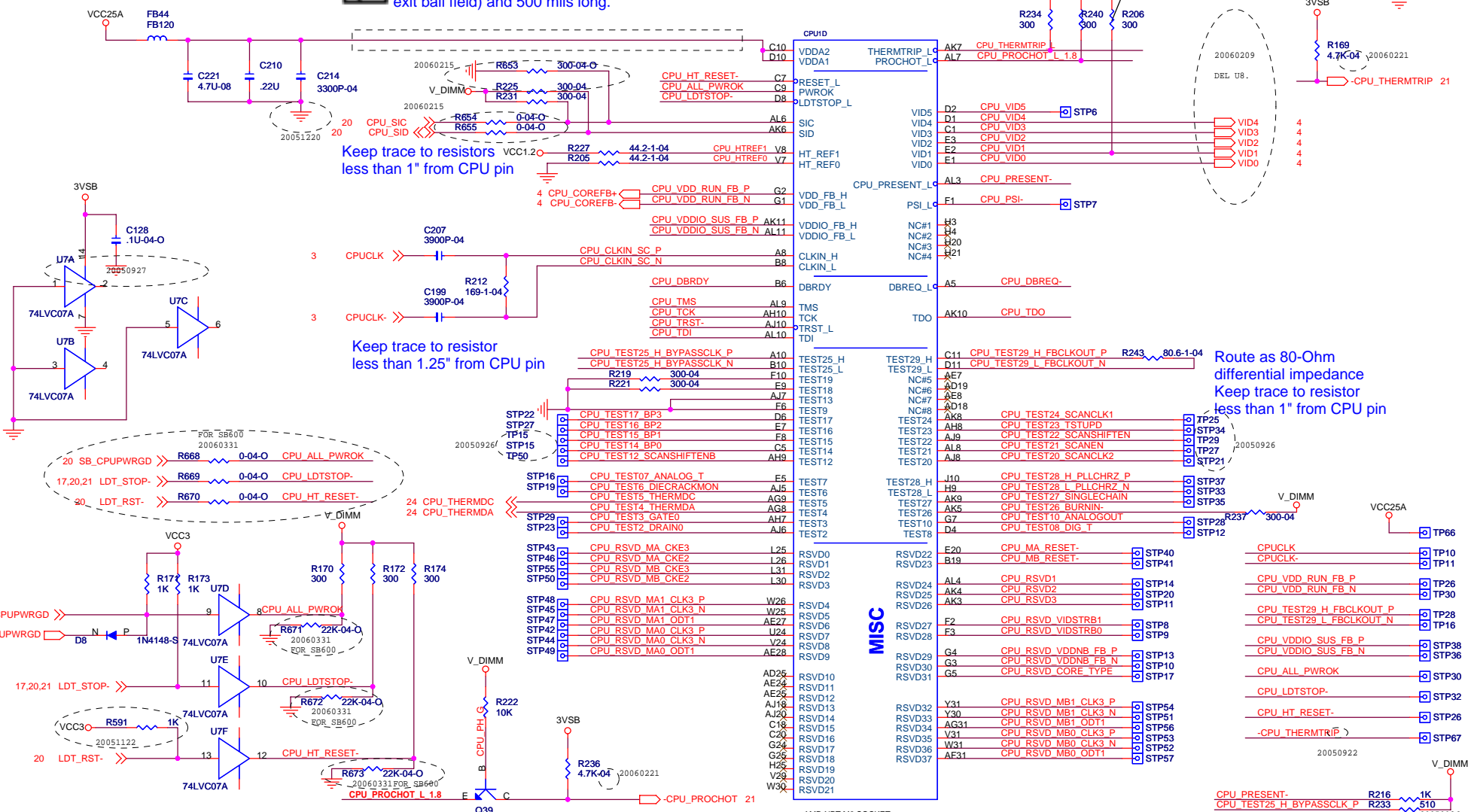
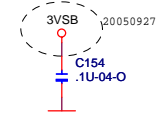
ATHLON Control and Debug

Required for compatibility with future processors

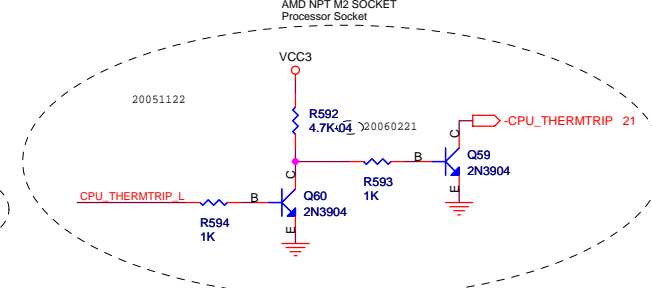
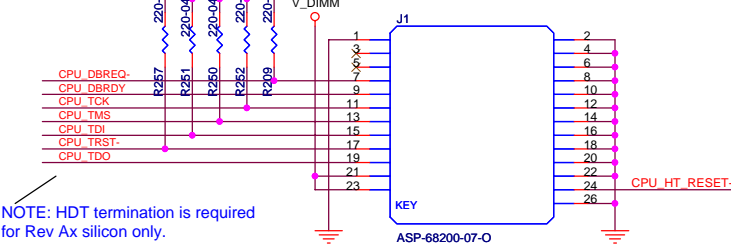


LAYOUT: Route VDDA trace approx. 50 mils wide (use 2x25 mil traces to exit ball field) and 500 mils long.

20060209
DEL R586, R589, R597, R599, R590.



HDT Connector



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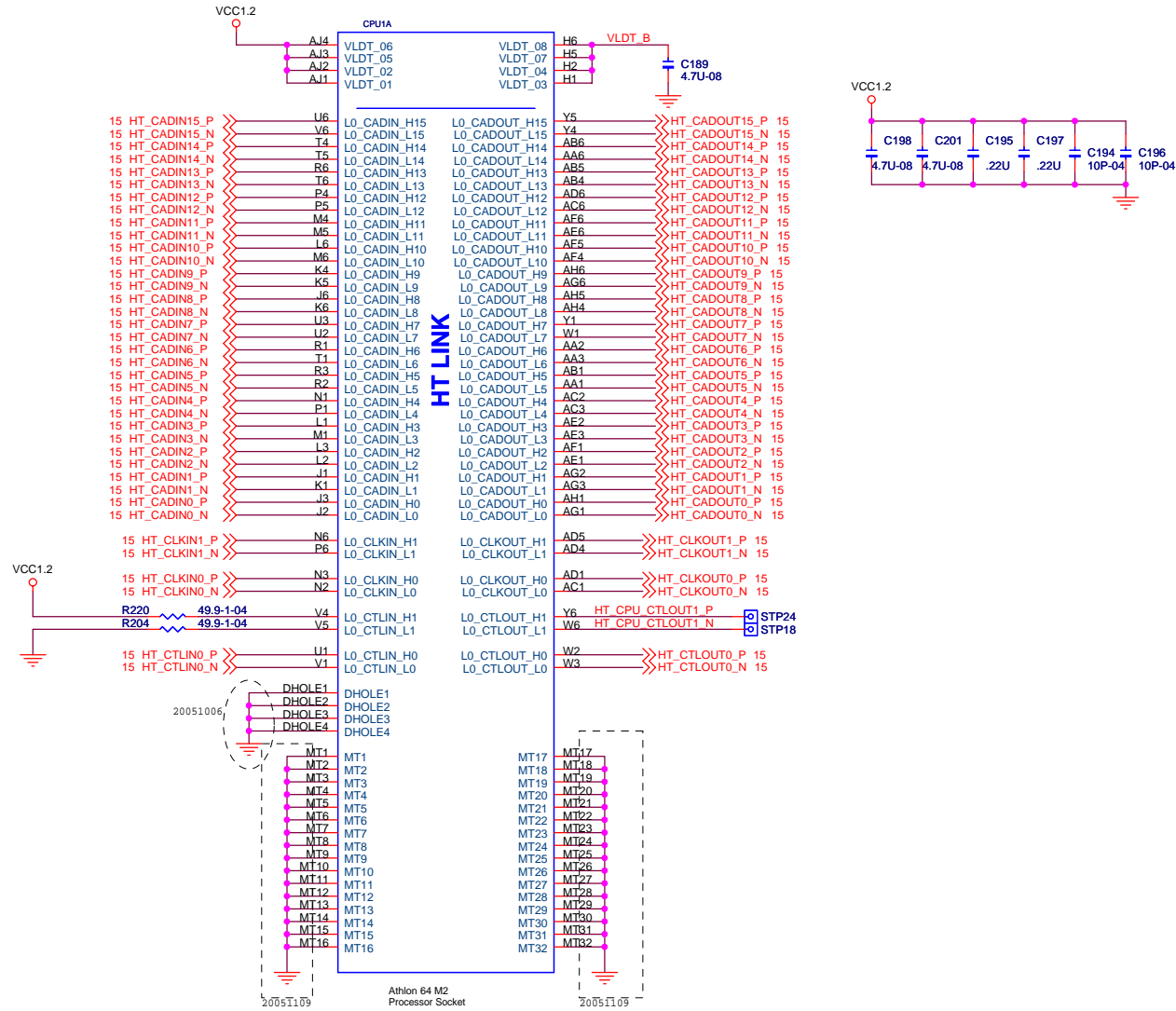
Title: **M2 HT I/F .CTRL & DEBUG PART1**

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CPU HyperTransport Interface

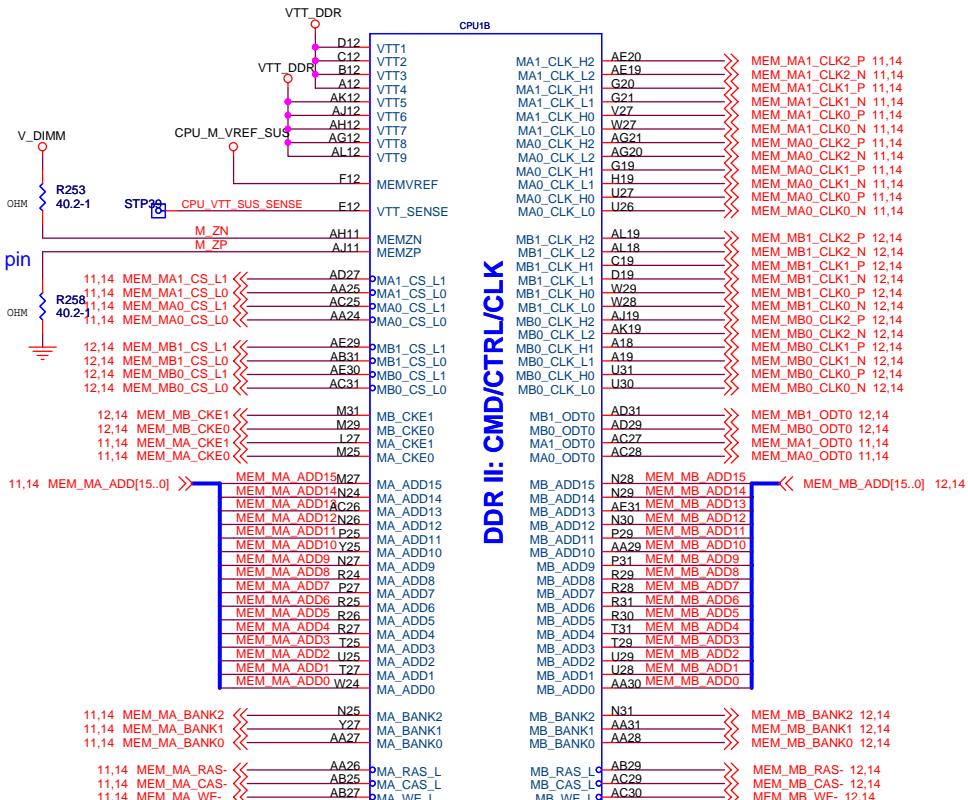
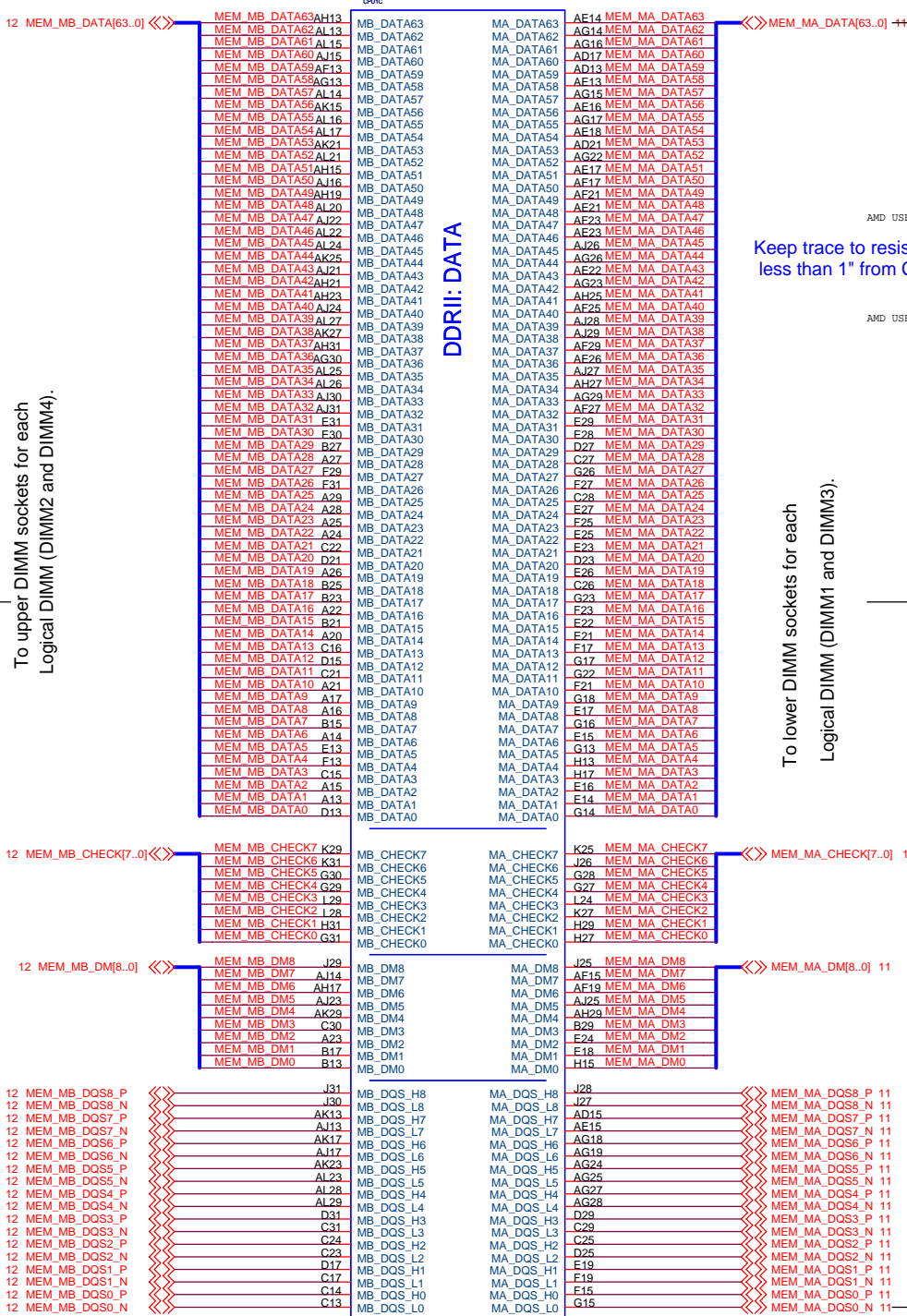
VDDLTRUNCPU is connected to the VDD_LDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



Processor DDR2 Memory Interface



VDD_VTT_SUS_CPU is connected to the VDD_VTT_SUS power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



VDD_VREF_SUS_CPU

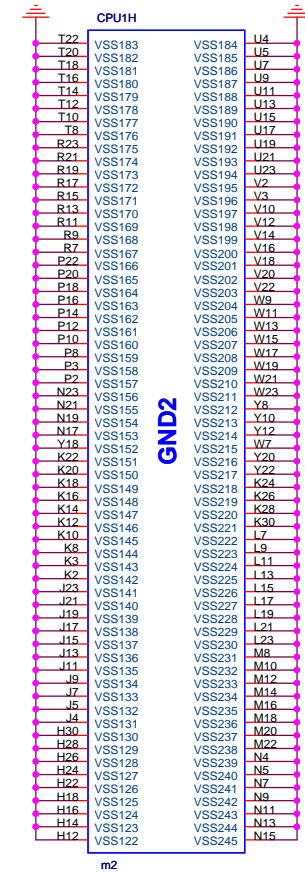
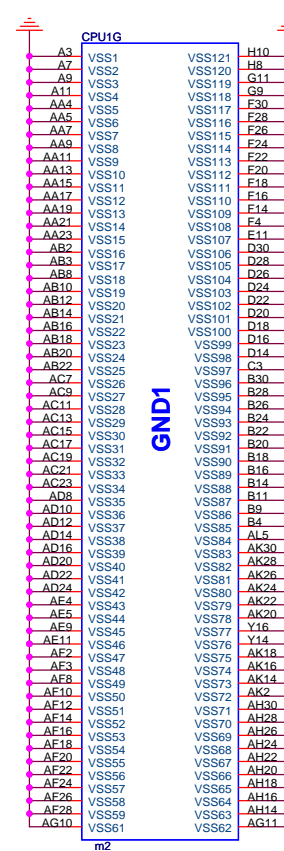
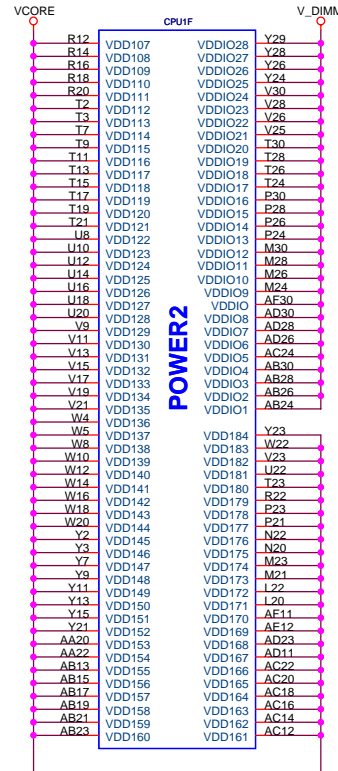
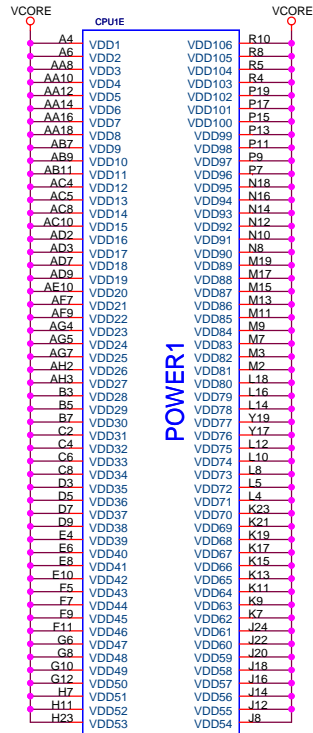
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Title: **M2 DDR2 MEMORY I/F**

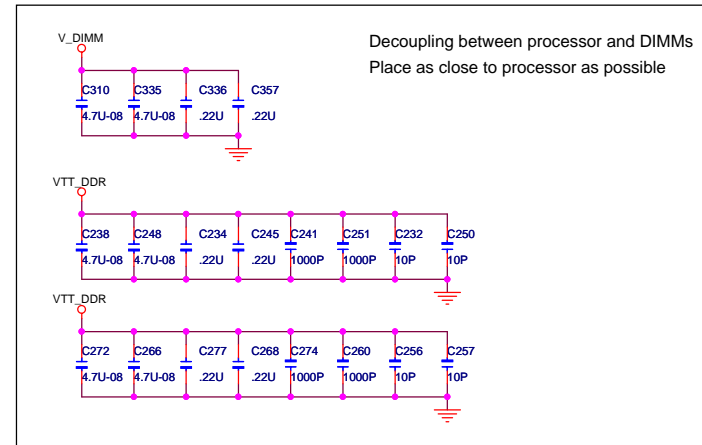
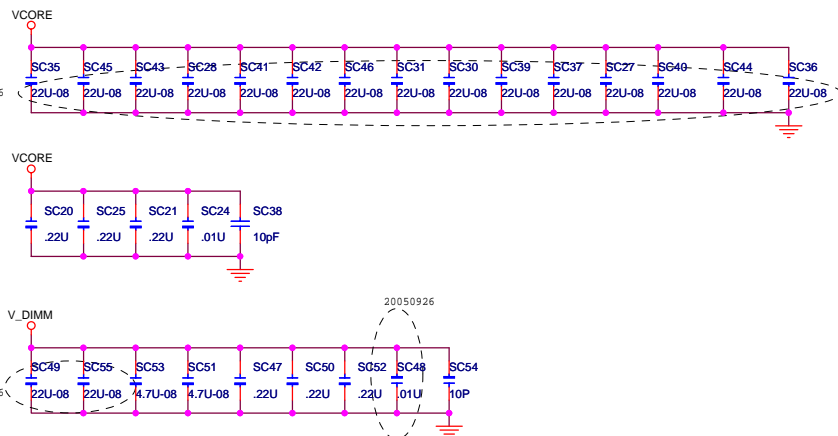
Size C Document Number: **RS485M-M** Rev: **1.0**

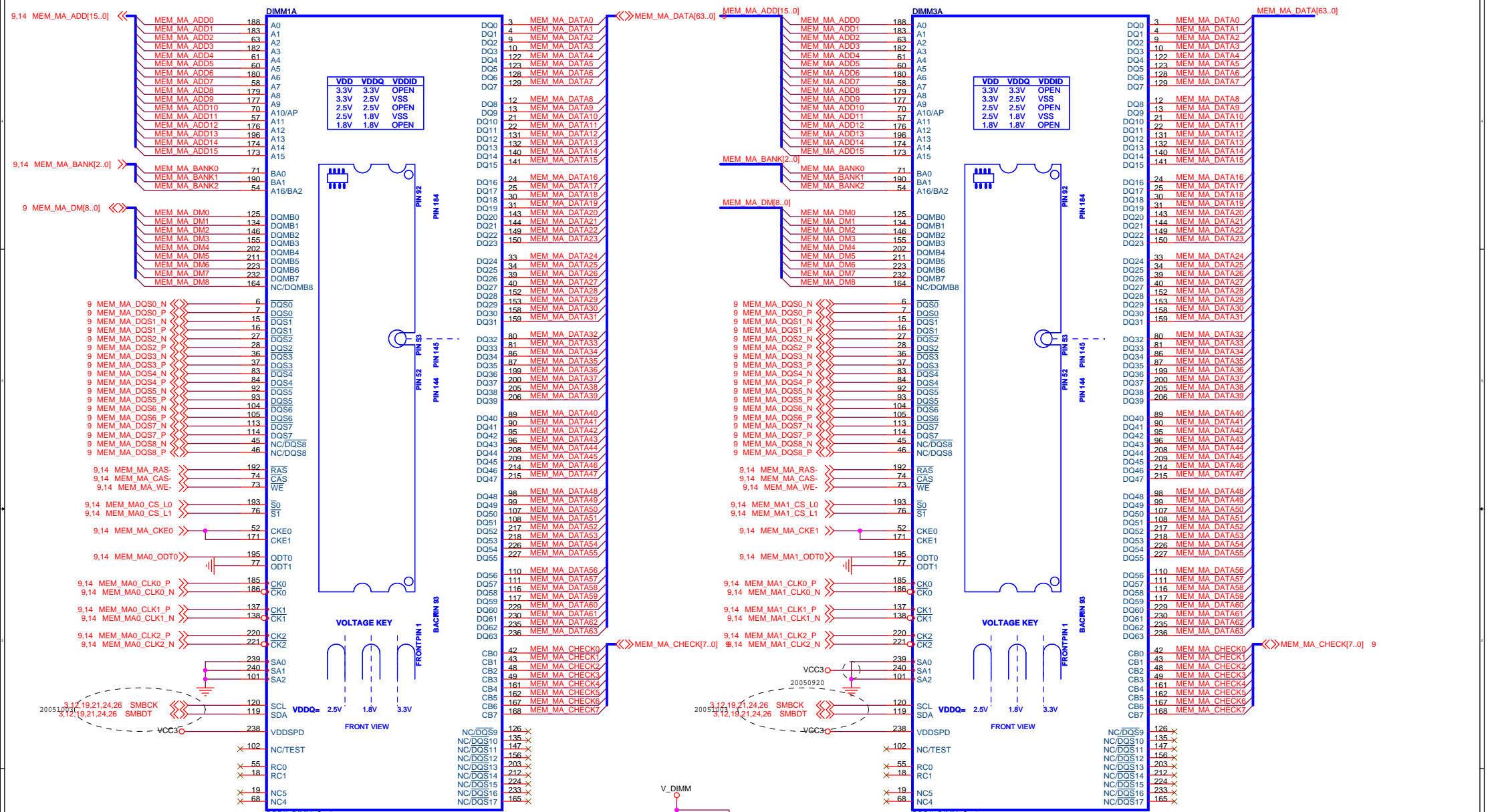
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Processor Power and Ground

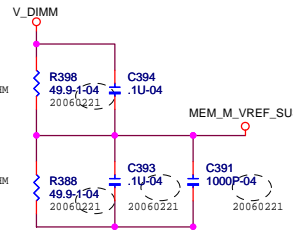


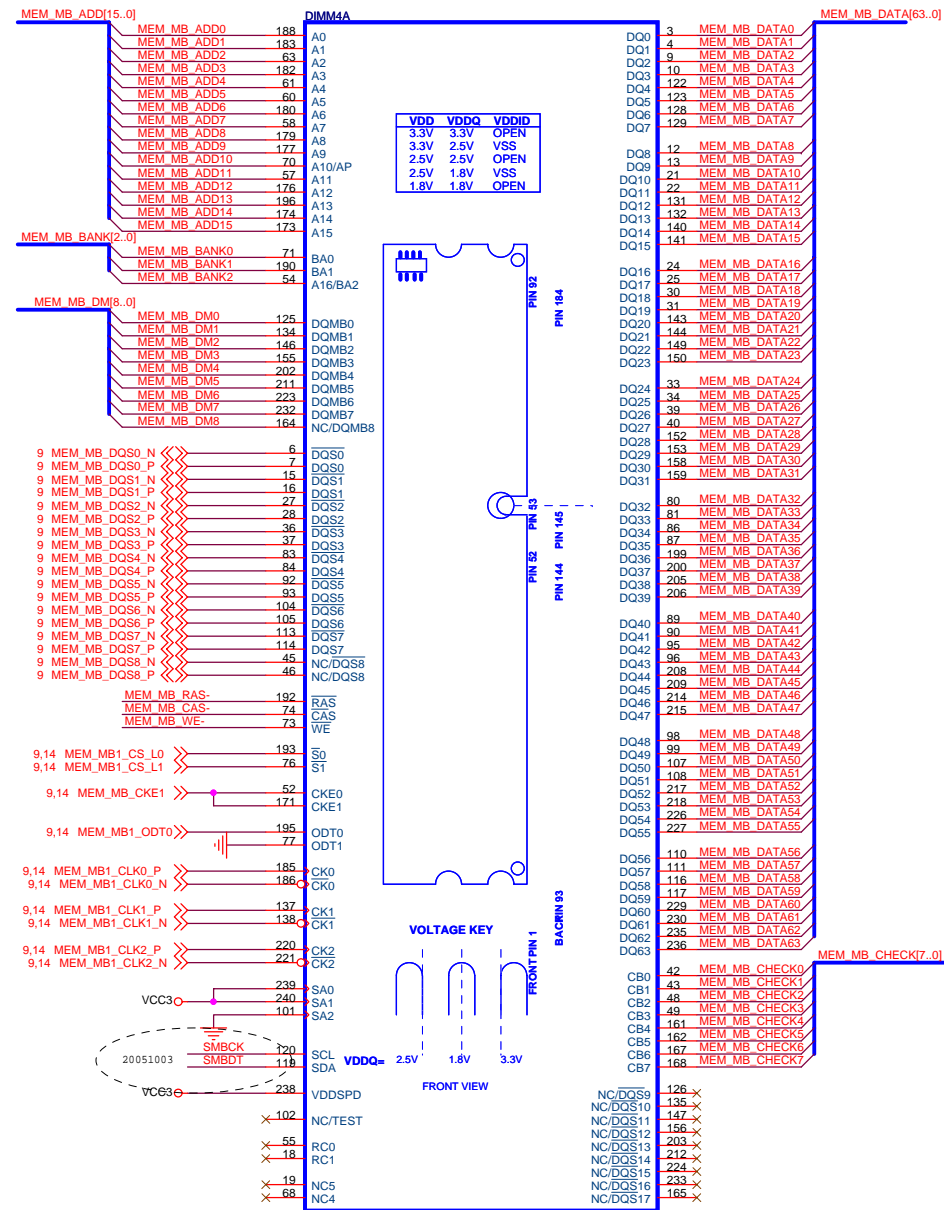
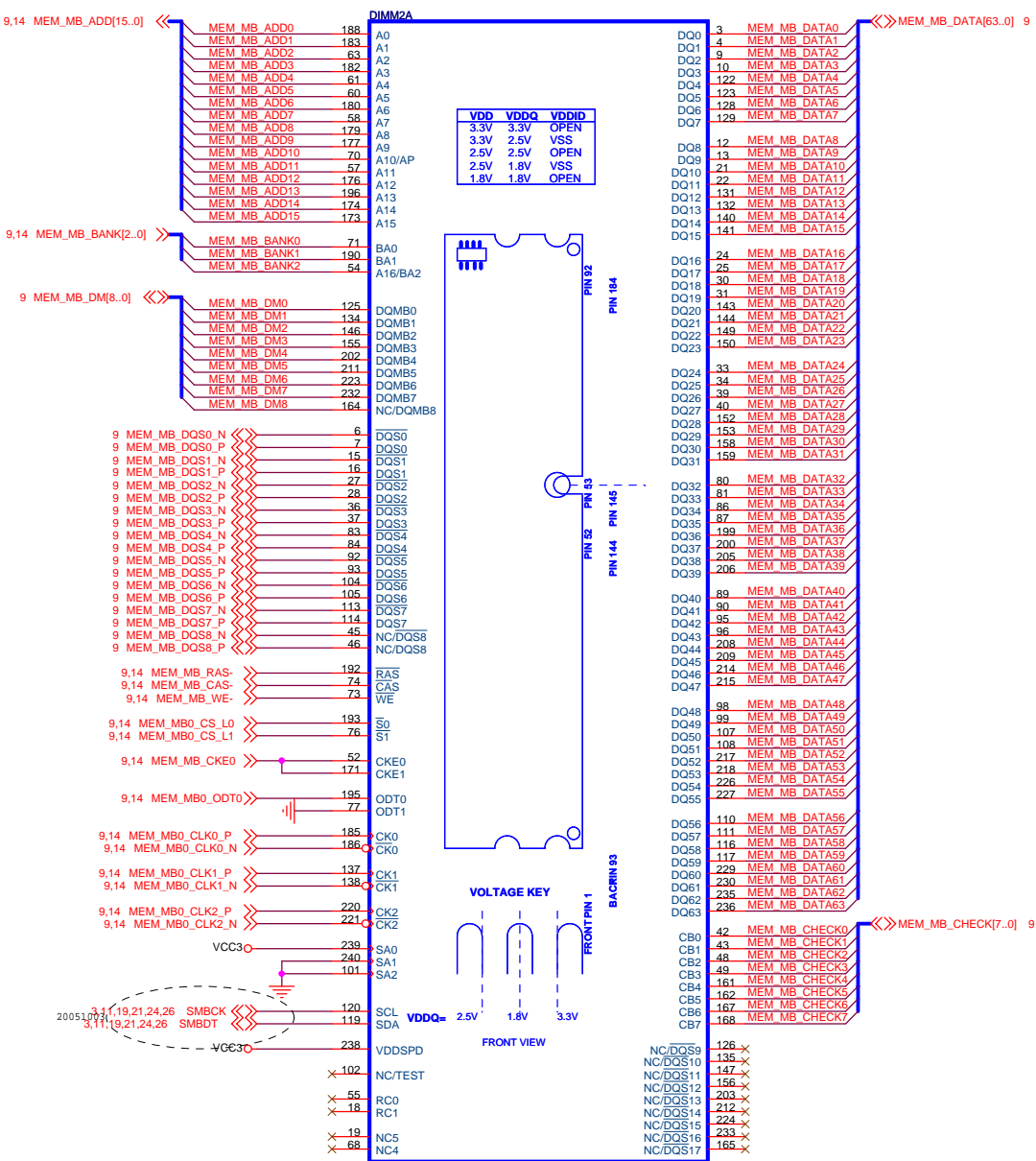
Bottomside Decoupling

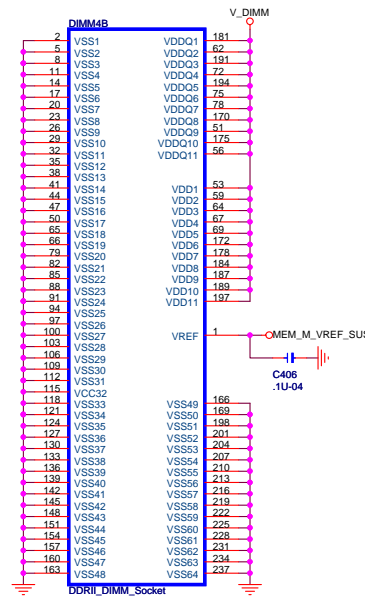
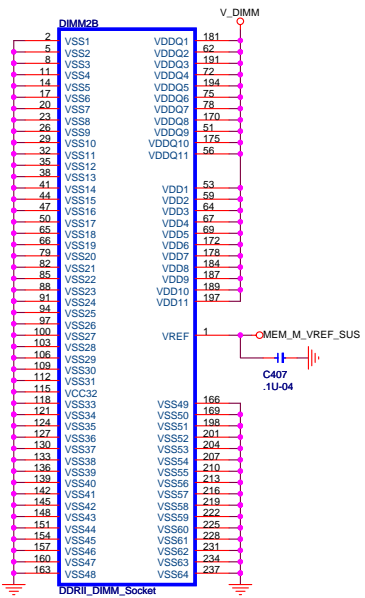
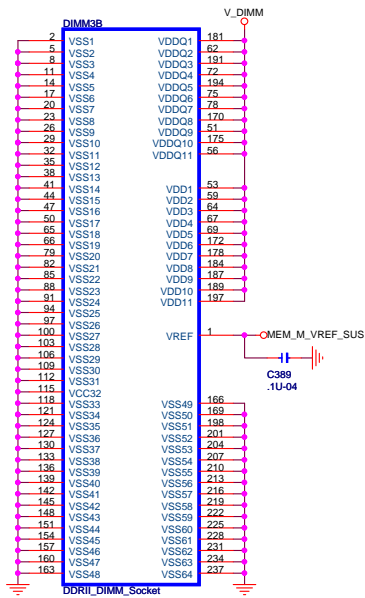
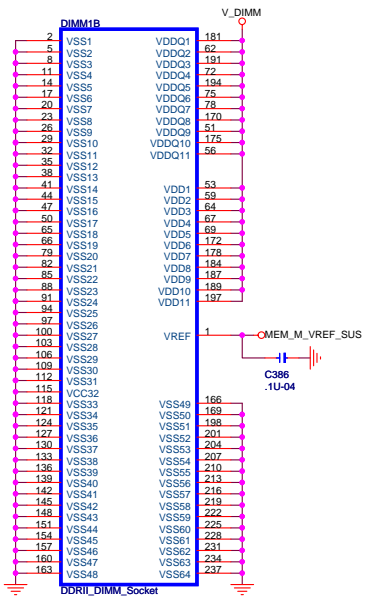


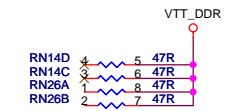
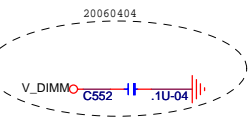
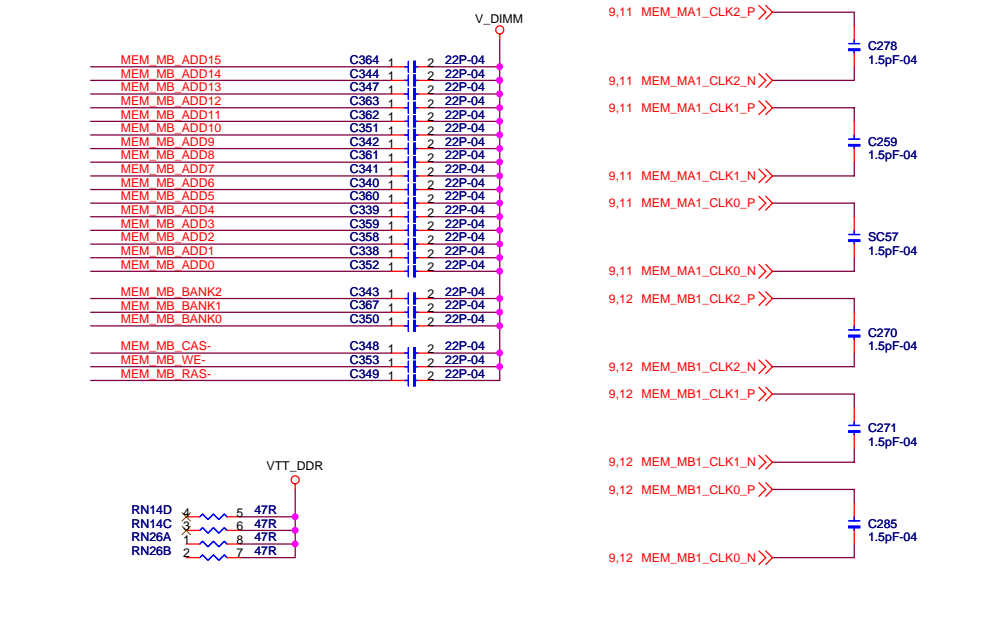
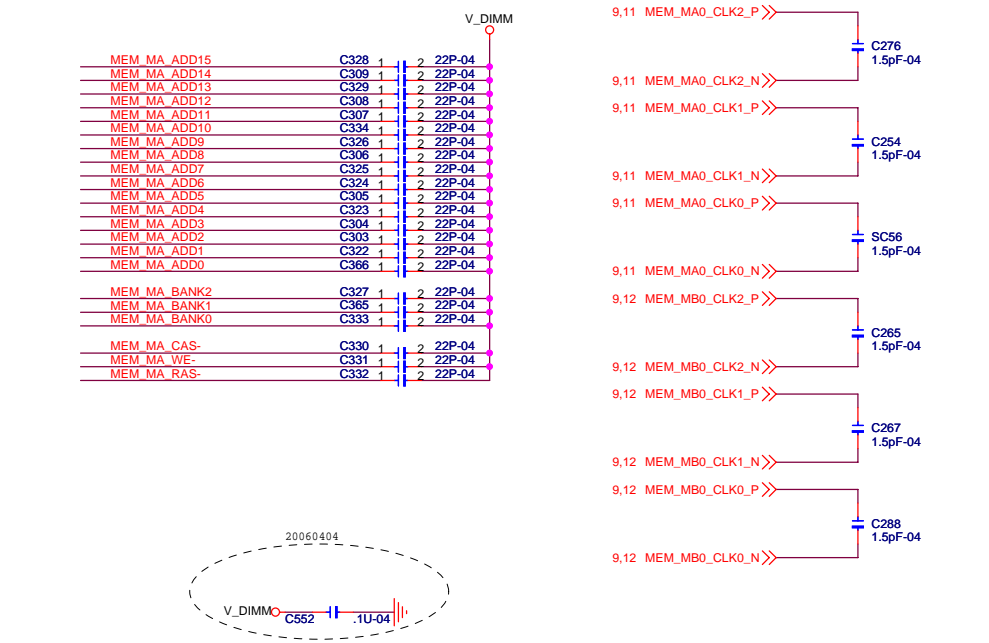
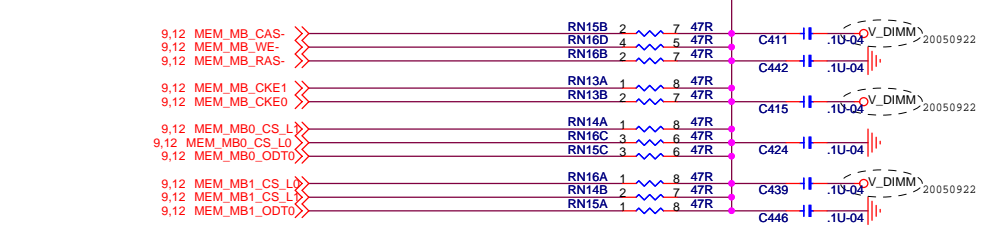
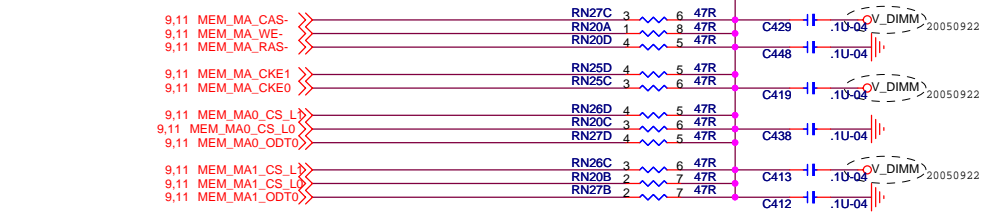
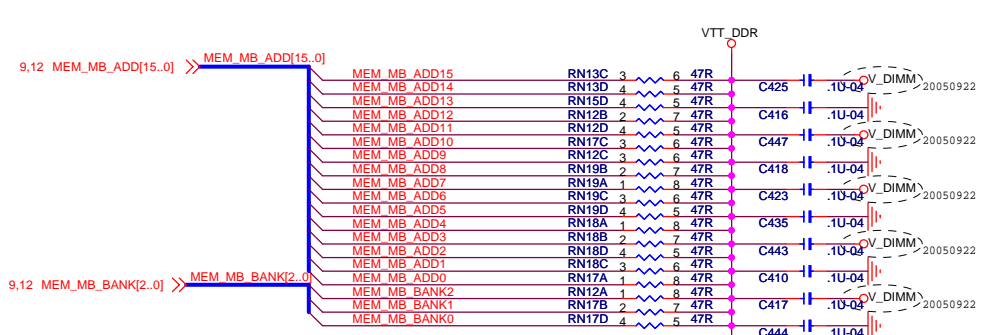
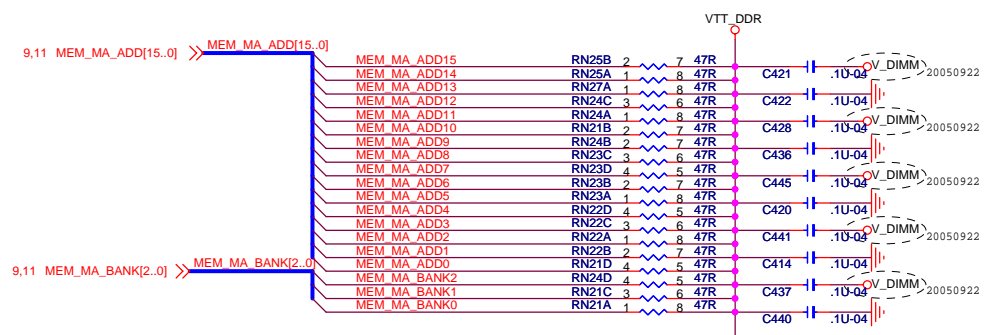


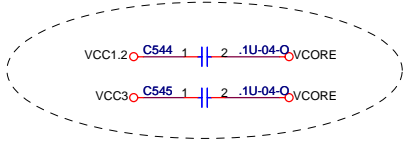
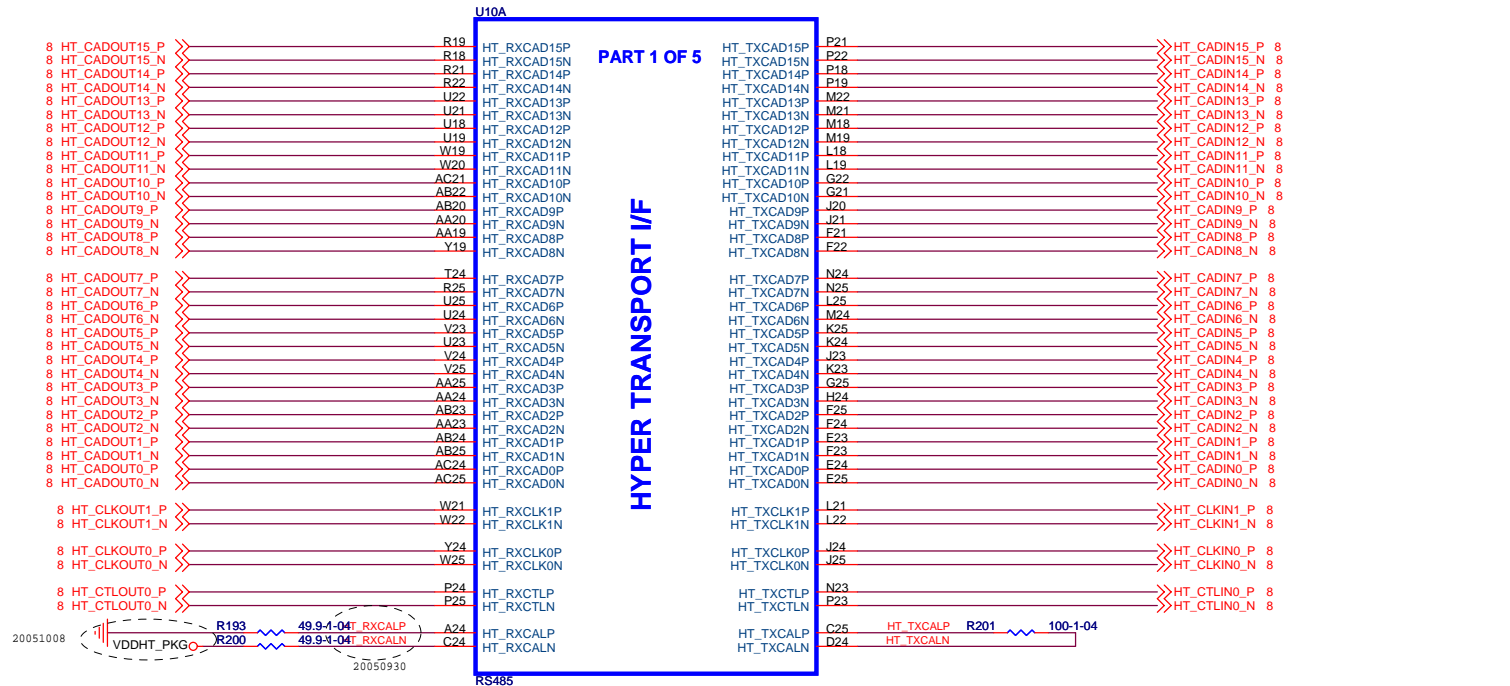
VDD_VREF_SUS_MEM







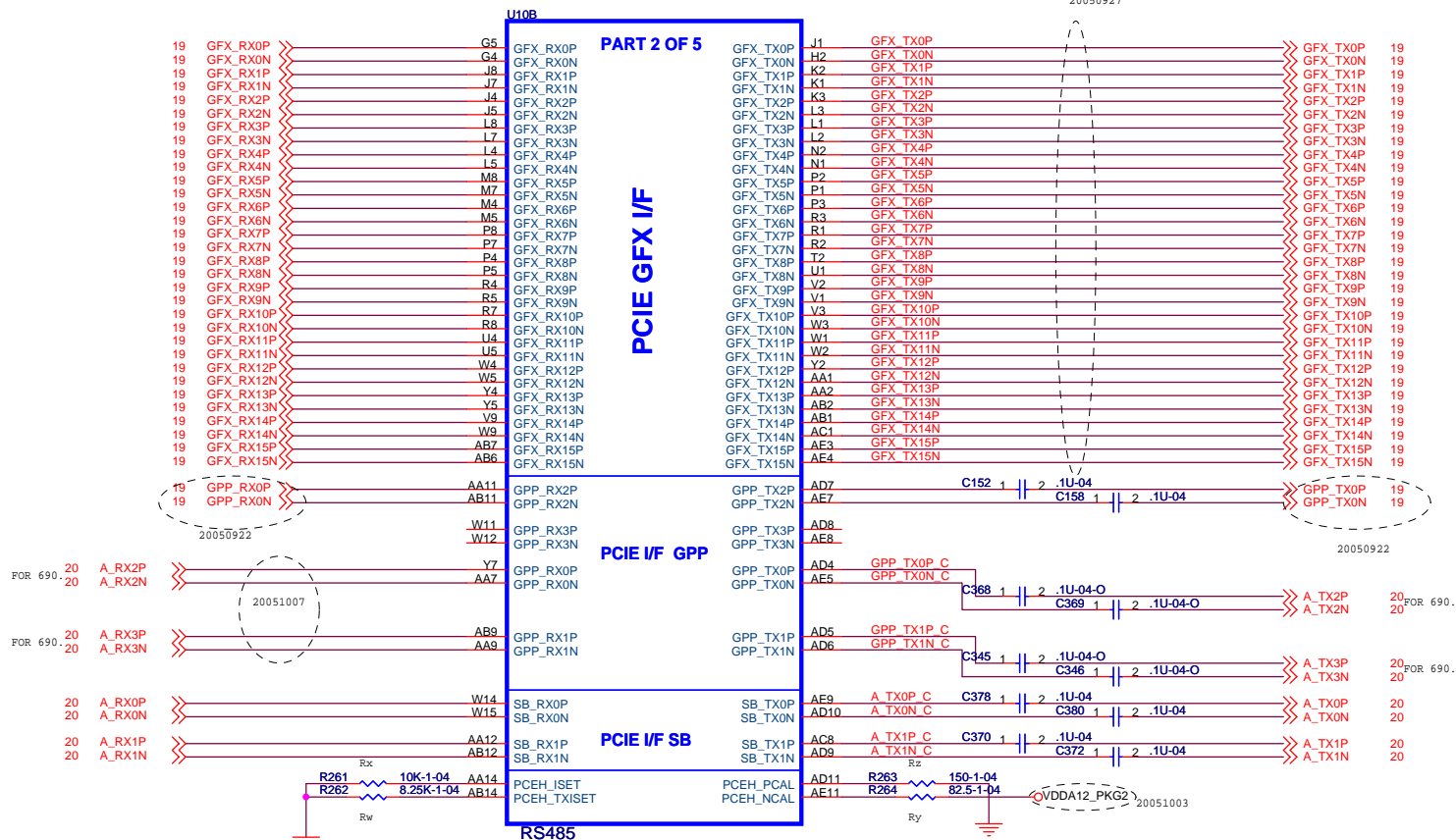




20060303
FOR BMI.



HT link stitching caps



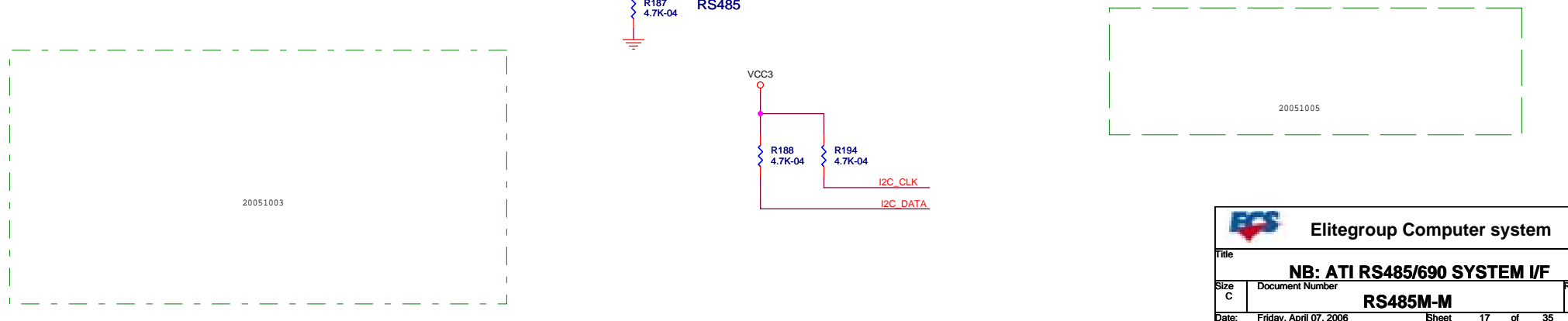
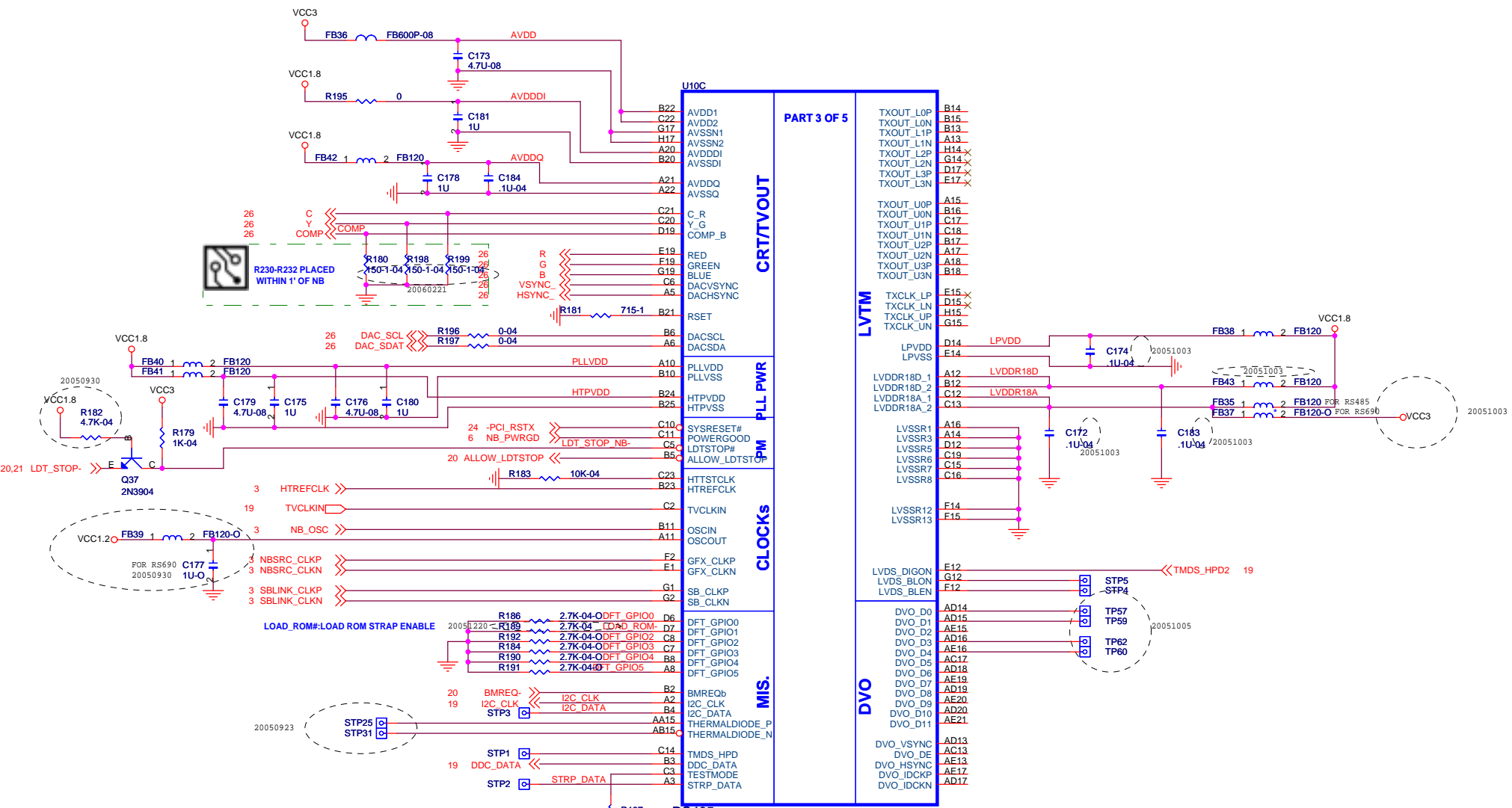
AVIOD STUB
RS690/485 2/4-LANE ALINK CONFIGURATION

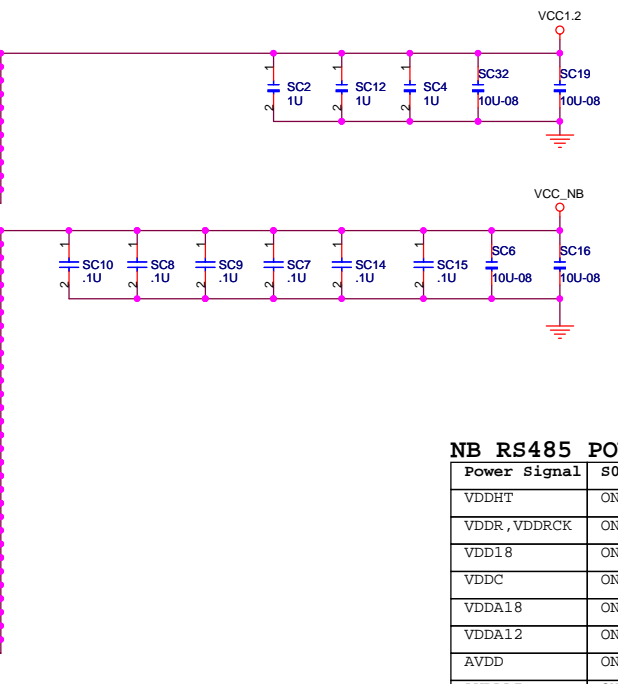
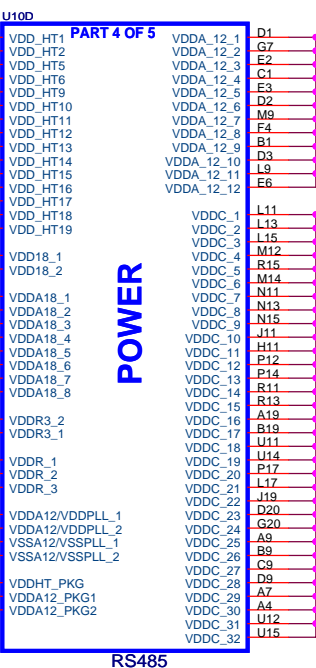
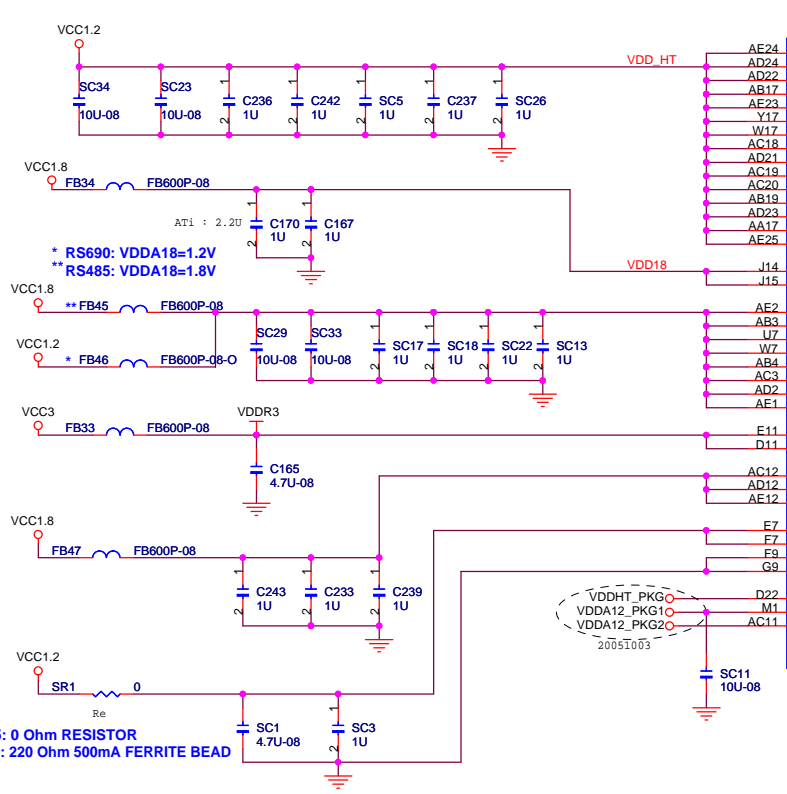
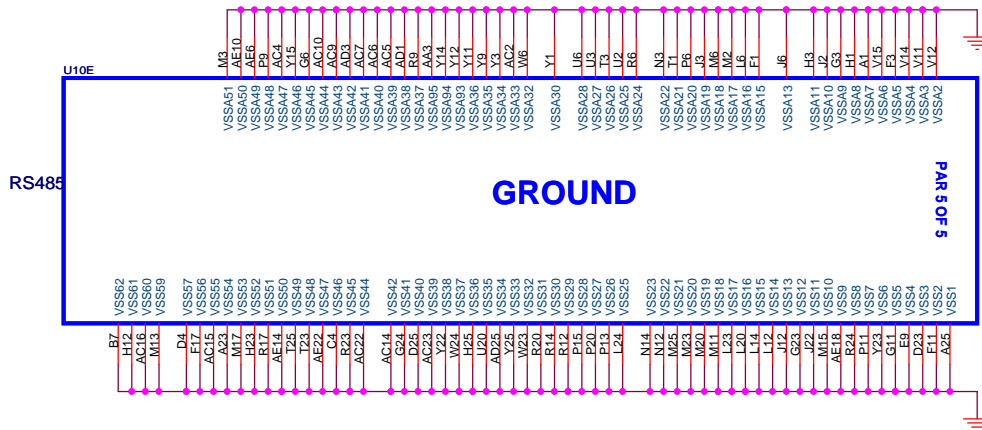


AVIOD STUB
RS690/485 2/4-LANE ALINK CONFIGURATION

RS690/RS485 CHANGE TABLE

NB/DIFF	Rw	Rx	Ry	Rz
RS690	DNI	1.47K	2K	562R
RS485	8.25K	10K	82.5R	150R





NB RS485 POWER STATES

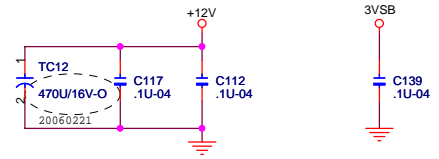
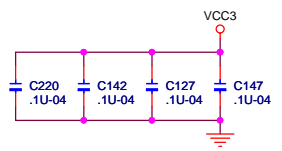
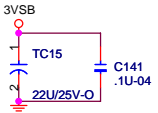
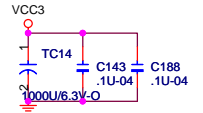
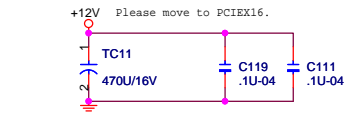
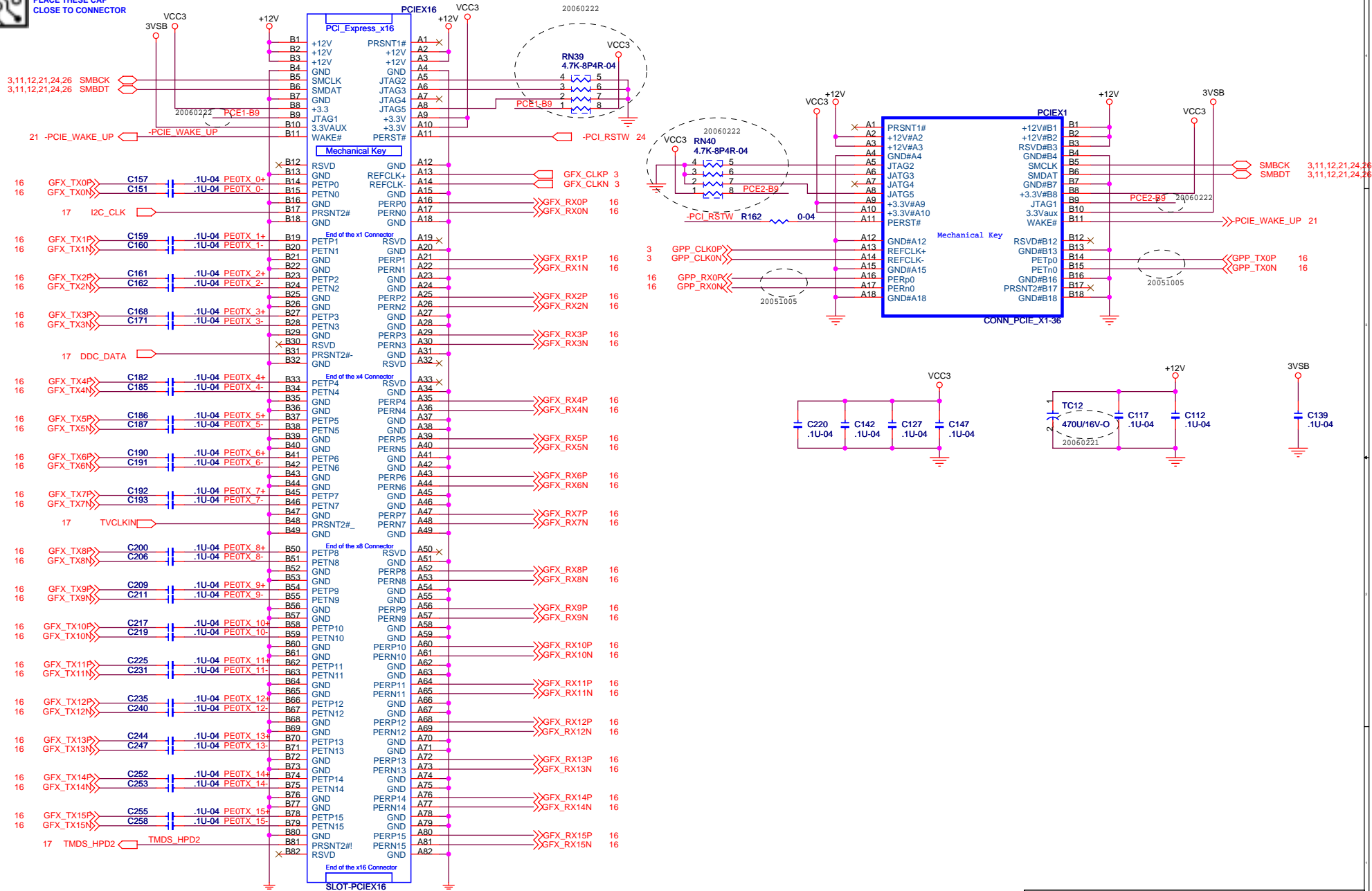
Power signal	s0	s1	s3	s4/s5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR, VDDRCK	ON	ON	ON	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF


PCI_EXPRESS_x16

+12V : 5 . 5Amp

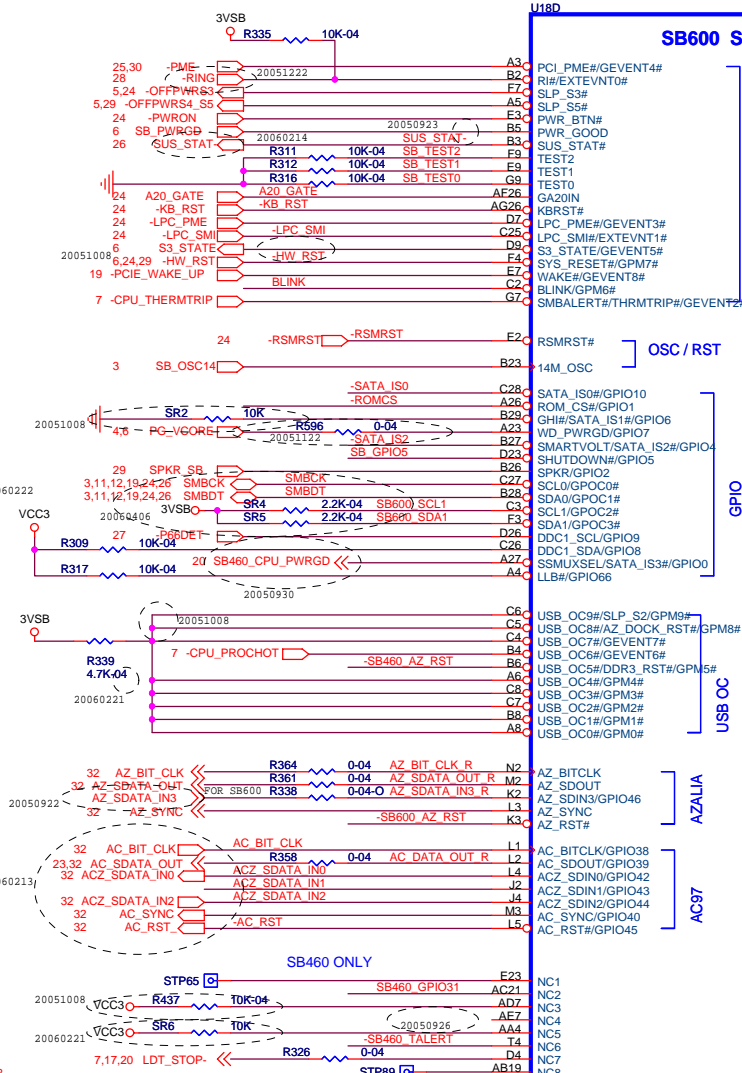
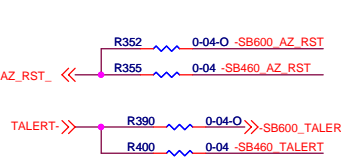
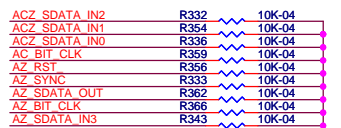
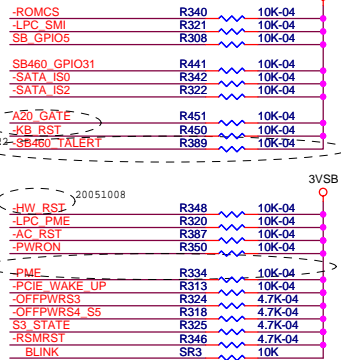


PLACE THESE CAP
CLOSE TO CONNECTOR

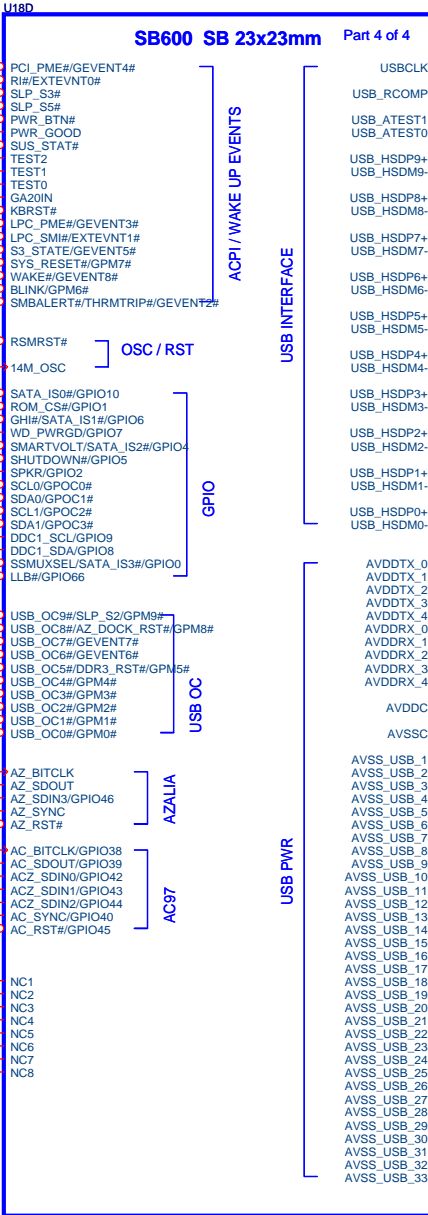


 Elitegroup Computer system		
Title PCI EXPRESS x16 SLOTS		
Size C	Document Number RS485M-M	Rev 1.0
Date:	Friday, April 07, 2006	Sheet 19 of 35

SB460 ONLY



FOR SB460, DPLSLP_OD#/GPIO37 TO NC4



ACPI / WAKE UP EVENTS

OSC / RST

GPIO

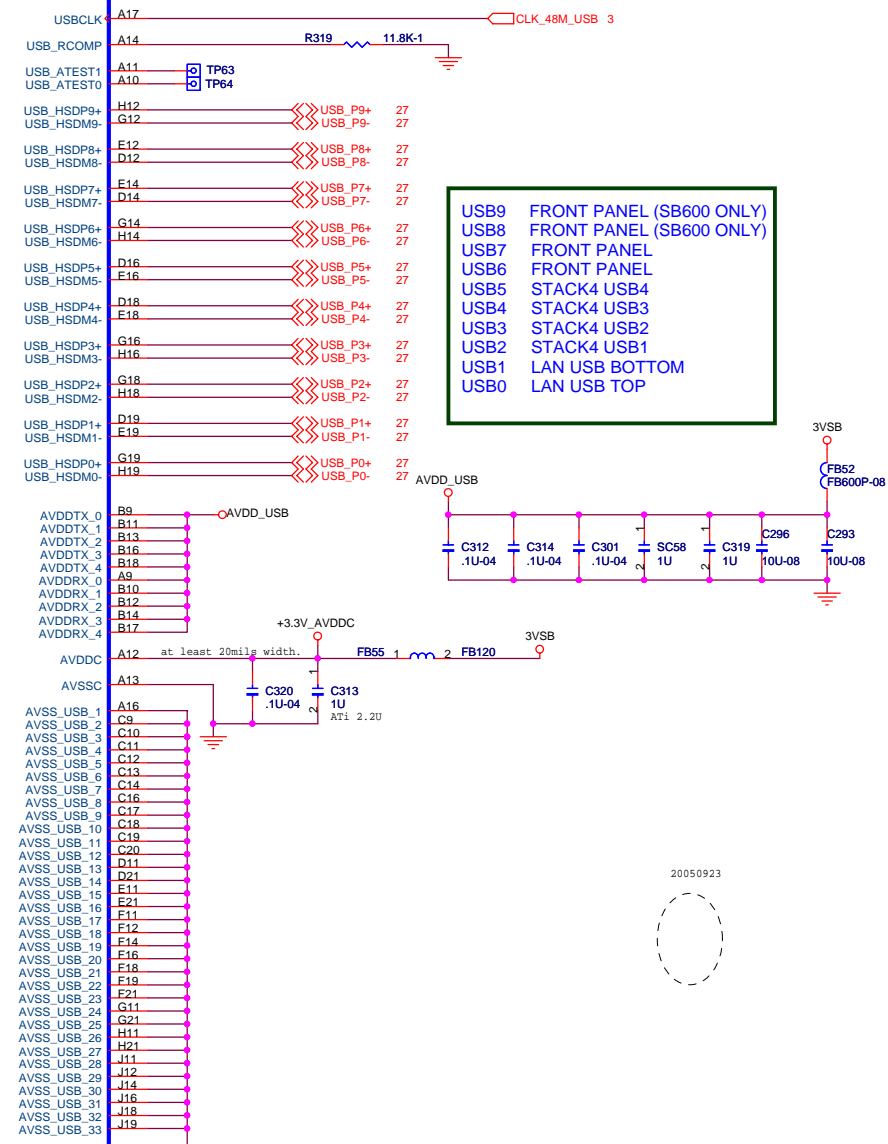
USB OC

AZALIA

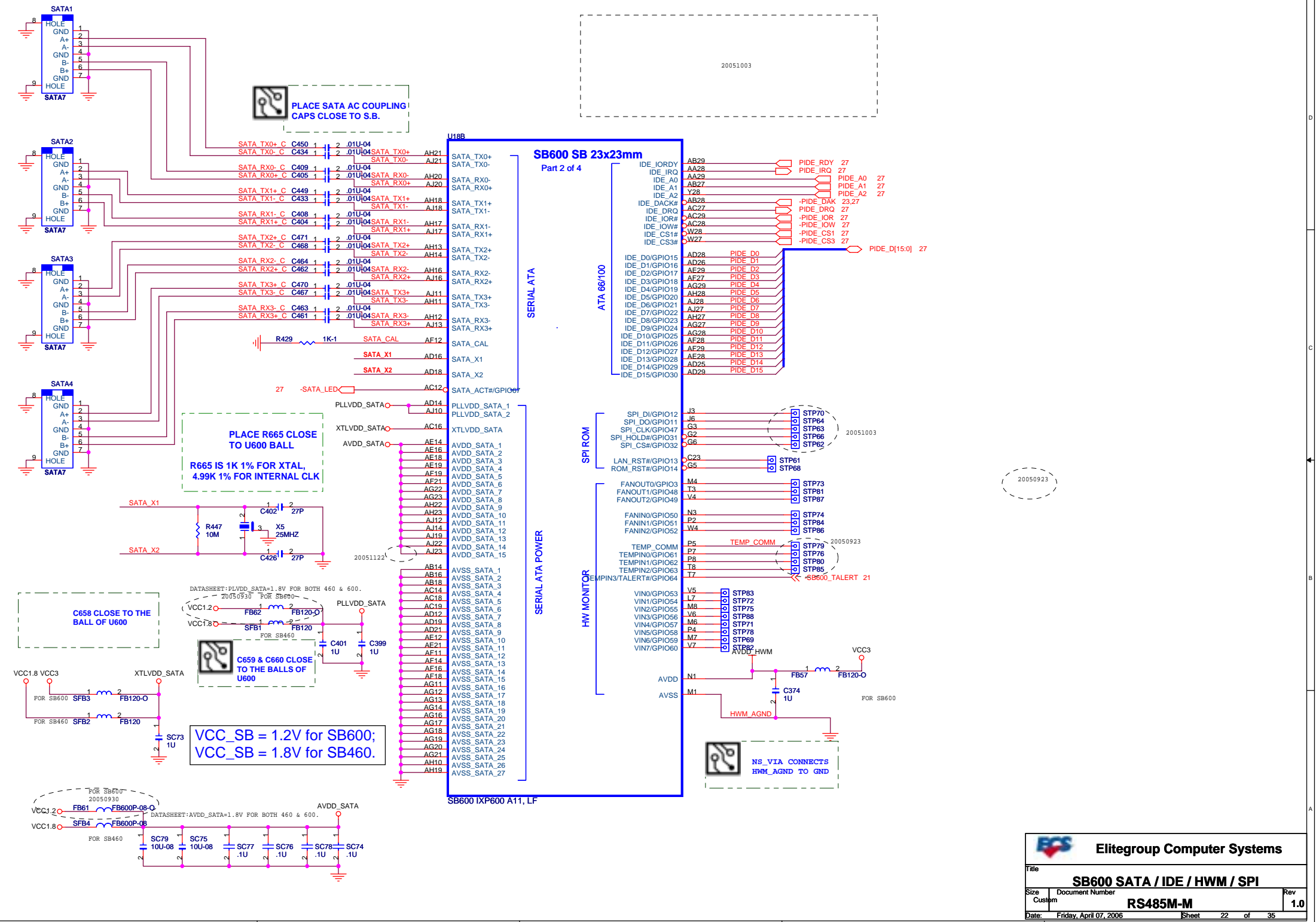
AC97

USB INTERFACE

USB PWR

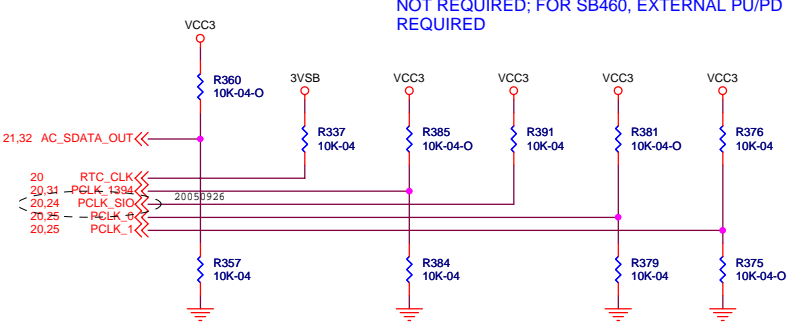


USB9 FRONT PANEL (SB600 ONLY)
 USB8 FRONT PANEL (SB600 ONLY)
 USB7 FRONT PANEL
 USB6 STACK4 USB4
 USB4 STACK4 USB3
 USB3 STACK4 USB2
 USB2 STACK4 USB1
 USB1 LAN USB BOTTOM
 USB0 LAN USB TOP



REQUIRED STRAPS

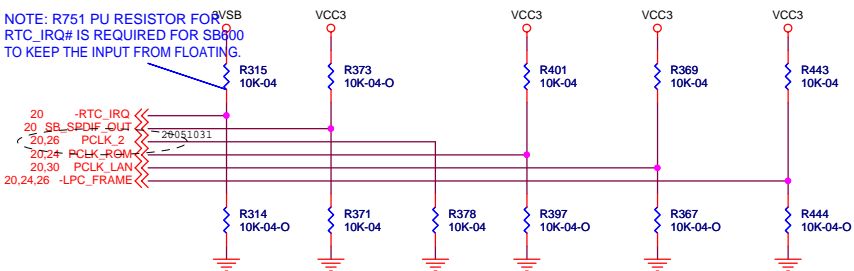
SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT, 15K PU FOR RTC_CLK, EXTERNAL PU/PD IS NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE REQUIRED



		SB600				SB460	
		AC_SDOUT	RTC_CLK	PCI_CLK4 (PCLK_1394)	PCI_CLK6 (PCLK_SIO)	PCI_CLK0 (PCLK_0)	PCI_CLK1 (PCLK_1)
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC II ROM L, L = FWH ROM	ROM TYPE: H, H = PCI ROM H, L = LPC II ROM L, H = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	DEFAULT	NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]	DEFAULT

ADDITIONAL SB460 STRAPS

NOTE: R751 PU RESISTOR FOR RTC_IRQ# IS REQUIRED FOR SB600 TO KEEP THE INPUT FROM FLOATING.

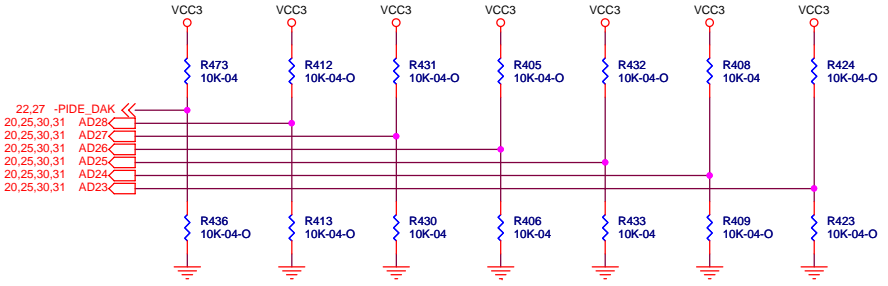


		ACPWRON (RTC_IRQ)	SPDIF_OUT	PCI_CLK2 (PCLK_2)	PCI_CLK3 (PCLK_ROM)	PCI_CLK5 (PCLK_LAN)	LFRAME# (-LPC_FRAME#)
PULL HIGH	MANUAL PWR ON	SIO 24MHz	XTAL MODE	USB PHY POWERDOWN DISABLE	PCIE_CM_SET LOW	ENABLE THERMTRIP#	
PULL LOW	AUTO PWR ON	SIO 48MHz	48MHZ OSC MODE	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#	

SB460 ONLY SB460 ONLY SB460 ONLY SB460 ONLY SB460 ONLY SB460 ONLY

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

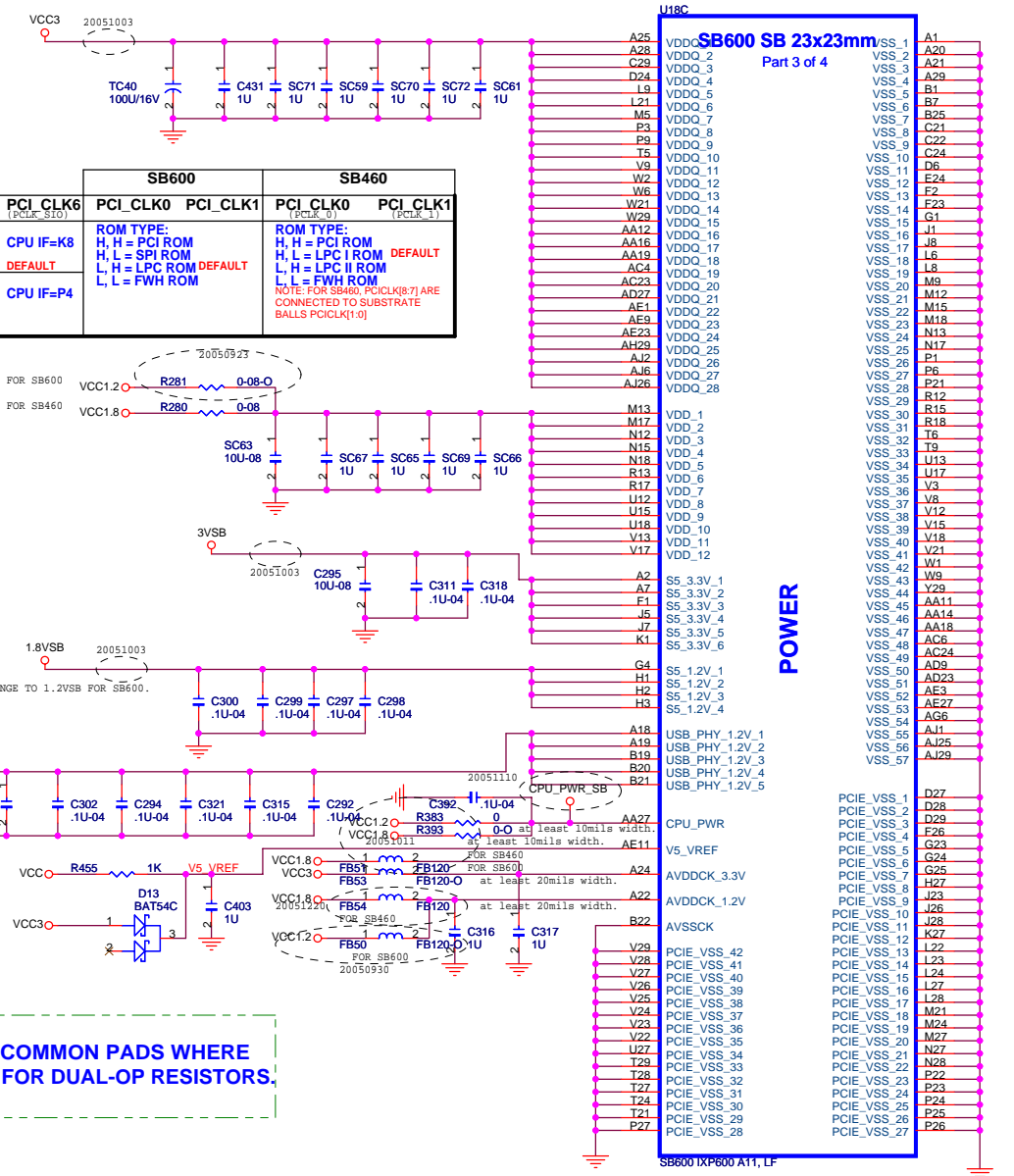


		IDE_DACK# (-PIDE_DAK)	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCI STRAPS	BOOTFAILTIMER DISABLED	
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCI STRAPS	BOOTFAILTIMER ENABLED	

SB460 ONLY SB600 ONLY

2.2K IF USED FOR SB600.
10K IF USED FOR SB460.

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

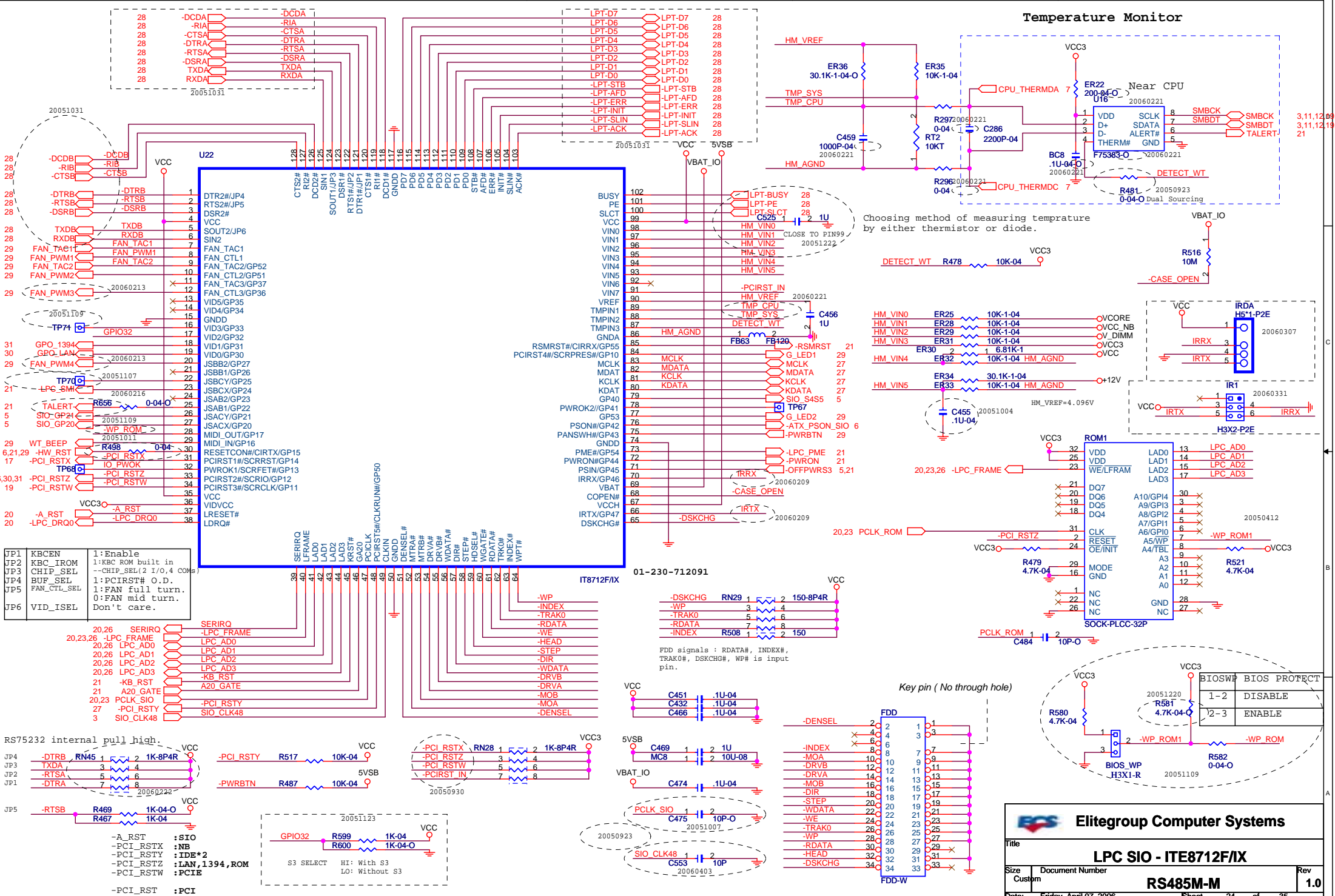


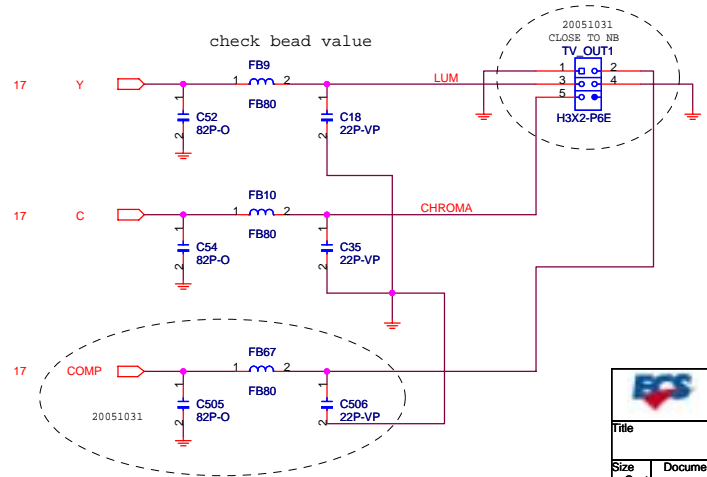
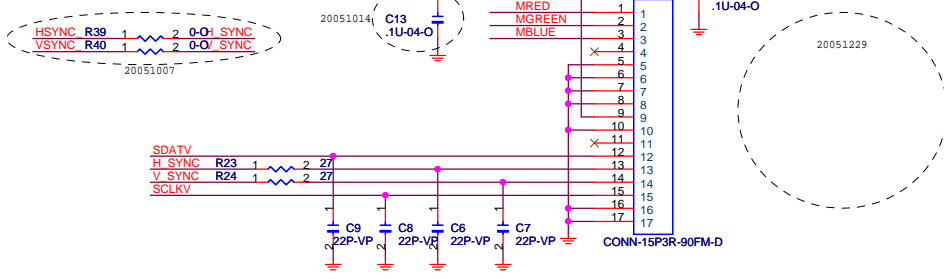
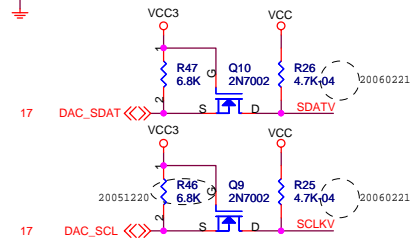
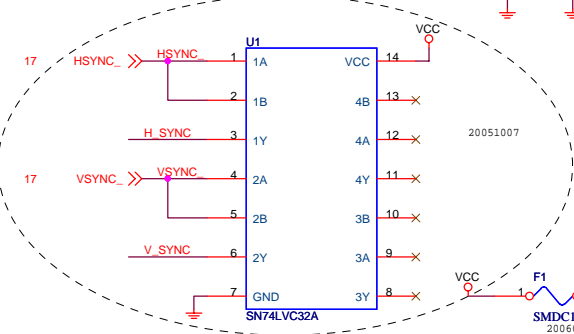
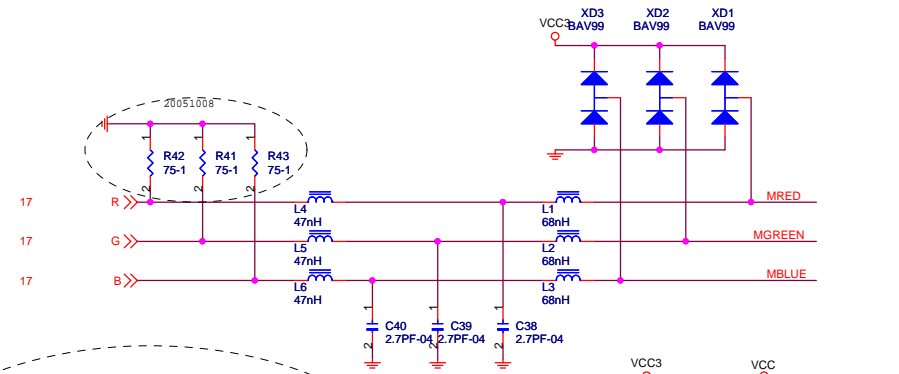
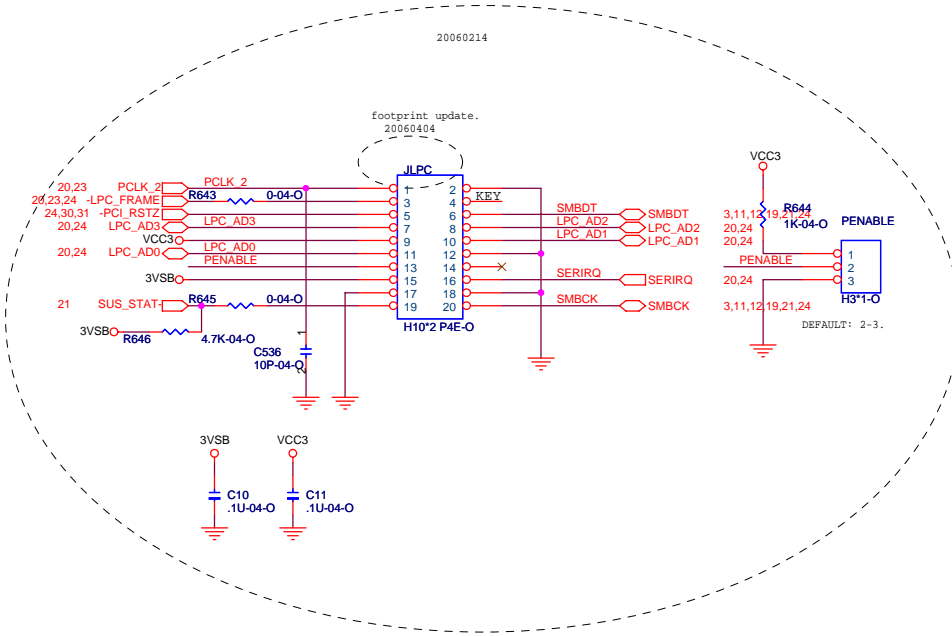
Elitegroup Computer Systems

Title: **SB600 STRAPS/ PWR/ DECOUPLING**

Size: Document Number **RS485M-M** Rev **1.0**

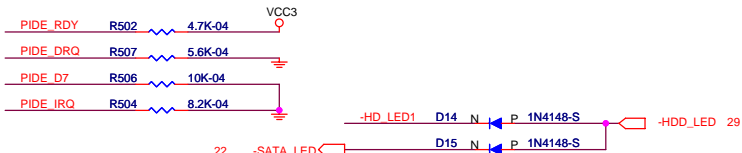
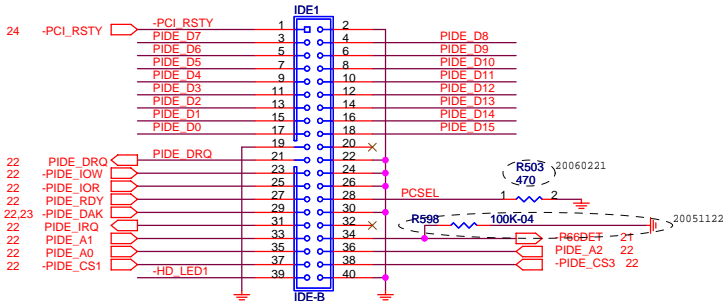
Date: Friday, April 07, 2006 Sheet 23 of 35



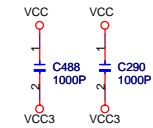
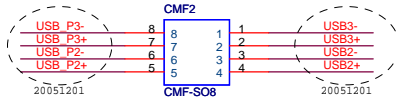
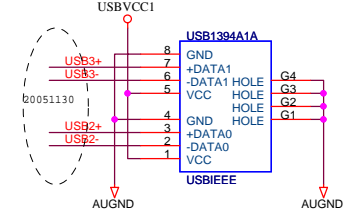
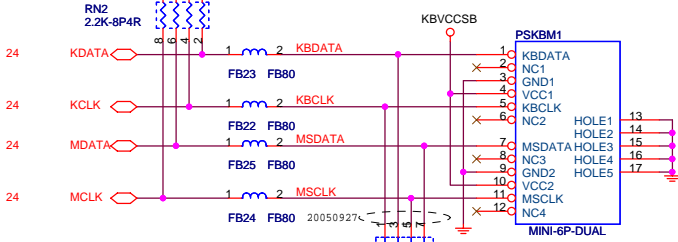
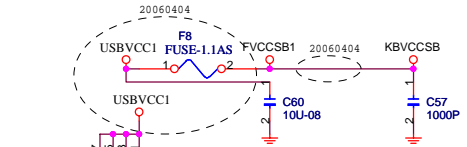
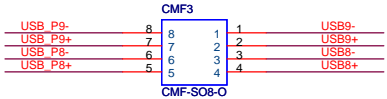
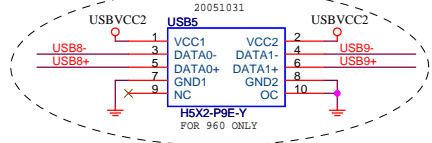
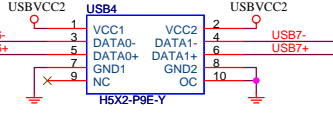
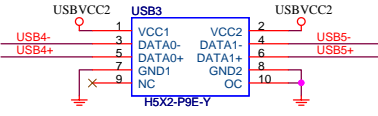
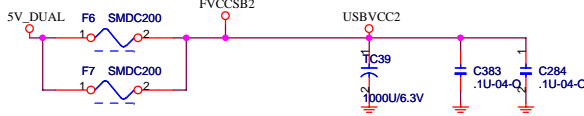
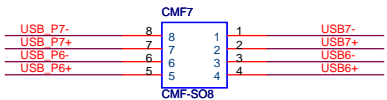
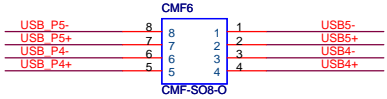
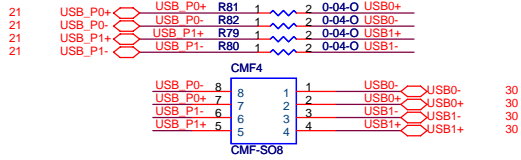
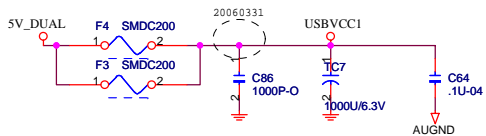


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Title	VGA	
Size	Document Number	Rev
Custom	RS485M-M	1.0
Date:	Friday, April 07, 2006	Sheet 26 of 35

22 PIDE_D[15:0]



USB 0-1



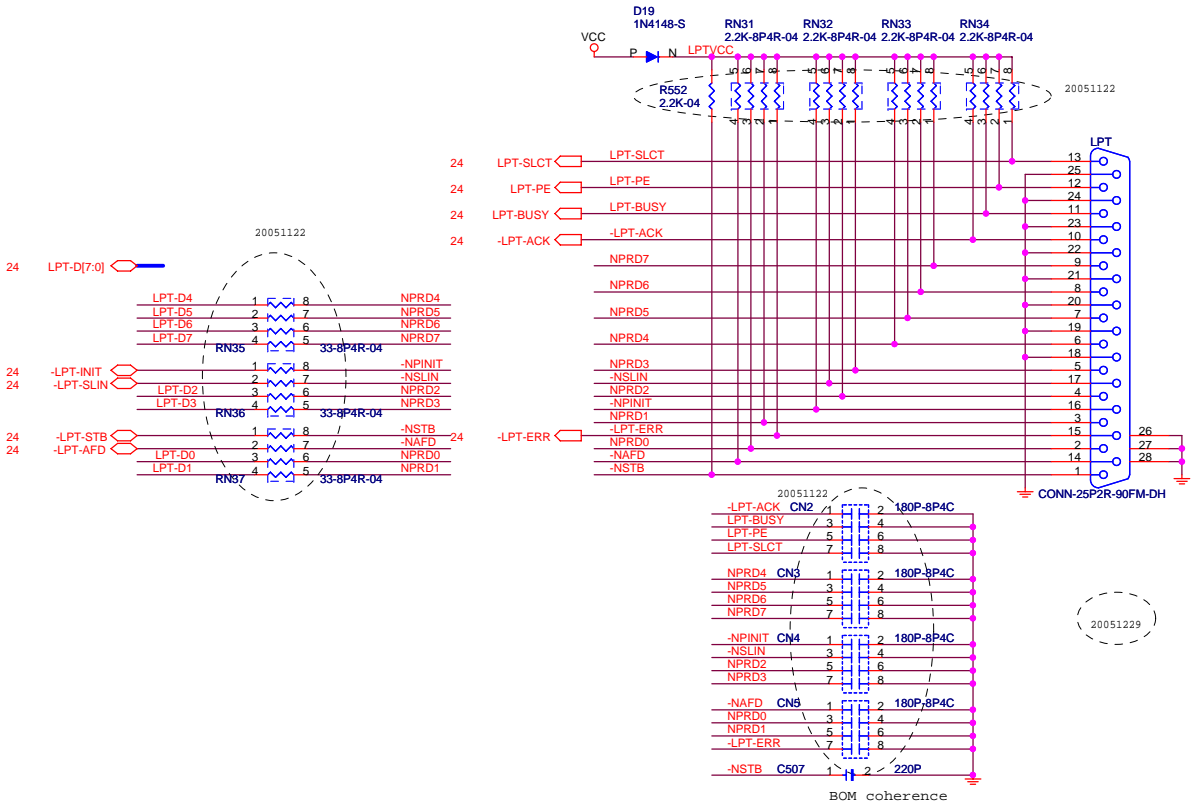
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Title: **USB, IDE**

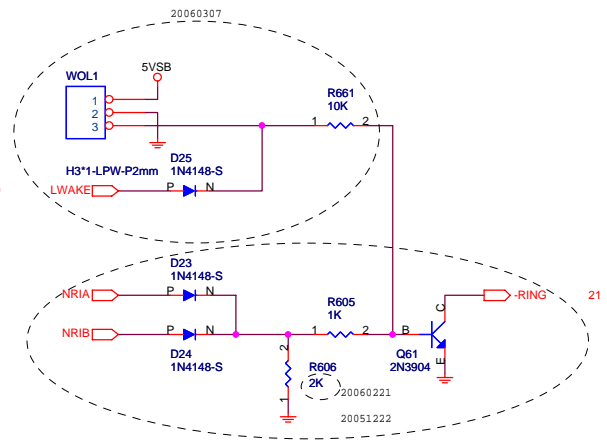
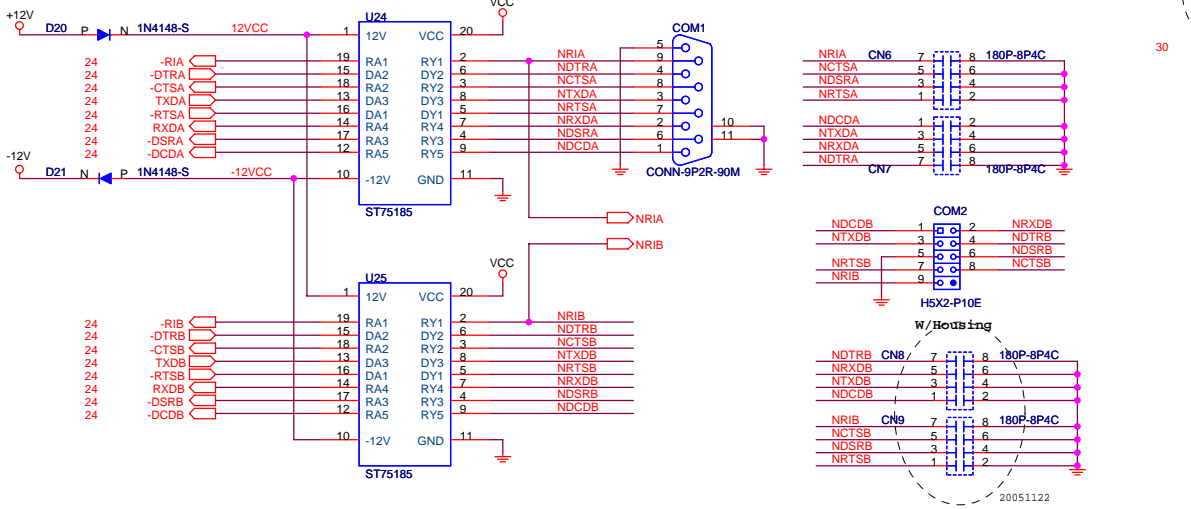
Size: Custom Document Number: **RS485M-M** Rev: **1.0**

Date: Friday, April 07, 2006 Sheet: 27 of 35

LPT



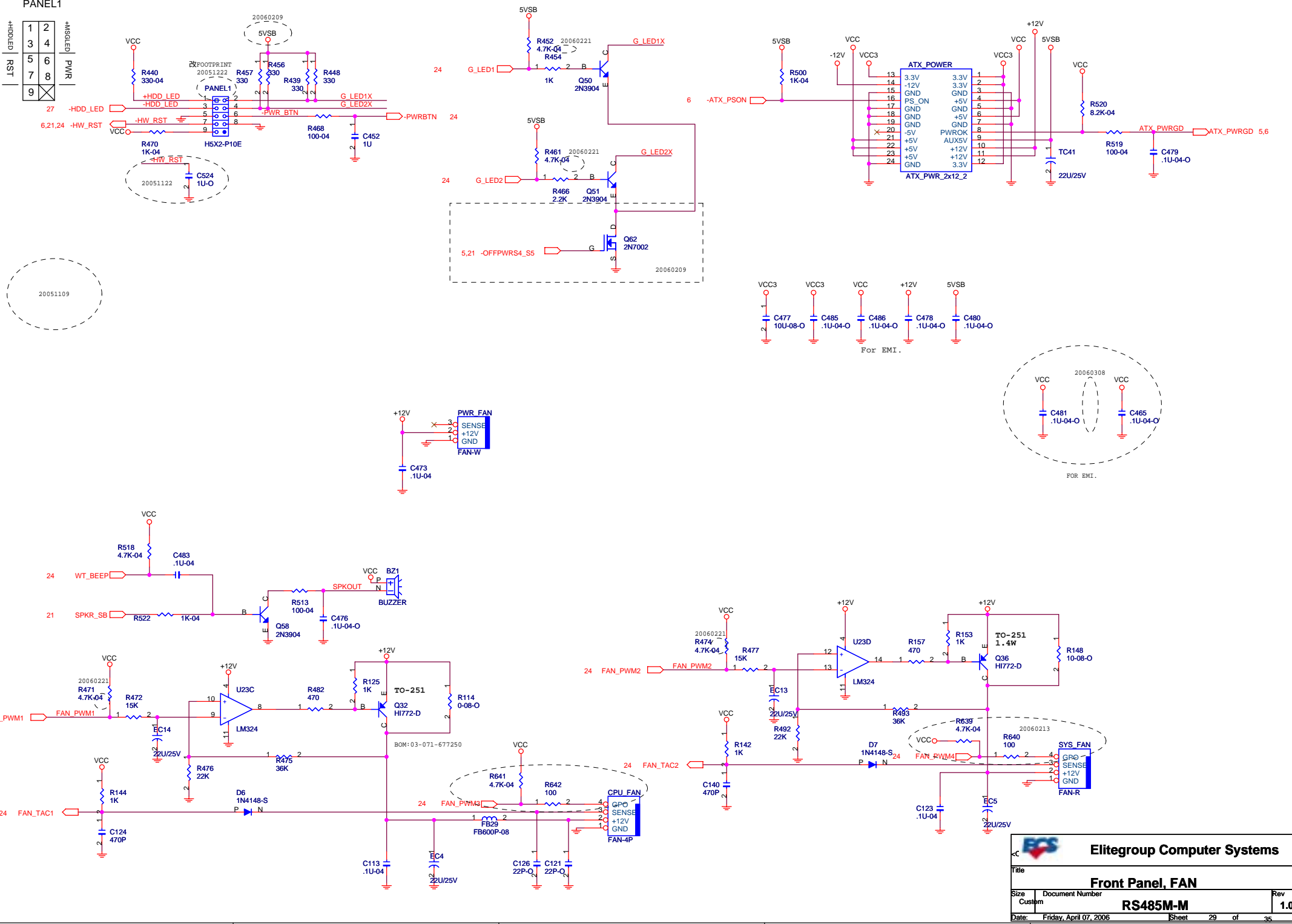
COM 1



Elitegroup Computer Systems		
COM, LPT		
Title	COM, LPT	
Size	Document Number	Rev
Custom	RS485M-M	1.0
Date:	Friday, April 07, 2006	Sheet 28 of 35

PANEL1

1	2	+HSD_LED
3	4	
5	6	PWR
7	8	
9	9	RST

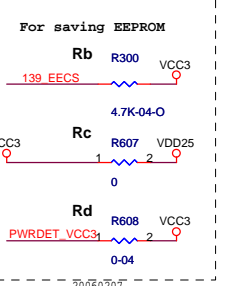


Elitegroup Computer Systems		
Front Panel, FAN		
Title	Document Number	Rev
Size	Custom	1.0
RS485M-M		
Date:	Friday, April 07, 2006	Sheet 29 of 35

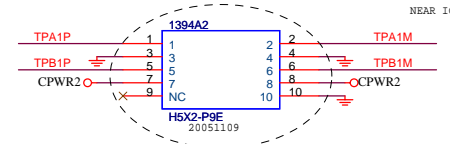
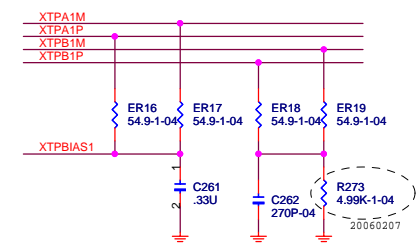
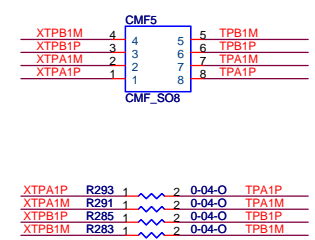
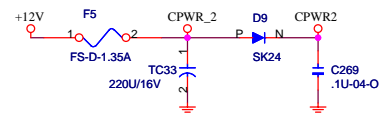
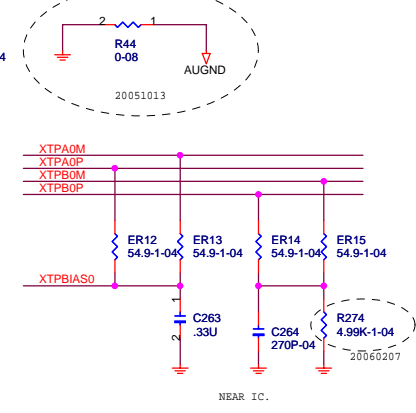
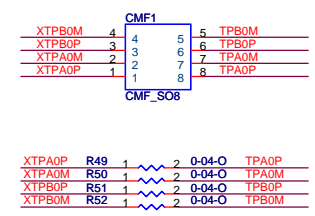
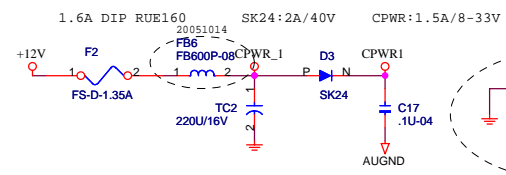
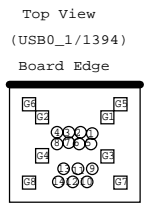
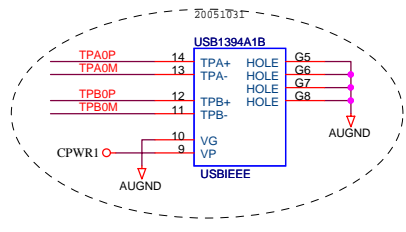
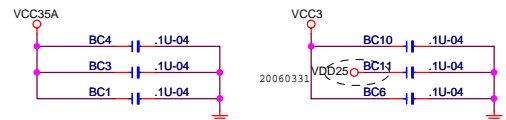
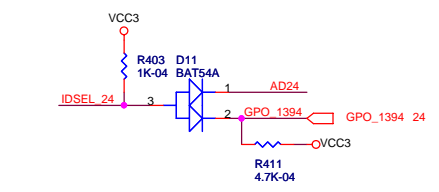
Bandgap Resistor	Ra
VT6307	6.34K-1
VT6308P	6.2K-1

BJT_SEL	Internal MOS turn on
0(default)	Use external BJT
1	

Power Pin		
Pin	VT6307	VT6308P
84	NC	BJT_CTL
87	NC	REG_FB
88	NC	REG_OUT
35	VCC	PWRDET
38	VCC	VCC
49	PVD	VDD
24	VCC	VDD
114	VCC	VDD
33	VCC	VDD



1394 CHIP (Ua)	EEPROM LESS M/B only(Rb)	EEPROM (Ub)	VDD25 Power (Rc)	PWRDET_VCC3 (Rd)
* VT6307	NC(WHQL fail)	ON	ON	0 ohm
VT6308P	ON	NC	NC	4.7K



1394a:100/200/400 Mbit/sec
Impedance: Diff = 110 Ohm
Single=55 Ohm

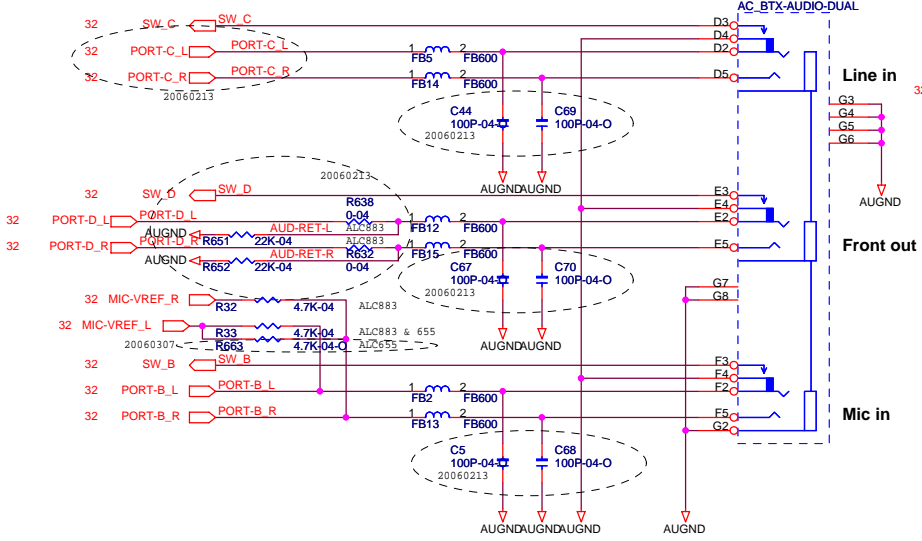
Elitegroup Computer Systems

Title: **1394a (VT6307/6308P)**

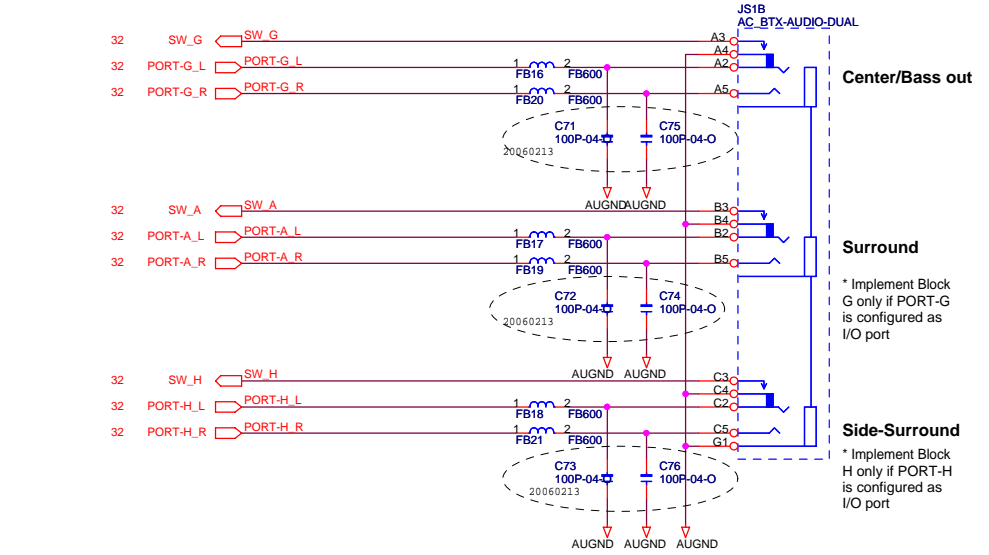
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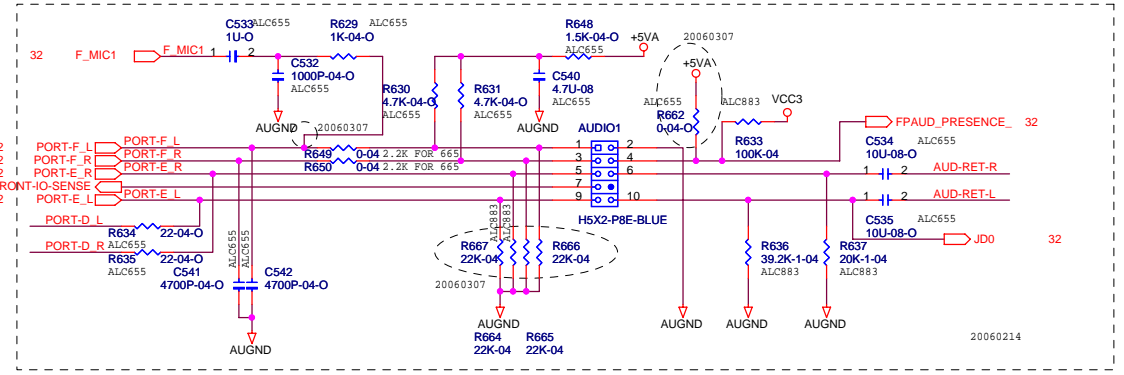
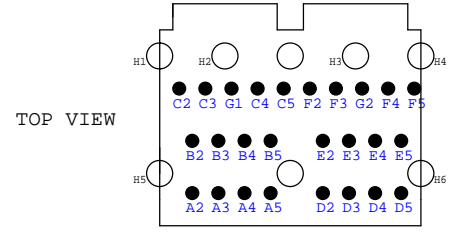
Rear Panel Onboard Analog I/O



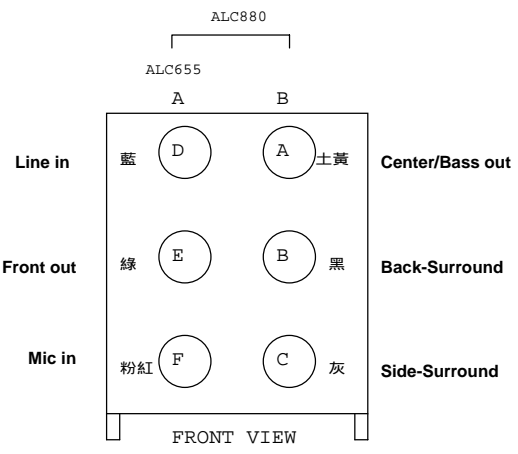
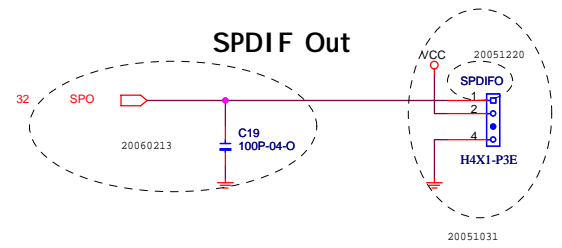
Rear Panel (Optional Rear Audio Panel)



The schematic should consist with PINS define of I/O connector.



SPDIF Out



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AUDIO AL655/C883 (PANEL)

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ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

CPU PW
12V
+/-5%

VRM SW REGULATOR

VDD_CPUCORE_RUN (S0, S1)

1.2V LINEAR REGULATOR

VDDHT_1V2 (S0, S1)

VCC 1.2V SW REGULATOR

VCC_NB (S0, S1)

2.5V LINEAR REGULATOR

AVDD(S0, S1)

1.8V SW REGULATOR

+1.8V(S0, S1)

2.5V SHUNT REGULATOR

VDDA_2.5_RUN (S0, S1)

2.5V SHUNT REGULATOR

VDD_2.5_RUN (S0, S1)

1.8V VDD SW REGULATOR

VTT_DDR_SUS (S0,S1,S3)

0.9V VTT_DDR REGULATOR

+3.3VSB REGULATOR
ACPI CONTROLLER

+5VDUAL_MEM (S0, S1, S3, S4, S5)

1.8V STB LDO REGULATOR

+1.8VSB (S0, S1, S3, S4, S5)

SVAA LDO REGULATOR

+5VAA (S0, S1,S3)

GBE	
3.3V 0.5A (S0, S1)	
3.3V 0.1A (S3)	

SATA	
3.3V 0.3A (S0, S1)	

SUPER I/O	
+5V SD 0.01A	
+5V 0.1A	

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3Vaux	0.375A
-12V	0.1A

X1 PCIE per	
3.3V	3.0A
12V	0.5A
3.3Vaux	0.1A

X16 PCIE	
3.3V	3.0A
12V	5.5A

CNR CONNECTOR	
5V	1.0A
3.3V	1.0A
12V	0.5A
3.3Vaux	1.0A
-12V	0.1A
5VDual	0.5A

USB X4 FR	
VDD	
5VDual	2.0A

USB X6 RL	
VDD	
5VDual	2.0A

2XPS/2	
5VDual	1.0A

VDDA_2.5_RUN (S0, S1)

VTT_DDR_SUS (S0,S1,S3)

VDD_2.5_SUS(S0,S1,S3)

M2	
VDDA 2.5V 0.1A	
VDDCORE 0.8-1.55V 80A	
DDRII MEM I/F VTT 0.125A, VDD 3A	
VLDT 1.2V 0.5A	

RS485/RS690	
VDDHT 1.2V 0.5A	
PCI-E CORE &VCO 2.25A	
NB CORE VDDC 1.0-1.2V 5A	
DAC 200mA LVDS 1.8V 300mA	
PLL & DAC-Q 0.1A	
PCI-E I/O 1500mA	

SB460/SB600	
X4 PCI-E 0.8A	
ATA I/O 0.2A	
ATA PLL 0.01A	
PCI-E PVDD 80mA	
SB CORE 0.6A	
1.8V S5 PW 0.22A	
3.3V S5 PW 0.01A	
USB CORE I/O 0.2A	
3.3V I/O 0.45A	

AC97/AZALIA	
3.3V CORE 0.3A	
5V ANALOG 0.1A	

+3.3VDUAL (S0, S1, S3)

POWER DELIVERY CHART		
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