

MCP61M-M

REV:A

PCB:15-V02-010010
BOM:81-605-V02000

REV:B

PCB:15-V02-010020
BOM:81-605-V02010


v.A --> v.B

01.P31.add R386
02.P31.change dual SW control from GPIO3 to GPIO7
03.P31.add R404

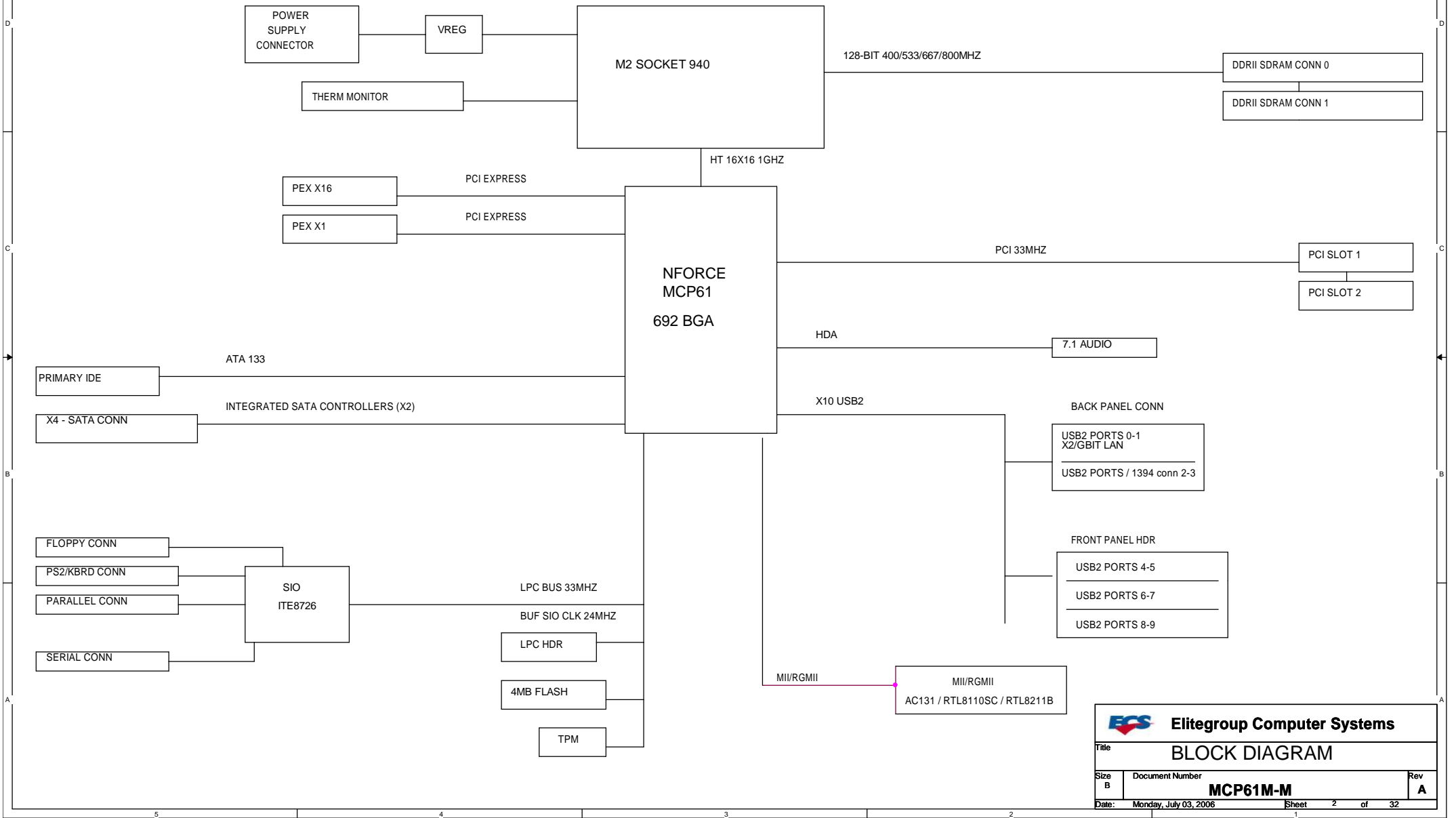
Page Index


01-COVER PAGE
02-BLOCK DIAGRAM
03-BLOCK DISTRIBUTION
04-CPU M2-1 HyperTransport
05-CPU M2-1 DDR2
06-CPU M2-3 Miscellany
07-CPU M2-4 Power and Ground
08-DDR2 DIMM
09-DDR2 Termination
10-MCP61 HT
11-MCP61 PCI-E X16
12-MCP61 PCI-E X1/RGMII/DAC
13-MCP61 PCI
14-MCP61 SATA/IDE
15-MCP61 AUDIO/USB/MISC
16-MCP61 PWR/GND
17-MCP61 DECOUPLING/SPI
18-VGA
19-1394(VT6307/VT6308P)
20-LAN AC131/GIGA RTL8110SC
21-PCI-E X16 CONN
22-PCI1/PCI2
23-PCI-E X1/TPM
24-LPC SIO-ITE8716F/FDD
25-PS2/COM/LPT
26-USB
27-AUDIO ALC861/660
28-AUDIO ALC861/660 (PANEL)
29-PWR CON/FNT PNL
30-CPU VCORE
31-DC-DC
32-ATTENTION

	<i>Signature</i>	<i>Date</i>
<i>Designer</i>	Vincent	05/02/2006
<i>Layout</i>		
<i>Check</i>		
<i>Approval</i>		

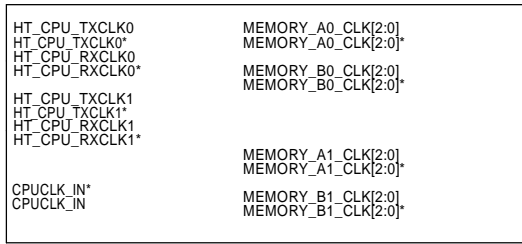
 Elitegroup Computer Systems		
Title: COVER PAGE		
Size: B	Document Number: MCP61M-M	Rev: B
Date: Wednesday, July 05, 2006		
Sheet 1 of 32		

BLOCK DIAGRAM



 Elitegroup Computer Systems		
Title BLOCK DIAGRAM		
Size B	Document Number MCP61M-M	Rev A
Date: Monday, July 03, 2006 Sheet 2 of 32		

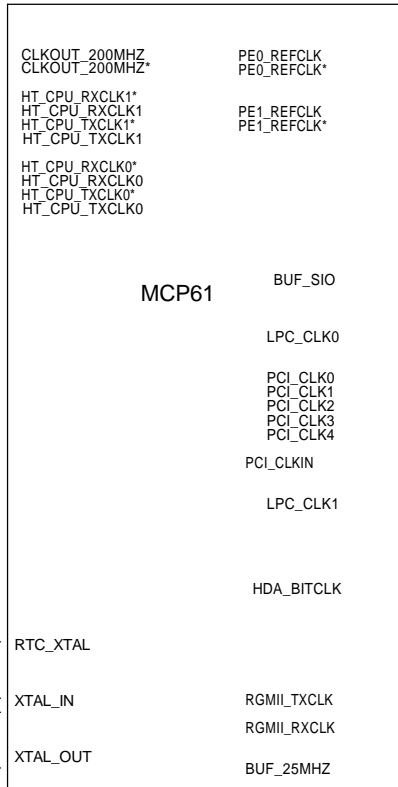
M2 SOCKET 940



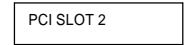
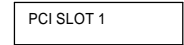
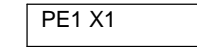
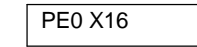
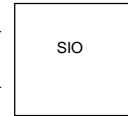
CHANNEL A0 0-63



CHANNEL B0 64-127




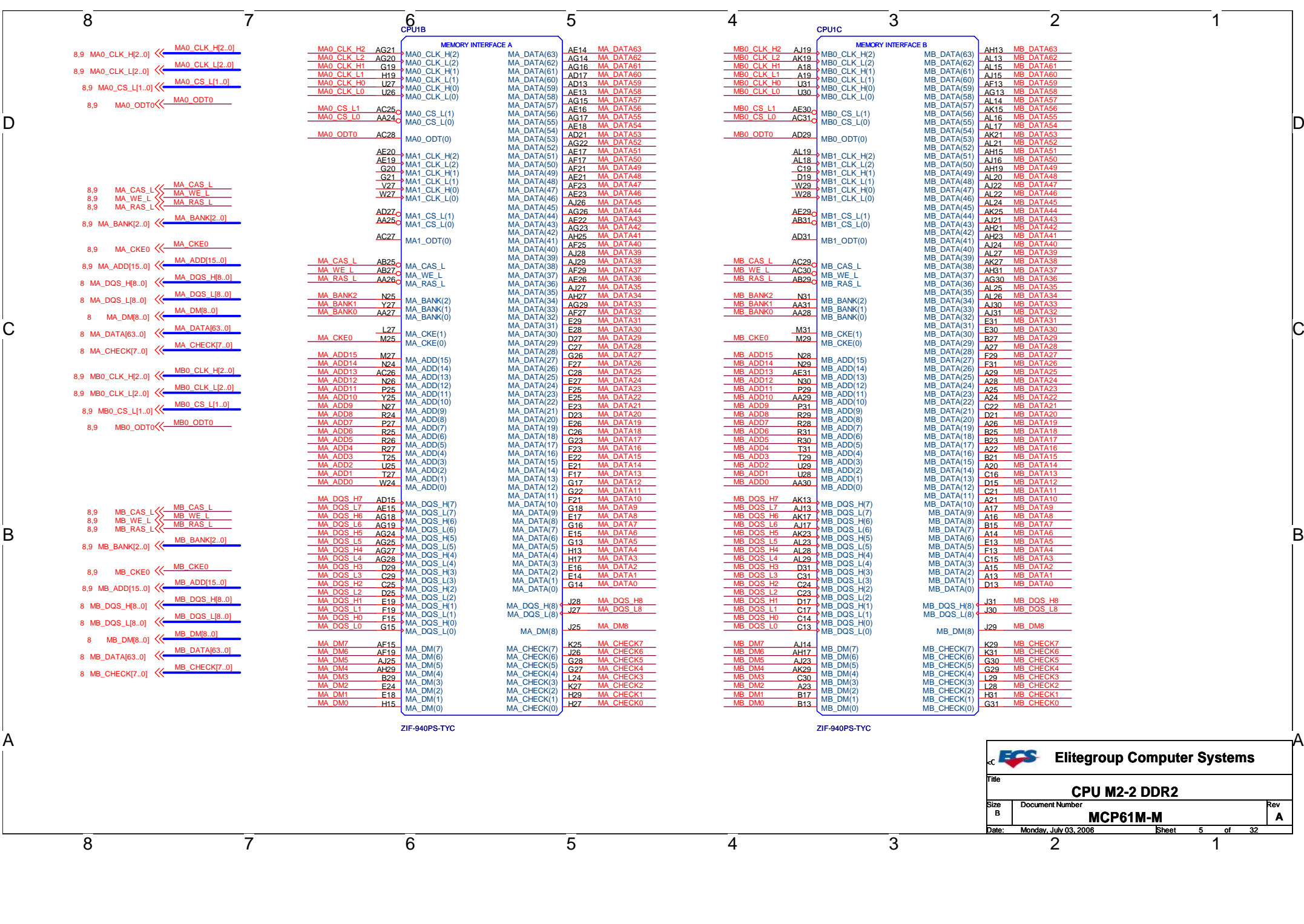
14MHZ OR 24MHZ*




32.0 KHZ

25 MHZ

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Title CLOCK DISTRIBUTION		
Size B	Document Number MCP61M-M	Rev A
Date: Monday, July 03, 2006	Sheet 3	of 32



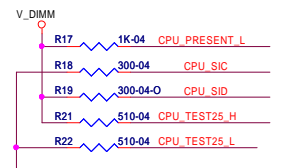
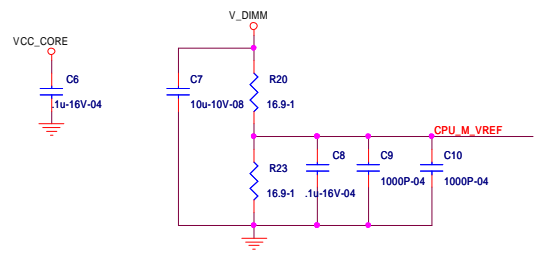
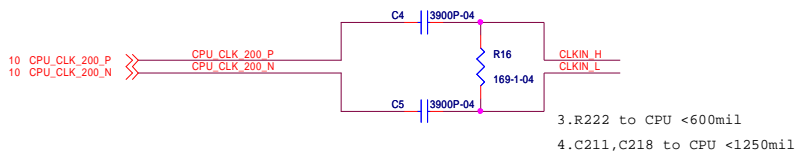
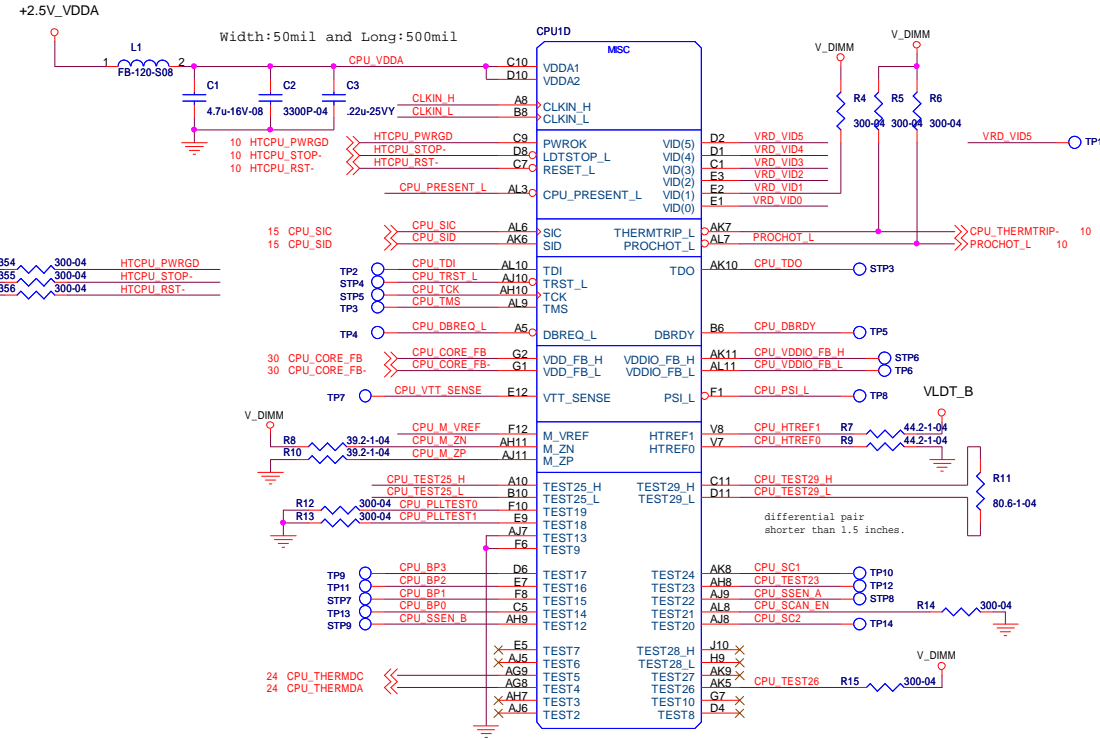
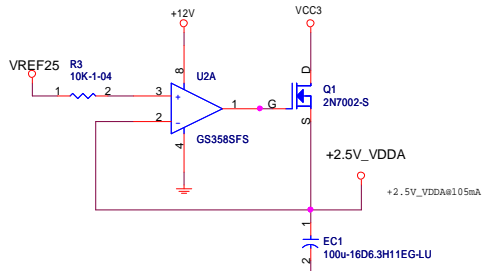
 **Elitegroup Computer Systems**

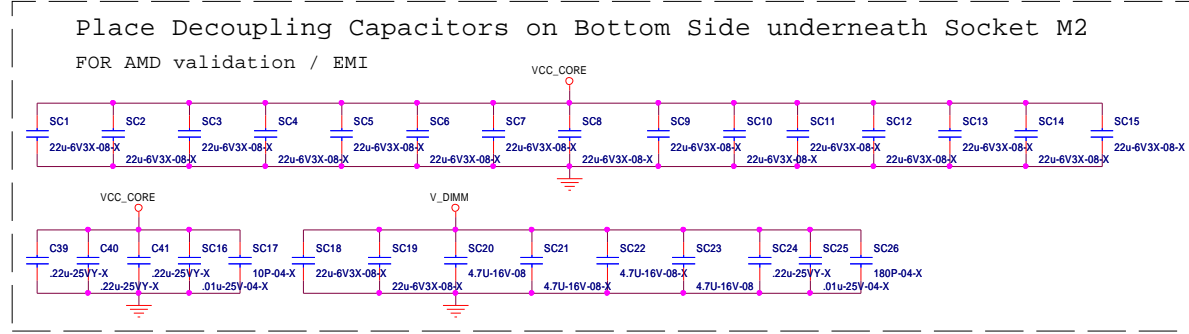
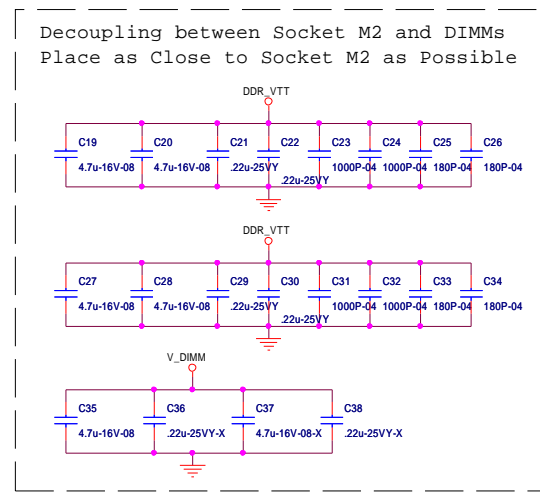
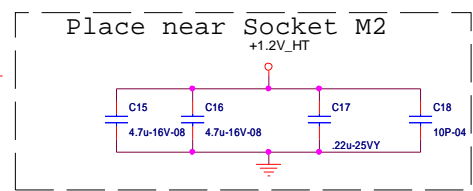
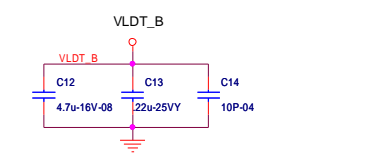
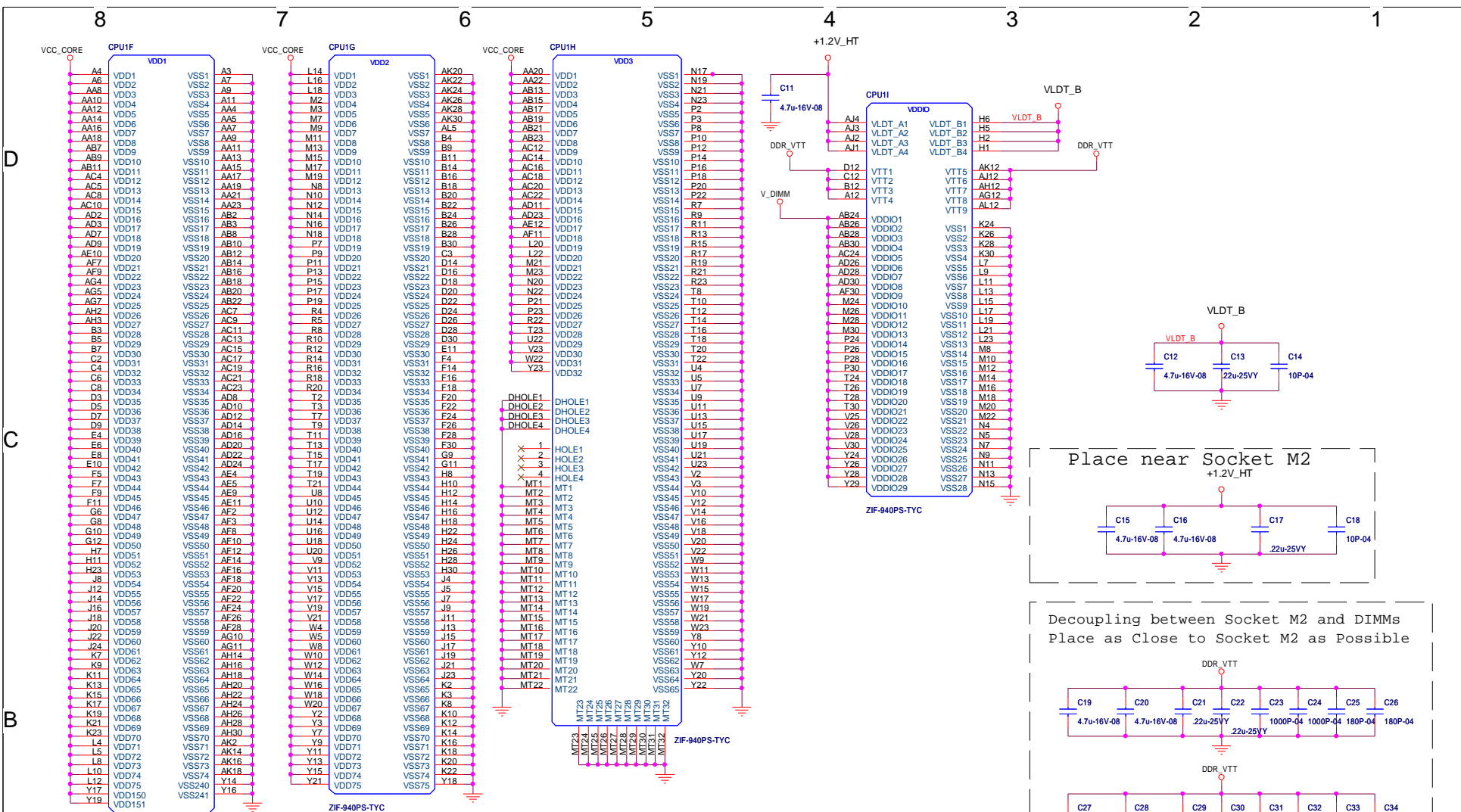
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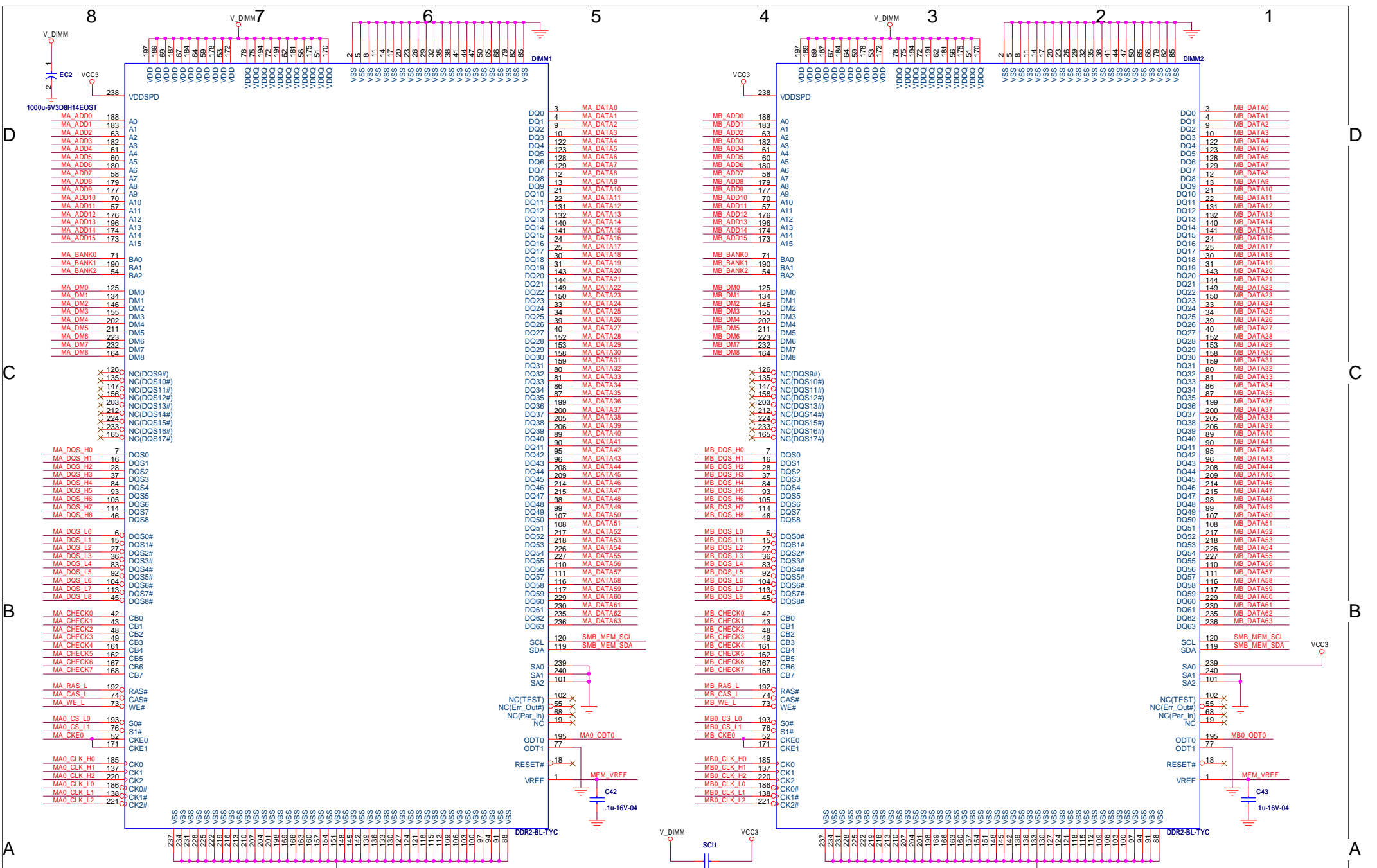
Size B | Document Number: **MCP61M-M** | Rev: **A**

Date: **Monday, July 03, 2006** | Sheet: **5** of **32**

+2.5V_VDDA for CPU PLL







5.9 MA0_CLK_H2[0]	MA0_CLK_H2[0]	15 SMB_MEM_SCL	SMB_MEM_SCL	5.9 MB0_ODT0	MB0_ODT0
5.9 MA0_CLK_L2[0]	MA0_CLK_L2[0]	15 SMB_MEM_SDA	SMB_MEM_SDA	5.9 MB0_CAS_L	MB0_CAS_L
5 MA_CHECK[7..0]	MA_CHECK[7..0]	5.9 MB_ADD[15..0]	MB_ADD[15..0]	5.9 MB_CAS_L	MB_CAS_L
5 MA_DQS_H[8..0]	MA_DQS_H[8..0]	5.9 MB_BANK[2..0]	MB_BANK[2..0]	5.9 MB_WE_L	MB_WE_L
5 MA_DQS_L[8..0]	MA_DQS_L[8..0]	5 MB_DM[8..0]	MB_DM[8..0]	5.9 MB0_CS_L[1..0]	MB0_CS_L[1..0]
5 MA_DM[8..0]	MA_DM[8..0]	5 MB_DQS_H[8..0]	MB_DQS_H[8..0]	5.9 MB_CKE0	MB_CKE0
5.9 MA_BANK[2..0]	MA_BANK[2..0]	5 MB_DQS_L[8..0]	MB_DQS_L[8..0]	5.9 MB0_CLK_H2[0]	MB0_CLK_H2[0]
5.9 MA_ADD[15..0]	MA_ADD[15..0]	5 MB_CHECK[7..0]	MB_CHECK[7..0]	5.9 MB0_CLK_L2[0]	MB0_CLK_L2[0]
5 MA_DATA[63..0]	MA_DATA[63..0]	5.9 MB_RAS_L	MB_RAS_L	5.9 MB0_DATA[63..0]	MB0_DATA[63..0]

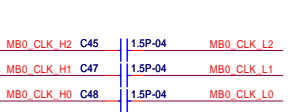
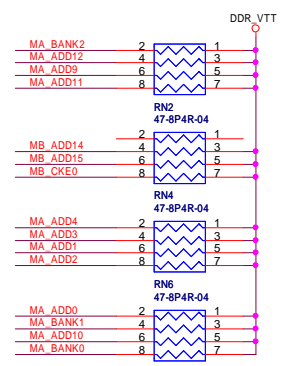
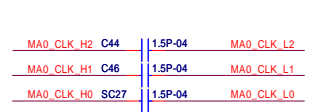
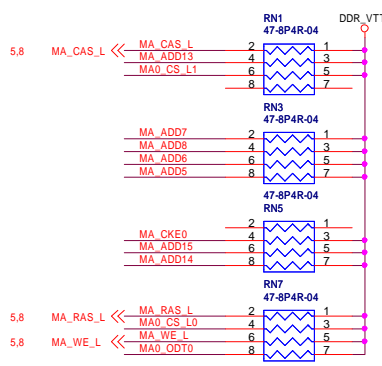
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Title: **DDR2 DIMM**

Size: A3 | Document Number: **MCP61M-M** | Rev: A

Date: Monday, July 03, 2006 | Sheet: 8 of 32

8 7 6 5 4 3 2 1

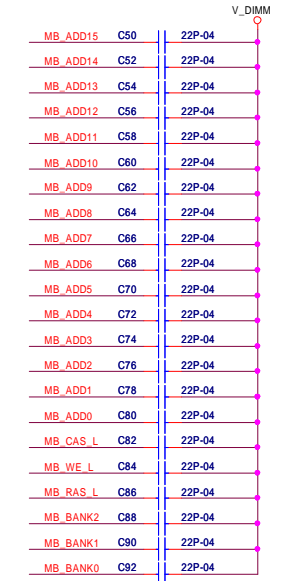
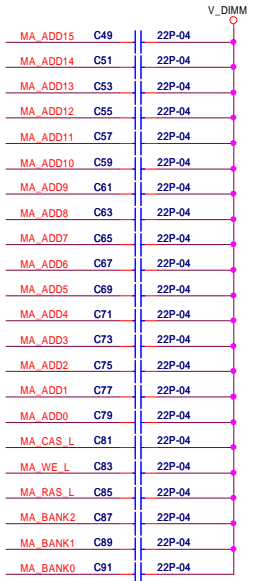
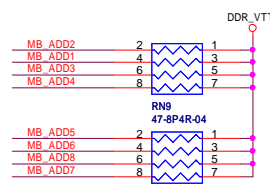


5.8 MA0_CLK_H2[0] << MA0_CLK_H2[0]
5.8 MA0_CLK_L2[0] << MA0_CLK_L2[0]

5.8 MB0_CLK_H2[0] << MB0_CLK_H2[0]
5.8 MB0_CLK_L2[0] << MB0_CLK_L2[0]

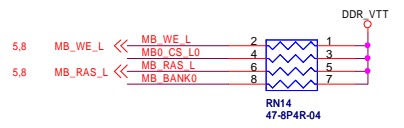
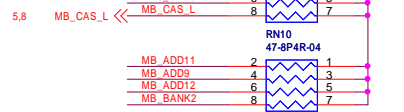
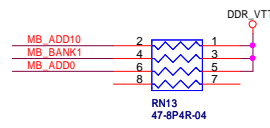
5.8 MA_ADD[15..0] << MA_ADD[15..0]

5.8 MB_ADD[15..0] << MB_ADD[15..0]



5.8 MA_BANK[2..0] << MA_BANK[2..0]

5.8 MB_BANK[2..0] << MB_BANK[2..0]

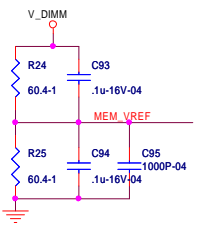
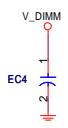


5.8 MA_CKE0 << MA_CKE0
5.8 MA0_ODT0 << MA0_ODT0

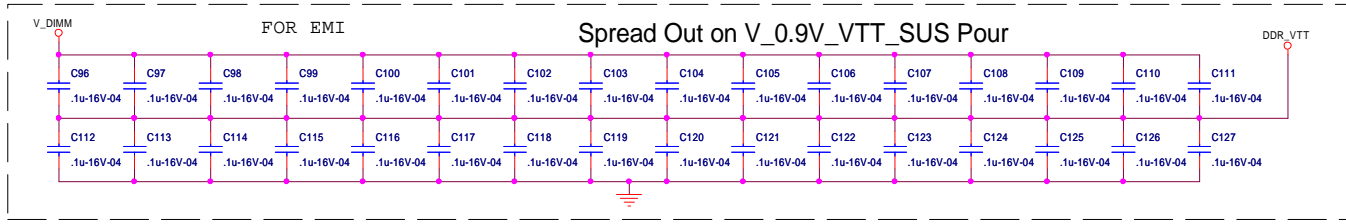
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5.8 MB0_ODT0 << MB0_ODT0

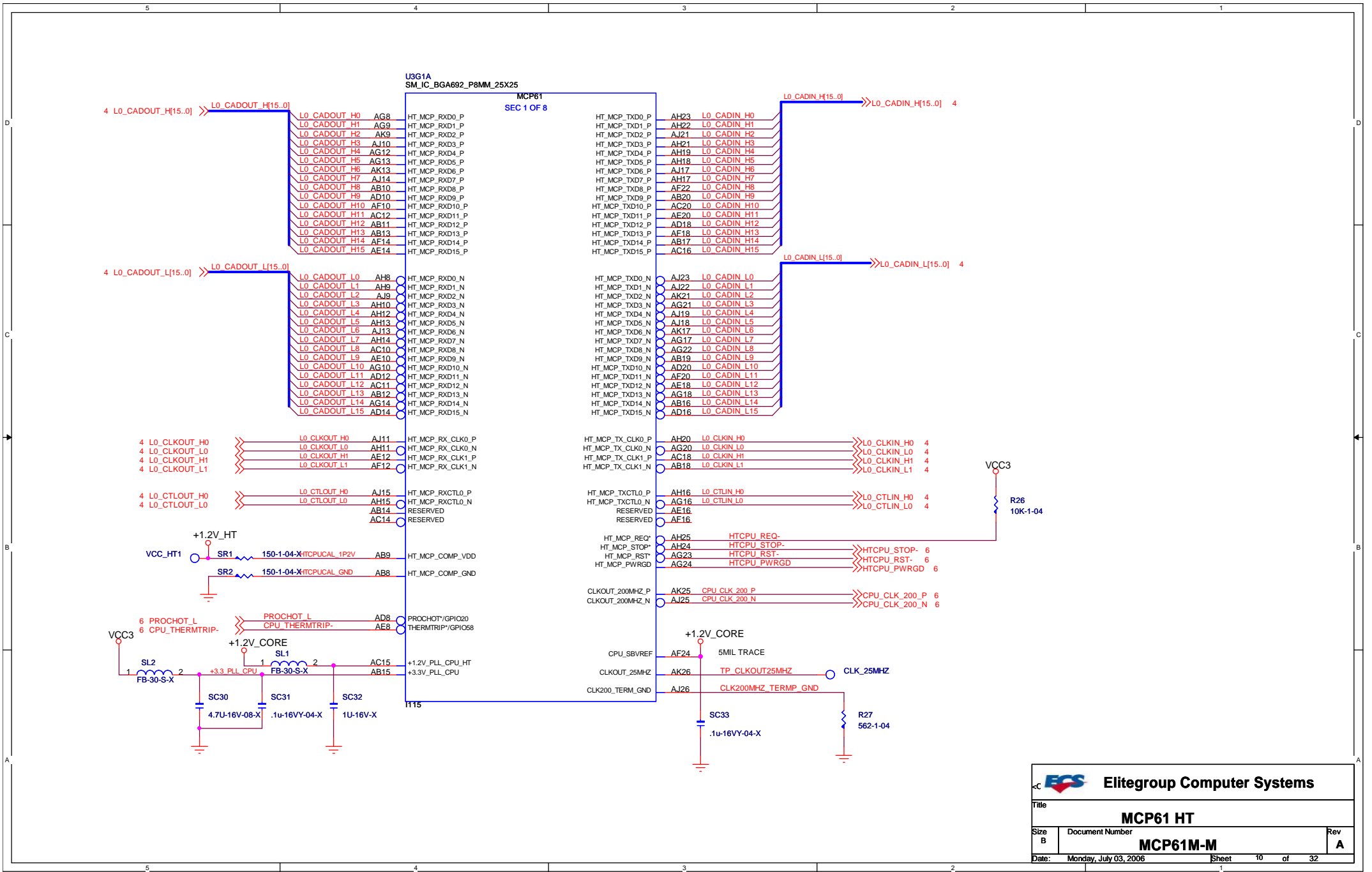
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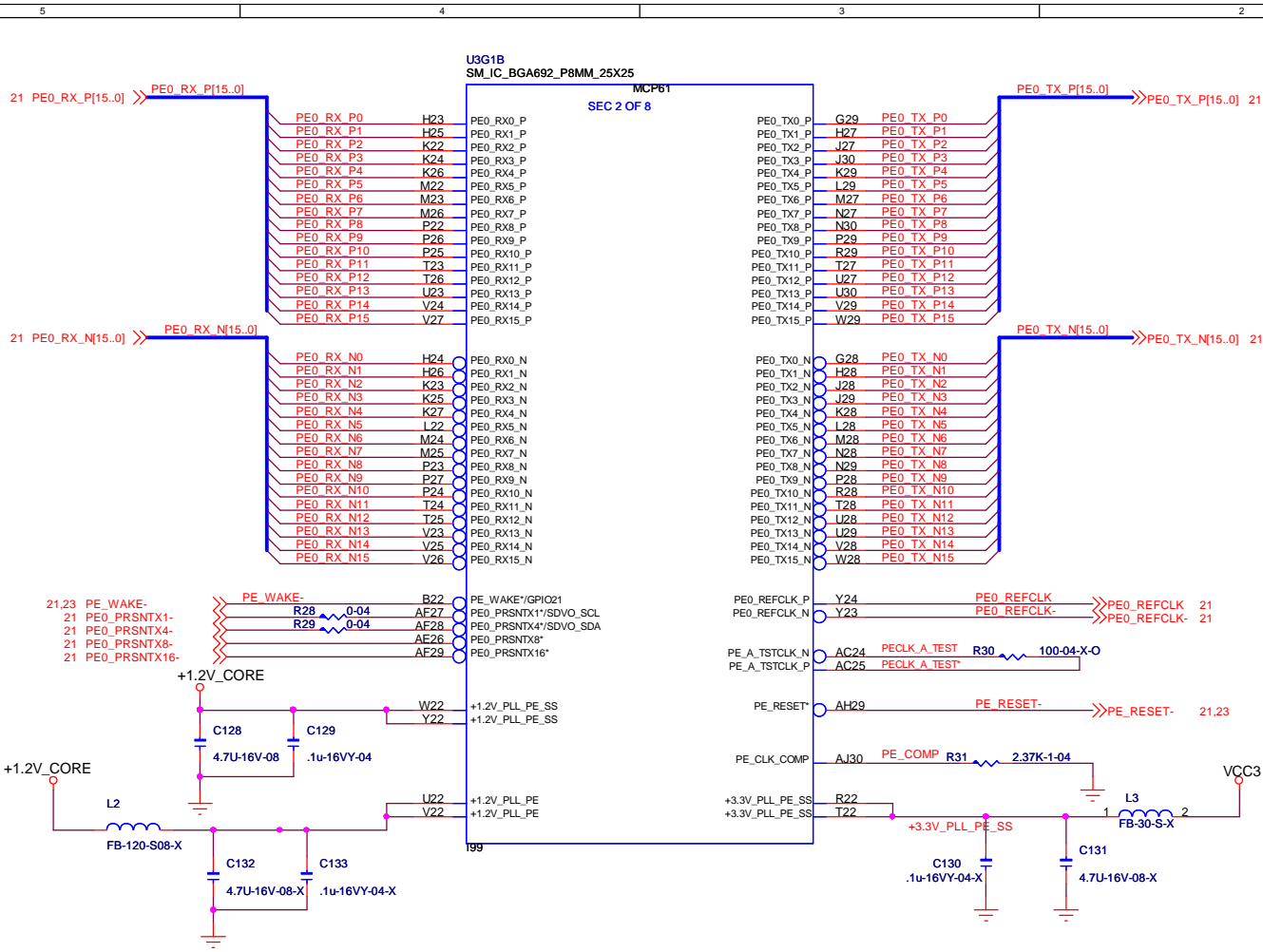
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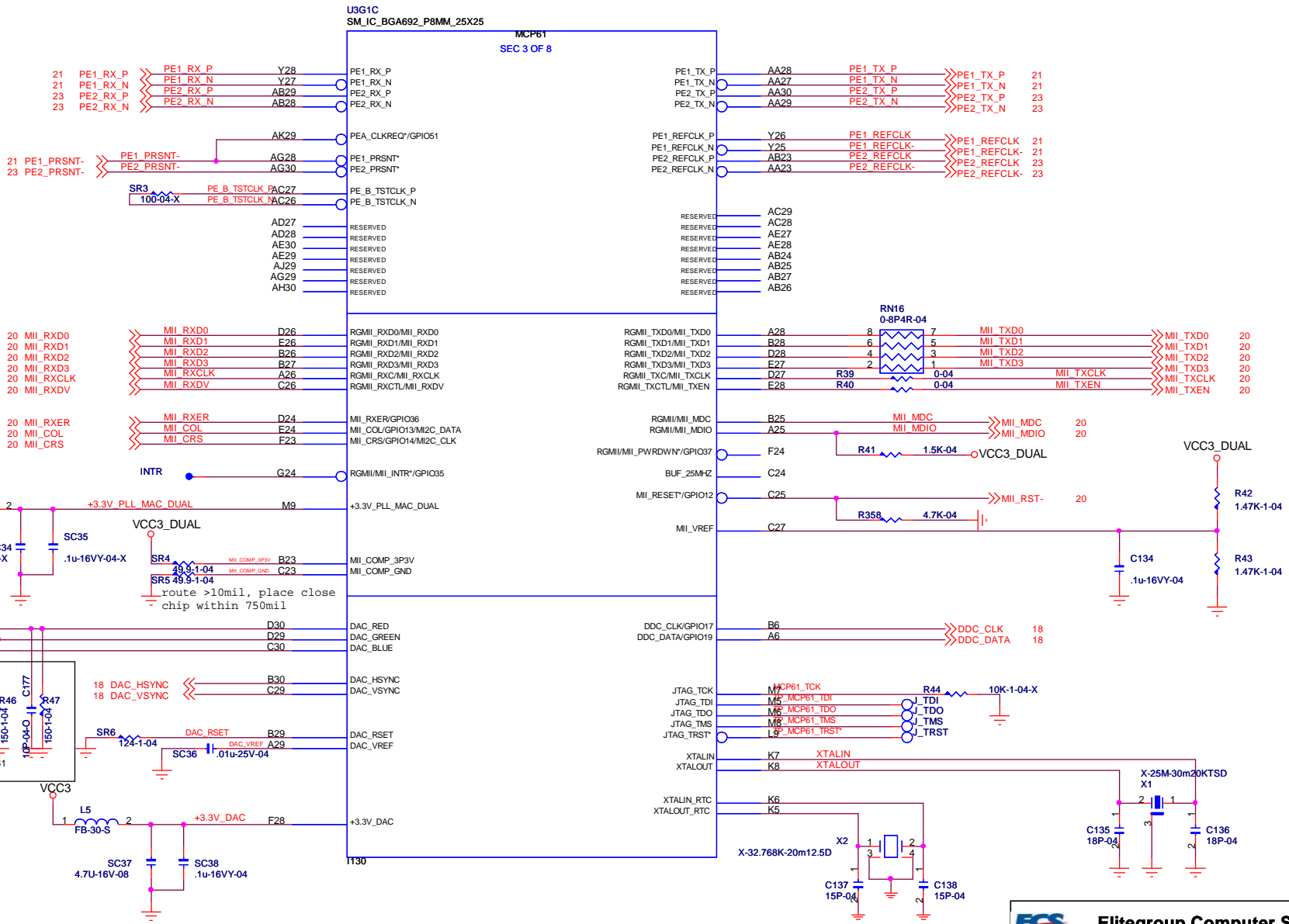
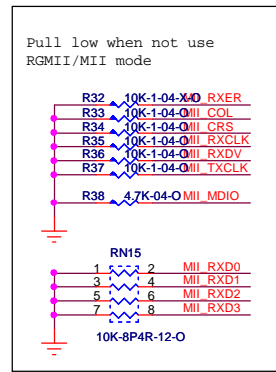


8 MEM_VREF << MEM_VREF

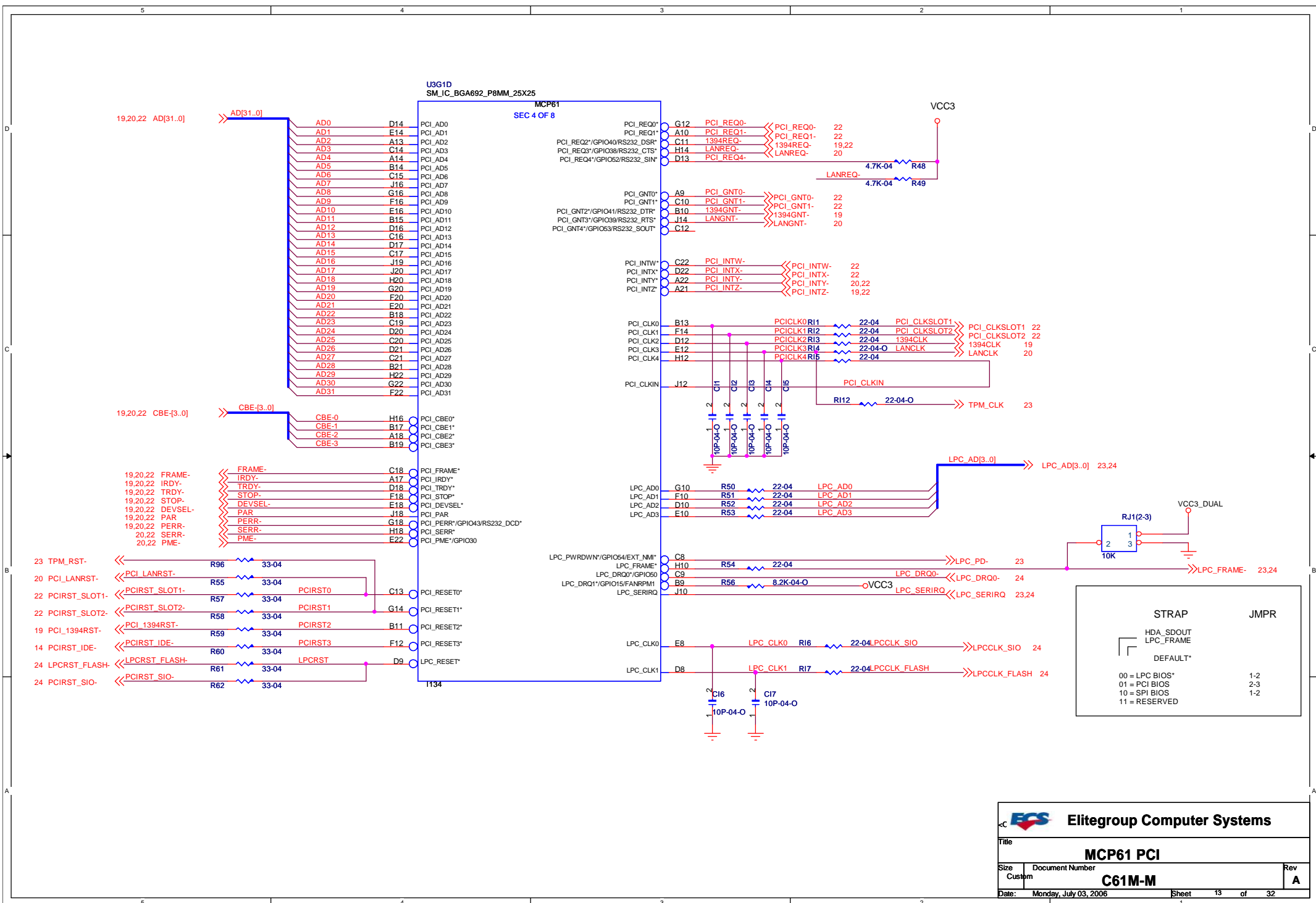








ECS Elitegroup Computer Systems		
Title MCP61 PCI-E X1/RGMII/DAC		
Size B	Document Number C61M-M	Rev A
Date Monday, July 03, 2006	Sheet 12 of 32	

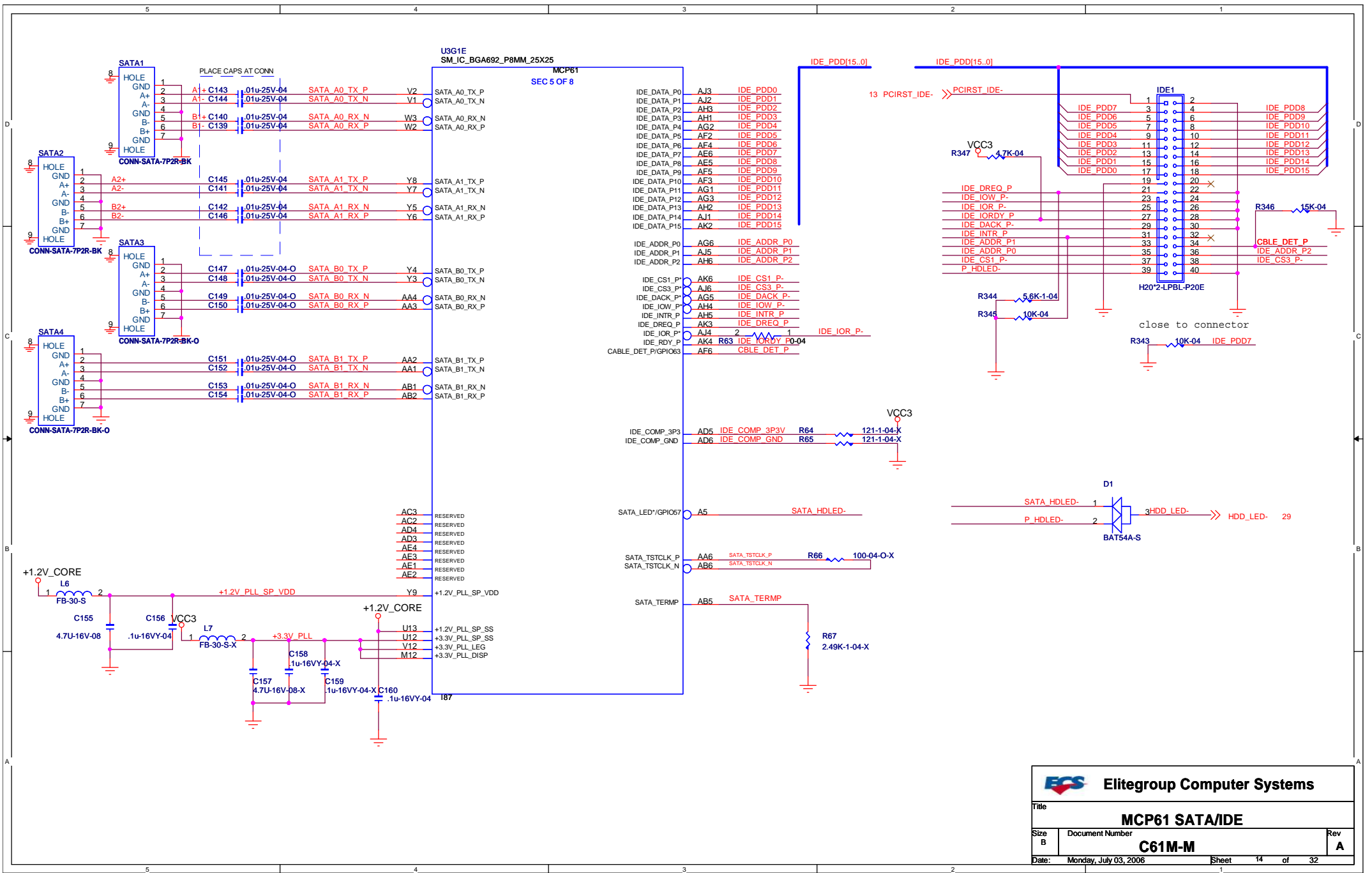


ECS Elitegroup Computer Systems

Title: **MCP61 PCI**

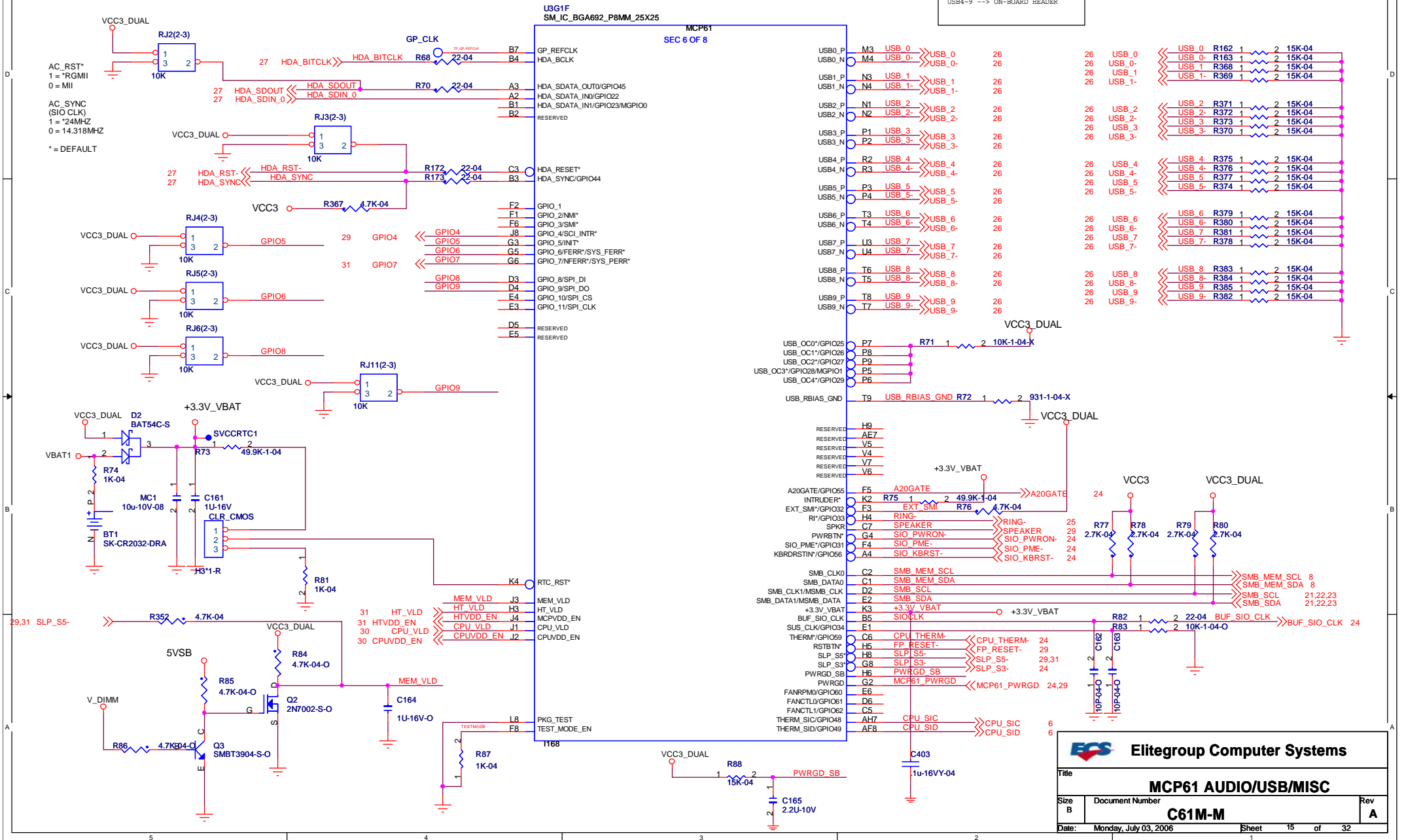
Size: Custom | Document Number: **C61M-M** | Rev: **A**

Date: Monday, July 03, 2006 | Sheet: 13 of 32

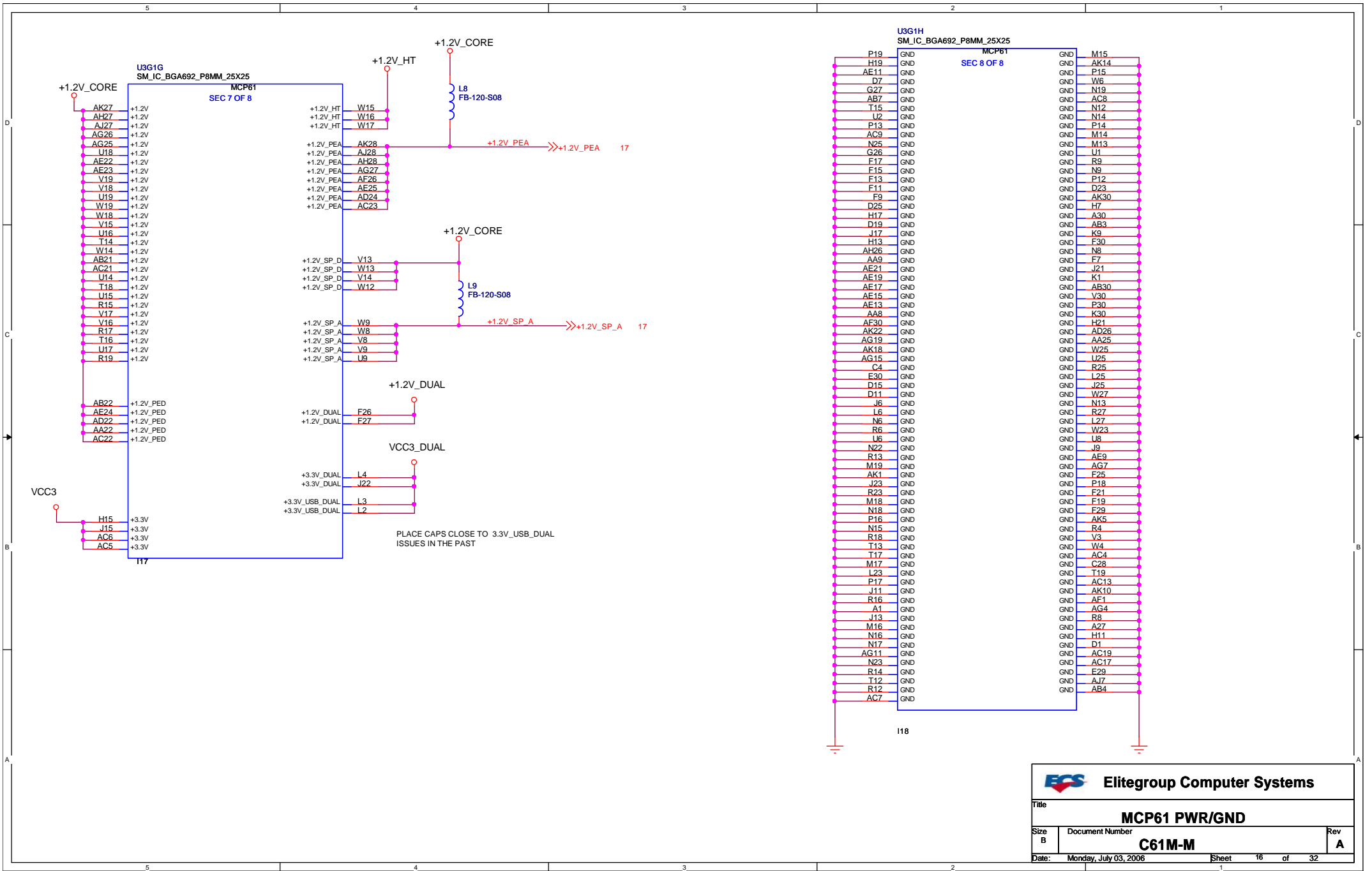


REMOVE FOR PRODUCTION

USB0-3 --> BACK CONNECTORS
USB4-9 --> ON-BOARD HEADER



ECS Elitegroup Computer Systems		
Title MCP61 AUDIO/USB/MISC		
Size B	Document Number C61M-M	Rev A
Date Monday, July 03, 2006	Sheet 15 of 32	



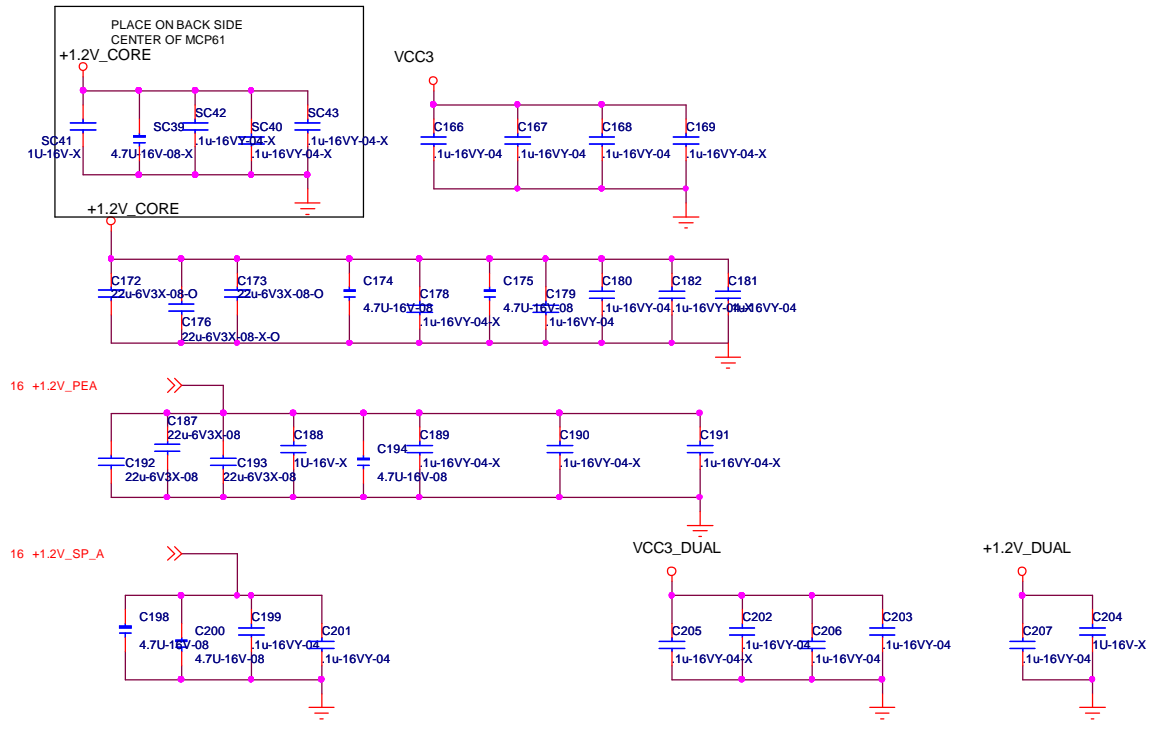
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Title: **MCP61 PWR/GND**

Size B | Document Number: **C61M-M** | Rev A

Date: Monday, July 03, 2006 | Sheet 16 of 32

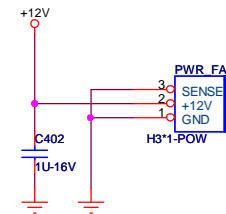
MCP61 DECOUPLING/EMI



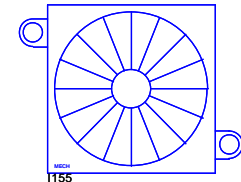
MCP61 INTERNAL PULL-UP/DWNS

PE0_PRSNTX16*	10K PU TO 3.3V
PE0_PRSNTX8*	10K PU TO 3.3V
PE1_PRSNT*	10K PU TO 3.3V
PE2_PRSNT*	10K PU TO 3.3V
PE1_CLKREQ*	10K PU TO 3.3V
PCI_PME*/GPIO_30	8.2K PU TO 3.3V_DUAL
LPC_AD0	8.2K PU TO 3.3V
LPC_AD1	8.2K PU TO 3.3V
LPC_AD2	8.2K PU TO 3.3V
LPC_AD3	8.2K PU TO 3.3V
LPC_DRQ0/LPC_CS*	8.2K PU TO 3.3V
LPC_DRQ0*	8.2K PU TO 3.3V
LPC_SERIRQ	10K PU TO 3.3V
HDA_SDATA_IN1/GPIO_23/MGPIO_0	10K PD TO GND
HDA_SDATA_IN0/GPIO_22	10K PD TO GND
JTAG_TMS	10K PU TO 3.3V
JTAG_TRST*	10K PD TO GND
JTAG_TDI	10K PU TO 3.3V
A20GATE	10K PU TO 3.3V
PE_WAKE*	10K PU TO 3.3V_DUAL
EXT_SMI*/GPIO32	10K PU TO 3.3V_DUAL
THERM*/GPIO_59	10K PU TO 3.3V
KBRDRSTIN*/GPIO_58	10K PU TO 3.3V
RP*/GPIO_33	10K PU TO 3.3V_DUAL
SIO_PME*/GPIO_31/MGPIO_2	10K PU TO 3.3V_DUAL
PWRBTN*	10K PU TO 3.3V_DUAL
RSTBTN*	10K PU TO 3.3V_DUAL

MCP61 FAN HDR



HS3G1
HEATSINK
45MM_PP_SQUARE
FANSINK

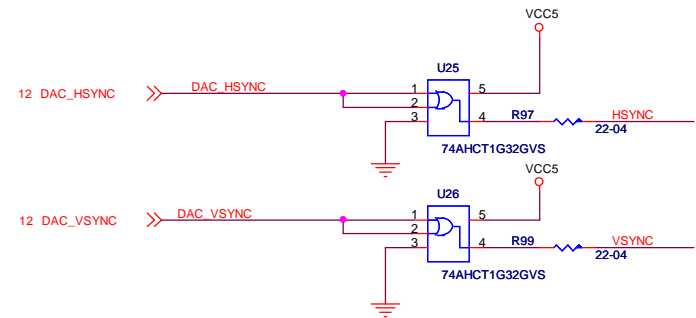
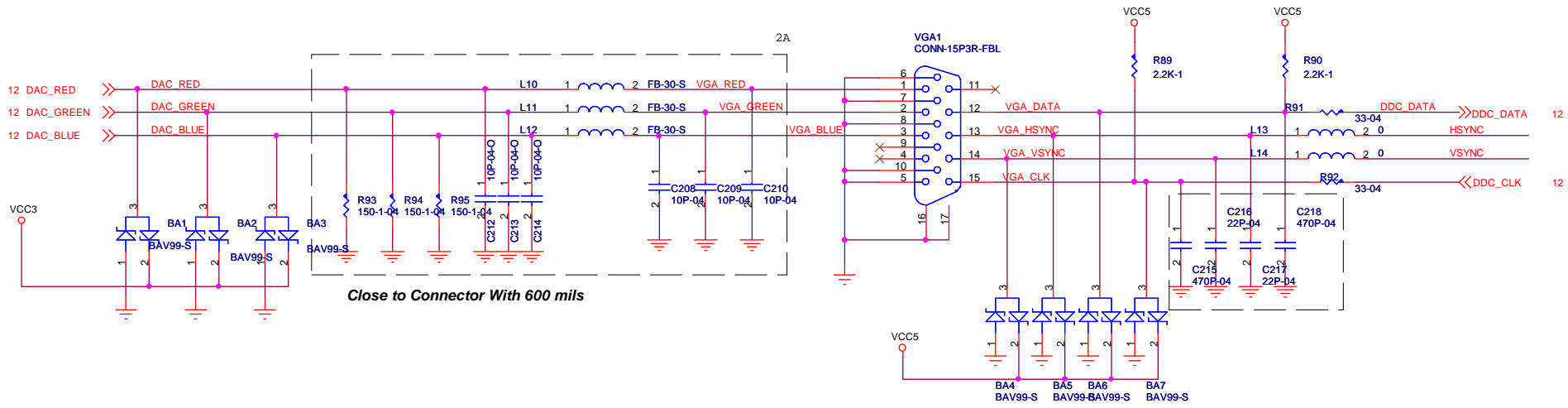


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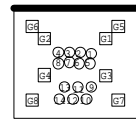
Title: **MCP51 SATA / IDE / CONN**

Size B Document Number: **MCP61M-M** Rev **A**

Date: Monday, July 03, 2006 Sheet 17 of 32



ECS Elitegroup Computer Systems		
Title VGA		
Size B	Document Number C61M-M	Rev A
Date: Monday, July 03, 2006	Sheet 18 of 32	



Bandgap Resistor	Ra
VT6307	6.2K-1
VT6308P	6.2K-1

BJT_SEL	Internal MOS turn on
0 (default)	Use external BJT
1	Use external BJT

13.20.22 CBE-0[.3] << CBE-0[.3]
13.20.22 AD0[.31] << AD0[.31]

1394 CHIP (Ua)	EEPROM LESS M/B only (Rb)	EEPROM (Ub)	VDD25 Power (Rc)	PWRDET_VCC3 (Rd)
VT6307	NC(WHQL fail)	ON	ON	0 ohm
VT6308P	ON	NC	NC	4.7k

INT:Z
IDSEL:AD25
Co-layout VT6308P(PQFP)

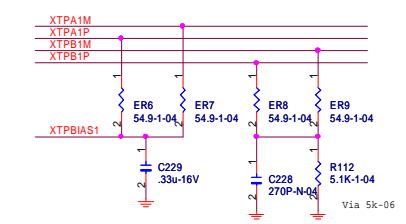
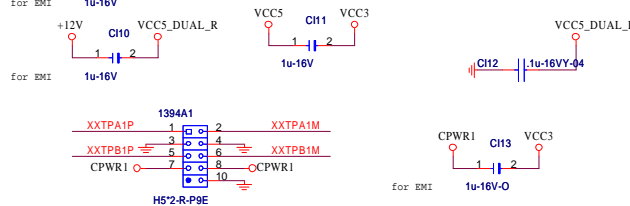
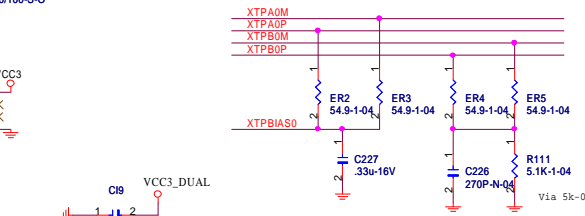
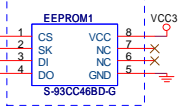
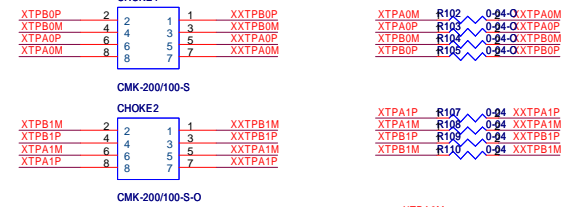
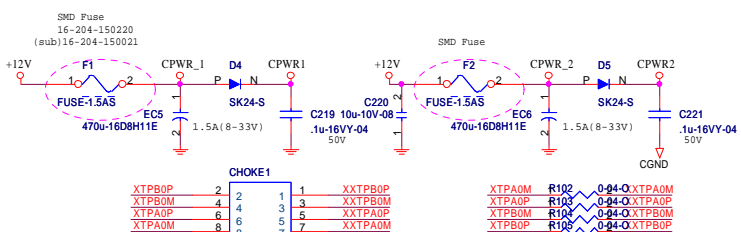
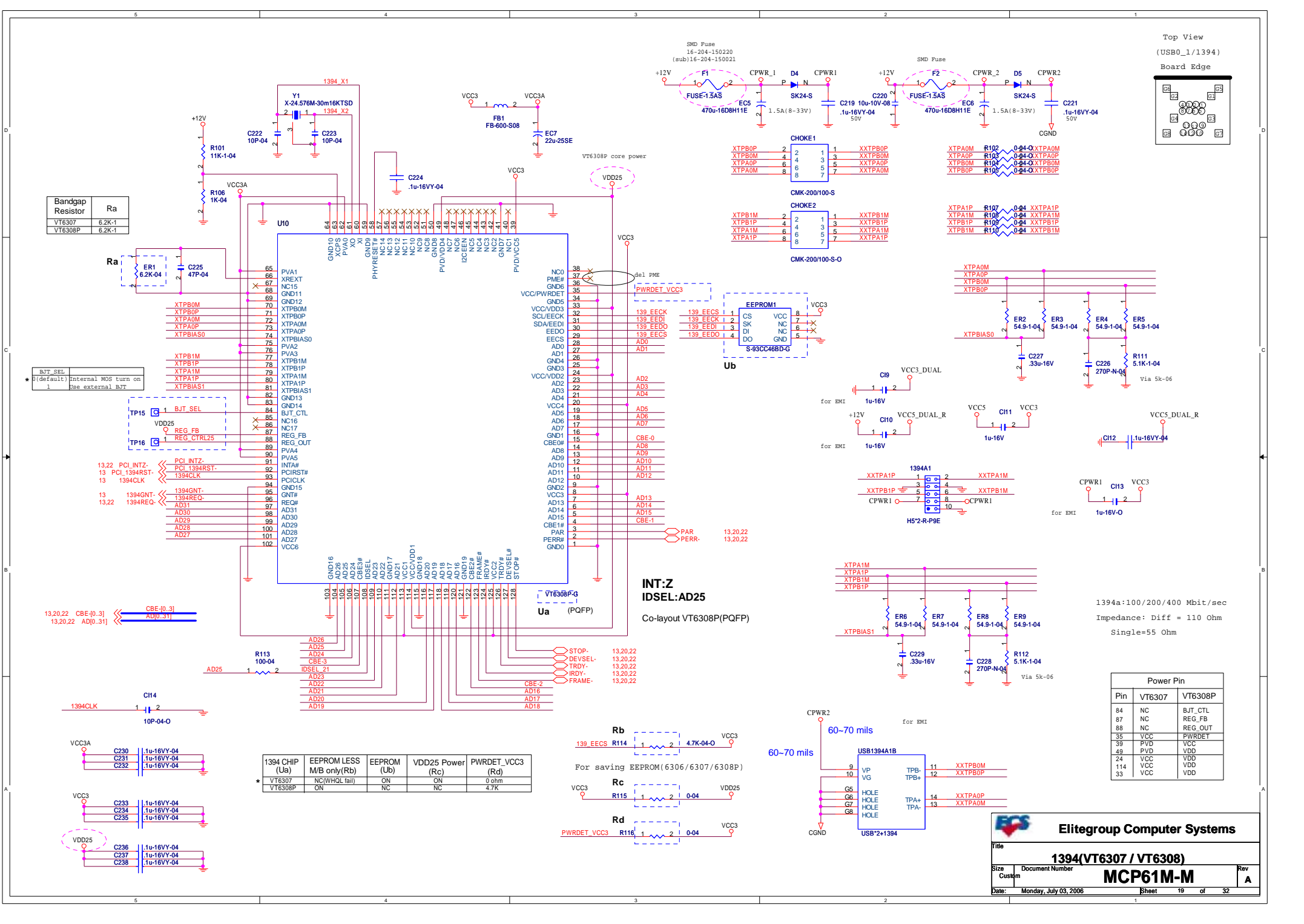
Power Pin		
84	NC	BIT_CTL
87	NC	REG_FB
88	NC	REG_OUT
35	VCC	PWRDET
39	PVD	VCC
49	PVD	VDD
24	VCC	VDD
114	VCC	VDD
33	VCC	VDD

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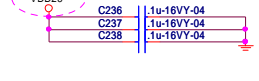
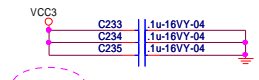
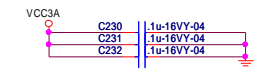
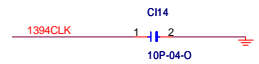
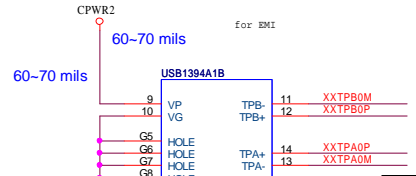
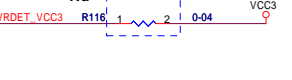
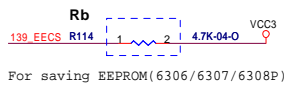
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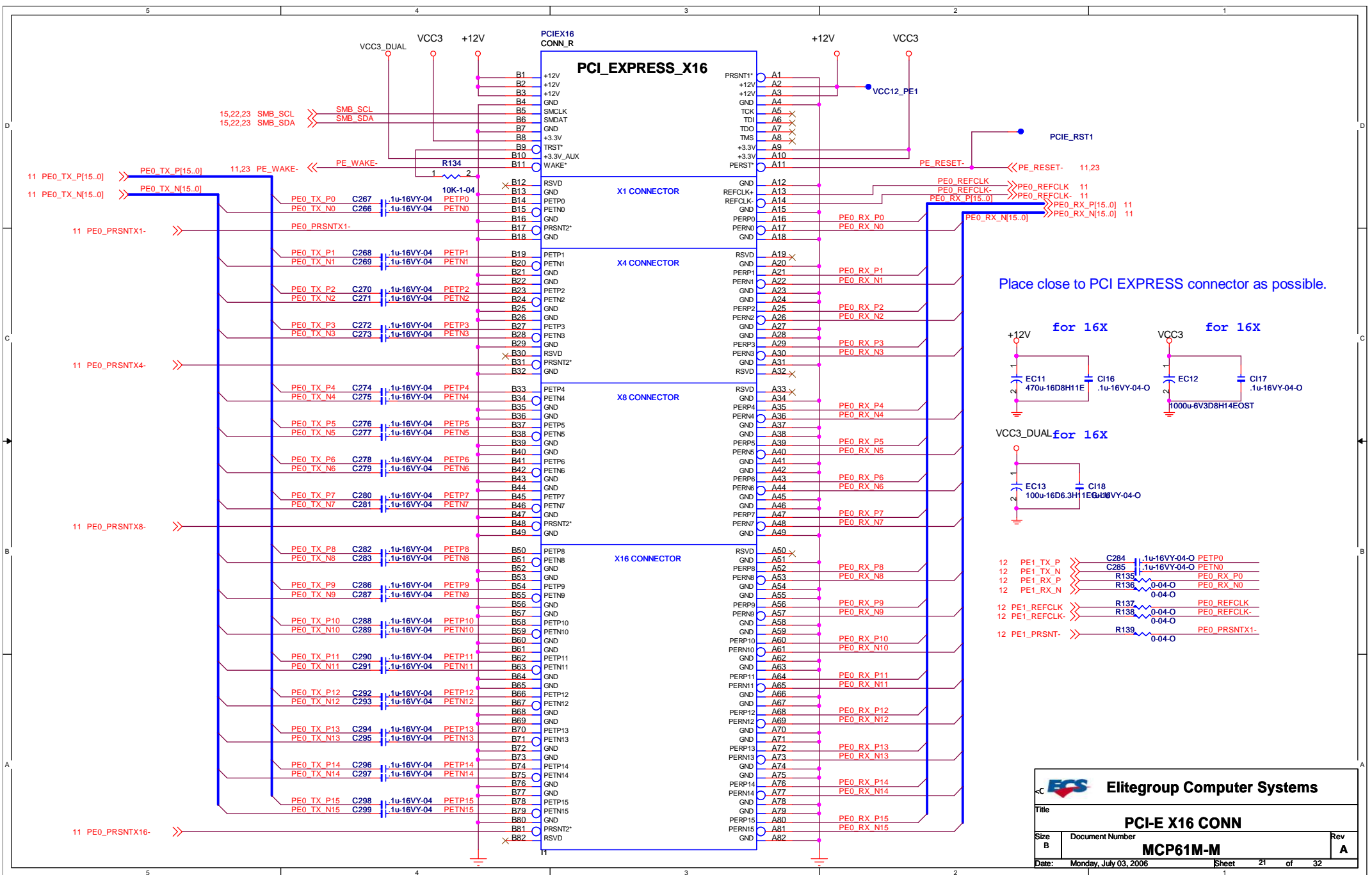
Size: Custom Document Number: **MCP61M-M** Rev: **A**


Date: Monday, July 03, 2006 Sheet: 19 of 32



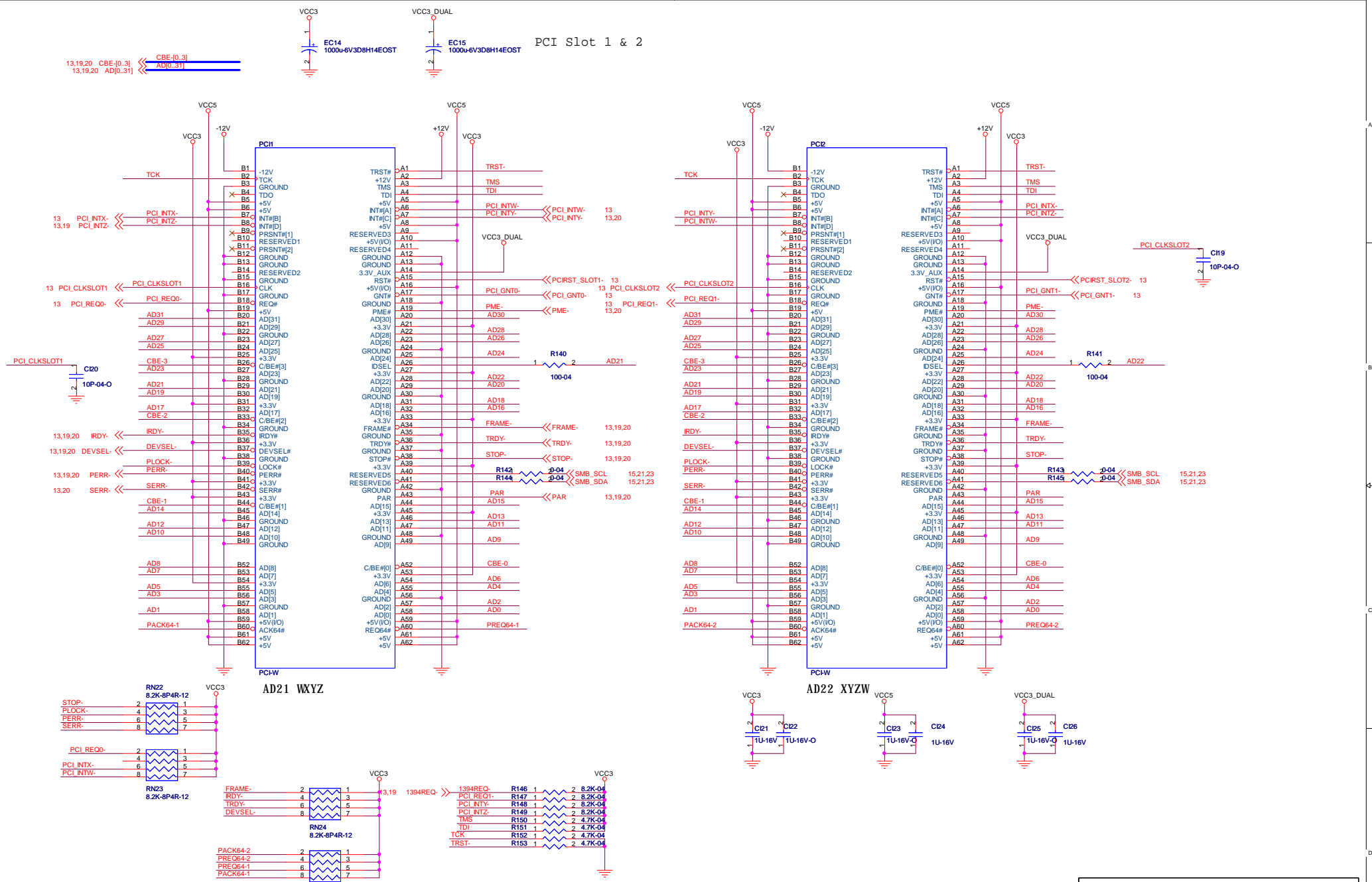
1394a:100/200/400 Mbit/sec
Impedance: Diff = 110 Ohm
Single=55 Ohm





 Elitegroup Computer Systems	
Title PCI-E X16 CONN	
Size B	Document Number MCP61M-M
Date Monday, July 03, 2006	Rev A
Sheet 21 of 32	

PCI Slot 1 & 2

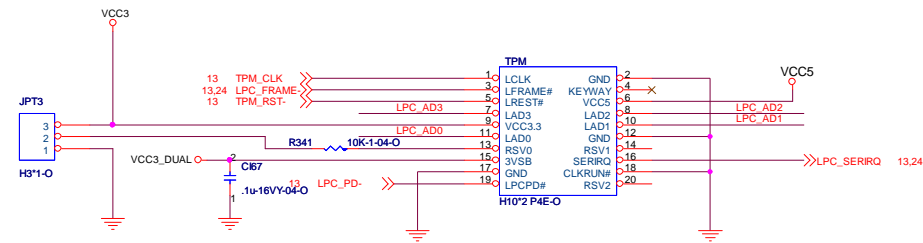
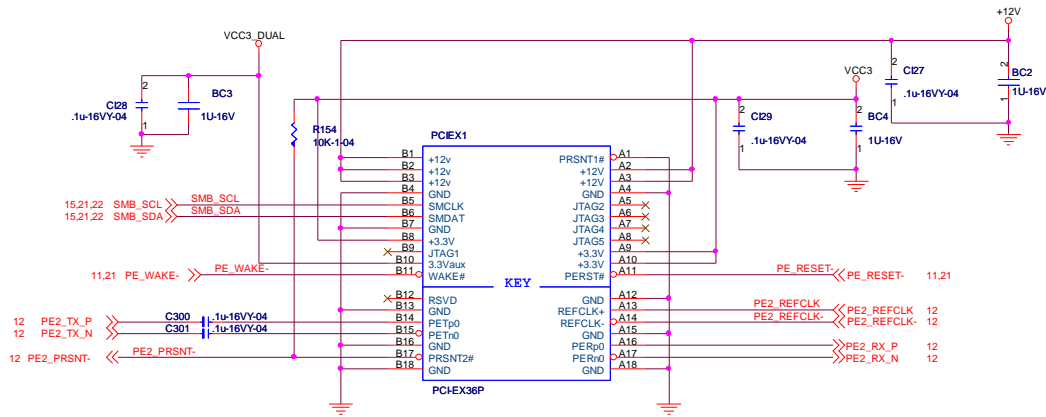


Elitegroup Computer Systems

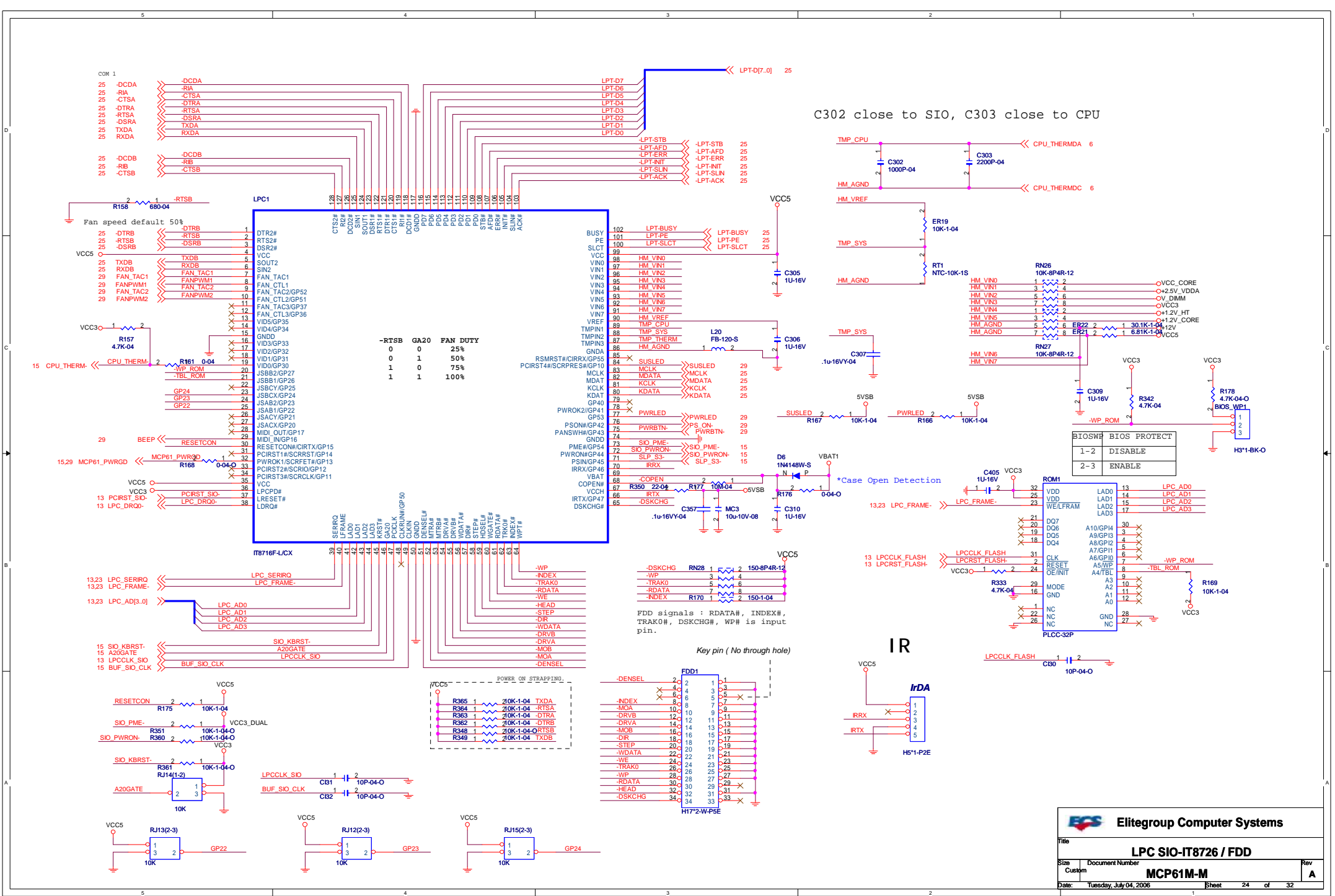
Title: **PCI 1&2**

Size: Custom Document Number: **C61M-M** Rev: **A**

Date: Monday, July 03, 2006 Sheet: 22 of 32

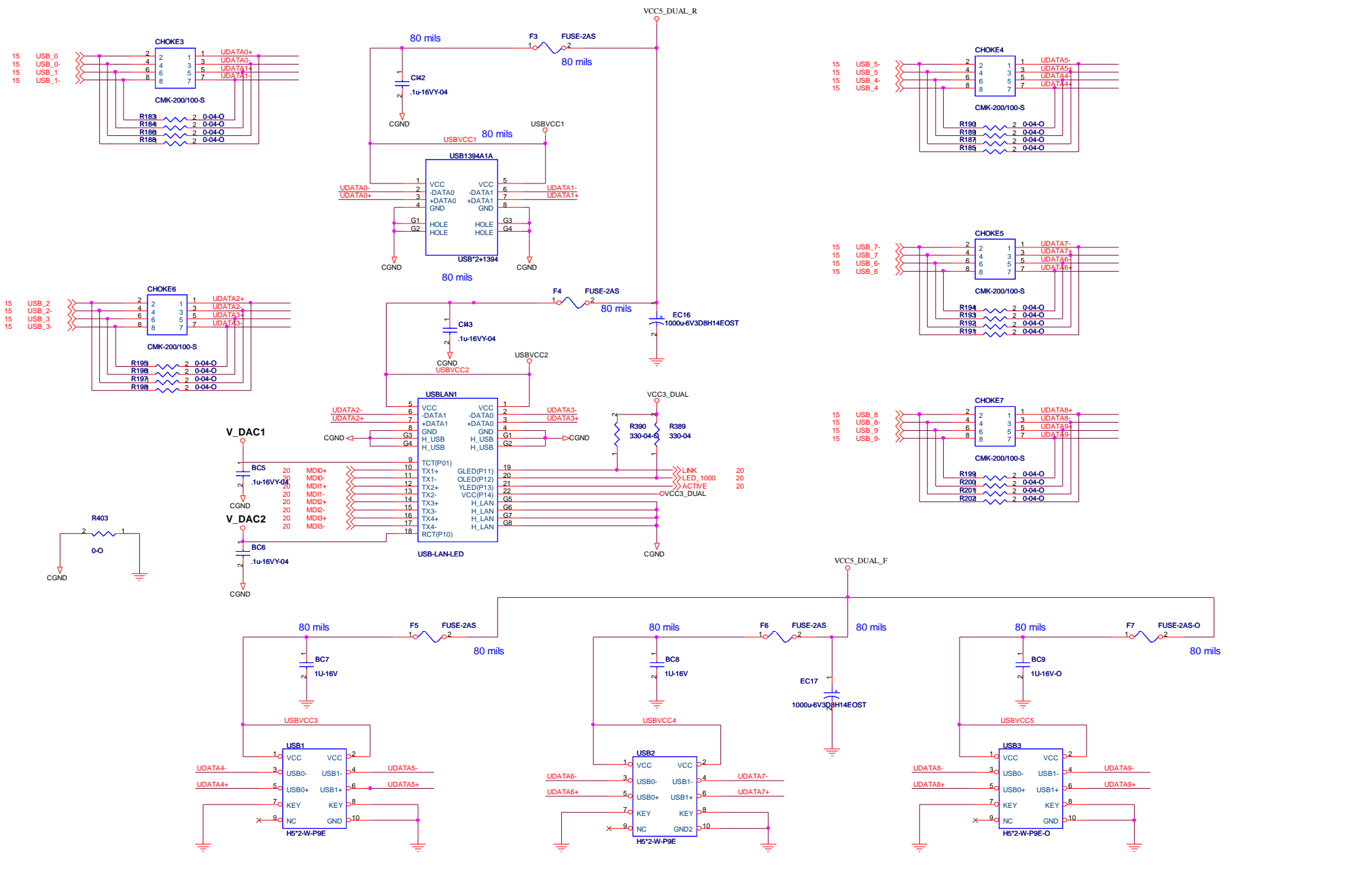


13.24 LPC_AD[3..0] >>



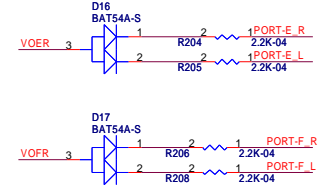
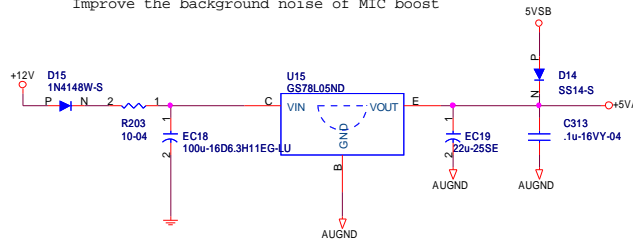
C302 close to SIO, C303 close to CPU

Title LPC SIO-IT8726 / FDD		
Size Custom	Document Number MCP61M-M	Rev A
Date: Tuesday, July 04, 2006		
Sheet 24		of 32



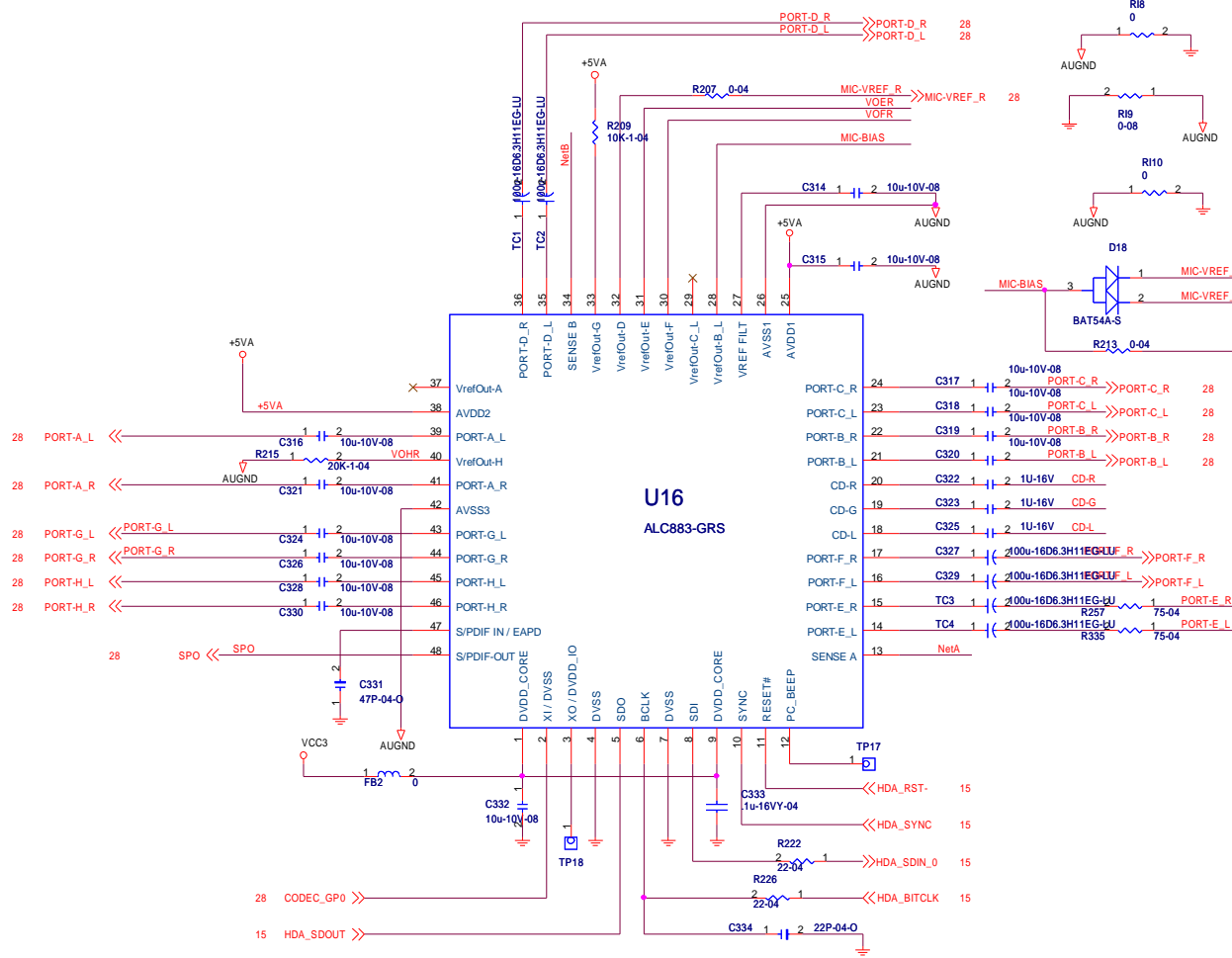
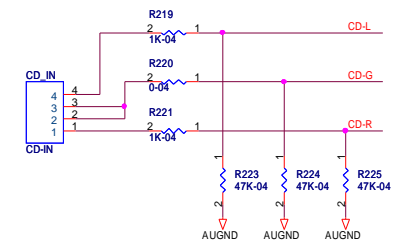
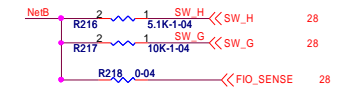
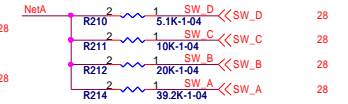
Improve the background noise of MIC boost

Verfourt bias for stereo microphone.

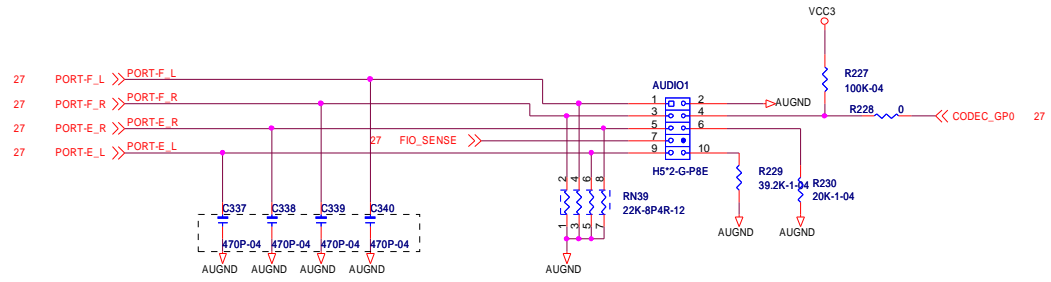
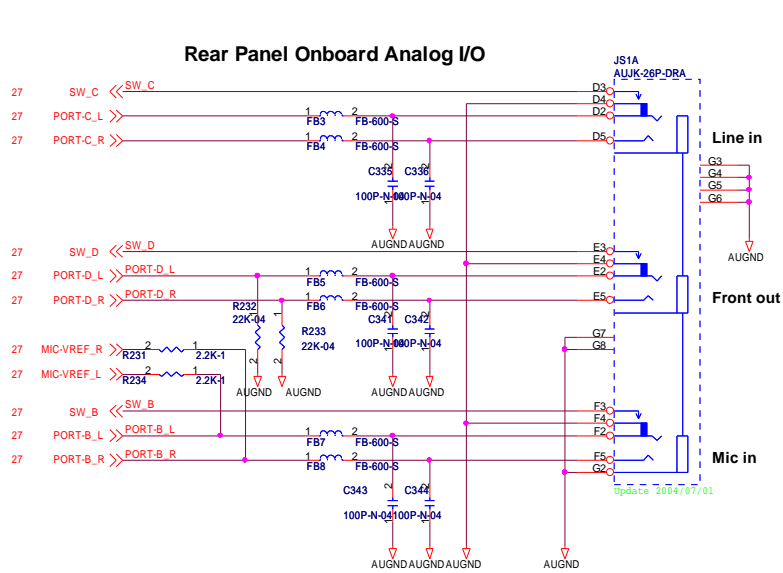


Place near Chip

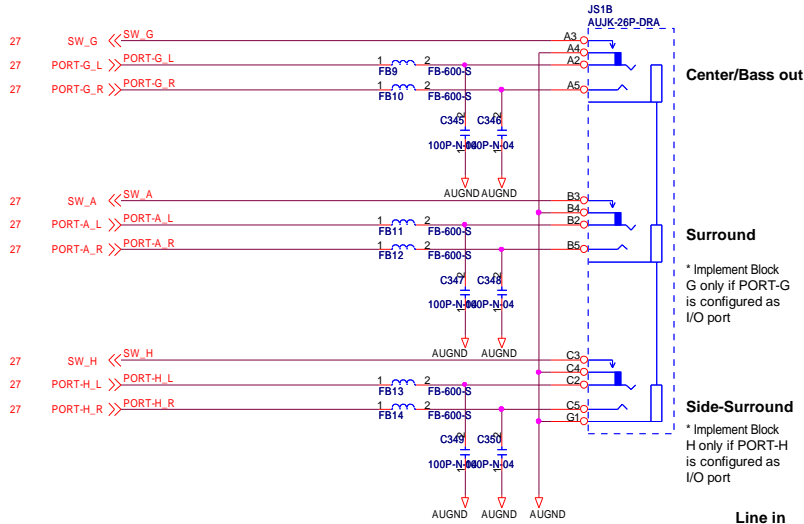
Resistors Networks



Rear Panel Onboard Analog I/O



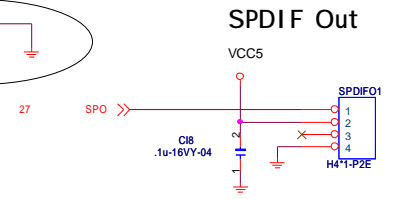
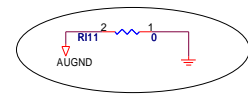
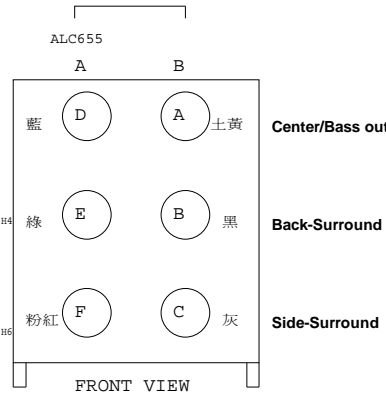
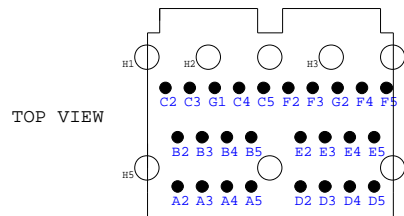
Rear Panel (Optional Rear Audio Panel)



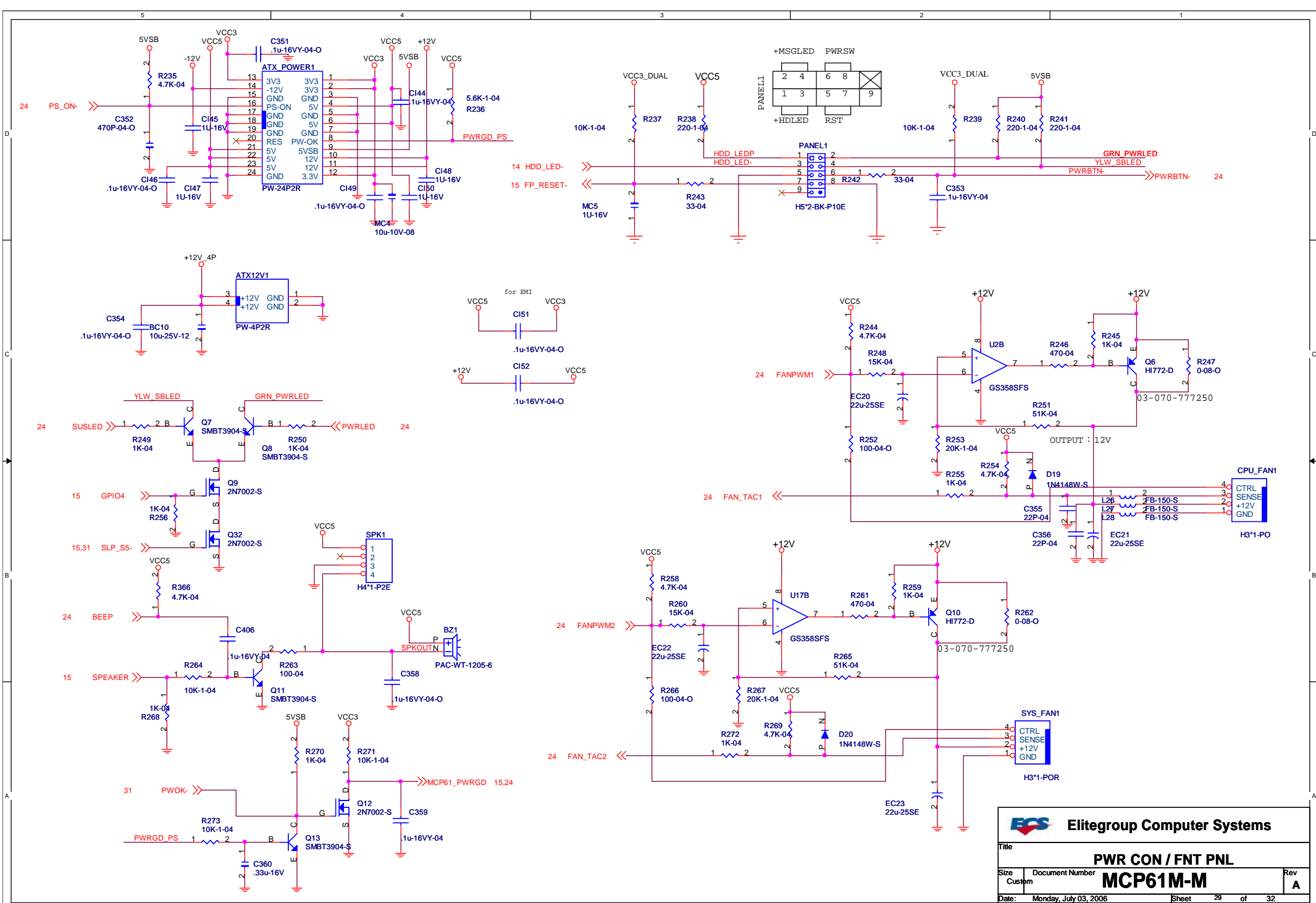
* Implement Block G only if PORT-G is configured as I/O port

* Implement Block H only if PORT-H is configured as I/O port

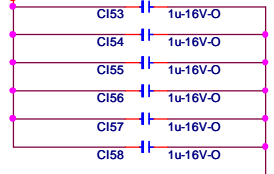
The schematic should consist with PINs define of I/O connector.



Elitegroup Computer Systems			
Title AUDIO ALC861/660(PANEL)			
Size Custom	Document Number	MCP61M-M	
Date: Monday, July 03, 2006	Sheet	28	of 32
			Rev A

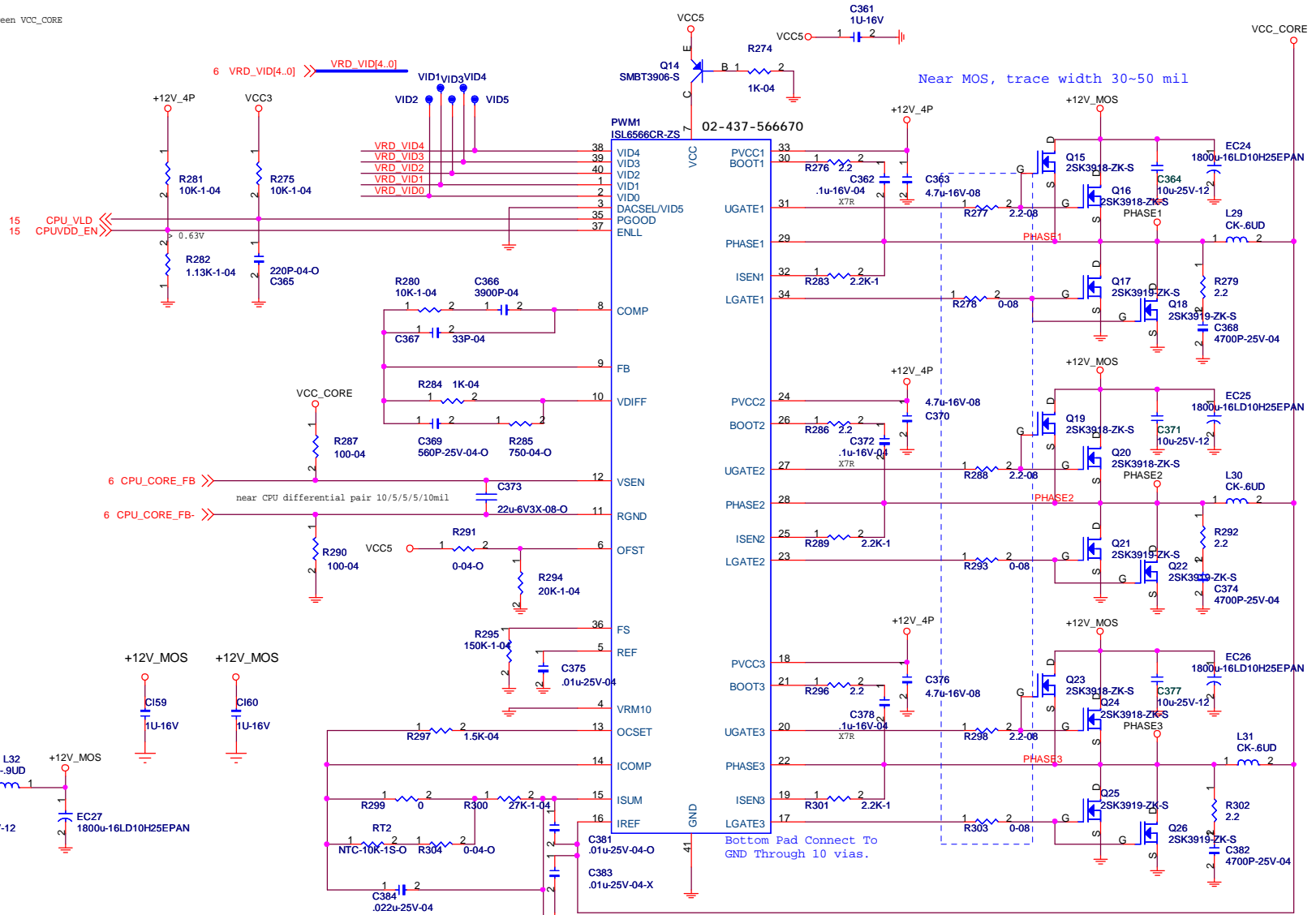


VCC_CORE For EMI suggest, average distribute between VCC_CORE



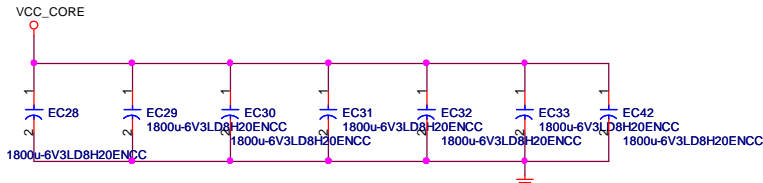
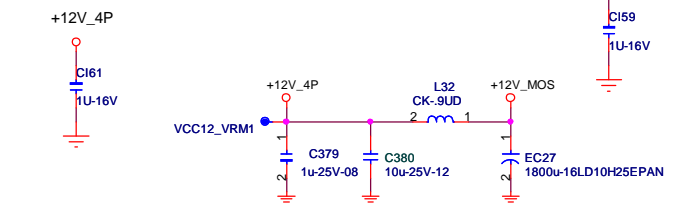
VID Codes

VID[4:0]	VCC_CORE	VID[4:0]	VCC_CORE
00000	1.550	10000	1.150
00001	1.525	10001	1.125
00010	1.500	10010	1.100
00011	1.475	10011	1.075
00100	1.450	10100	1.050
00101	1.425	10101	1.025
00110	1.400	10110	1.000
00111	1.375	10111	0.975
01000	1.350	11000	0.950
01001	1.325	11001	0.925
01010	1.300	11010	0.900
01011	1.275	11011	0.875
01100	1.250	11100	0.850
01101	1.225	11101	0.825
01110	1.200	11110	0.800
01111	1.175	11111	No CPU



Near MOS, trace width 30-50 mil

Bottom Pad Connect To GND Through 10 vias.



- R305 1 2 121K-1-04 PHASE1
- R306 1 2 121K-1-04 PHASE2
- R307 1 2 121K-1-04 PHASE3

ECS Elitegroup Computer Systems

Title: **CPU VCORE**

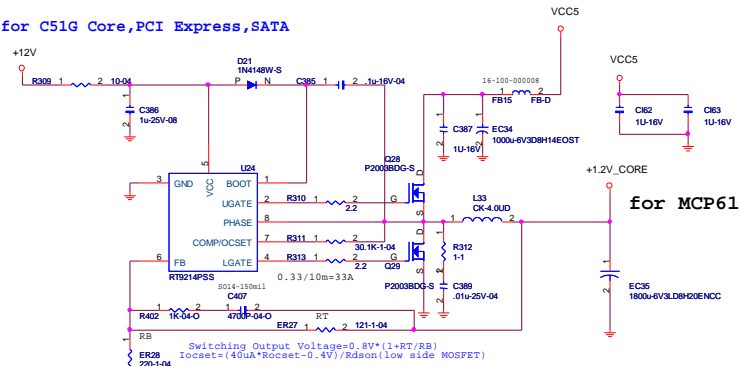
Document Number: **MCP61M-M**

Date: Tuesday, July 04, 2006

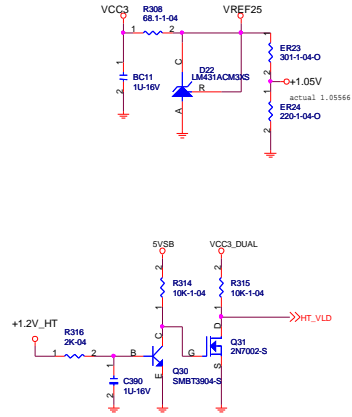
Sheet 30 of 32

Rev A

Power for C51G Core,PCI Express,SATA

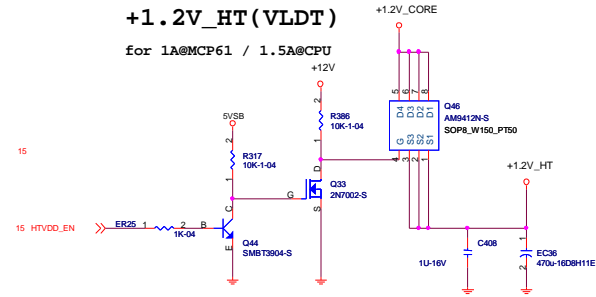


for MCP61@10A

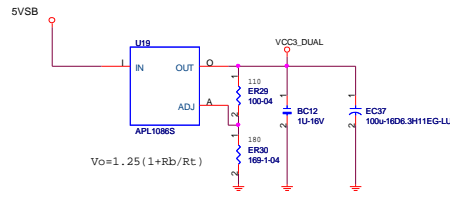


+1.2V_HT (VLDI)

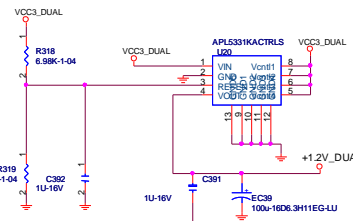
for 1A@MCP61 / 1.5A@CPU



+3.3V_DUAL



MCP61 AUX(1.2V) @250mA



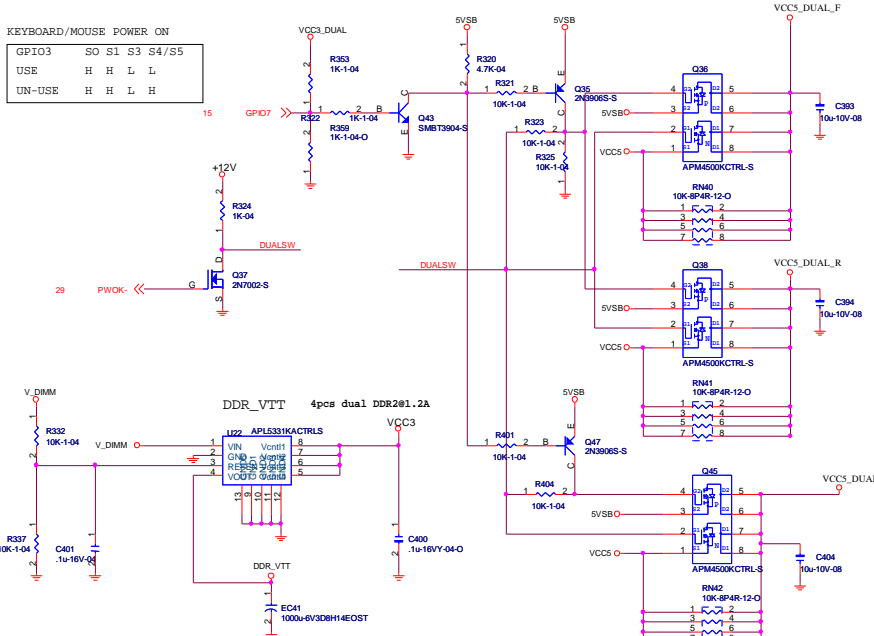
5VSB



+5V_DUAL FOR USB,PS2

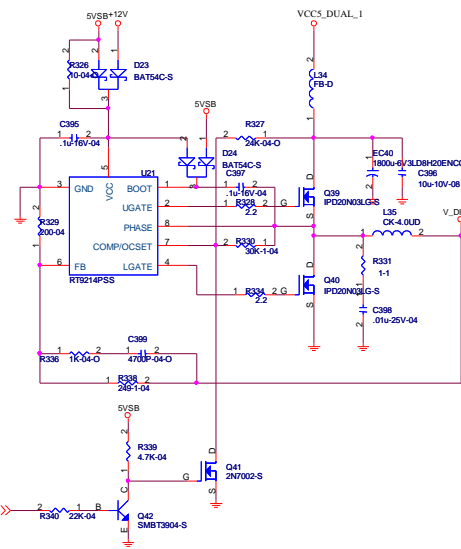
KEYBOARD/MOUSE POWER ON

GPIO3	SO	S1	S3	S4/S5
USE	H	H	L	L
UN-USE	H	H	L	H



R2922	R2924	
R345	1.0	x
D30	x	v
R344	x	100
R762	24K	x

1pcs DDR2@2.5A



PCI_SLOT1 : REQ0, GNT0, CLK0, AD21, INT WXYX
 PCI_SLOT2 : REQ1, GNT1, CLK1, AD22, INT XYZW
 PCI_1394 : REQ2, GNT2, CLK2, AD25, INT Z
 PCI_LAN : REQ3, GNT3, CLK3, AD24, INT Y
 CNR :

CLR_CMOS	CLEAR_CMOS
1-2	NORMAL
2-3	CLEAR

