

A928 SCHEMATICS

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36. DDR POWER
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P/N : KK0A928012030
 GERBER : KK0A928012030.ZIP

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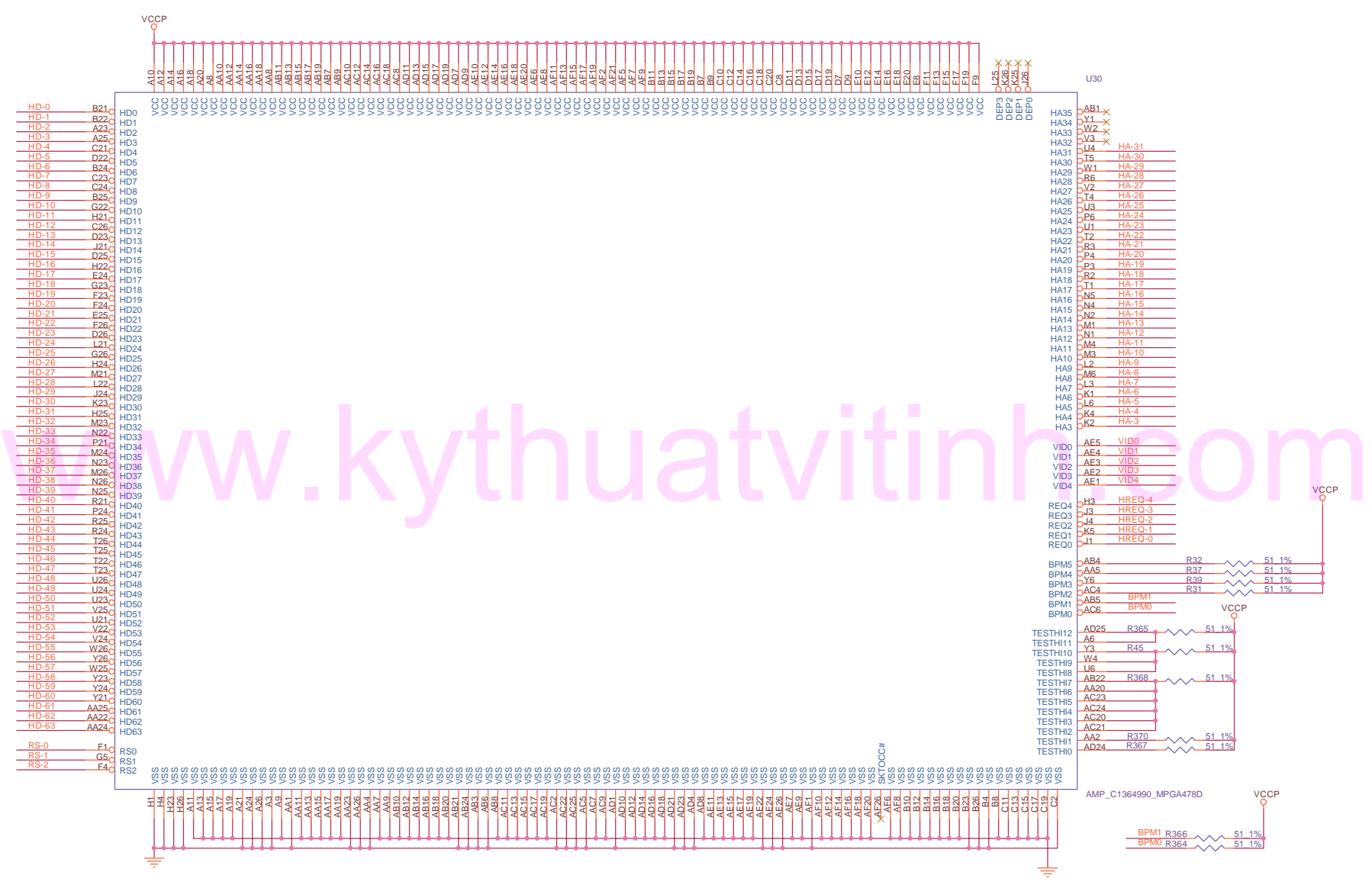
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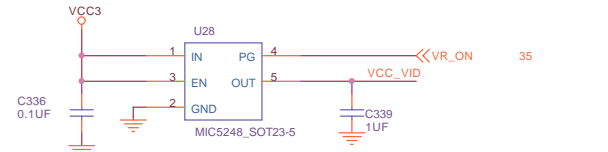
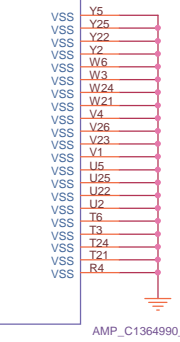
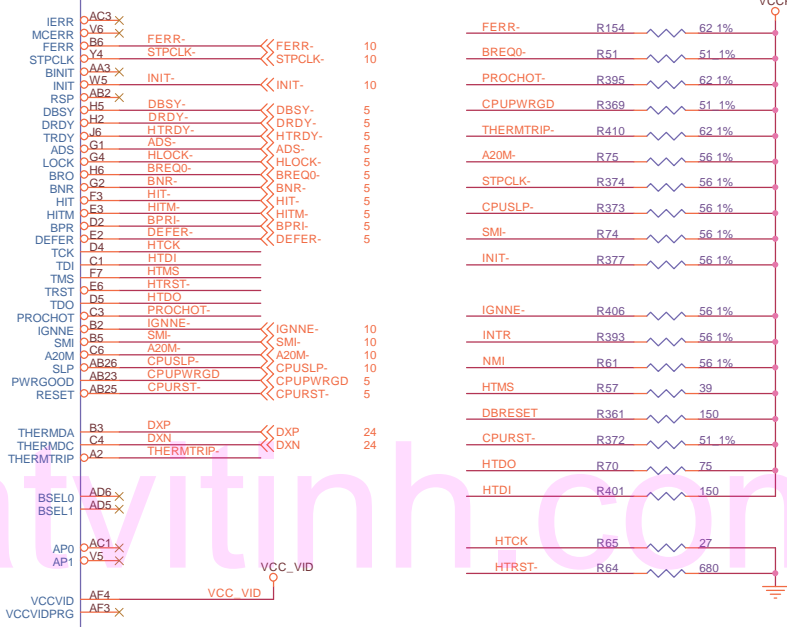
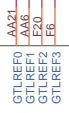
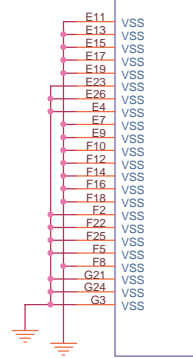
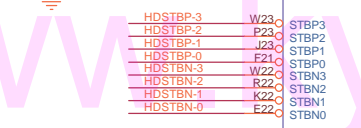
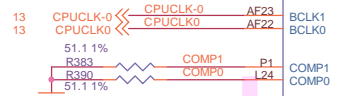
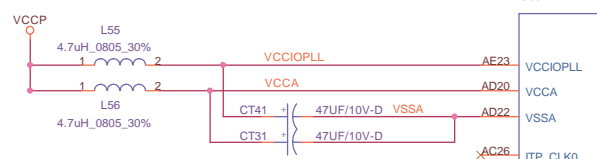
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- 5 HD-[0..63] << HD-[0..63]
- 5 HA-[3..31] << HA-[3..31]
- 5 HREQ-[0..4] << HREQ-[0..4]
- 35 VID-[0..4] << VID-[0..4]

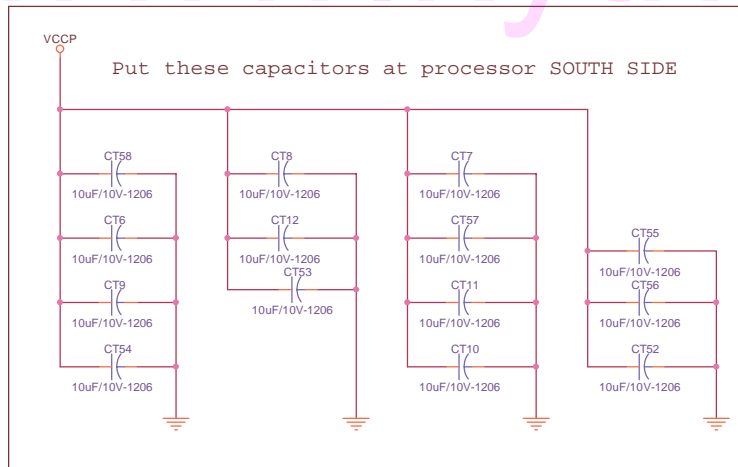
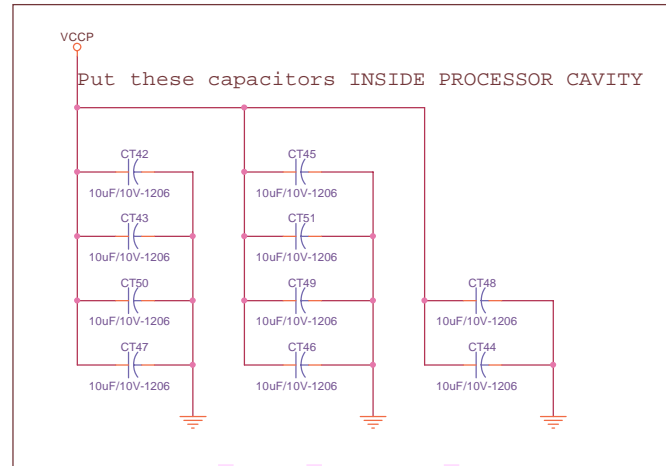
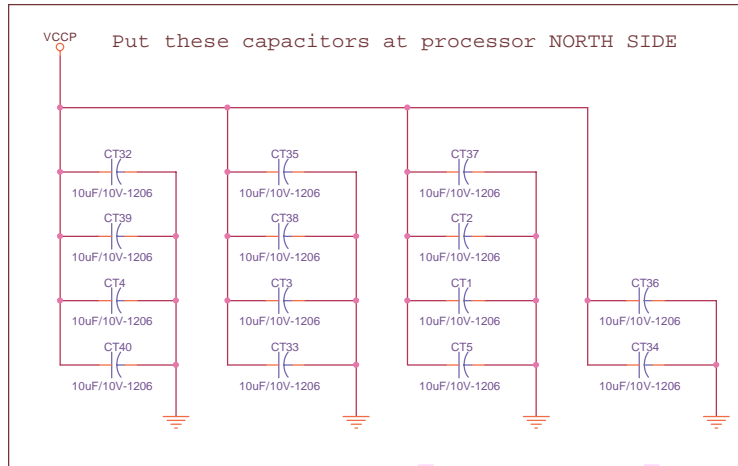
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- 5 HDSTBN-[0..3] << HDSTBN-[0..3]
- 5 DBI-[0..3] << DBI-[0..3]
- 5 HASTB-[0..1] << HASTB-[0..1]



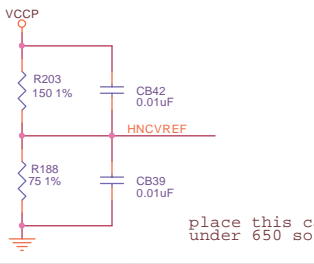
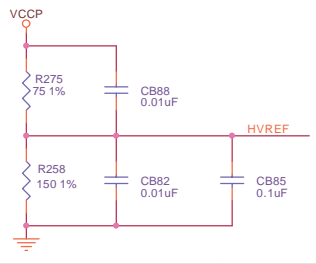
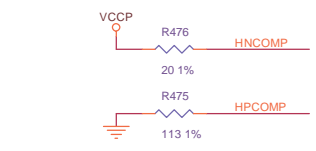
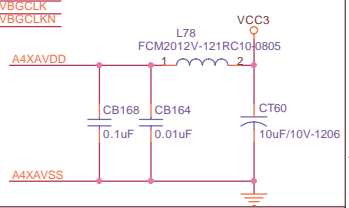
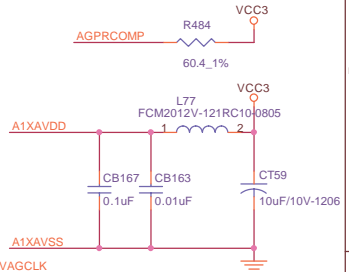
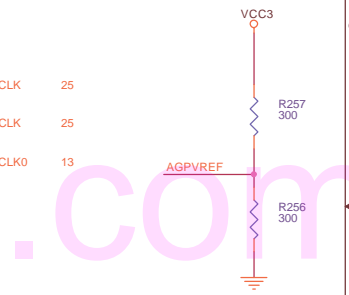
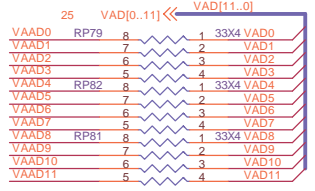
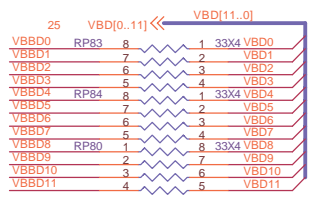
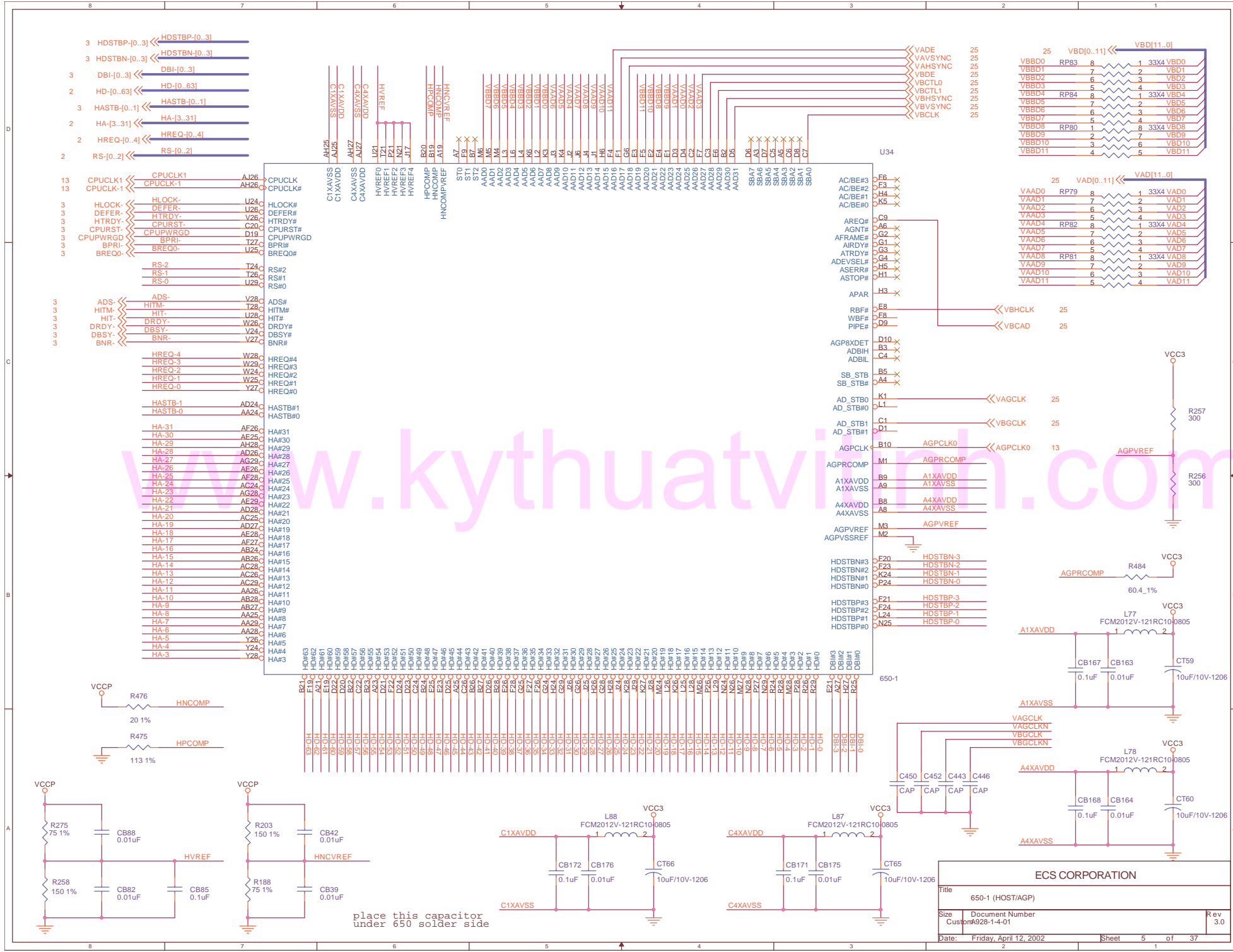
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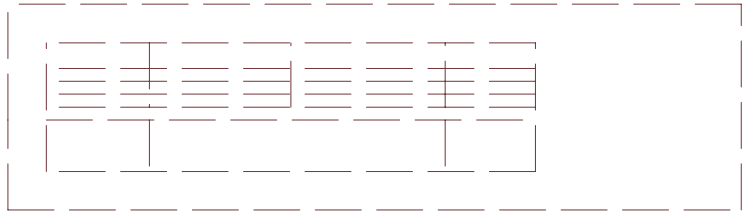
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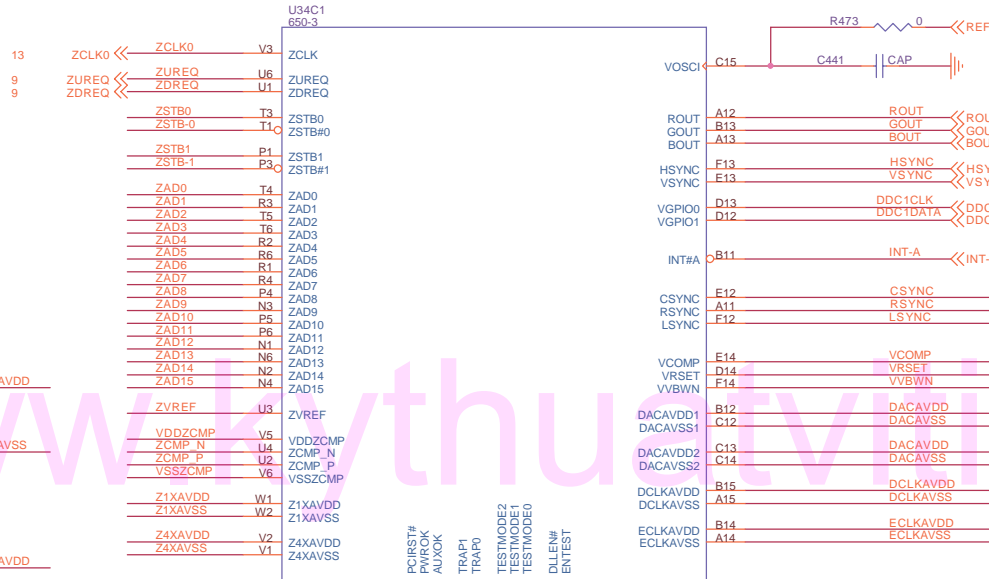
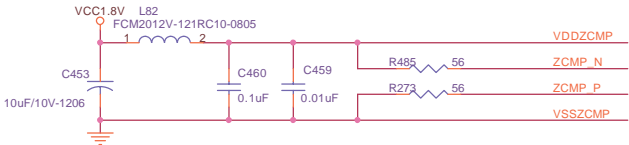
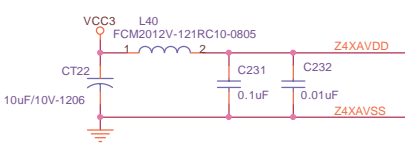
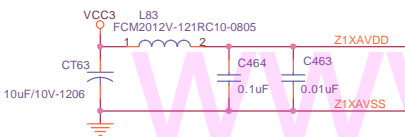
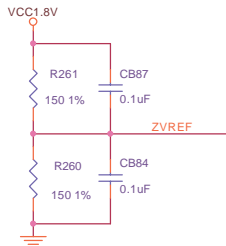
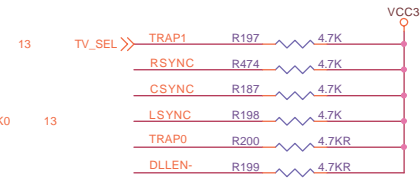
place this capacitor under 650 solder side

ECS CORPORATION			
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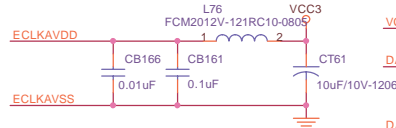
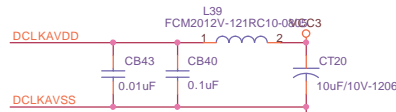
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 9 ZSTB[0..1] << ZSTB[0..1]
 9 ZSTB-[0..1] << ZSTB-[0..1]



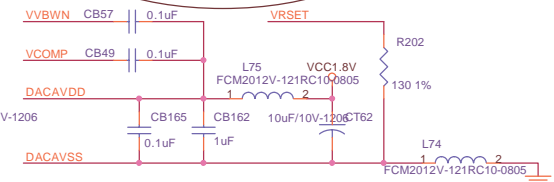
for 650 only



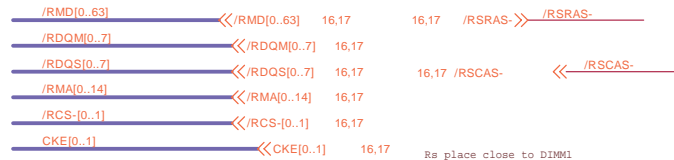
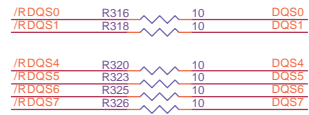
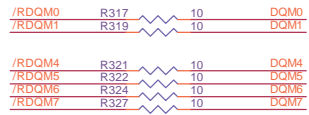
9,21,22,25,27,30,32 PCIRST- << PCIRST-
 10,29 PWRGD << PWRGD
 10,29 AUXOK << AUXOK



DEL CB17, CB18, L8, CE1
 Del one filter from APCKT0.91

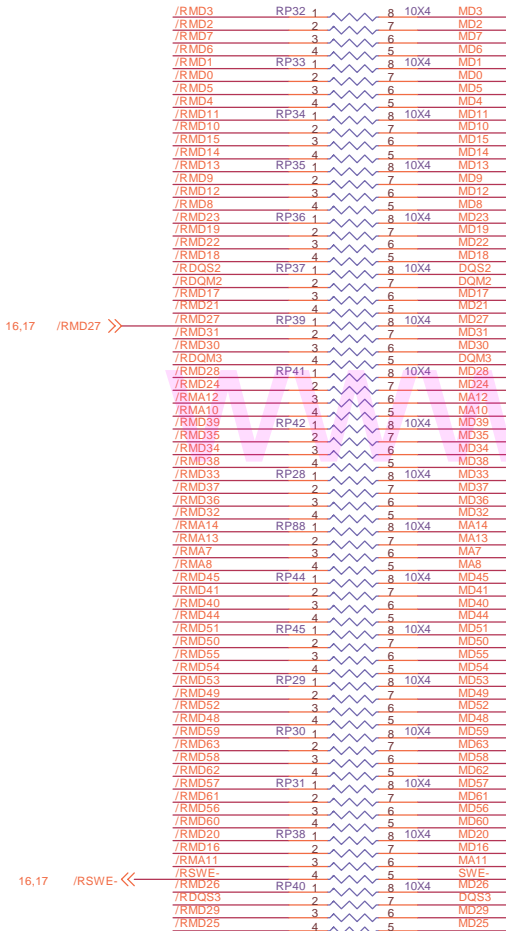


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Resistors place close to DIMM1

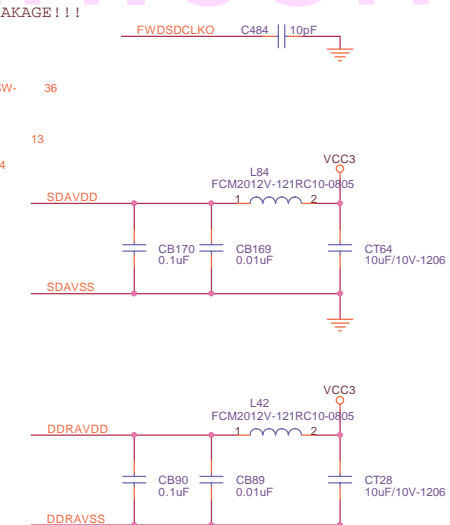
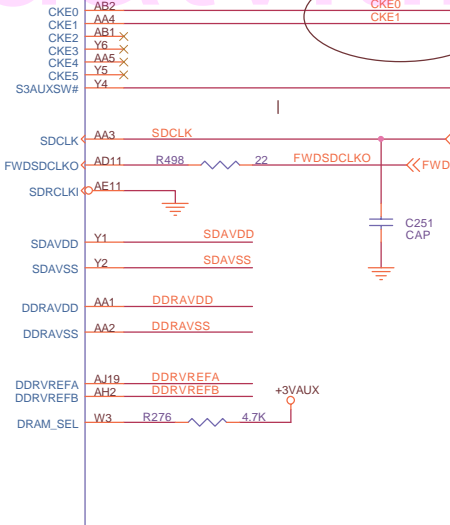
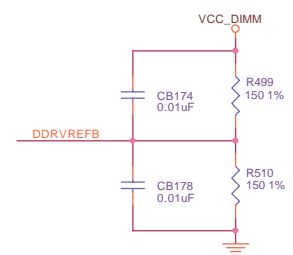
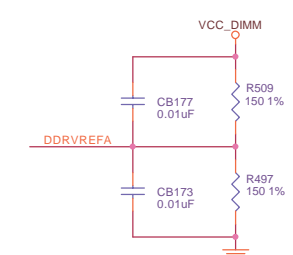
Rs place close to DIMM1



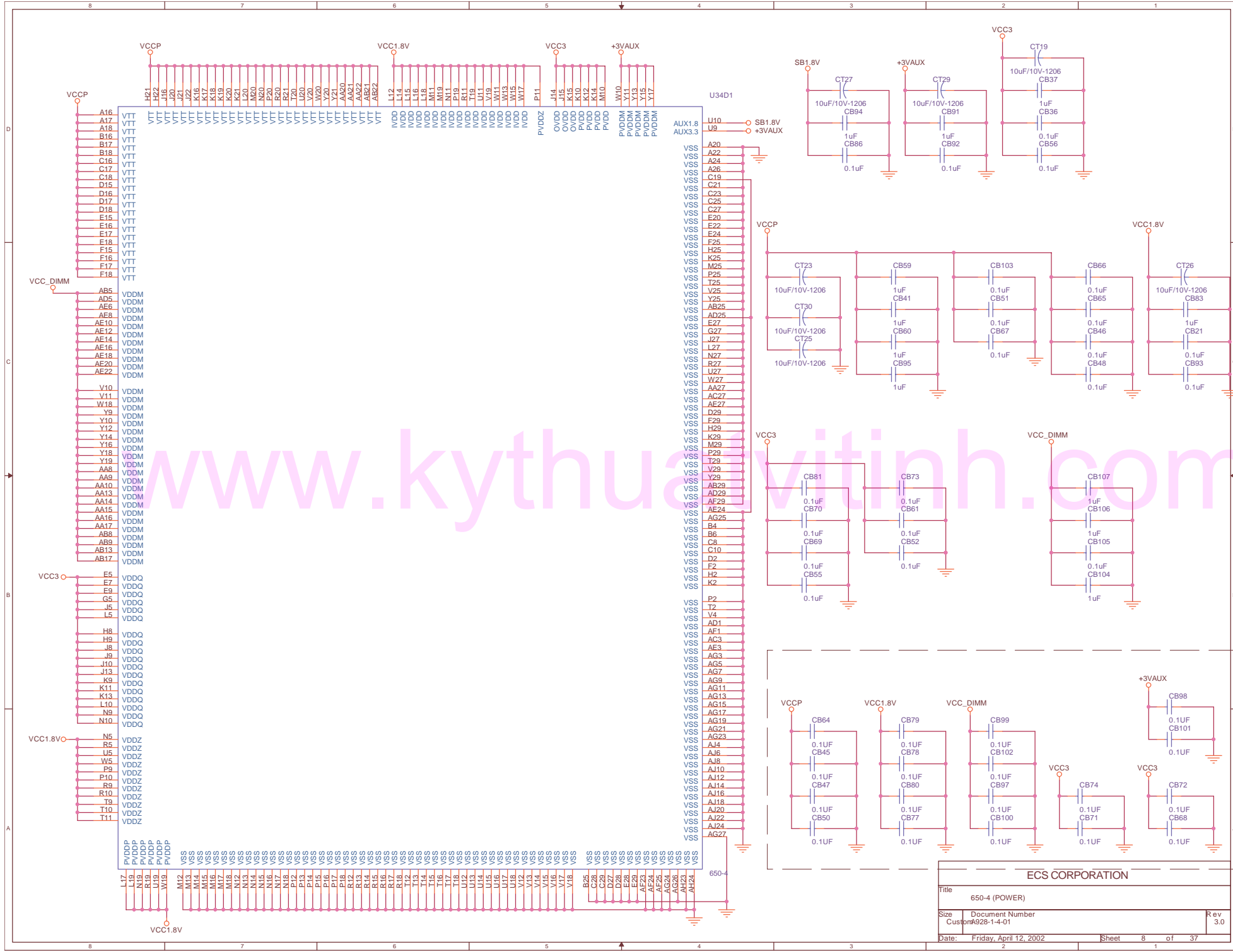
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MD7	AF21	MD7
MD8	AD22	MD8
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MD10	AE19	MD10
MD11	AF19	MD11
MD12	AE21	MD12
MD13	AD20	MD13
MD14	AD19	MD14
MD15	AH19	MD15
MD16	AF20	MD16
MD17	AH20	MD17
MD18	AG18	MD18
MD19	AD18	MD19
MD20	AD17	MD20
MD21	AD17	MD21
MD22	AE17	MD22
MD23	AJ17	MD23
MD24	AE17	MD24
MD25	AH18	MD25
MD26	AD14	MD26
MD27	AG14	MD27
MD28	AJ13	MD28
MD29	AE13	MD29
MD30	AJ13	MD30
MD31	AD13	MD31
MD32	AE13	MD32
MD33	AH14	MD33
MD34	AD10	MD34
MD35	AH10	MD35
MD36	AE9	MD36
MD37	AD8	MD37
MD38	AD9	MD38
MD39	AH9	MD39
MD40	AH5	MD40
MD41	AG4	MD41
MD42	AE5	MD42
MD43	AH3	MD43
MD44	AG6	MD44
MD45	AF6	MD45
MD46	AF5	MD46
MD47	AF4	MD47
MD48	AH4	MD48
MD49	AD6	MD49
MD50	AE2	MD50
MD51	AG5	MD51
MD52	AG2	MD52
MD53	AG1	MD53
MD54	AF3	MD54
MD55	AG6	MD55
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MD60	AG4	MD60
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MD62	AD2	MD62
MD63	AC1	MD63
MD64	AD4	MD64
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MD69	AD2	MD69
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MD71	AD2	MD71
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MD74	AD1	MD74
MD75	AD2	MD75
MD76	AD1	MD76
MD77	AD2	MD77
MD78	AD1	MD78
MD79	AD2	MD79
MD80	AD1	MD80
MD81	AD2	MD81
MD82	AD1	MD82
MD83	AD2	MD83
MD84	AD1	MD84
MD85	AD2	MD85
MD86	AD1	MD86
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MD94	AD1	MD94
MD95	AD2	MD95
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MD98	AD1	MD98
MD99	AD2	MD99
MD100	AD1	MD100

650-2

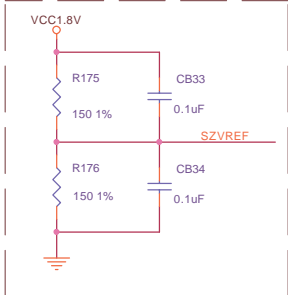
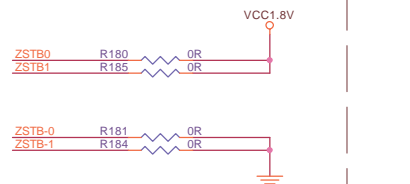
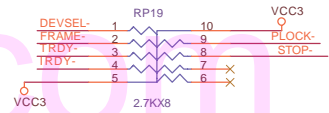
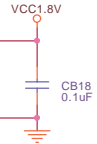
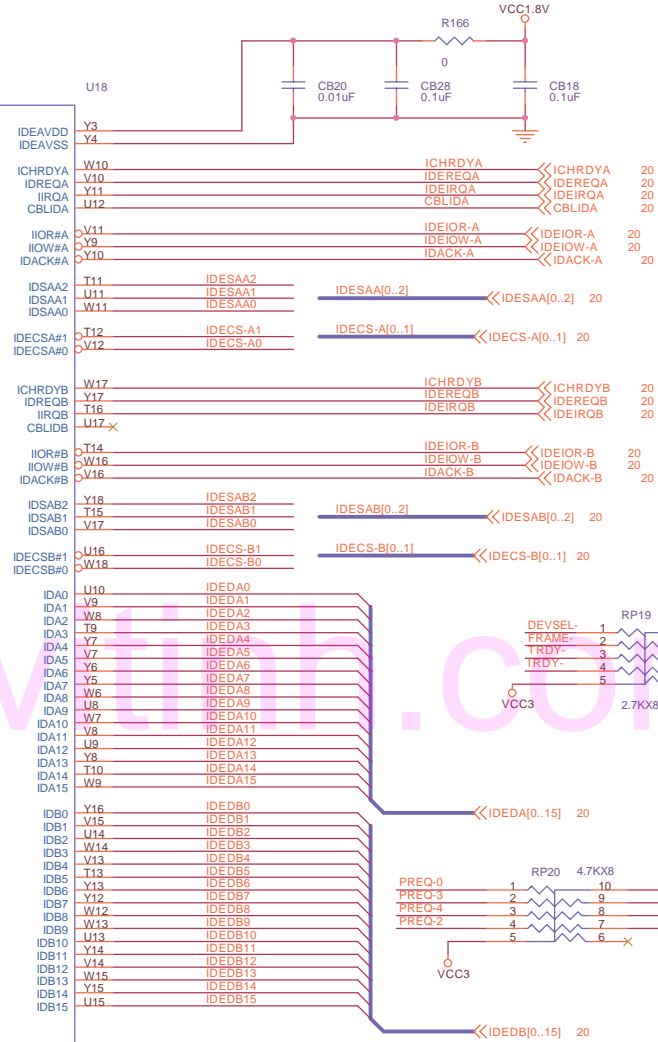
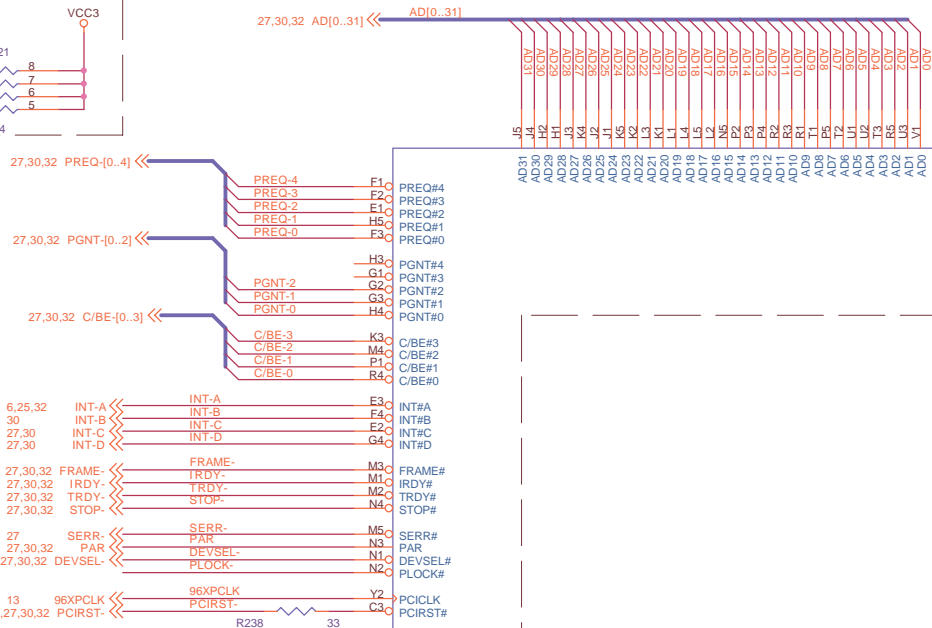
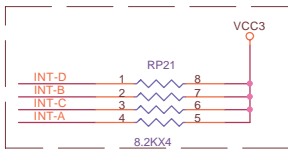
CURRENT LEAKAGE !!!



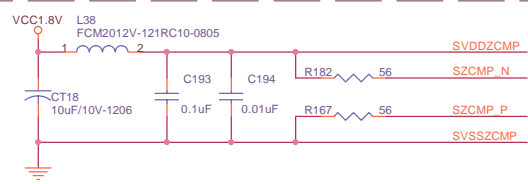
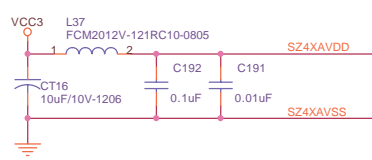
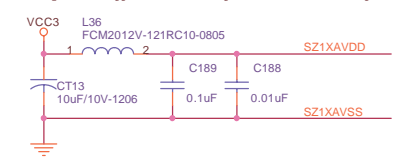
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Size: Custom	Document Number: 928-1-4-01	Rev: 3.0
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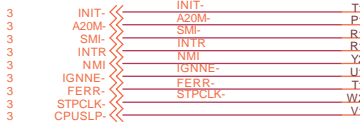


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Analog Power supplies of Transzip function for 961 Chip.





CPU_S



APIC



LPC



RTC

961A-2



GPIO



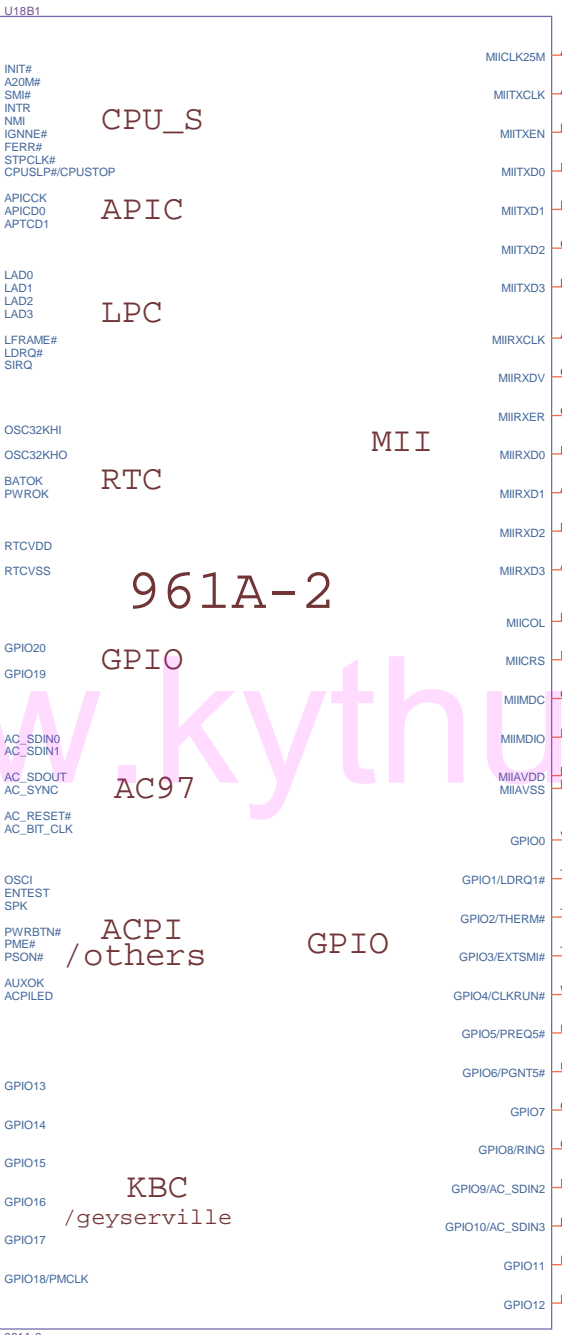
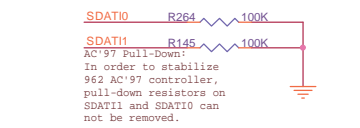
AC97



ACPI /others

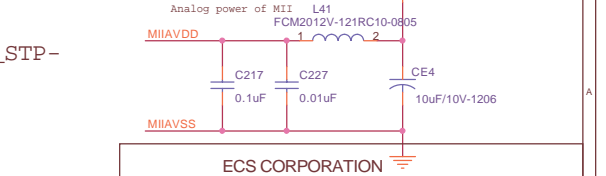
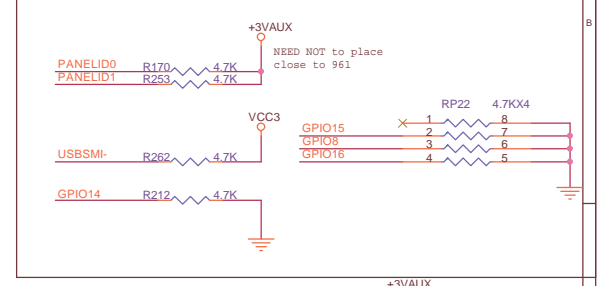
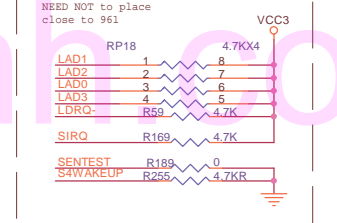
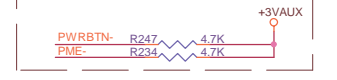
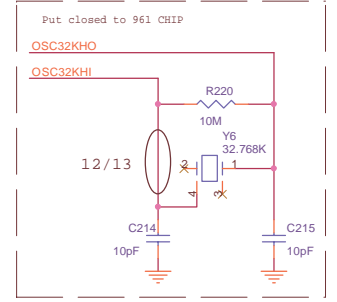
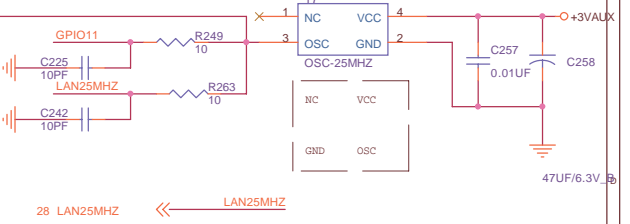
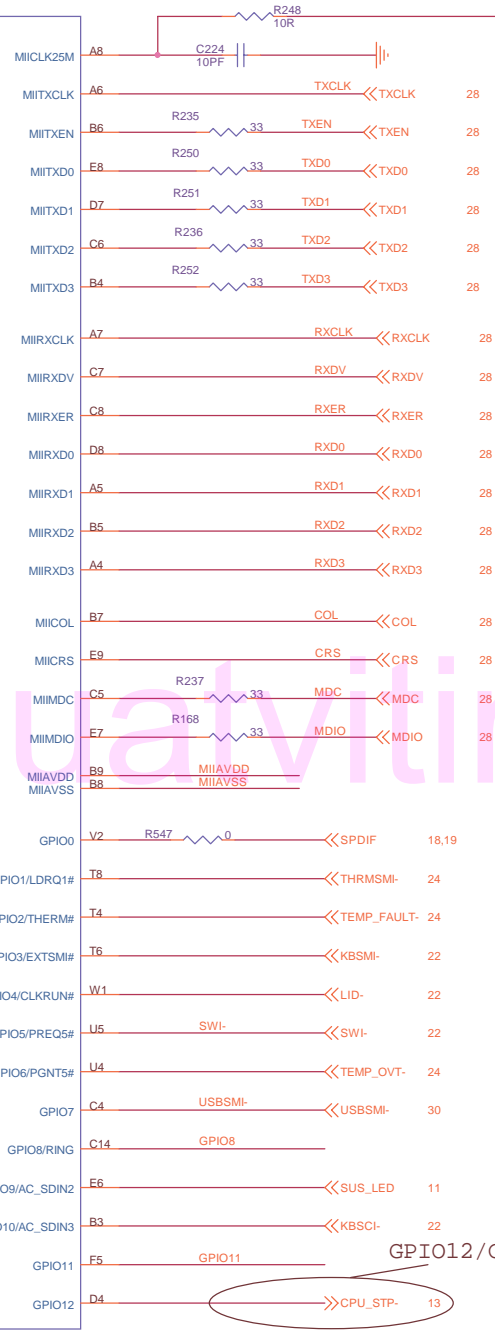


KBC /geyserville

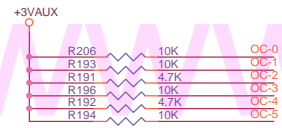
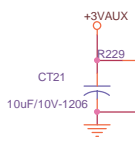
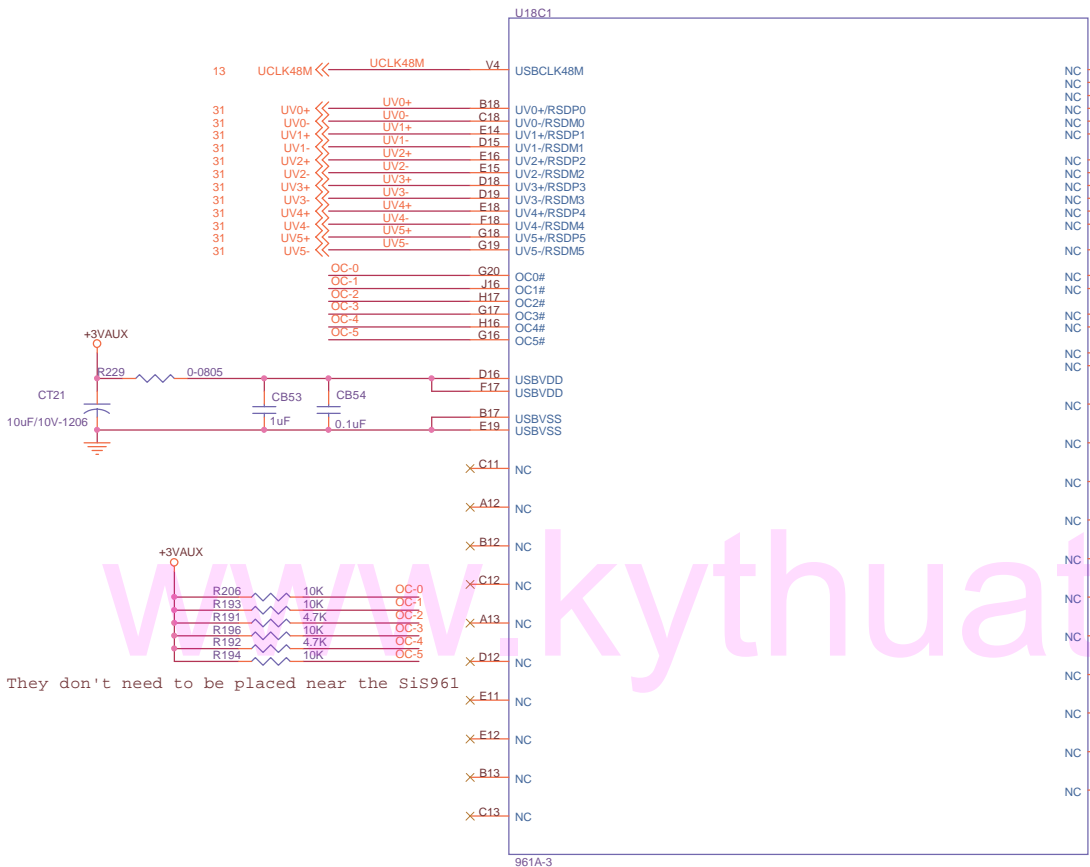


MII

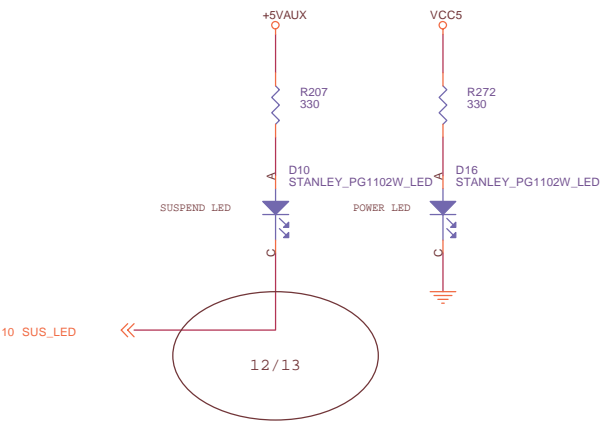
GPIO



ECS CORPORATION		
Title: 962-2 (Misc Signals)		
Size: Custom	Document Number: 928-1-4-01	Rev: 3.0
Date: Friday, April 12, 2002	Sheet: 10	of 37

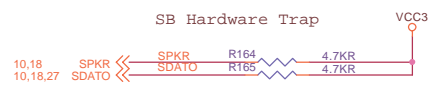


They don't need to be placed near the SiS961



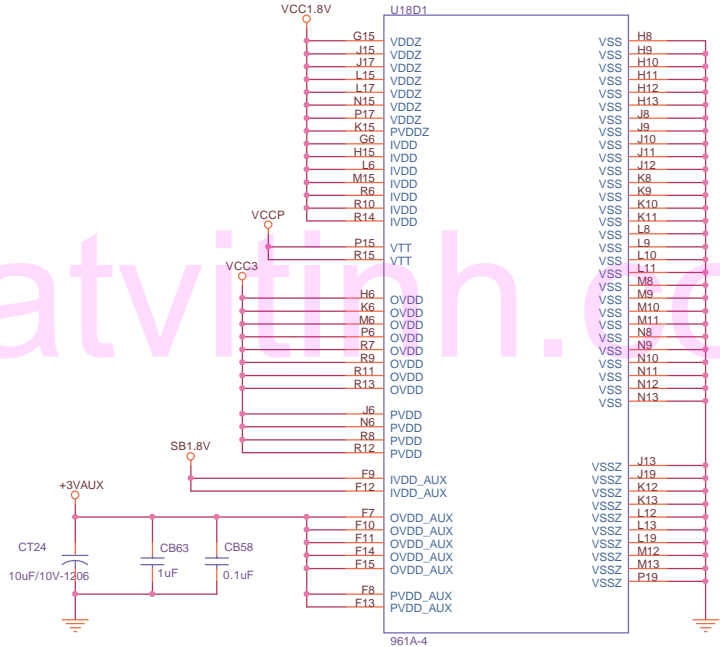
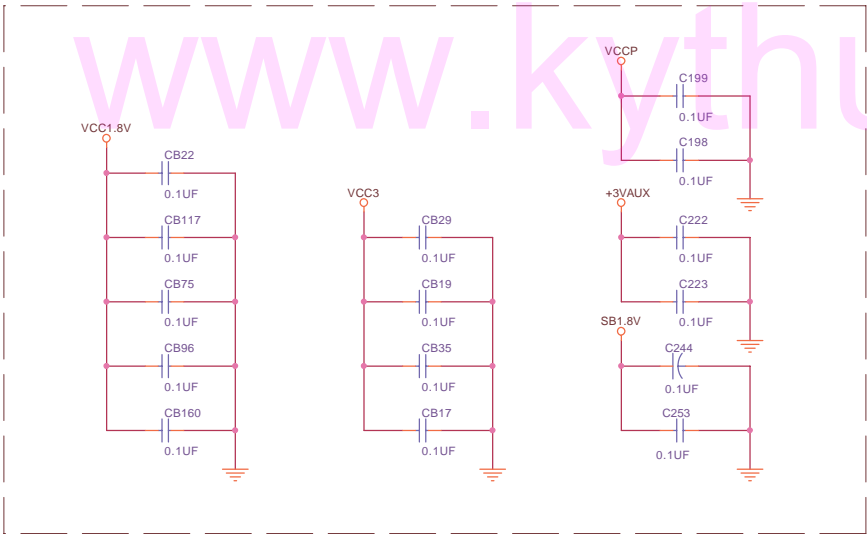
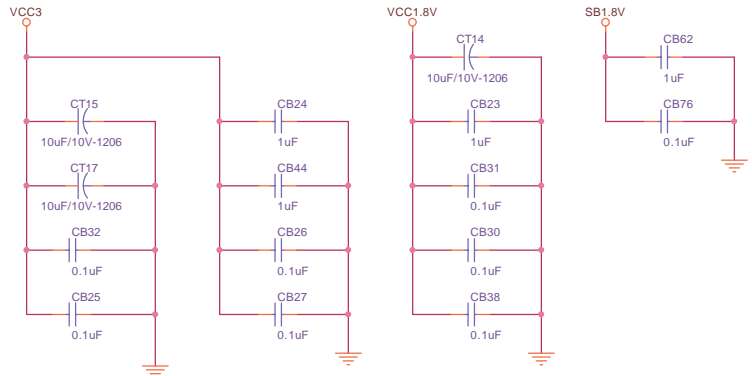
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SB Hardware Trap



	0	1	Default
SPKR(LPC addr mapping)	disable	enable	0
SDATO(PCICLK PLL)	enable	disable	0
OC2-(SB debug mode)	enable	disable	1
OC5-(Trap mode)	PCI AD	ROM	1

ECS CORPORATION		
Title	962-3 (USB/Others)	
Size	Document Number	Rev
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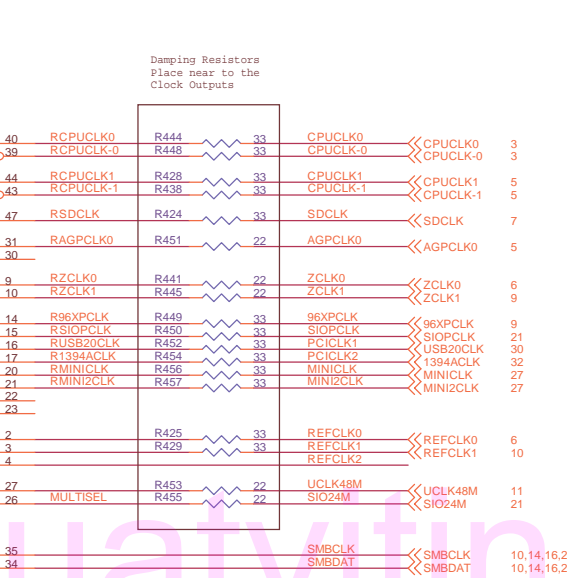
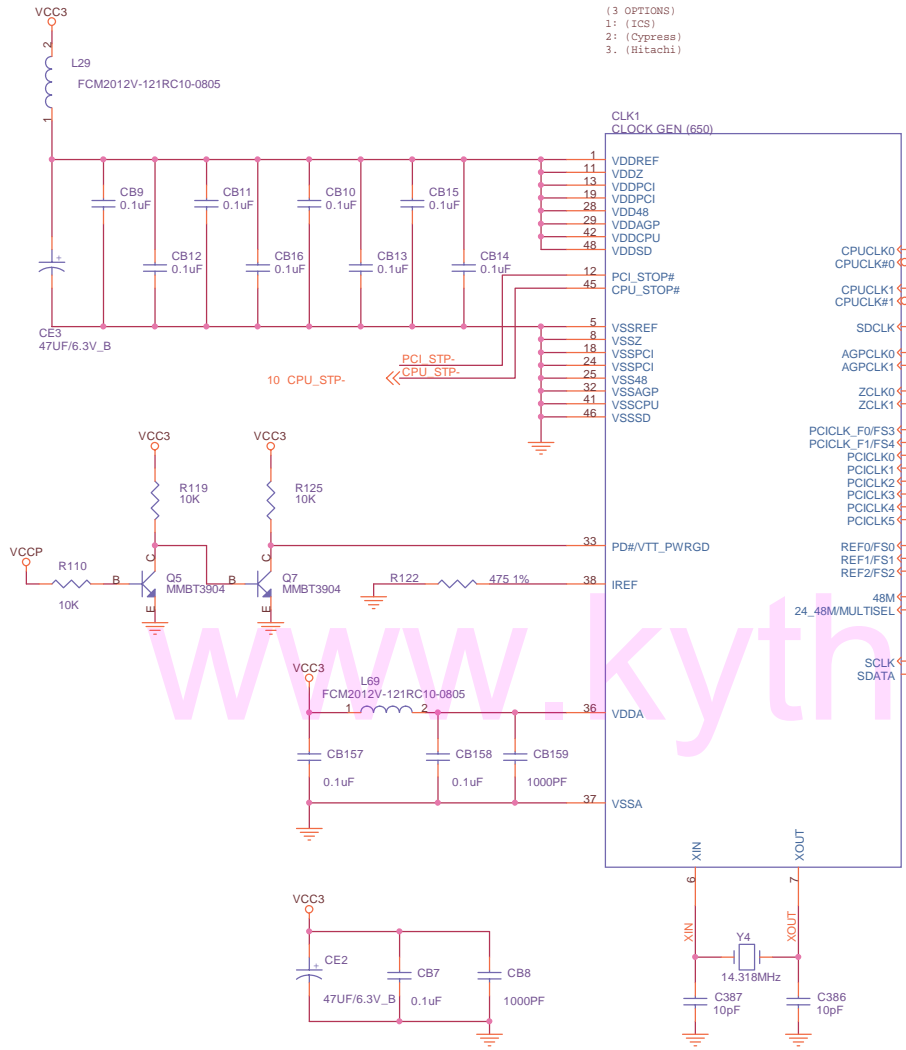


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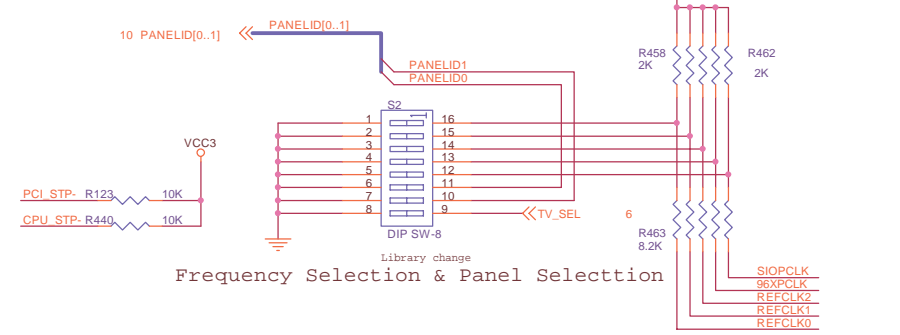
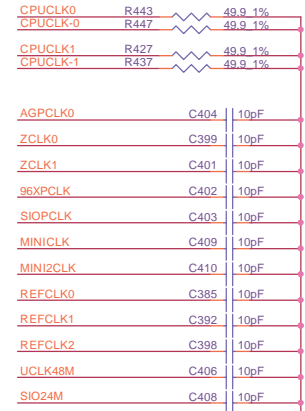
ECS CORPORATION			
Title			
962-4 (Powers)			
Size	Document Number		Rev
Custom	928-1-4-01		3.0
Date:	Friday, April 12, 2002	Sheet	12 of 37

Main Clock Generator

(3 OPTIONS)
 1: (ICS)
 2: (Cypress)
 3: (Hitachi)



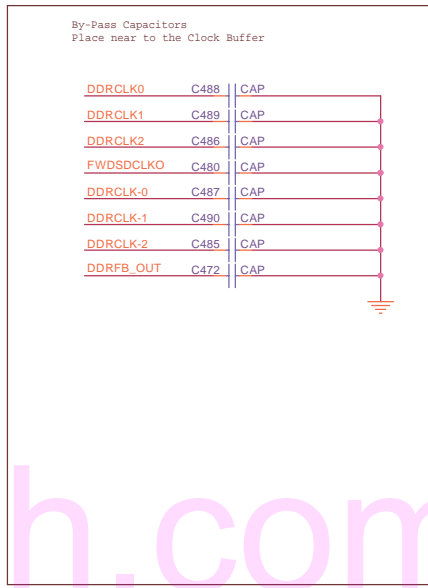
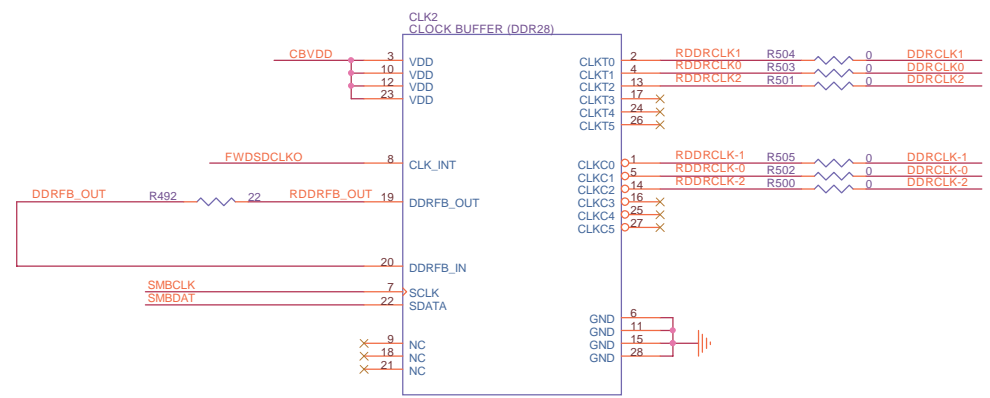
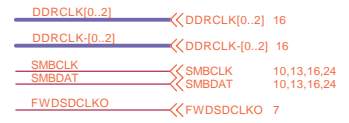
By-Pass Capacitors
Place near to the Clock Outputs



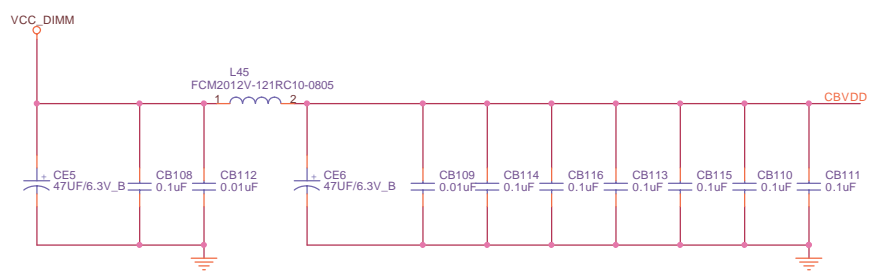
SIS650 CLOCK									
FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)
0	0	0	0	0	0				
0	0	0	0	1	0				
0	0	0	1	0	1				
0	0	0	1	1	0				
0	0	1	0	0	0				
0	0	1	0	1	0				
0	0	1	1	0	0				
0	0	1	1	1	0				
0	1	0	0	0	1				
0	1	0	0	1	0				
0	1	0	1	0	0				
0	1	0	1	1	0				
0	1	1	0	0	1				
0	1	1	0	1	0				
0	1	1	1	0	0				
0	1	1	1	1	0				

SIS650 CLOCK									
FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)
1	0	0	0	0	0				
1	0	0	0	1	0				
1	0	0	1	0	1				
1	0	0	1	1	0				
1	0	1	0	0	0				
1	0	1	0	1	0				
1	0	1	1	0	0				
1	0	1	1	1	0				
1	1	0	0	0	1				
1	1	0	0	1	0				
1	1	0	1	0	0				
1	1	0	1	1	0				
1	1	1	0	0	1				
1	1	1	0	1	0				
1	1	1	1	0	0				
1	1	1	1	1	0				

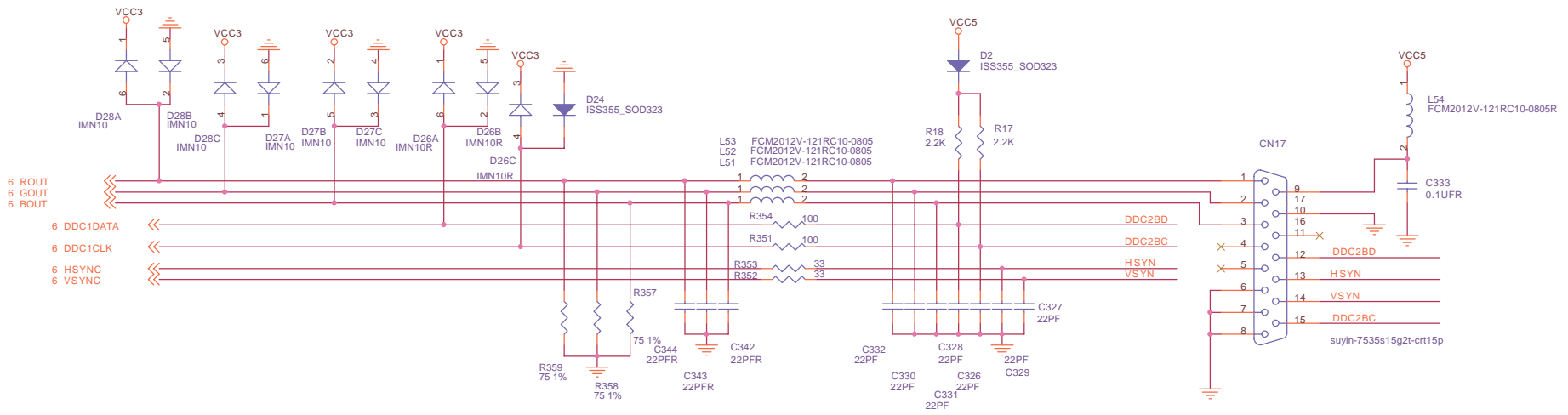




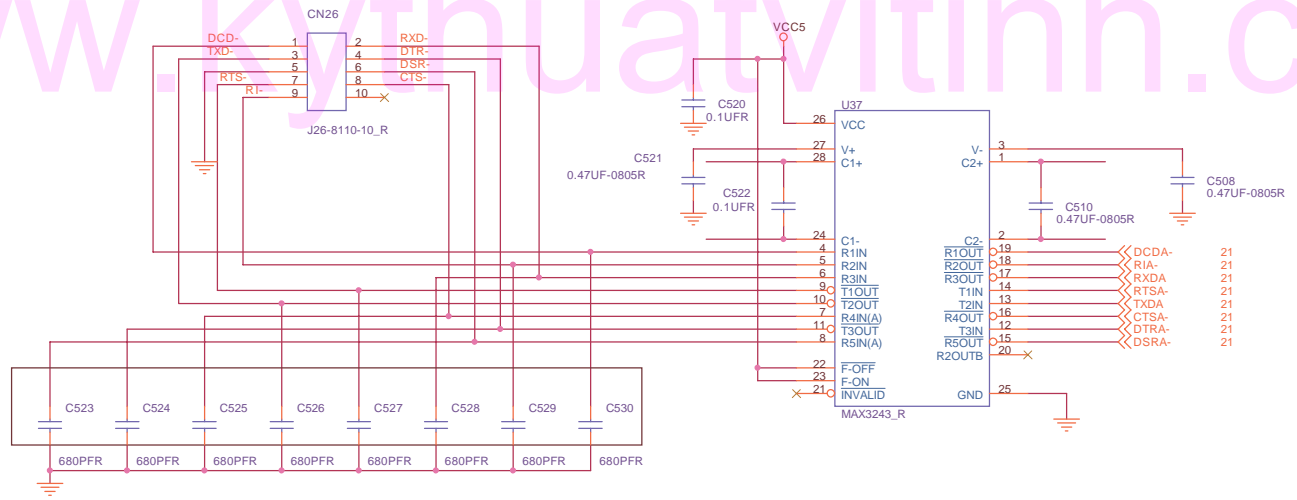
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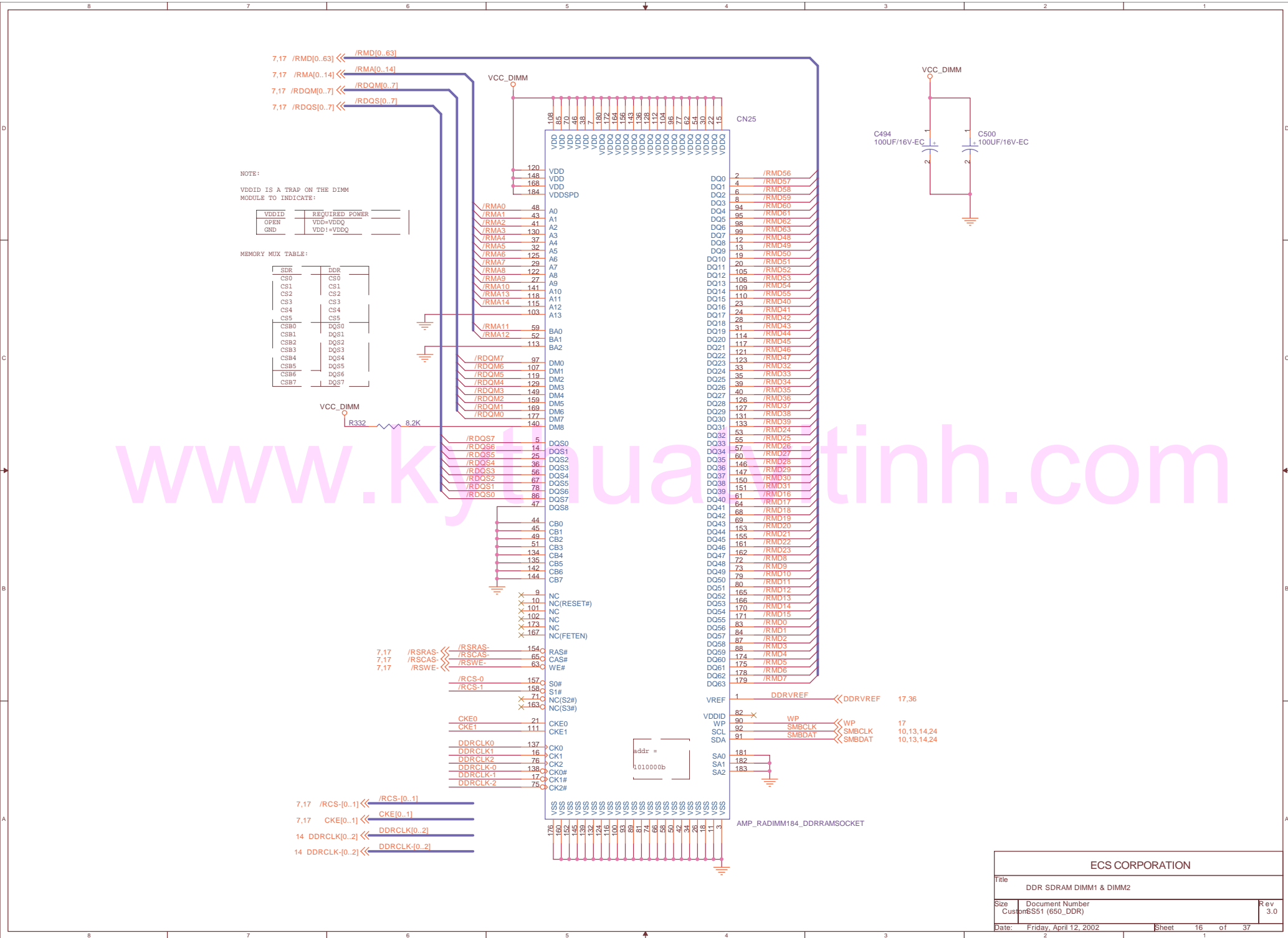
ECS CORPORATION		
Title CLOCK_BUFFER (DDR)		
Size Custom	Document Number A928-1-4-01	Rev 3.0
Date Friday, April 12, 2002	Sheet 14	of 37



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ECS CORPORATION		
Title CRT CONN.		
Size	Document Number	Rev
Customer	928-1-4-01	3.0
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NOTE:

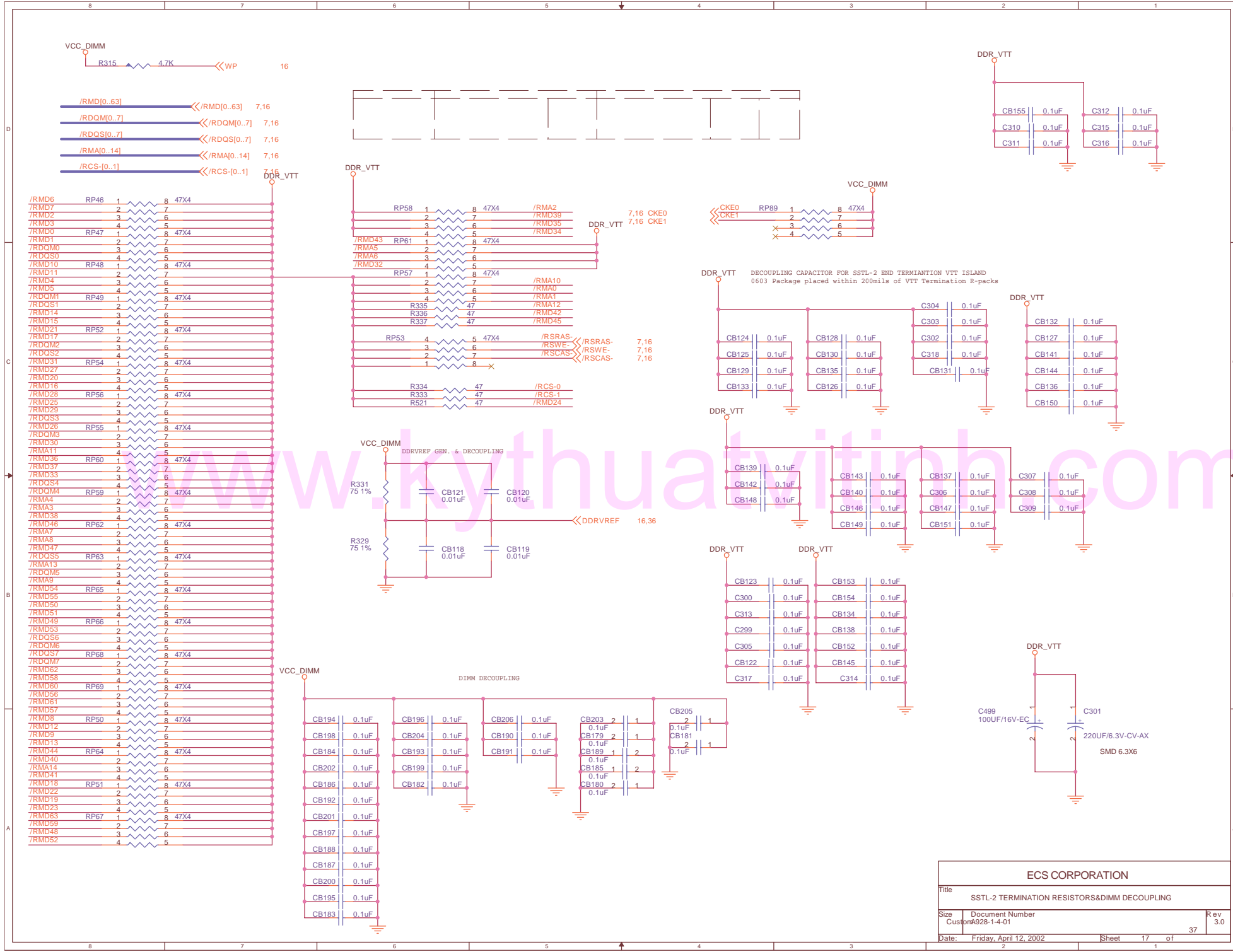
VDDID IS A TRAP ON THE DIMM MODULE TO INDICATE:

VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDD!=VDDQ

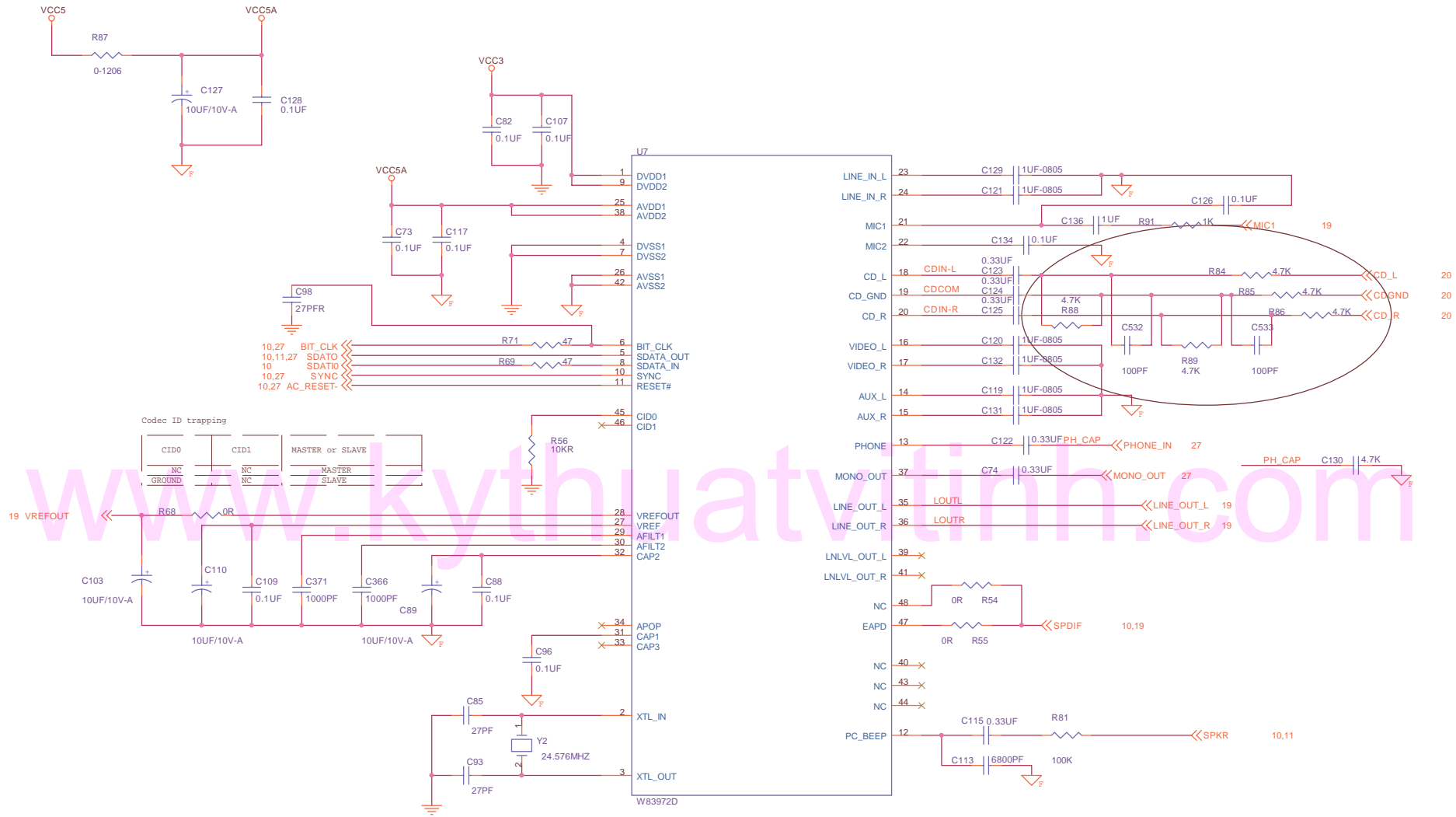
MEMORY MIX TABLE:

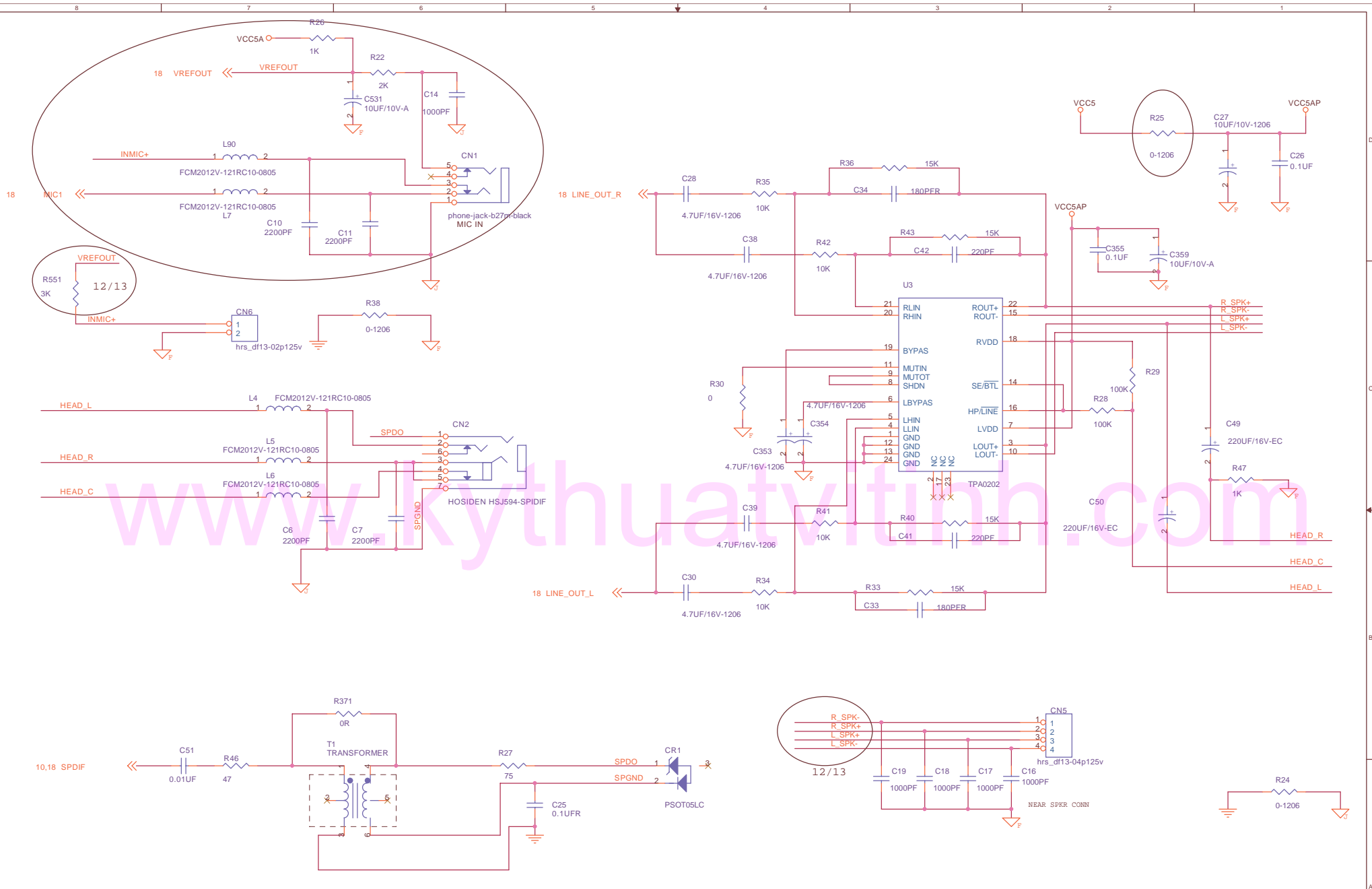
SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQ80
CSB1	DQ81
CSB2	DQ82
CSB3	DQ83
CSB4	DQ84
CSB5	DQ85
CSB6	DQ86
CSB7	DQ87

ECS CORPORATION			
Title DDR SDRAM DIMM1 & DIMM2			
Size	Document Number	Rev	
Customer	SS51 (650_DDR)	3.0	
Date:	Friday, April 12, 2002	Sheet	16 of 37



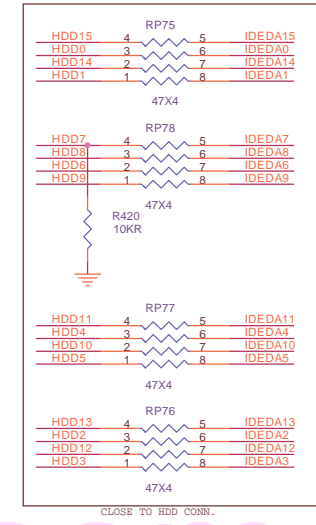
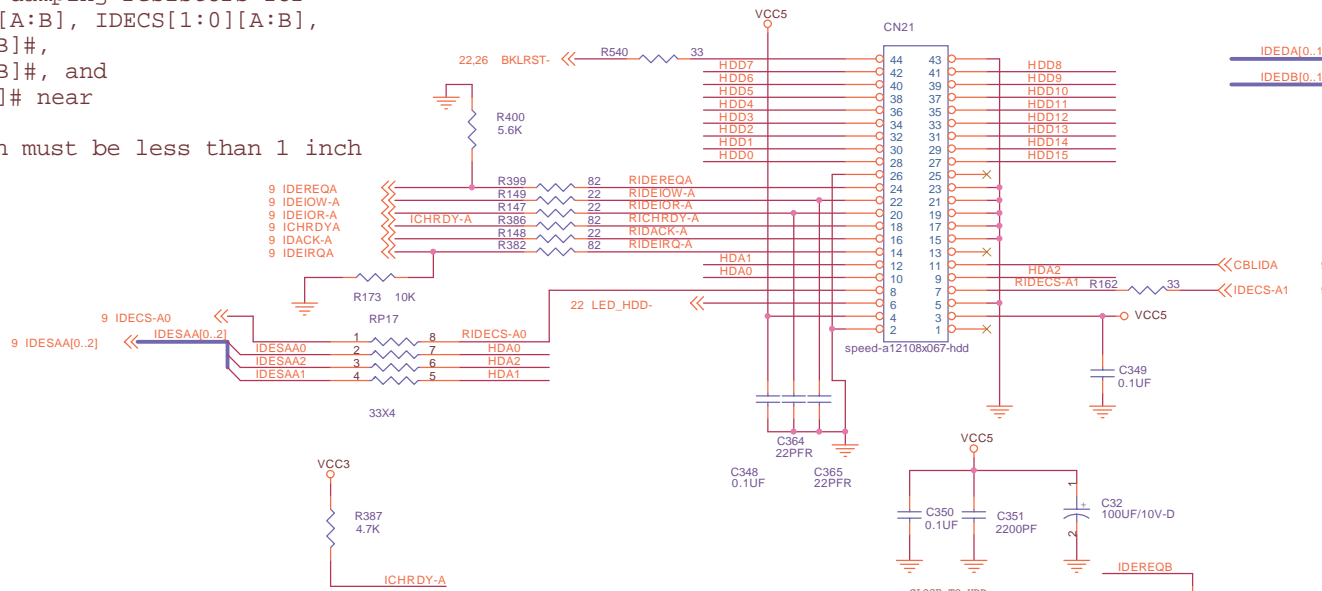
ECS CORPORATION		
Title		
SSTL-2 TERMINATION RESISTORS&DIMM DECOUPLING		
Size	Document Number	Rev
Custom#928-1-4-01		3.0
Date:	Friday, April 12, 2002	Sheet 17 of 37



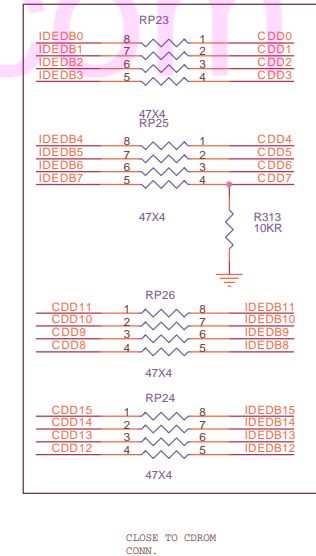
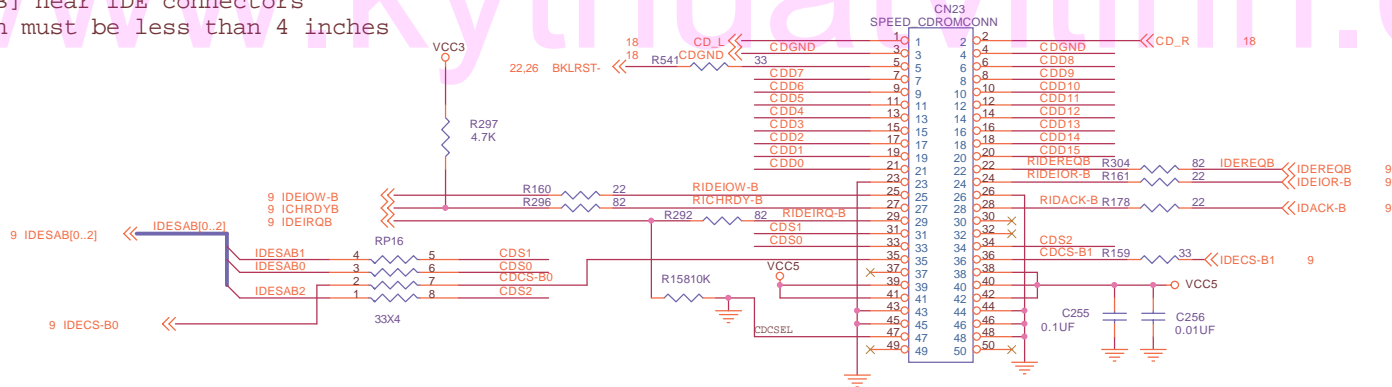


ECS CORPORATION		
Title OP AMPLIFIER		
Size B	Document Number A928-1-4-01	Rev 3.0
Date: Friday, April 12, 2002	Sheet 19	of 37

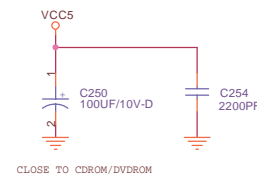
Place the damping resistors for
 IDEA[2:0][A:B], IDECS[1:0][A:B],
 IDEIOR[A:B]#,
 IDEIOW[A:B]#, and
 IDACK[A:B]# near
 SiS650
 The length must be less than 1 inch

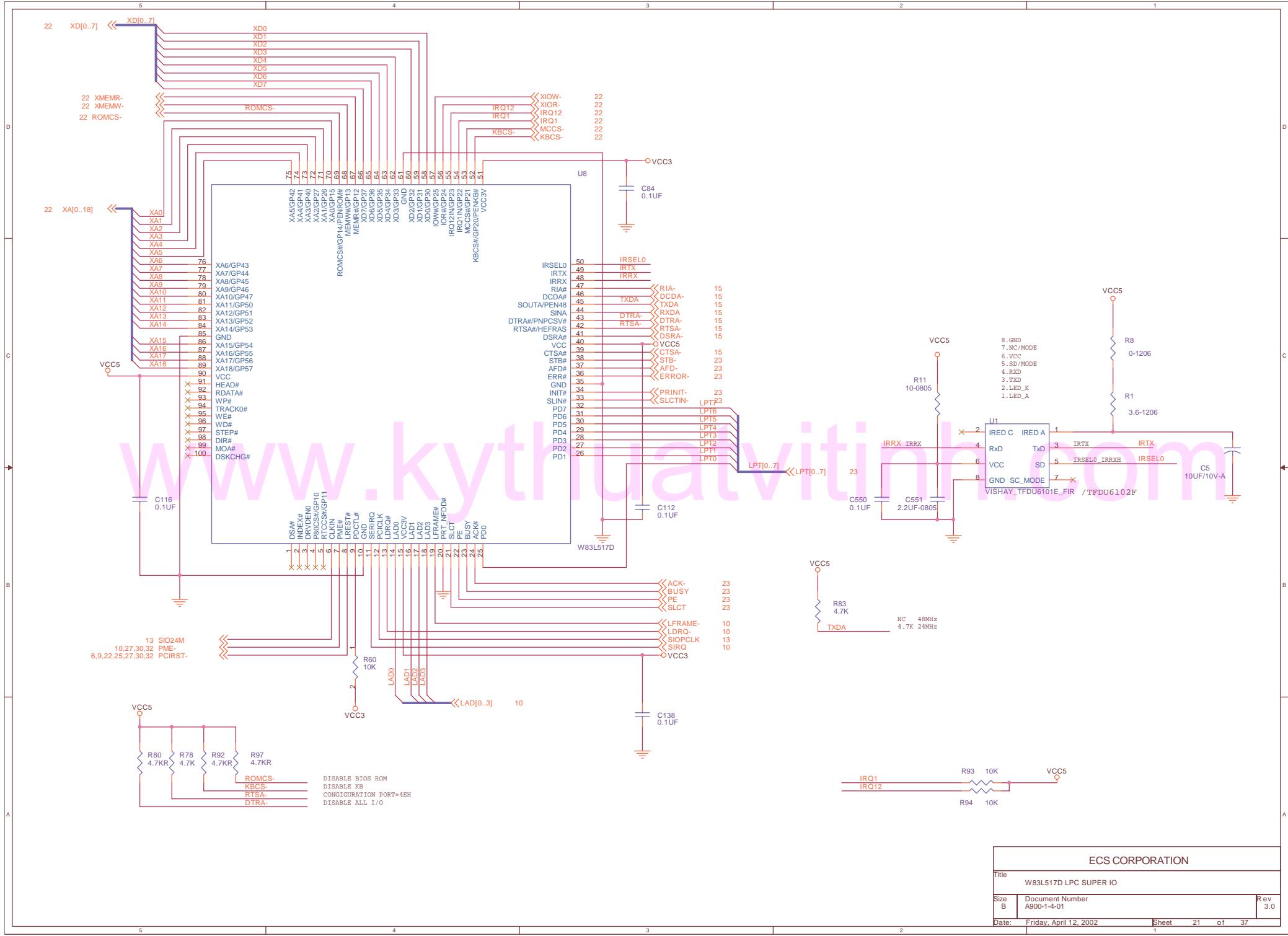


Place the damping resistors for IDED[15:0][A:B], IDREQ[A:B], ICHRDY[A:B], and
 IDEIRQ[A:B] near IDE connectors
 The length must be less than 4 inches

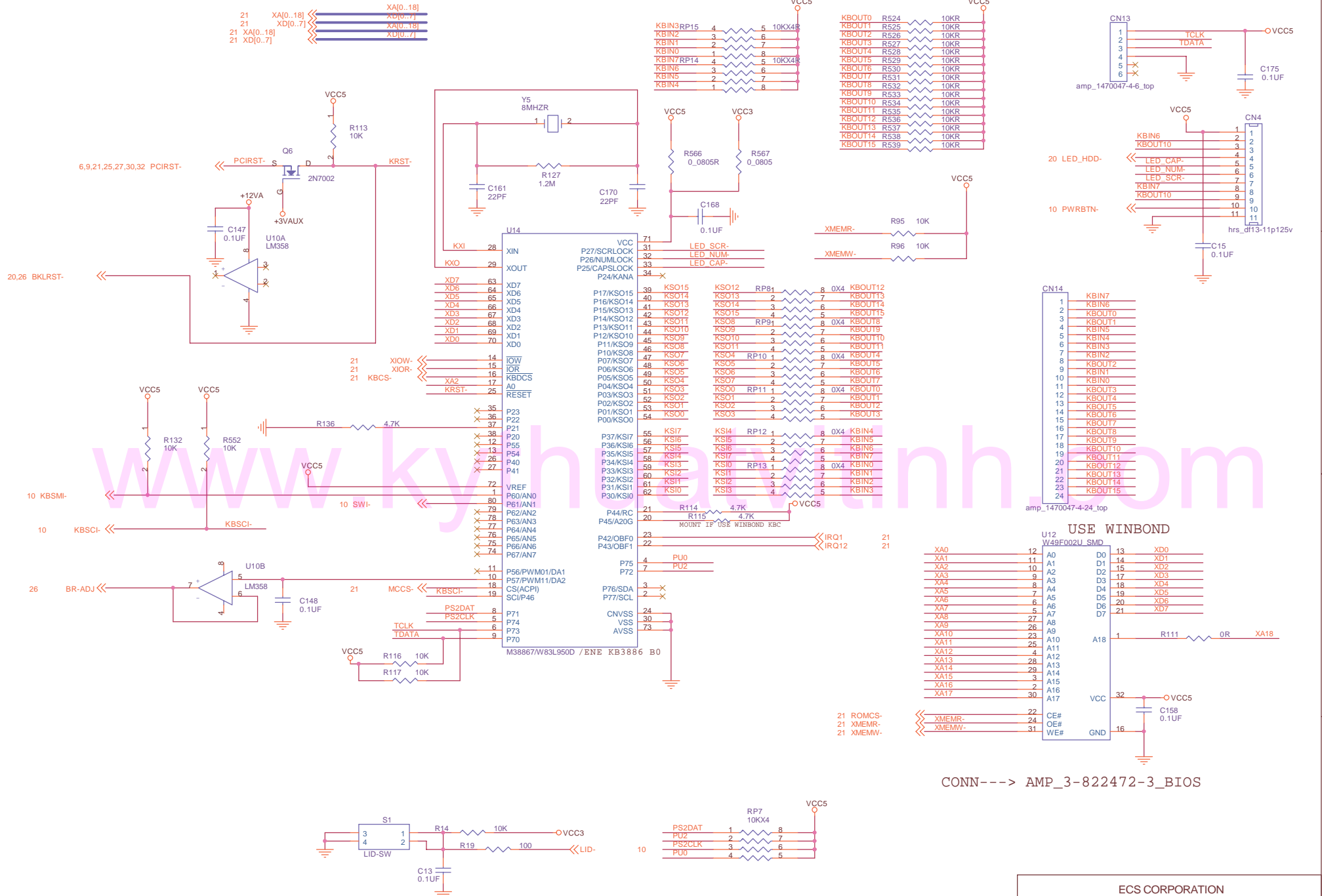


CSEL : "NC" ; "H1" --> Master(CDR0M)/Slave(DVDR0M)
 CSEL : "Low" --> Slave(CDR0M)/Master(DVDR0M)



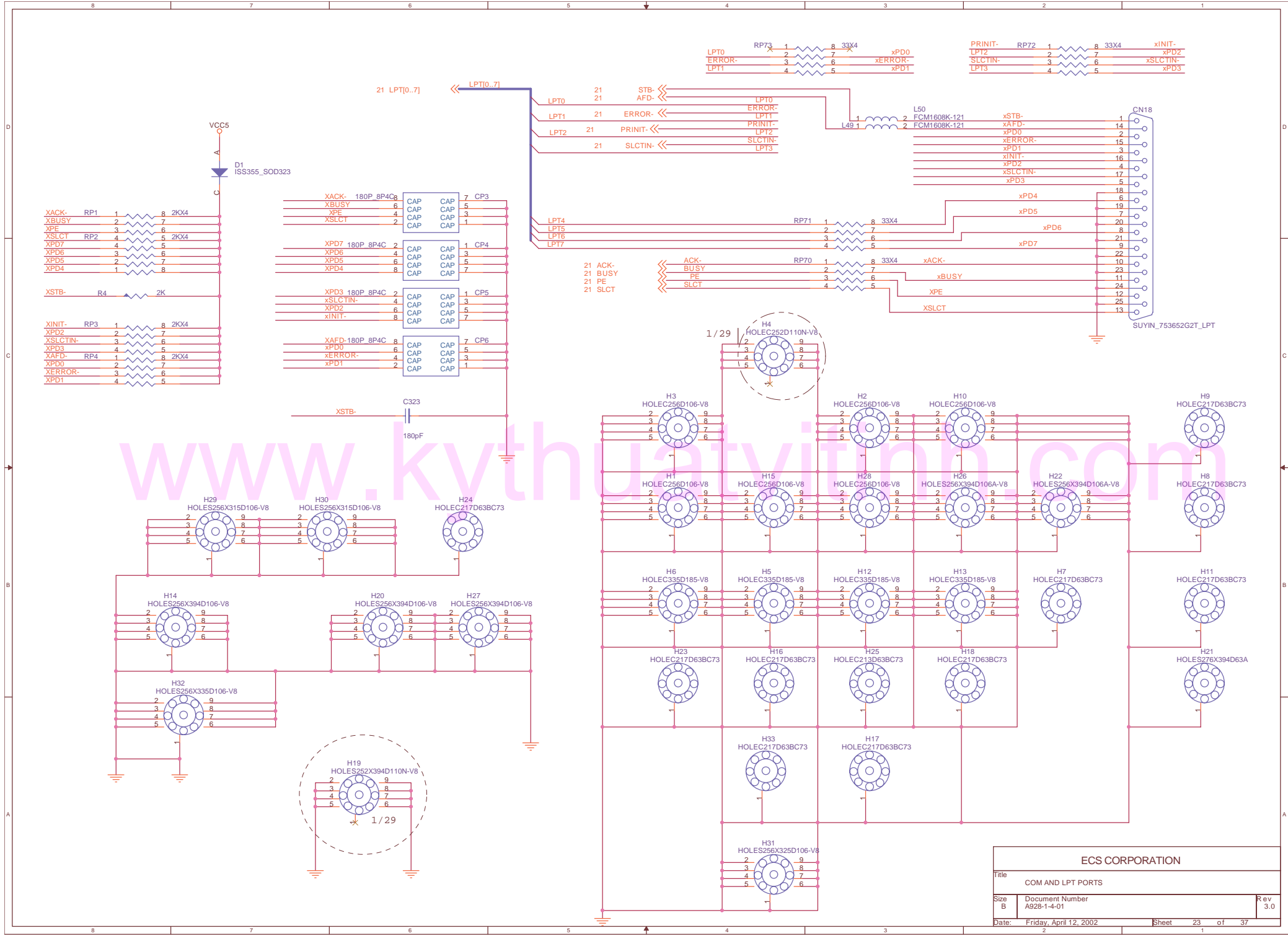


ECS CORPORATION		
Title W83L517D LPC SUPER IO		
Size B	Document Number A900-1-4-01	Rev 3.0
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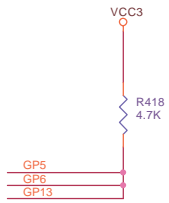


ECS CORPORATION		
Title KBC M38867		
Size B	Document Number A900-1-4-01	Rev 3.0
Date: Friday, April 12, 2002	Sheet 22	of 37

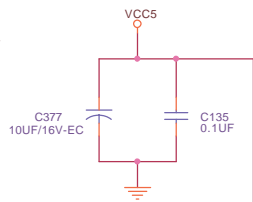
CONN----> AMP_3-822472-3_BIOS



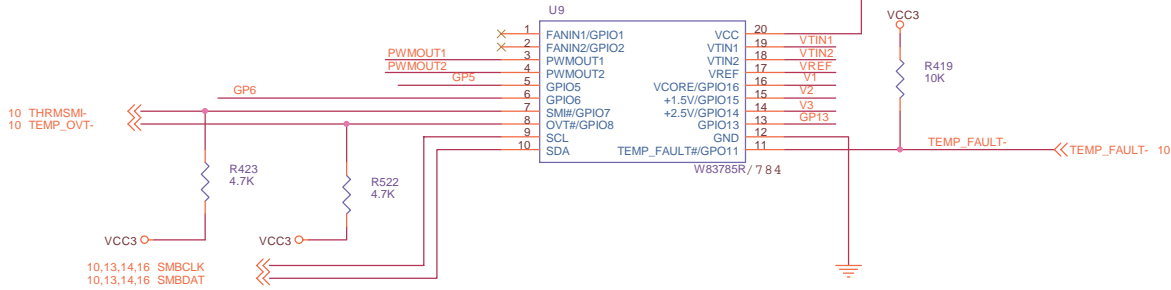
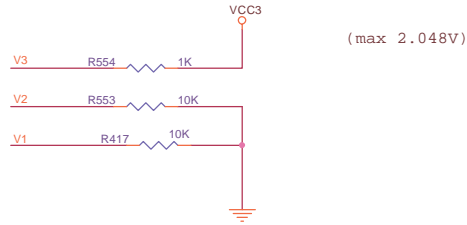
ECS CORPORATION		
Title	COM AND LPT PORTS	
Size	Document Number	Rev
B	A928-1-4-01	3.0
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ALL GPIO PIN Must add pull-up resistor

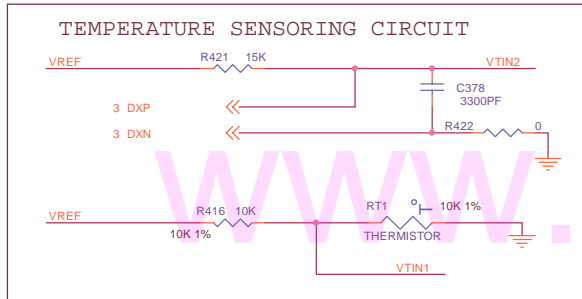


VOLTAGE SENSING CIRCUIT

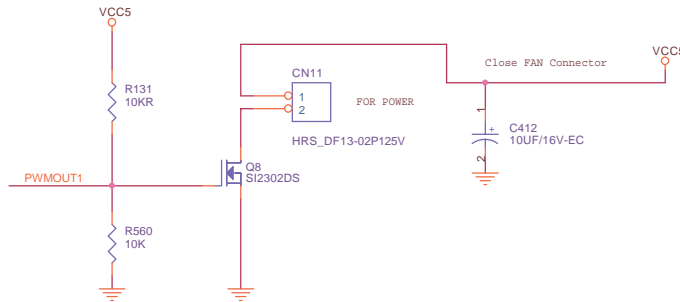
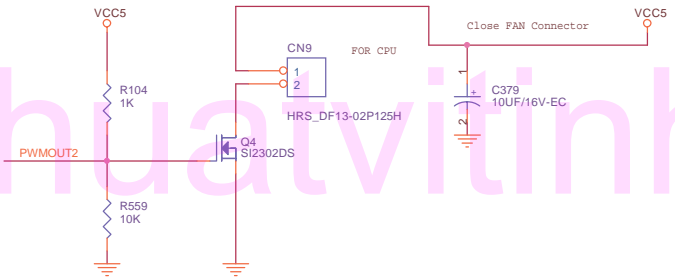


Rev.

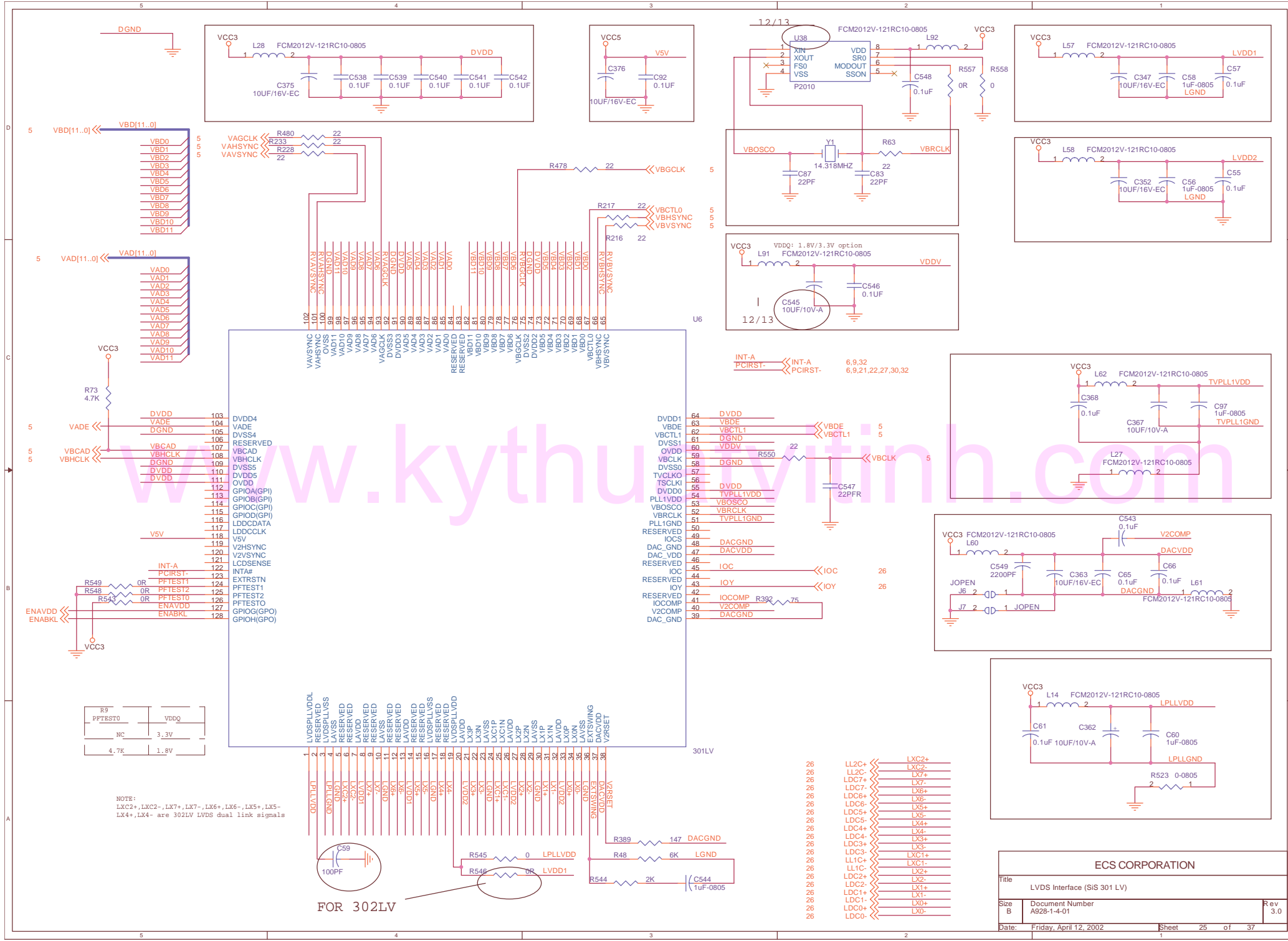
- 0.1:W83L785R application circuit. 3.3VCC
- 0.2:R29 30K change to 15K
- 0.3:R44,R45,R46 1K change to 4.7K



W83784 : MOUNT R559 R560 ; REMOVE R104 R131
 W83785 : MOUNT R104 R131 ; REMOVE R559 R560



ECS CORPORATION		
Title	W83L785R	
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NOTE:
 LXC2+, LXC2-, LX7+, LX7-, LX6+, LX6-, LX5+, LX5-, LX4+, LX4- are 302LV LVDS dual link signals

FOR 302LV

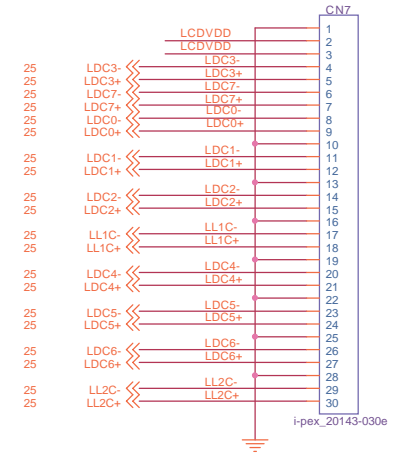
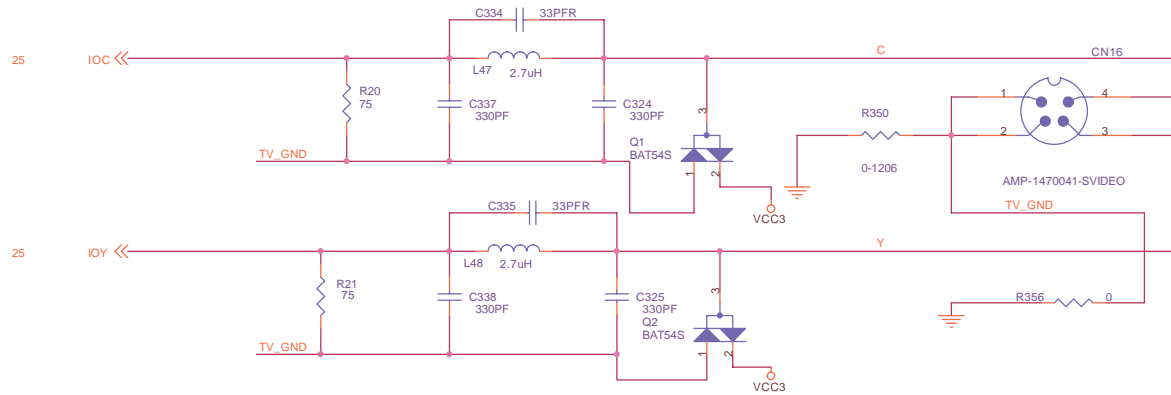
ECS CORPORATION		
Title LVDS Interface (SIS 301 LV)		
Size B	Document Number A928-1-4-01	Rev 3.0
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- 26 LL2C+ << LXC2+
- 26 LL2C- << LXC2-
- 26 LDC7+ << LX7+
- 26 LDC7- << LX7-
- 26 LDC6+ << LX6+
- 26 LDC6- << LX6-
- 26 LDC5+ << LX5+
- 26 LDC5- << LX5-
- 26 LDC4+ << LX4+
- 26 LDC4- << LX4-
- 26 LDC3+ << LX3+
- 26 LDC3- << LX3-
- 26 LL1C+ << LXC1+
- 26 LL1C- << LXC1-
- 26 LDC2+ << LX2+
- 26 LDC2- << LX2-
- 26 LDC1+ << LX1+
- 26 LDC1- << LX1-
- 26 LDC0+ << LX0+
- 26 LDC0- << LX0-

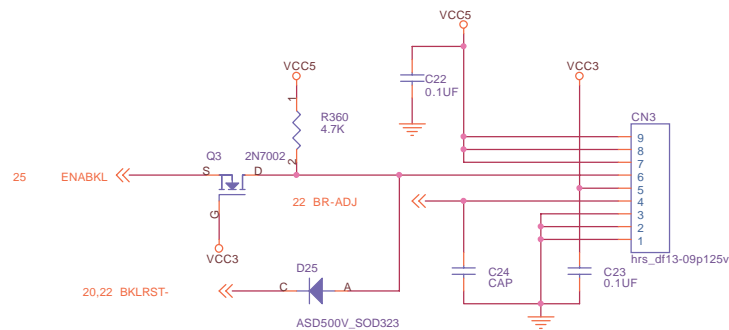
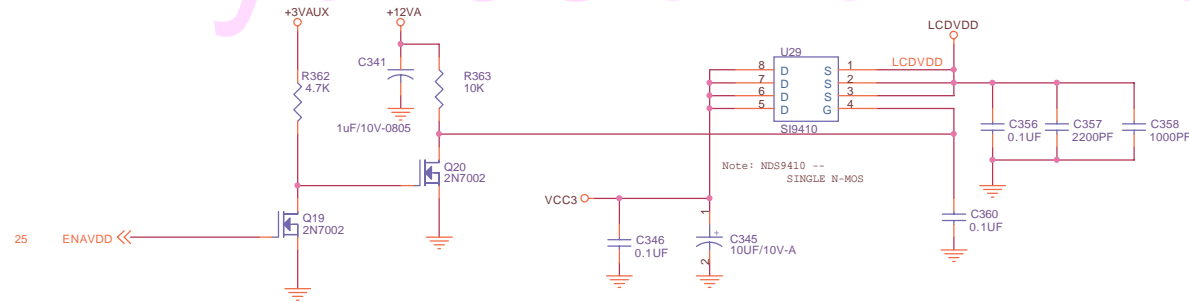
- 64 DVDD1 << DVDD
- 63 VBDE << VBDE
- 62 VBCTL1 << VBCTL1
- 61 D_GND << D_GND
- 60 VDDV << VDDV
- 59 D_GND << D_GND
- 58 D_GND << D_GND
- 57 D_GND << D_GND
- 56 D_GND << D_GND
- 55 DVDD << DVDD
- 54 TVPLL1VDD << TVPLL1VDD
- 53 VBOSCO << VBOSCO
- 52 VBCKLK << VBCKLK
- 51 TVPLL1GND << TVPLL1GND
- 50 D_GND << D_GND
- 49 RESERVED << RESERVED
- 48 DAC_GND << DACGND
- 47 DAC_VDD << DACVDD
- 46 RESERVED << RESERVED
- 45 IOC << IOC
- 44 IOC << IOC
- 43 IOY << IOY
- 42 RESERVED << RESERVED
- 41 IOC_COMP << IOC_COMP
- 40 V2COMP << V2COMP
- 39 DAC_GND << DACGND

- 1 LVDSPLLVDL << LVDSPLLVDL
- 2 RESERVED << RESERVED
- 3 LVDSPLLVS << LVDSPLLVS
- 4 LAVSS << LAVSS
- 5 RESERVED << RESERVED
- 6 +20X1 << +20X1
- 7 -20X1 << -20X1
- 8 100V1 << 100V1
- 9 100V2 << 100V2
- 10 RESERVED << RESERVED
- 11 -X1 << -X1
- 12 GND1 << GND1
- 13 +9X1 << +9X1
- 14 10X1 << 10X1
- 15 10X2 << 10X2
- 16 -5X1 << -5X1
- 17 GND1 << GND1
- 18 +9X1 << +9X1
- 19 -X1 << -X1
- 20 200V1 << 200V1
- 21 200V2 << 200V2
- 22 +X1 << +X1
- 23 LX3N << LX3N
- 24 LX3P << LX3P
- 25 +10X1 << +10X1
- 26 -10X1 << -10X1
- 27 200V1 << 200V1
- 28 +X1 << +X1
- 29 GND1 << GND1
- 30 LX2N << LX2N
- 31 LX1P << LX1P
- 32 LX1N << LX1N
- 33 200V1 << 200V1
- 34 LX0N << LX0N
- 35 LX0P << LX0P
- 36 GND1 << GND1
- 37 LVDSPLLVD << LVDSPLLVD
- 38 V2RSET << V2RSET

R9	PFTTEST0	VDDQ
	NC	3.3V
		4.7K
		1.8V



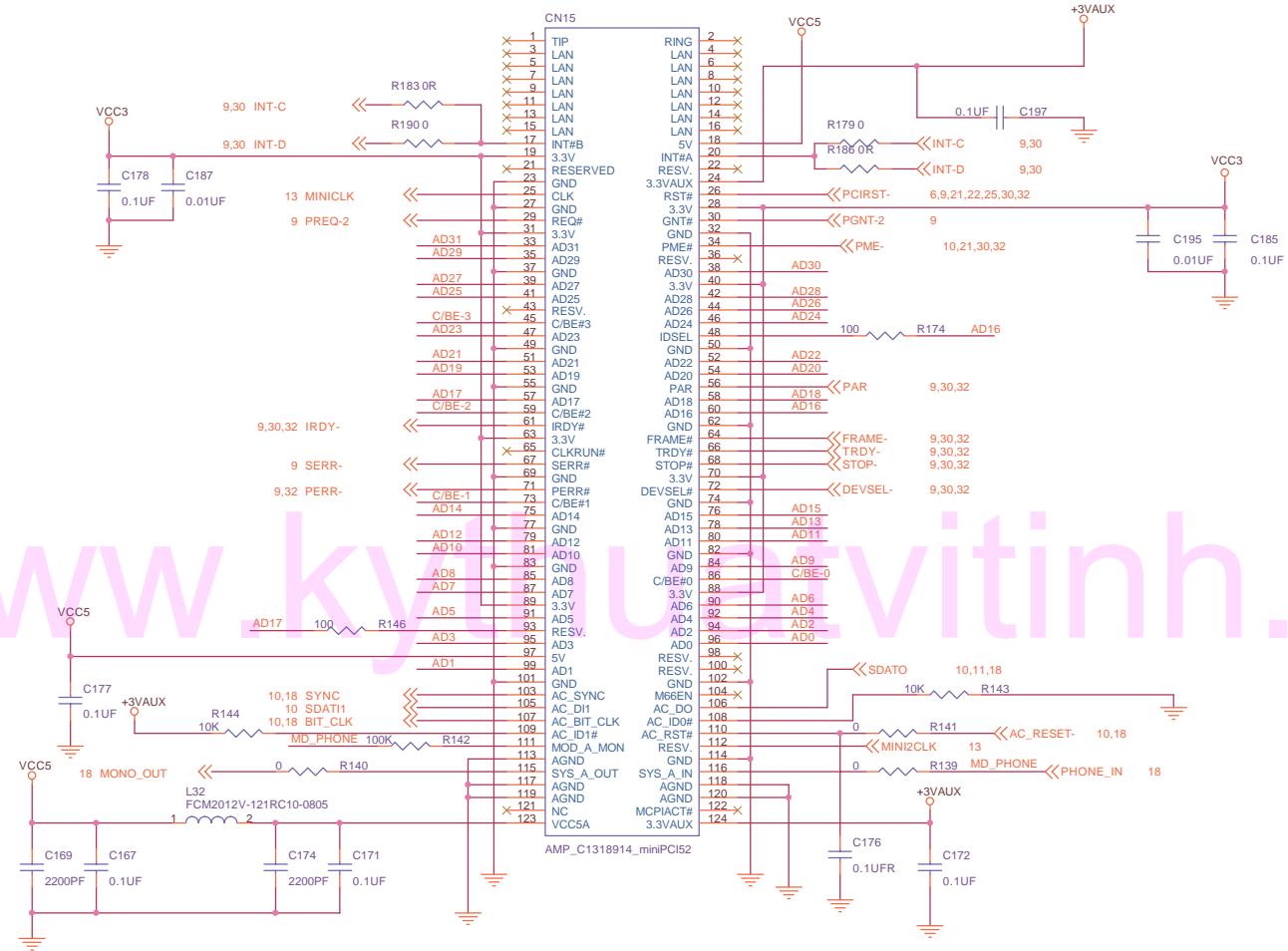
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ECS CORPORATION		
Title LCD/TC CONN.		
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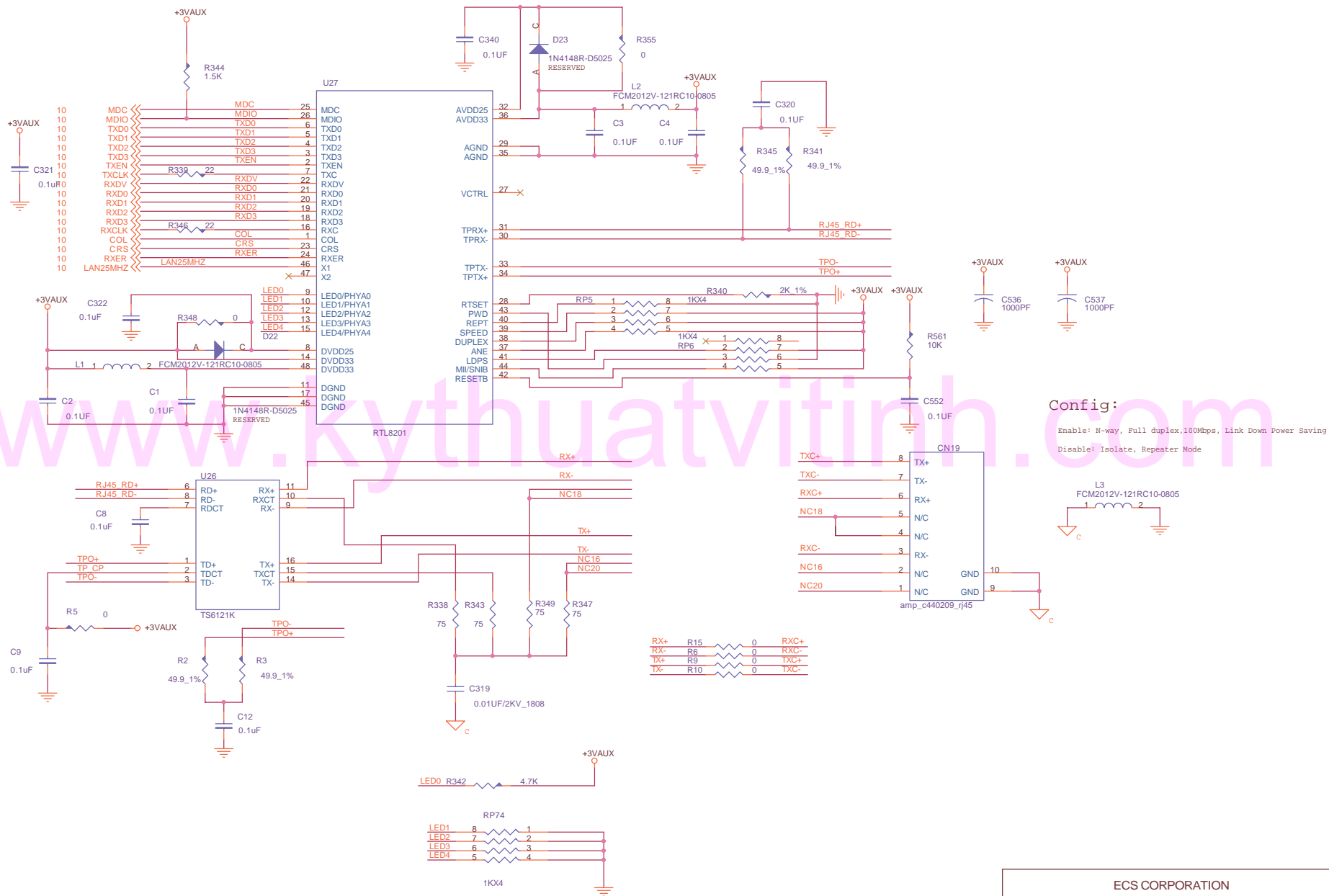
9,30,32 AD[0..31] << AD[0..31]
 9,30,32 C/BE[0..3] << C/BE[0..3]

MINI PCI SOCKET



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ECS CORPORATION		
Title MINI PCI CONN.		
Size B	Document Number A928-1-4-01	Rev 3.0
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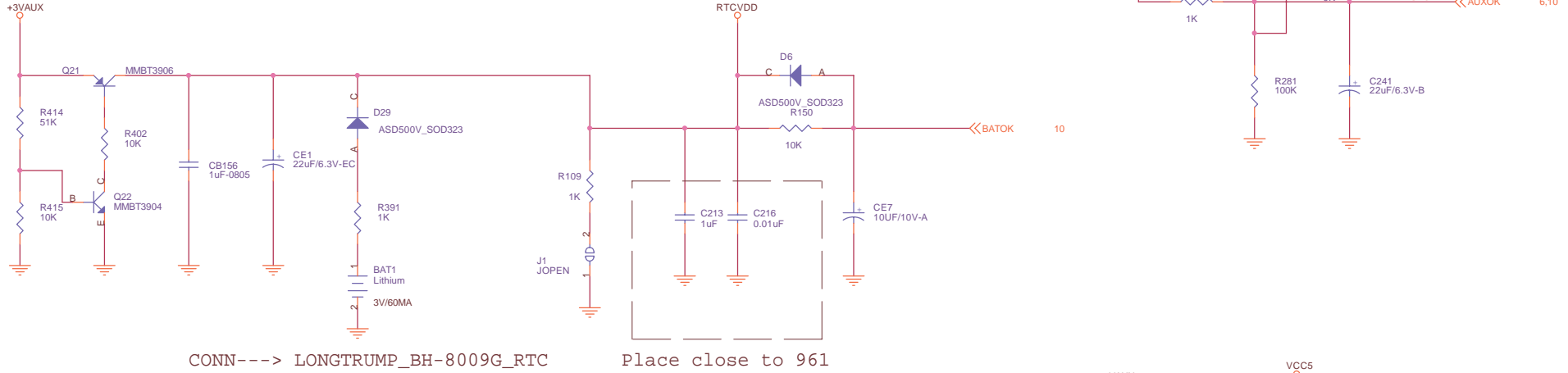


Config:
 Enable: N-way, Full duplex, 100Mbps, Link Down Power Saving
 Disable: Isolate, Repeater Mode

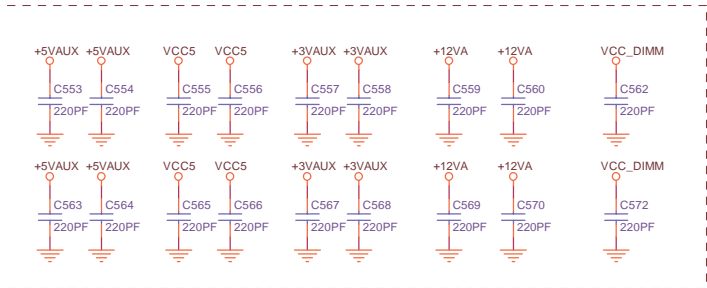
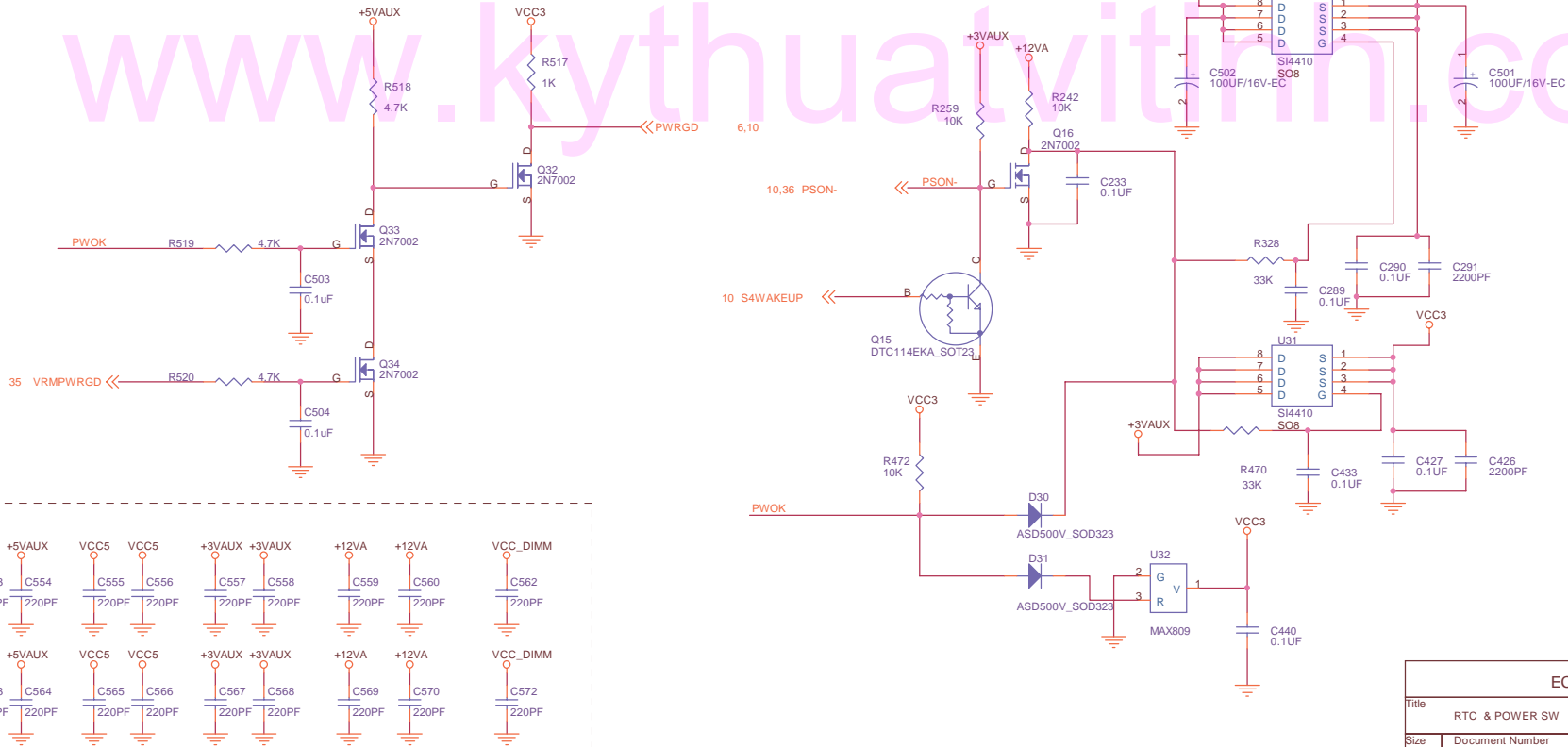
ECS CORPORATION		
Title	RTL8201	
Size B	Document Number	Rev
	A928-1-4-01	3.0
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NOTE!

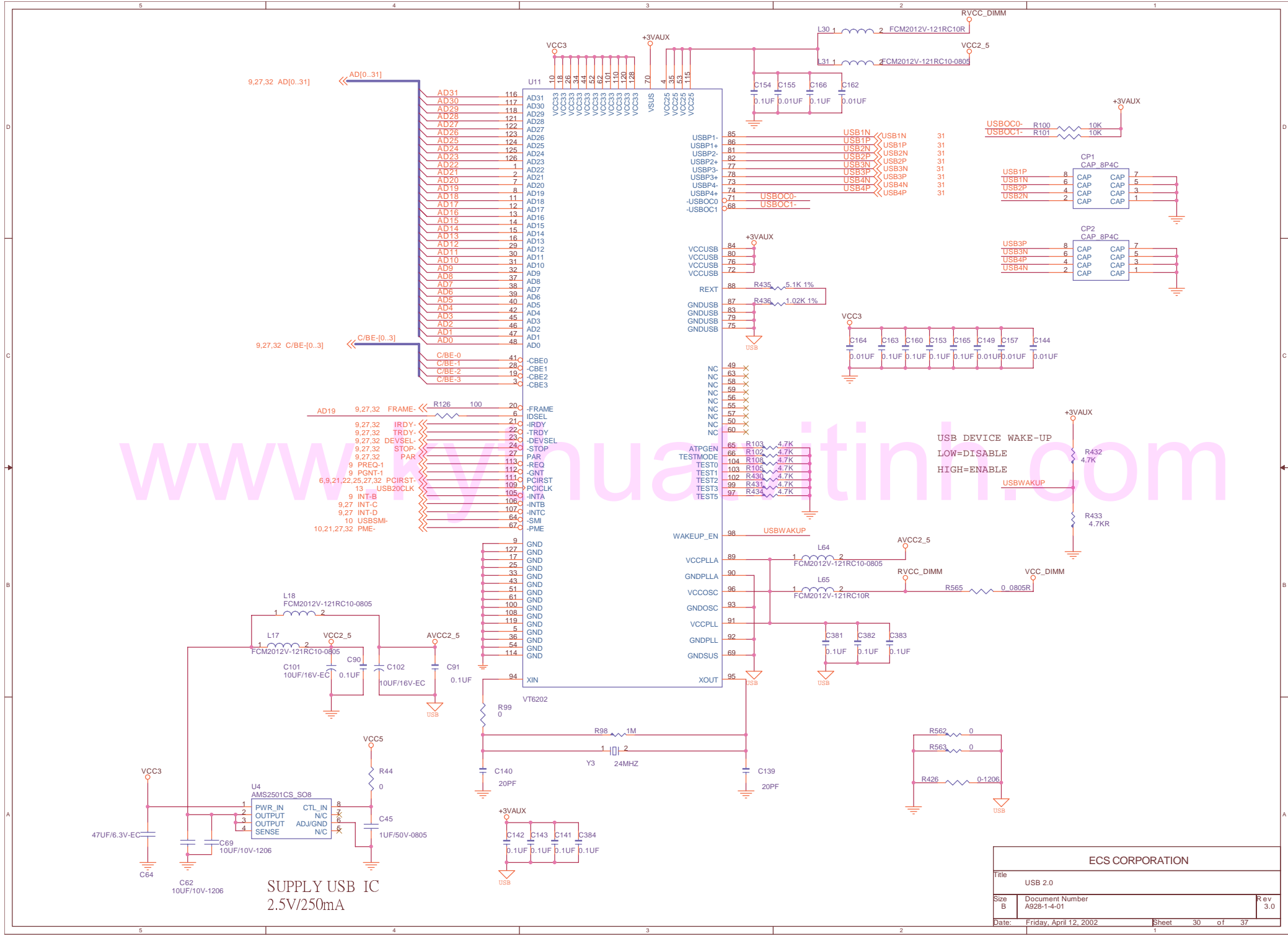
- 1.The RTCVDD is 3V
- 2.Decoupling capacitor must be close to 650 RTCVDD pin.
- 3.RTC circuit must strictly follow SiS's recommended design
SiS is not responsible for RTC problems from foreign designs.



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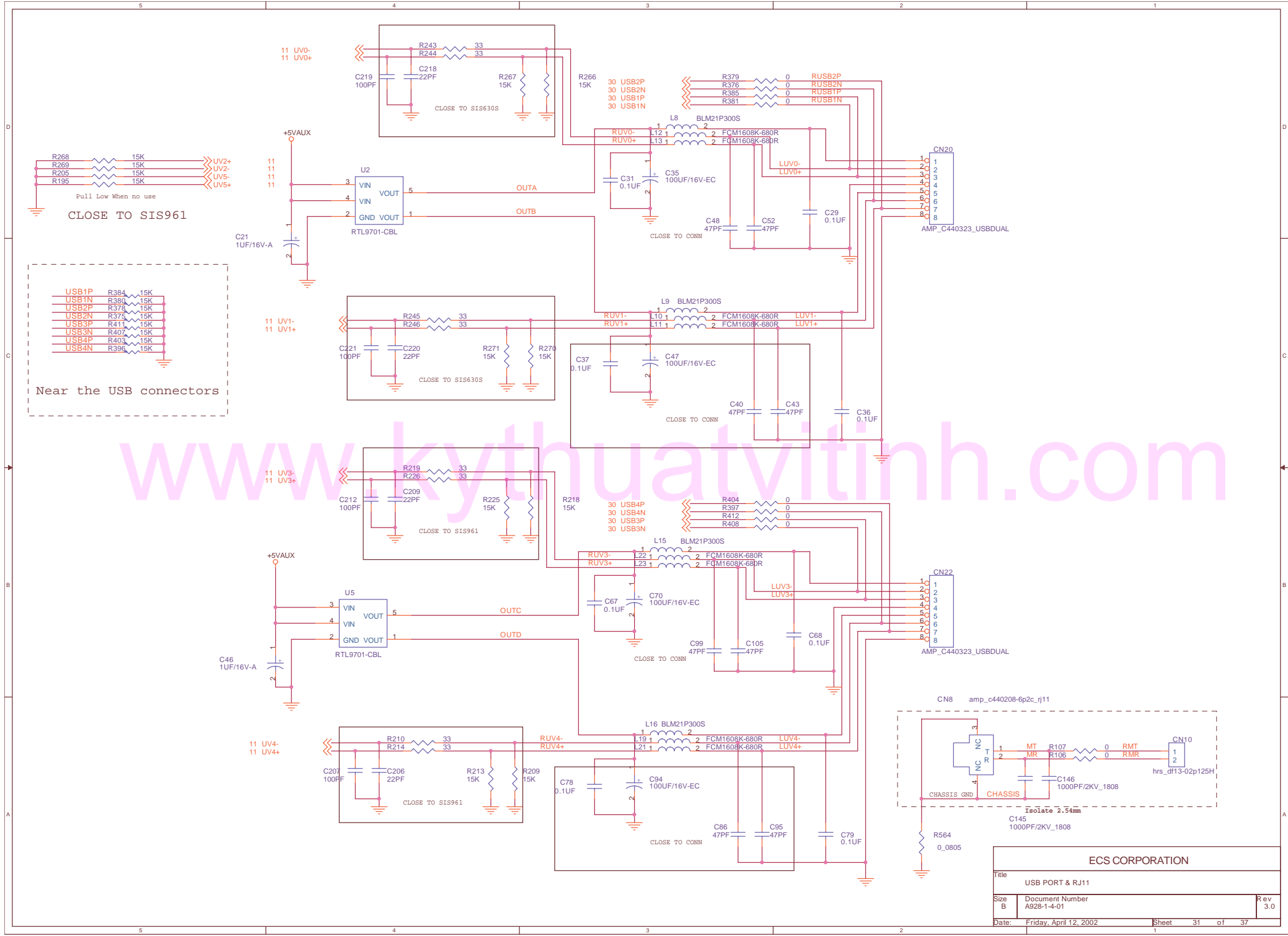


ECS CORPORATION		
Title RTC & POWER SW		
Size B	Document Number A928-1-4-01	Rev 3.0
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SUPPLY USB IC
2.5V/250mA

ECS CORPORATION			
Title USB 2.0			
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R268 15K
R269 15K
R205 15K
R195 15K

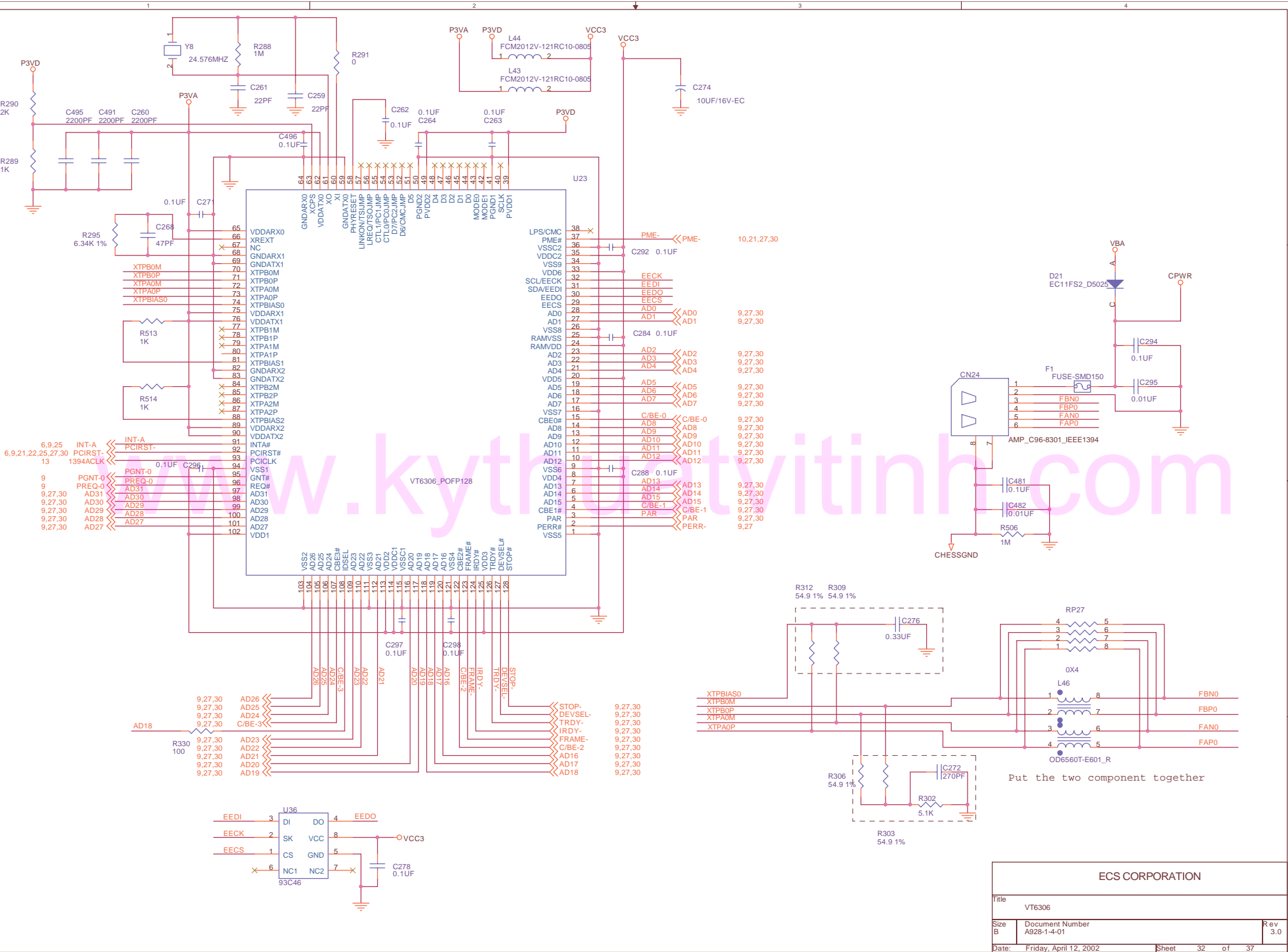
Pull Low When no use

CLOSE TO SIS961

USB1P R394 15K
USB1N R380 15K
USB2P R378 15K
USB2N R375 15K
USB3P R411 15K
USB3N R407 15K
USB4P R403 15K
USB4N R396 15K

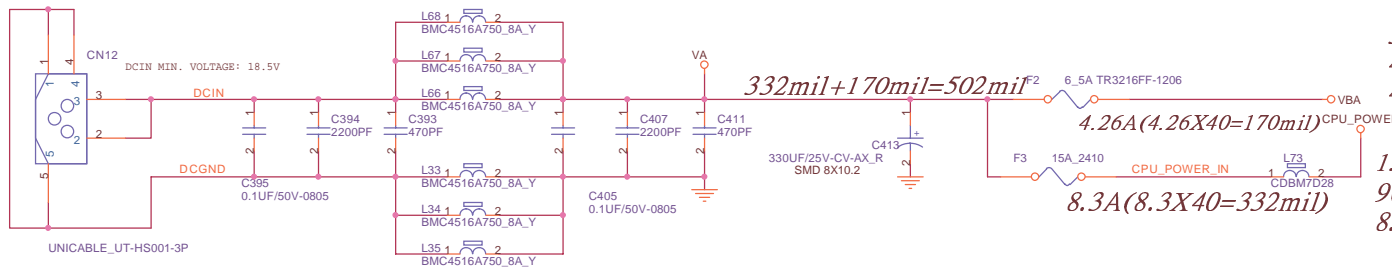
Near the USB connectors

ECS CORPORATION		
Title USB PORT & RJ11		
Size B	Document Number A928-1-4-01	Rev 3.0
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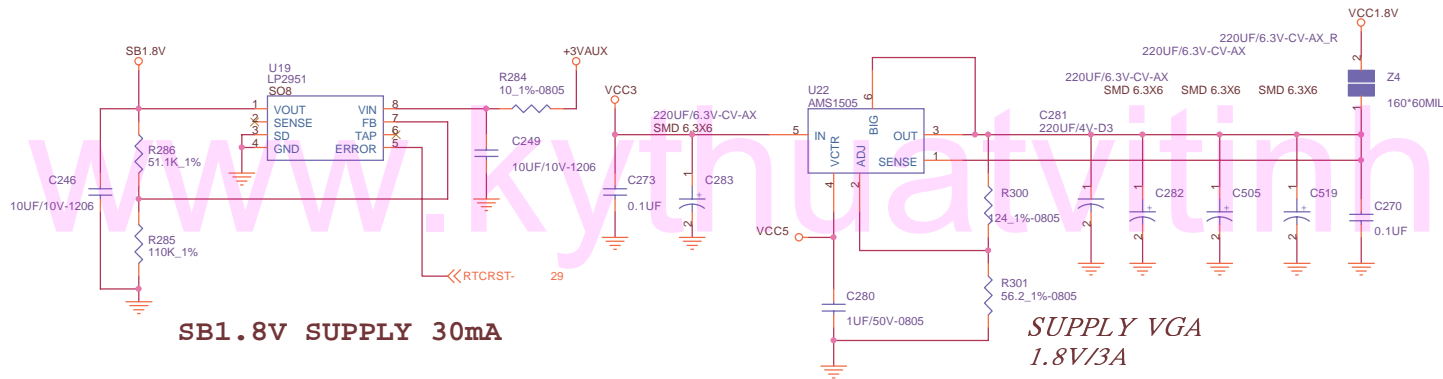


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ECS CORPORATION		
Title VT6306		
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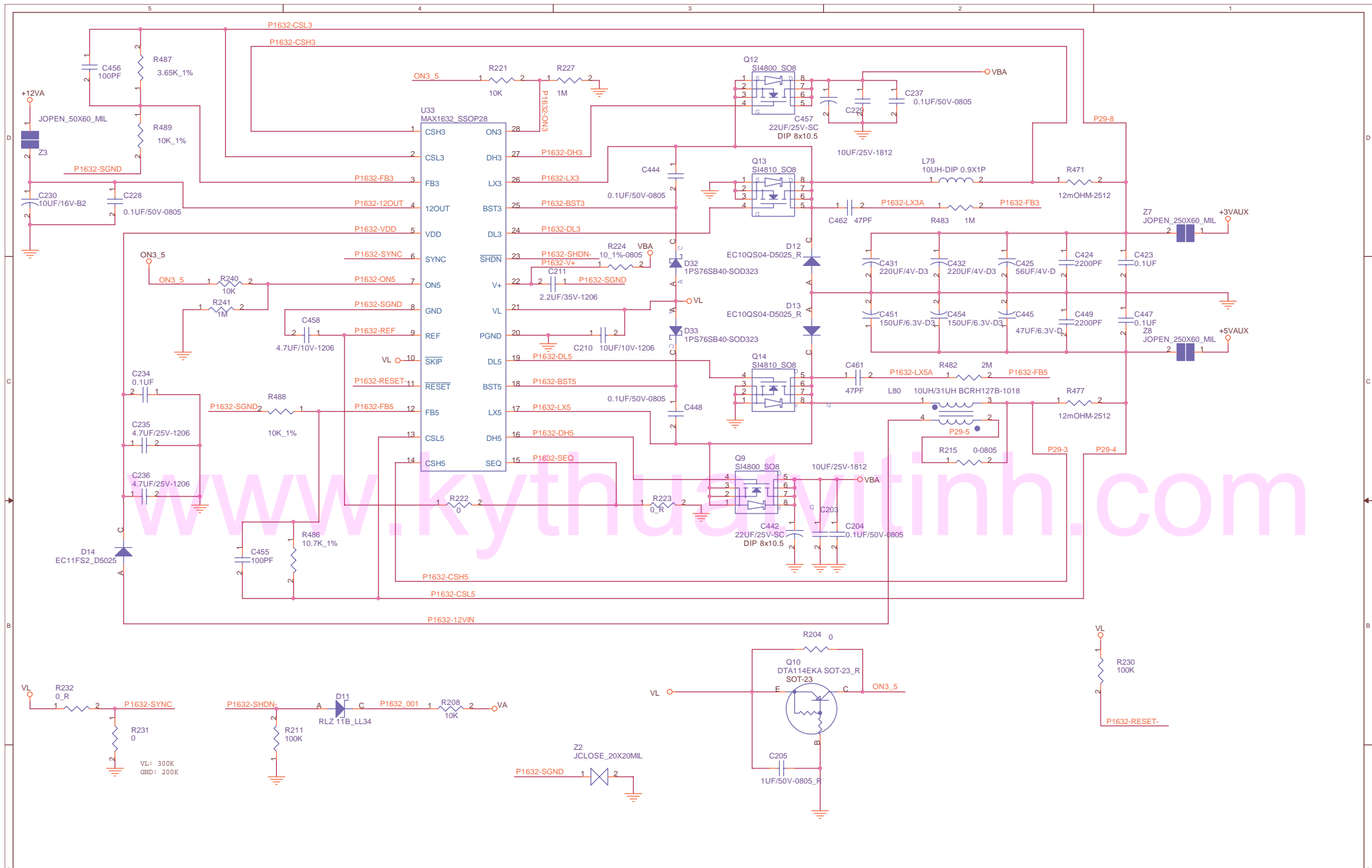
$3.3V \times 5A + 5V \times 4.5A + 2.5V \times 3A + 1.25V \times 2A = 49W$
 $49W / 11.5V = 4.26A$
 $4.26A (4.26 \times 40mil = 170mil)$
 $1.6V \times 60A = 96W$
 $96W / 11.5V = 8.3A$
 $8.3A (8.3 \times 40mil = 332mil)$



SB1.8V SUPPLY 30mA

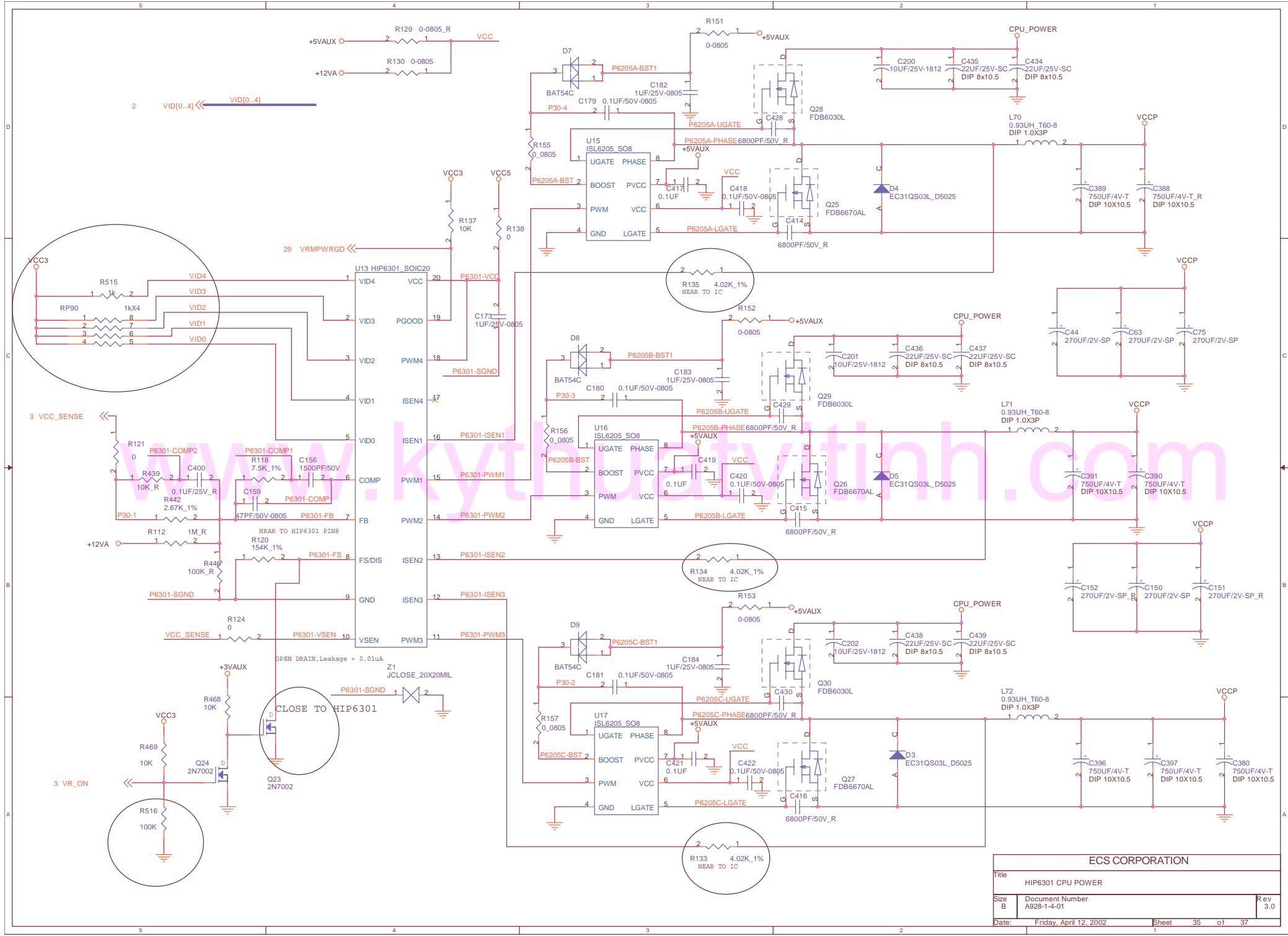
**SUPPLY VGA
1.8V/3A**

ECS CORPORATION		
Title DC IN & VGA, CLOCK AUX, VTT		
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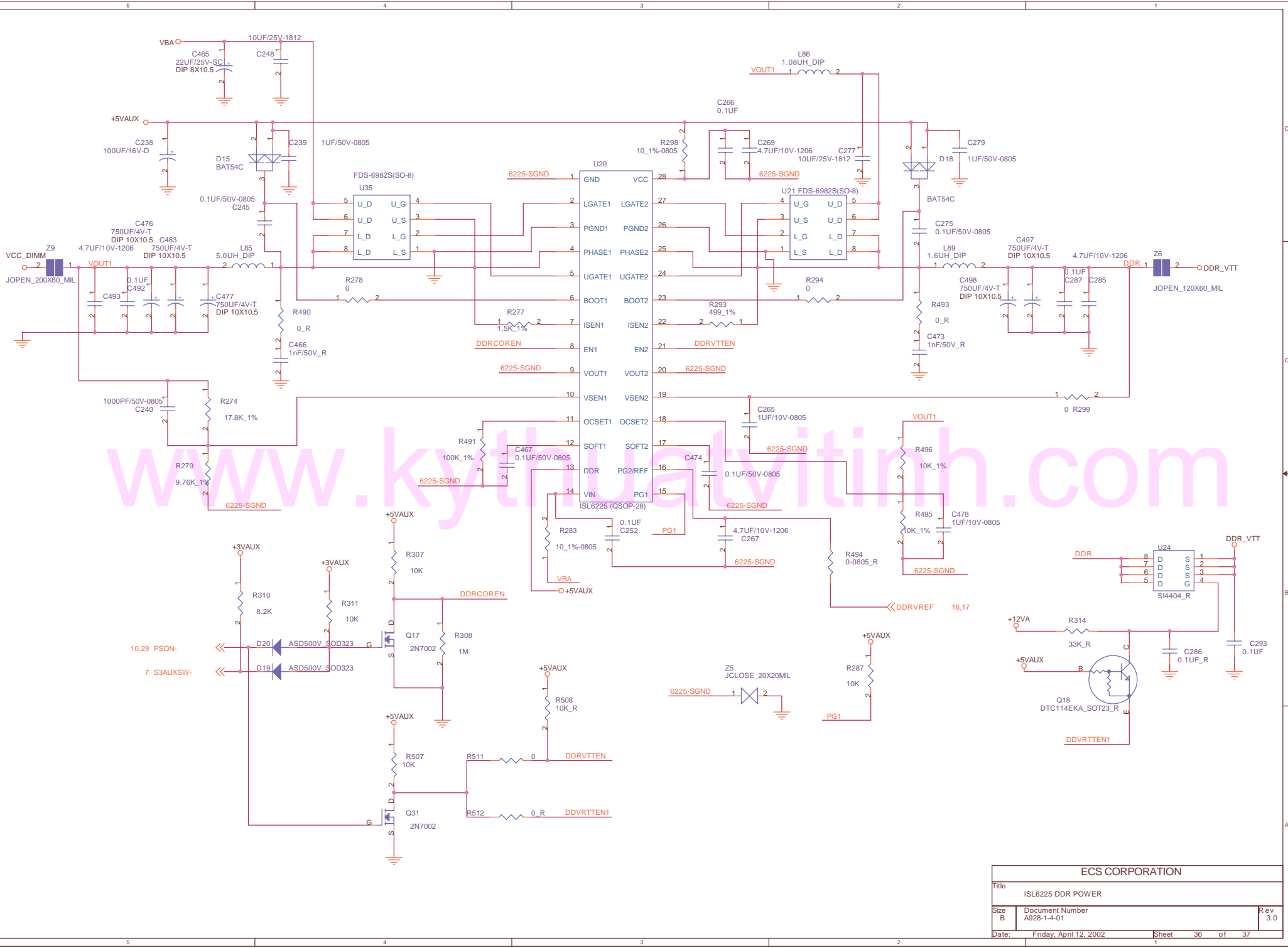


+5VAUX / 3VAUX / +12VA SUPPLY

ECS CORPORATION		
Title MAX 1632 SYSTEM POWER		
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Title HIP6301 CPU POWER		
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ECS CORPORATION		
Title ISL6225 DDR POWER		
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- 1.0 : Schematic Release.
- 2.0 : Schematic Release.
 - 1. Add new source KBC(KB3668 B0,ENE).
 - 2. Solution for EMI.
 - 3. Solution for lan wake up error before suspend mode.
- 2.A : Schematic Release.
 - 1. Modify page 24 ,U9 W83L785R change to W83L784AR
 - 2. Modify page 36 ,add soft start time.C474,C467 change to 0.1UF/50V 0805
- 2.B : Schematic Release.
 - 1. Modify page 22 ,Removing Y5,R567 component that short with cdrom device.
- 3.0 : Schematic Release.
 - 1. Modify pcb layout to R3 version.
 - 2. Resume R567 0 ohm 0805 because it's been away cdrom.

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ECS CORPORATION			
Title			
HISTORY			
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