

945GCT/GZT-M Rev: 1.0

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B	B	33		12/01/' 06
1.0	1.0	33		12/23/' 06

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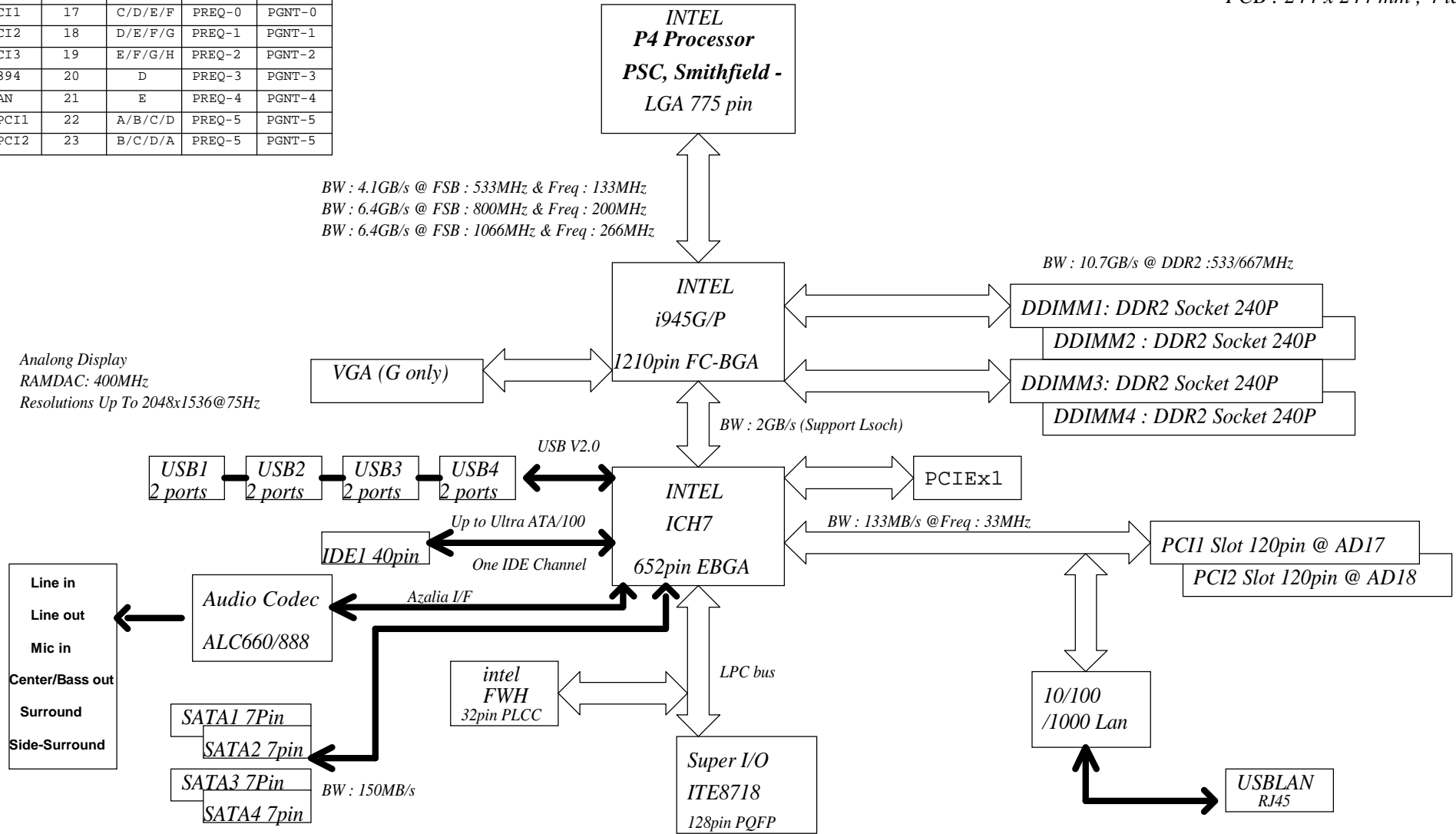
PCB : 244 x 244 mm ; 4 layers

DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	C/D/E/F	PREQ-0	PGNT-0
PCI2	18	D/E/F/G	PREQ-1	PGNT-1
PCI3	19	E/F/G/H	PREQ-2	PGNT-2
1394	20	D	PREQ-3	PGNT-3
LAN	21	E	PREQ-4	PGNT-4
EPCI1	22	A/B/C/D	PREQ-5	PGNT-5
EPCI2	23	B/C/D/A	PREQ-5	PGNT-5

BW : 4.1GB/s @ FSB : 533MHz & Freq : 133MHz
 BW : 6.4GB/s @ FSB : 800MHz & Freq : 200MHz
 BW : 6.4GB/s @ FSB : 1066MHz & Freq : 266MHz

BW : 10.7GB/s @ DDR2 : 533/667MHz

Analog Display
 RAMDAC: 400MHz
 Resolutions Up To 2048x1536@75Hz

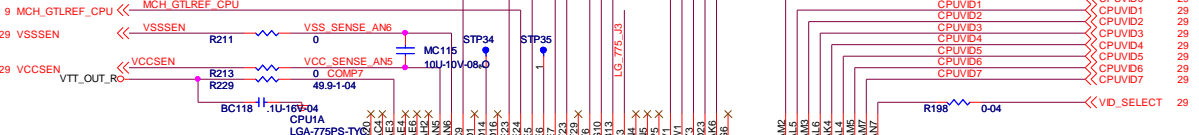
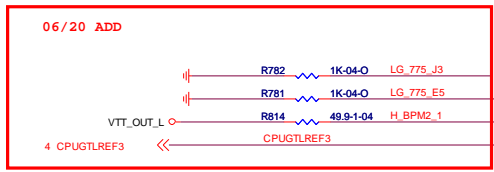


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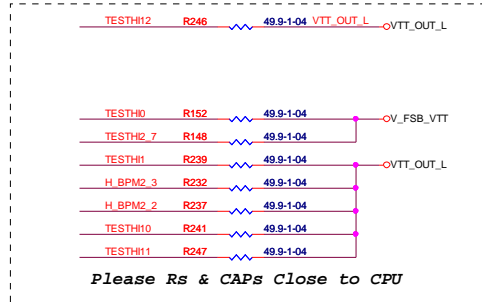
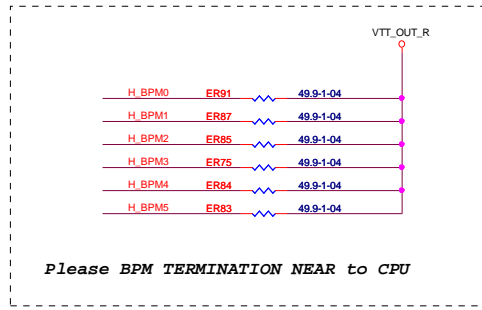
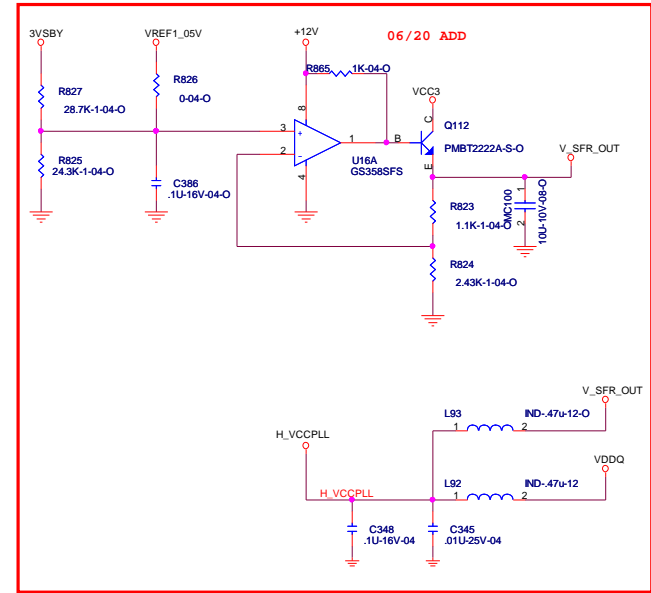
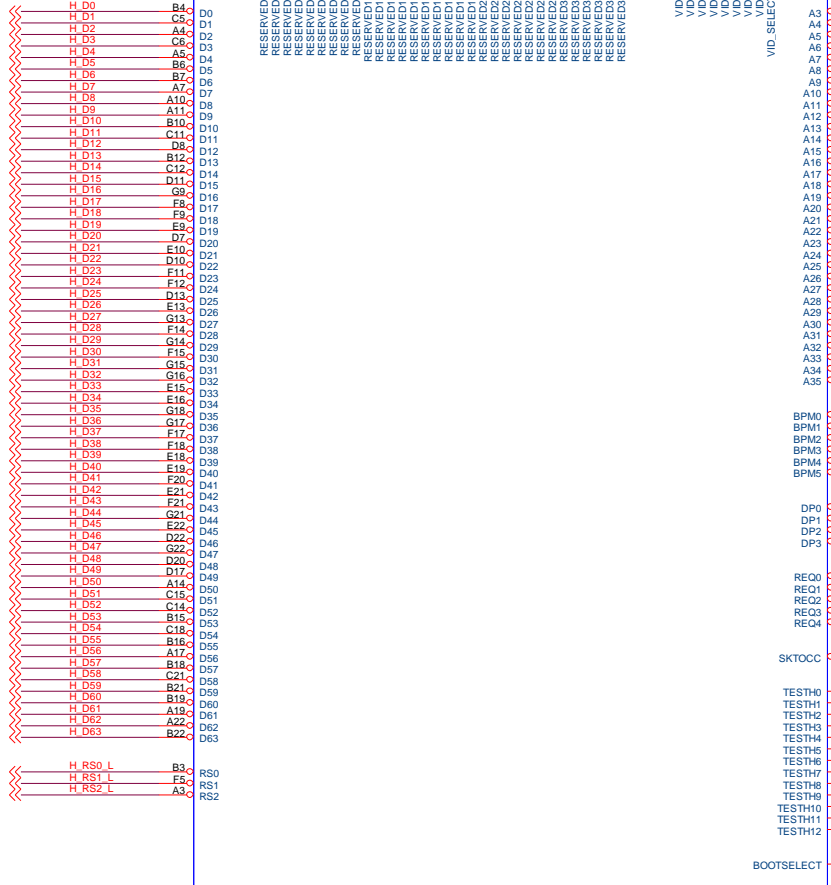
Title: **System Block Diagram**

Size: B Document Number: **945GCT/GZT-M** Rev: 1.0

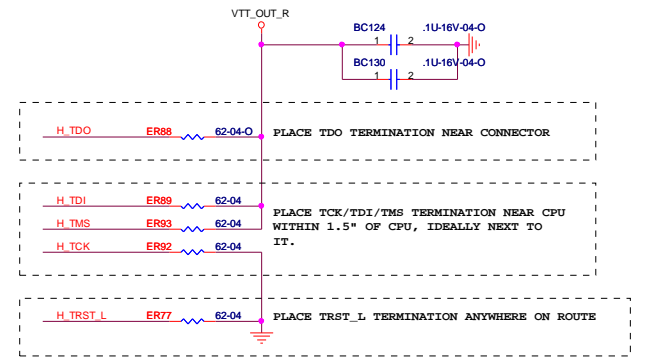
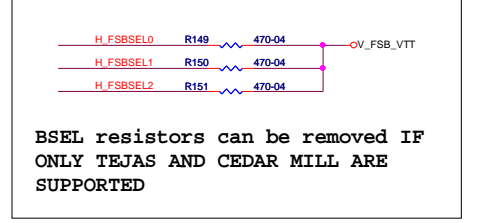
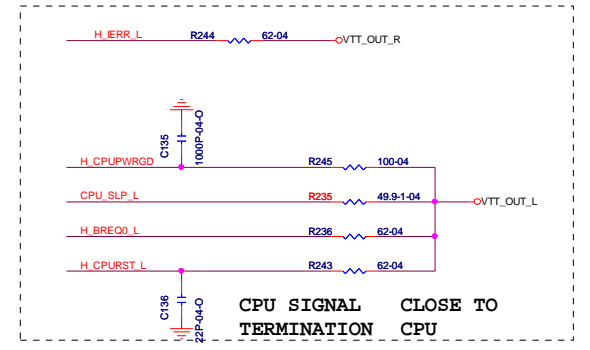
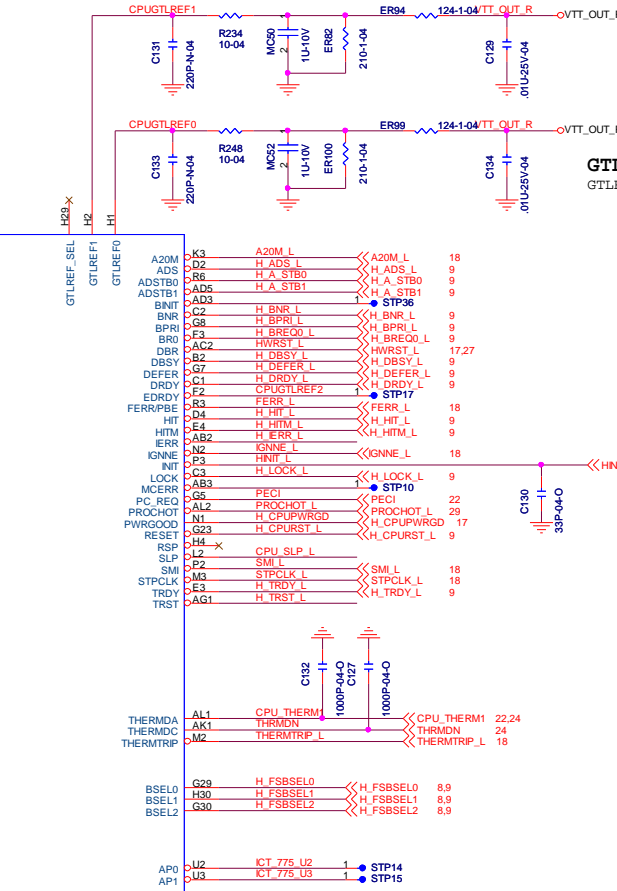
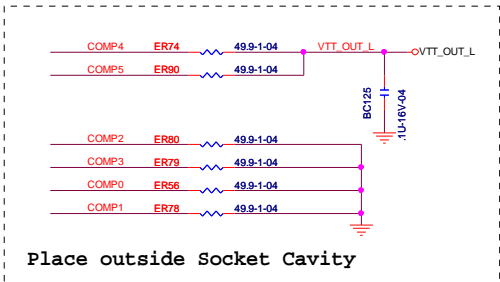
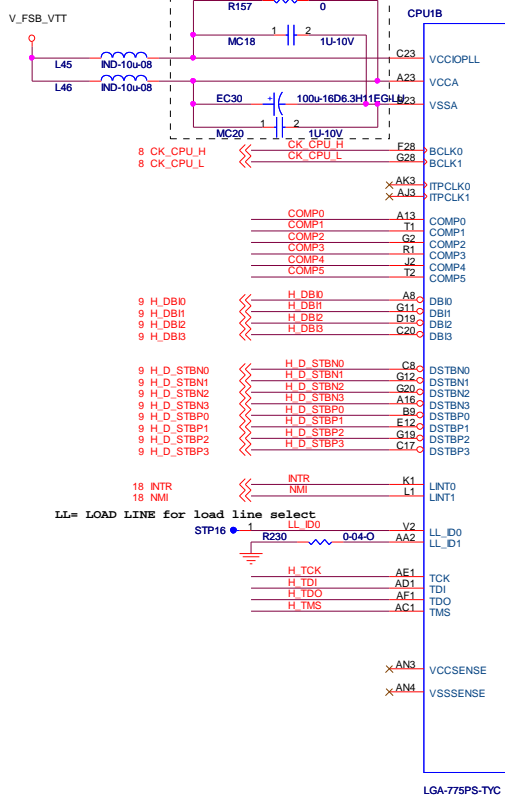
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- 9 H_D0
- 9 H_D1
- 9 H_D2
- 9 H_D3
- 9 H_D4
- 9 H_D5
- 9 H_D6
- 9 H_D7
- 9 H_D8
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- 9 H_D12
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- 9 H_D56
- 9 H_D57
- 9 H_D58
- 9 H_D59
- 9 H_D60
- 9 H_D61
- 9 H_D62
- 9 H_D63
- 9 H_RS0_L
- 9 H_RS1_L
- 9 H_RS2_L




Place components as close as possible to Processor socket
trace width to cap must be no smaller than 12 Mils

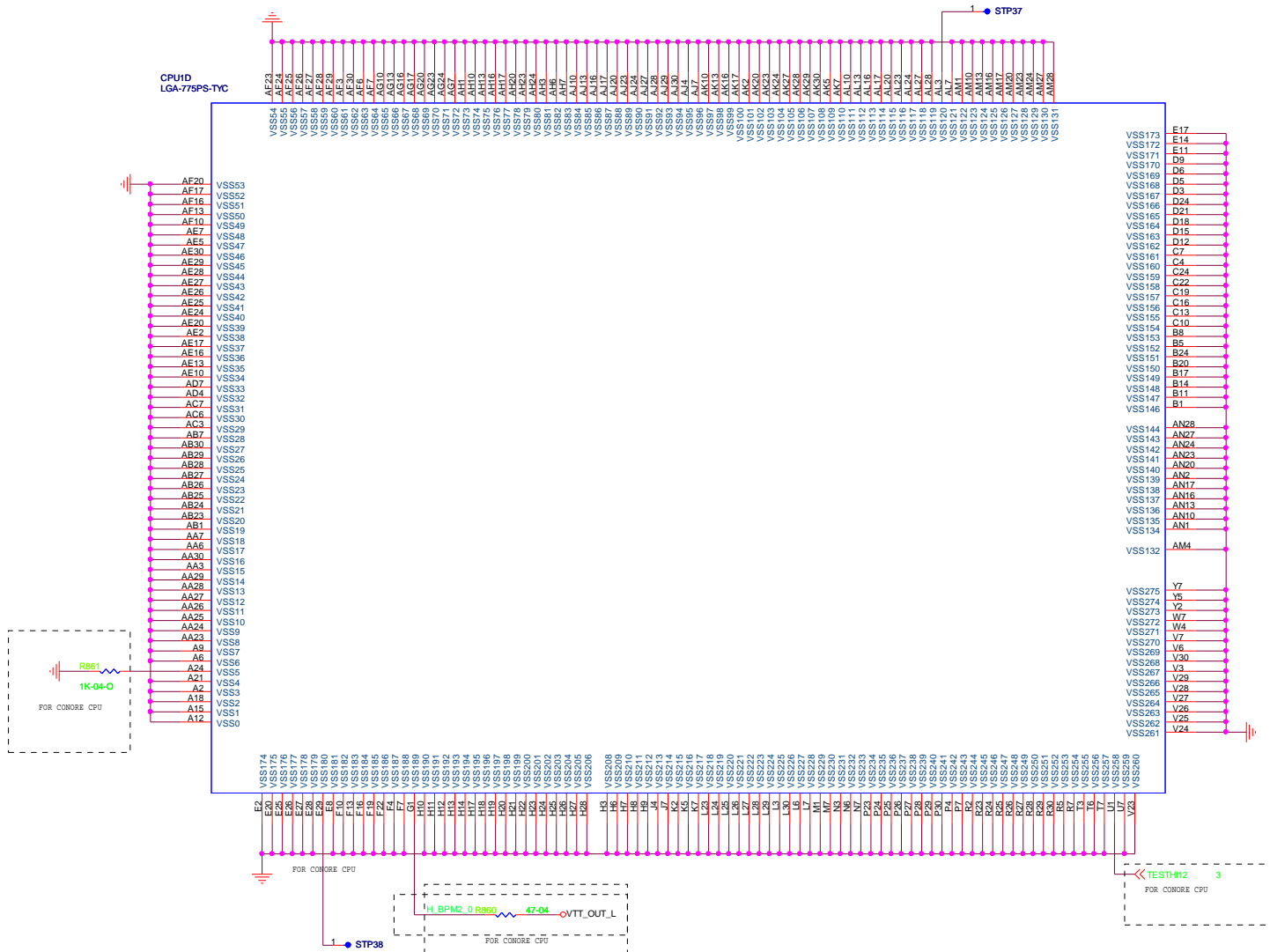


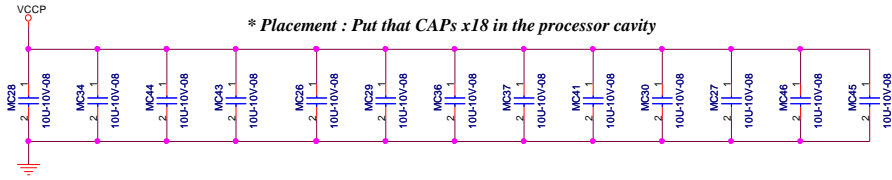


CPU1C
LGA-775PS-TYC

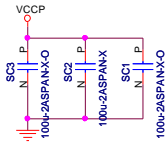
 Elitegroup Computer Systems		
Title P4 LGA775P Part C		
Size Custom	Document Number 945GCT/GZT-M	Rev 1.0
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**CPUID
LGA-775FS-TYC**

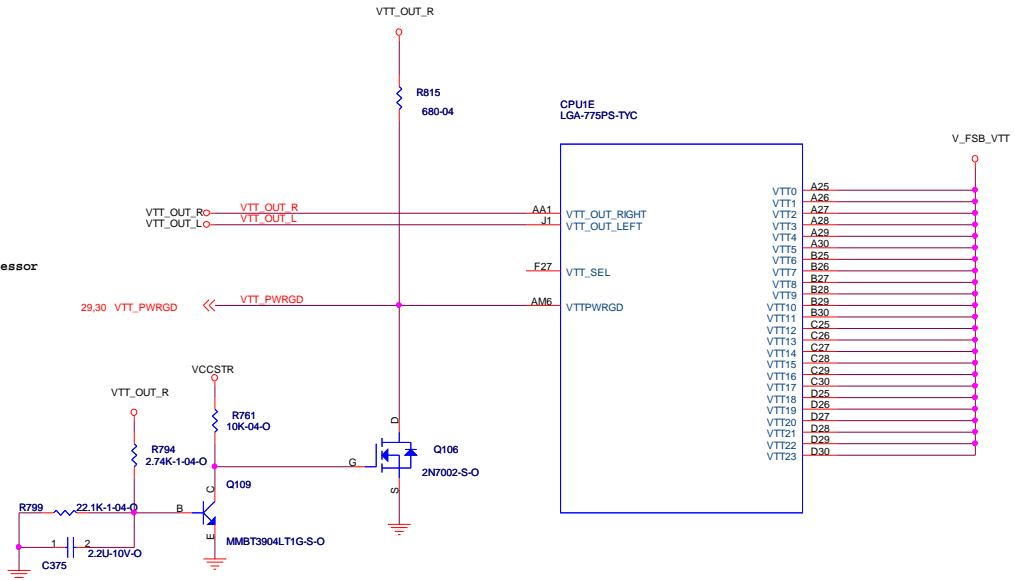


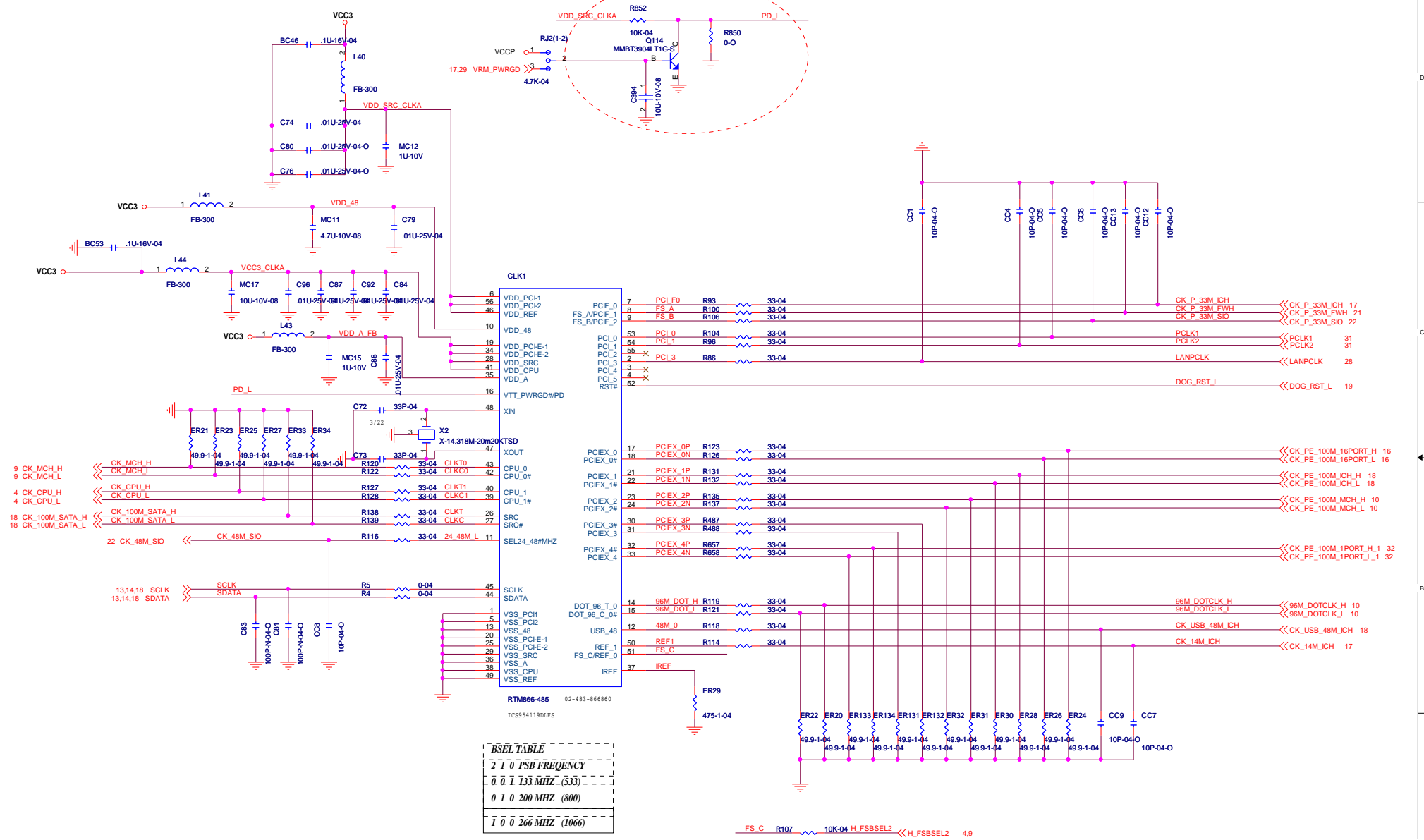


* Placement : Put that CAPs x2 on solder side



VTT_SEL=0 for the Tejas processor





- 9 CK_MCH_H
- 9 CK_MCH_L
- 4 CK_CPU_H
- 4 CK_CPU_L
- 18 CK_100M_SATA_H
- 18 CK_100M_SATA_L

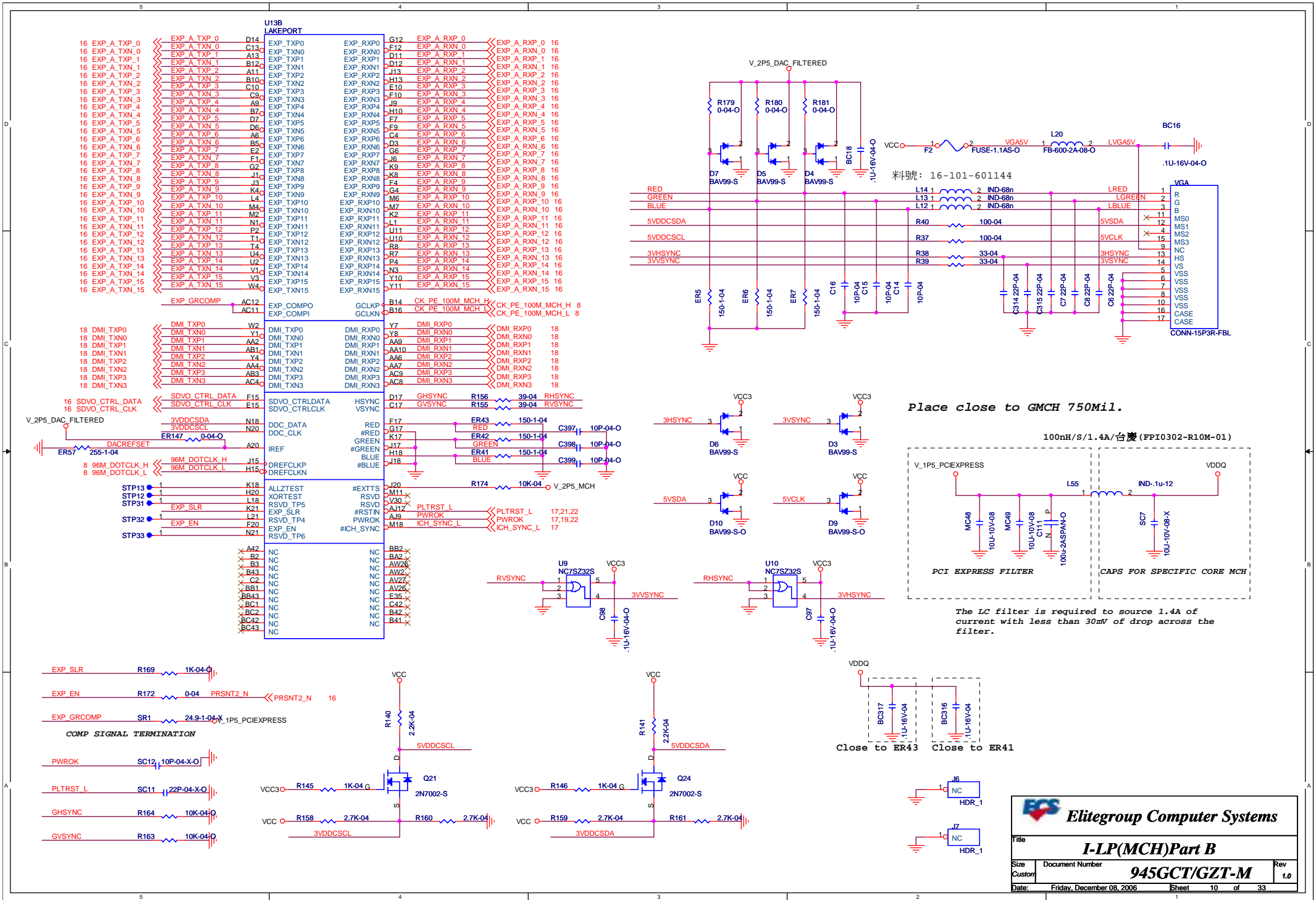
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Title: **Clock Generator(CK410)**

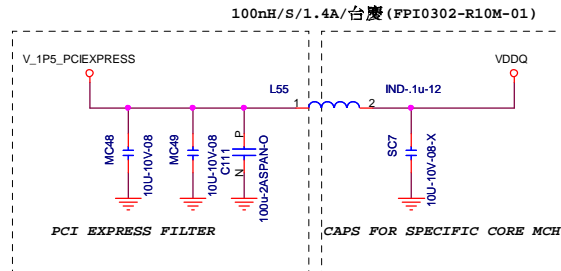
Size: Document Number **945GCT/GZT-M** Rev: **1.0**

Customer: **945GCT/GZT-M**

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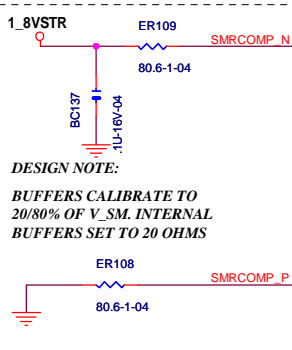
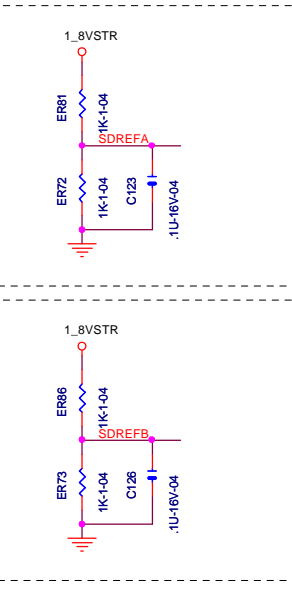
Place close to GMCH 750mil.



Close to ER43 Close to ER41

Elitegroup Computer Systems			
I-LP(MCH)Part B			
File	Document Number	Rev	
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U13C LAKEPORT					U13D LAKEPORT						
DQS_H A4	AU35	SDQS_A4	SDQS_A0	AU4	DQS_H A0	DQS_H B4	AT29	SDQS_B4	AM8	DQS_H B0	
DQS_L A4	AV35	#SDQS_A4	#SDQS_A0	AR2	DQS_L A0	DQS_L B4	AV29	#SDQS_B0	AM6	DQS_L B0	
MPD_A4	AT34	SDM_A4	SDM_A0	AR3	MPD_A0	MPD_B4	AR29	SDM_B0	AL11	MPD_B0	
MD_A32	AP32	SDQ_A32	SDQ_A0	AP3	MD A0	MD B32	AU27	SDQ_B32	AL6	MD B0	
MD_A33	AV34	SDQ_A33	SDQ_A1	AP2	MD A1	MD B33	AN29	SDQ_B33	AL8	MD B1	
MD_A34	AV38	SDQ_A34	SDQ_A2	AU3	MD A2	MD B34	AR31	SDQ_B34	AP8	MD B2	
MD_A35	AU39	SDQ_A35	SDQ_A3	AV4	MD A3	MD B35	AM31	SDQ_B35	AP9	MD B3	
MD_A36	AV32	SDQ_A36	SDQ_A4	AR4	MD A4	MD B36	AP27	SDQ_B36	AL11	MD B4	
MD_A37	AT32	SDQ_A37	SDQ_A5	AR4	MD A5	MD B37	AP27	SDQ_B37	AL9	MD B5	
MD_A38	AR34	SDQ_A38	SDQ_A6	AU5	MD A6	MD B38	AP31	SDQ_B38	AM10	MD B6	
MD_A39	AU37	SDQ_A39	SDQ_A7	AU2	MD A7	MD B39	AU31	SDQ_B39	AP6	MD B7	
DQS_H A5	AP42	SDQS_A5	SDQS_A1	BA3	DQS_H A1	DQS_H B5	AP36	SDQS_B5	AV7	DQS_H B1	
DQS_L A5	AP40	#SDQS_A5	#SDQS_A1	BB4	DQS_L A1	DQS_L B5	AM35	#SDQS_B5	AR9	DQS_L B1	
MPD_A5	AP39	SDM_A5	SDM_A1	AY2	MPD A1	MPD_B5	AR38	SDM_B5	AW7	MPD B1	
MD_A40	AR41	SDQ_A40	SDQ_A8	AW3	MD A8	MD B40	AP35	SDQ_B40	AU7	MD B8	
MD_A41	AR42	SDQ_A41	SDQ_A9	AY3	MD A9	MD B41	AP37	SDQ_B41	AV6	MD B9	
MD_A42	AN43	SDQ_A42	SDQ_A10	BA7	MD A10	MD B42	AN32	SDQ_B42	AV12	MD B10	
MD_A43	AM40	SDQ_A43	SDQ_A11	BB7	MD A11	MD B43	AL35	SDQ_B43	AM11	MD B11	
MD_A44	AU41	SDQ_A44	SDQ_A12	AV1	MD A12	MD B44	AR35	SDQ_B44	AR5	MD B12	
MD_A45	AU42	SDQ_A45	SDQ_A13	AW4	MD A13	MD B45	AU38	SDQ_B45	AR7	MD B13	
MD_A46	AP41	SDQ_A46	SDQ_A14	BC6	MD A14	MD B46	AM38	SDQ_B46	AR12	MD B14	
MD_A47	AN40	SDQ_A47	SDQ_A15	AY7	MD A15	MD B47	AM34	SDQ_B47	AR10	MD B15	
DQS_H A6	AG42	SDQS_A6	SDQS_A2	AY11	DQS_H A2	DQS_H B6	AG34	SDQS_B6	AV13	DQS_H B2	
DQS_L A6	AG41	#SDQS_A6	#SDQS_A2	BA10	DQS_L A2	DQS_L B6	AG32	#SDQS_B6	AT13	DQS_L B2	
MPD_A6	AG40	SDM_A6	SDM_A2	BB10	MPD A2	MPD_B6	AJ39	SDM_B6	AP13	MPD B2	
MD_A48	AL41	SDQ_A48	SDQ_A16	AW12	MD A16	MD B48	AL34	SDQ_B48	AM15	MD B16	
MD_A49	AL42	SDQ_A49	SDQ_A17	AY10	MD A17	MD B49	AJ34	SDQ_B49	AM13	MD B17	
MD_A50	AF39	SDQ_A50	SDQ_A18	BA12	MD A18	MD B50	AF32	SDQ_B50	AM15	MD B18	
MD_A51	AF40	SDQ_A51	SDQ_A19	BB12	MD A19	MD B51	AF34	SDQ_B51	AM17	MD B19	
MD_A52	AM41	SDQ_A52	SDQ_A20	BA5	MD A20	MD B52	AL31	SDQ_B52	AM12	MD B20	
MD_A53	AM42	SDQ_A53	SDQ_A21	BB9	MD A21	MD B53	AJ32	SDQ_B53	AR13	MD B21	
MD_A54	AF41	SDQ_A54	SDQ_A22	BC11	MD A22	MD B54	AG35	SDQ_B54	AP15	MD B22	
MD_A55	AF42	SDQ_A55	SDQ_A23	AY12	MD A23	MD B55	AD32	SDQ_B55	AT15	MD B23	
DQS_H A7	AC42	SDQS_A7	SDQS_A3	AU18	DQS_H A3	DQS_H B7	AD36	SDQS_B7	AU23	DQS_H B3	
DQS_L A7	AC41	#SDQS_A7	#SDQS_A3	AR18	DQS_L A3	DQS_L B7	AD38	#SDQS_B7	AR23	DQS_L B3	
MPD_A7	AC40	SDM_A7	SDM_A3	AP18	MPD A3	MPD_B7	AD39	SDM_B7	AP23	MPD B3	
MD_A56	AD40	SDQ_A56	SDQ_A24	AM20	MD A24	MD B56	AC32	SDQ_B56	AM24	MD B24	
MD_A57	AD43	SDQ_A57	SDQ_A25	AM18	MD A25	MD B57	AD34	SDQ_B57	AM23	MD B25	
MD_A58	AA39	SDQ_A58	SDQ_A26	AV20	MD A26	MD B58	Y32	SDQ_B58	AV24	MD B26	
MD_A59	AA40	SDQ_A59	SDQ_A27	AM21	MD A27	MD B59	AA32	SDQ_B59	AM26	MD B27	
MD_A60	AE42	SDQ_A60	SDQ_A28	AP17	MD A28	MD B60	AF35	SDQ_B60	AP21	MD B28	
MD_A61	AF41	SDQ_A61	SDQ_A29	AR17	MD A29	MD B61	AF37	SDQ_B61	AR21	MD B29	
MD_A62	AB41	SDQ_A62	SDQ_A30	AP20	MD A30	MD B62	AC33	SDQ_B62	AP24	MD B30	
MD_A63	AB42	SDQ_A63	SDQ_A31	AT20	MD A31	MD B63	AC35	SDQ_B63	AT24	MD B31	
MAAA 0	BA32	SMA_A0	#SWE_A	BB35	SWE_L A	MAAB 0	BB22	SMA_B0	#SWE_B	BB23	SWE_L B
MAAA 1	AW32	SMA_A1	#SCAS_A	BA37	SCAS_L A	MAAB 1	BB21	SMA_B1	#SCAS_B	CAY24	SCAS_L B
MAAA 2	BB30	SMA_A2	#SRAS_A	BA34	SRAS_L A	MAAB 2	BA21	SMA_B2	#SRAS_B	AY23	SRAS_L B
MAAA 3	BA30	SMA_A3				MAAB 3	AY21	SMA_B3			
MAAA 4	AY30	SMA_A4				MAAB 4	BC20	SMA_B4			
MAAA 5	BA27	SMA_A5				MAAB 5	AY19	SMA_B5			
MAAA 6	BC28	SMA_A6				MAAB 6	AY20	SMA_B6			
MAAA 7	AY27	SMA_A7				MAAB 7	BA18	SMA_B7			
MAAA 8	AY28	SMA_A8				MAAB 8	BA19	SMA_B8			
MAAA 9	BB27	SMA_A9	#SCS_A0	BB37	CSA_L0	MAAB 9	BB18	SMA_B9	#SCS_B0	BA40	CSB_L0
MAAA 10	AY33	SMA_A10	#SCS_A1	BA35	CSA_L1	MAAB 10	BA22	SMA_B10	#SCS_B1	CBA41	CSB_L1
MAAA 11	AW27	SMA_A11	#SCS_A2	AY38		MAAB 11	BB17	SMA_B11	#SCS_B2	AW40	
MAAA 12	BB26	SMA_A12	#SCS_A3			MAAB 12	BA17	SMA_B12	#SCS_B3		
MAAA 13	BC38	SMA_A13				MAAB 13	AW42	SMA_B13			
DCLKA_H0	BB32	SCLK_A0	SCKE_A0	BB25	CKEA 0	DCLKB_H0	AM29	SCLK_B0	AY42	ODTB 0	
DCLKA_L0	AY32	#SCLK_A0	SCKE_A1	BA25	CKEA 1	DCLKB_L0	AM27	#SCLK_B0	AV40	ODTB 1	
DCLKA_H1	AY1	SCLK_A1	SCKE_A2			DCLKB_H1	AV3	SCLK_B1	AU43		
DCLKA_L1	BB5	#SCLK_A1	SCKE_A3			DCLKB_L1	AW9	#SCLK_B1	AU40		
DCLKA_H2	AK42	SCLK_A2	SODT_A0	AW37	ODTA 0	DCLKB_H2	AL38	#SCLK_B2			
DCLKA_L2	AK41	#SCLK_A2	SODT_A1	AY39	ODTA 1	DCLKB_L2	AL36	SCLK_B2			
	BA31	SCLK_A3	SODT_A2	BB40			AP26	SCLK_B3			
	BB31	#SCLK_A3	SODT_A3				AR26	#SCLK_B3			
	AY6	SCLK_A4	RSVD	BC16			AU10	SCLK_B4			
	BA5	#SCLK_A4	RSVD	AW14			AT10	#SCLK_B4			
	AH40	SCLK_A5	RSVD	AW19			AJ38	SCLK_B5			
	AH43	#SCLK_A5	RSVD	AK40			AJ36	#SCLK_B5			
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			RSVD	AK17				RSVD_TP2			
			SVREF0					SVREF1			

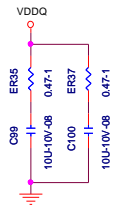
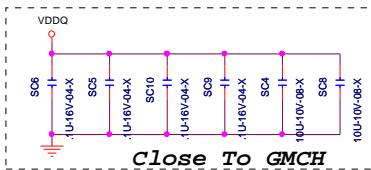
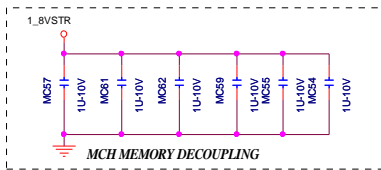
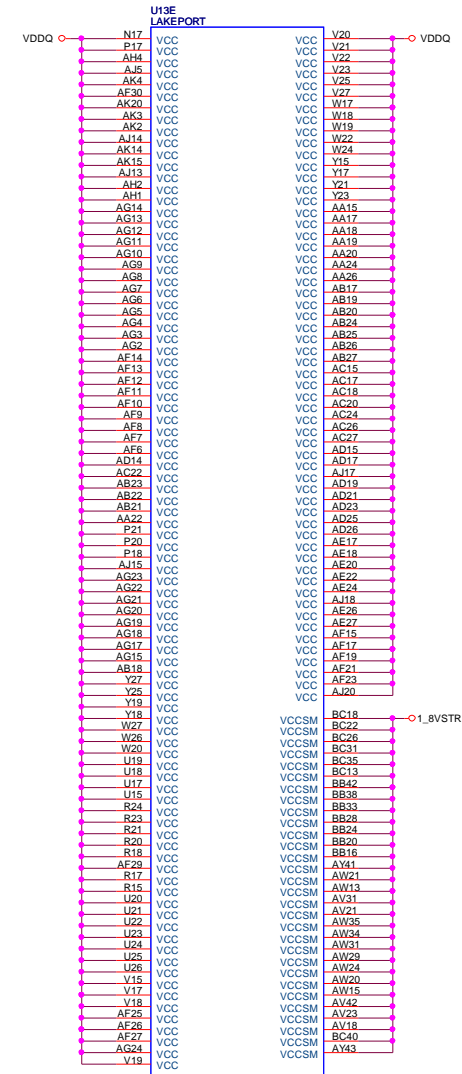
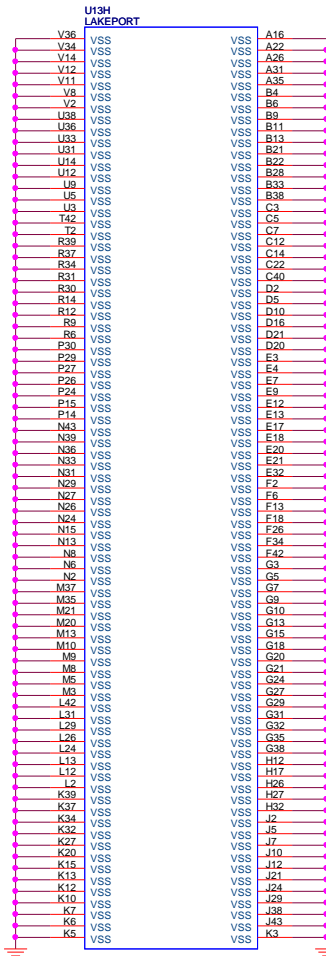
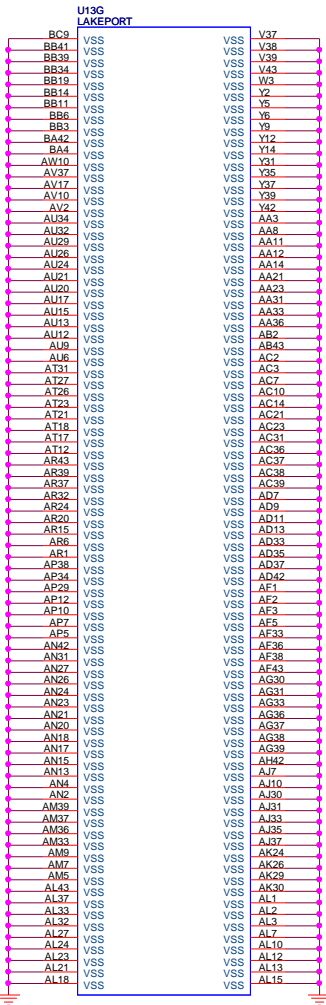


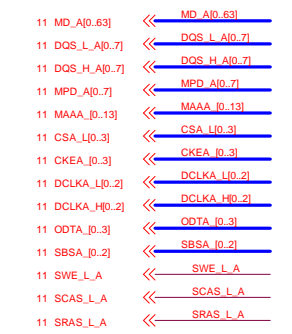
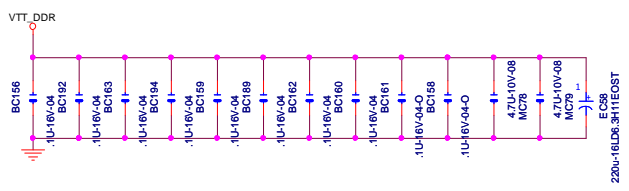
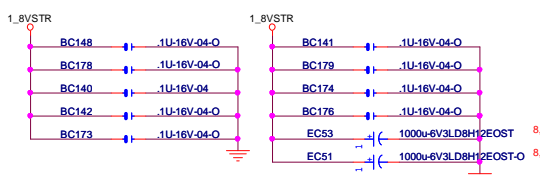
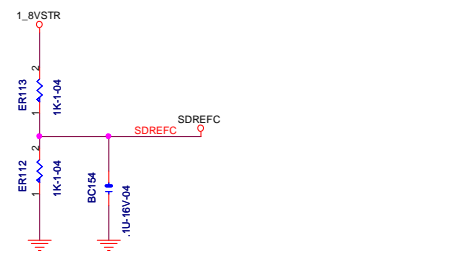
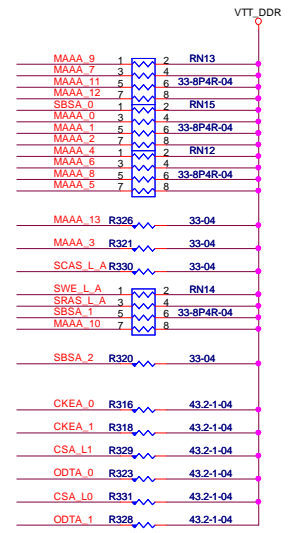
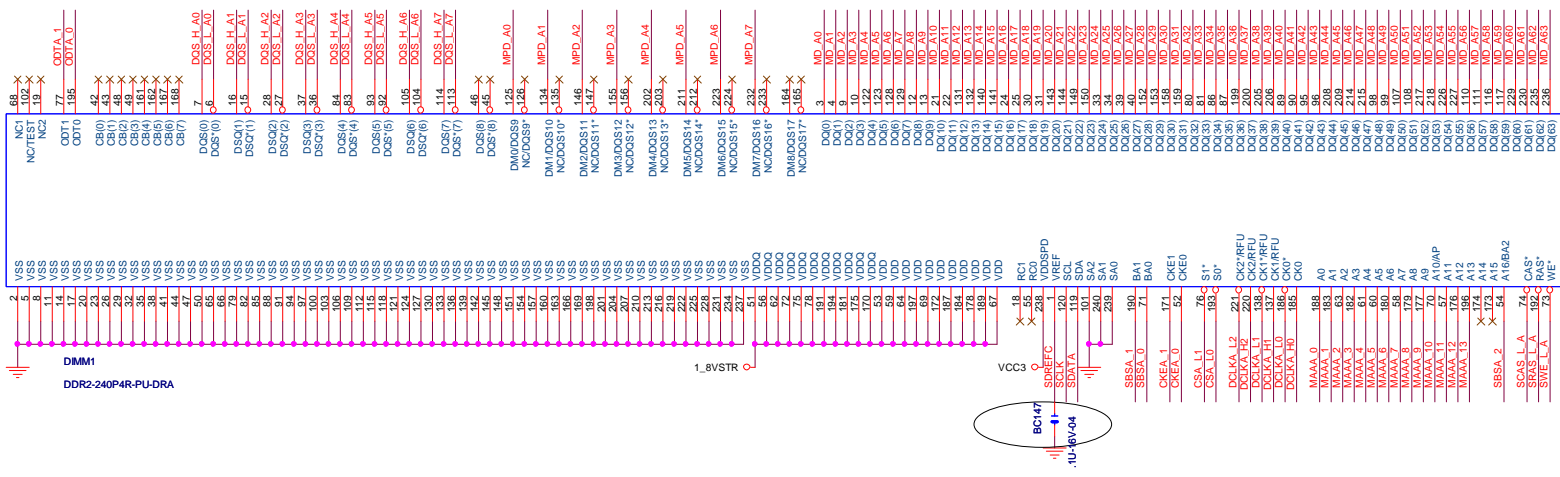
DESIGN NOTE:
BUFFERS CALIBRATE TO 20/80% OF V_{SM} INTERNAL BUFFERS SET TO 20 OHMS

STP22 1
STP21 1

STP20 1
STP19 1

TP3
STP18





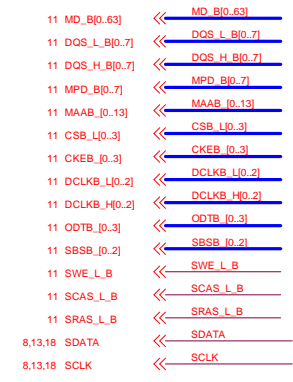
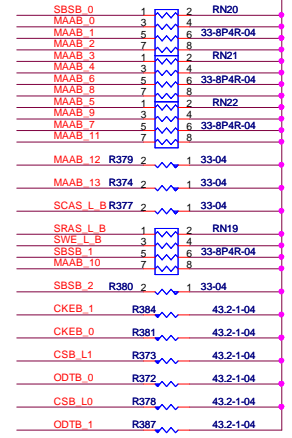
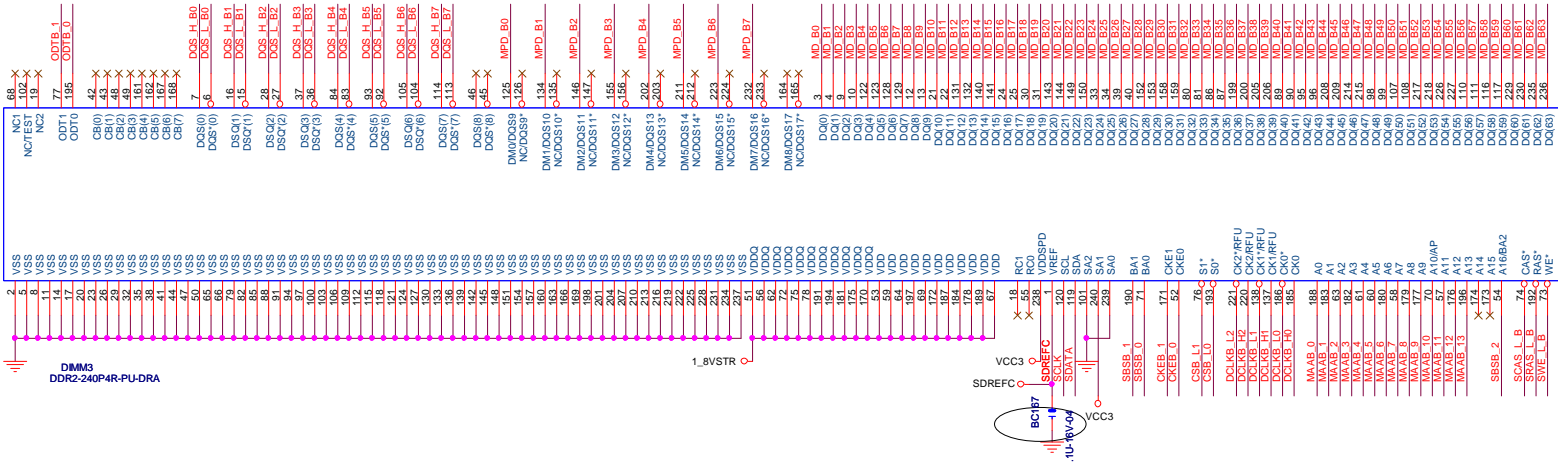
Elitegroup Computer Systems

Title: **DIMM1&2 (DDR2 SDRAM)**

Size: Document Number

Customer: **945GCT/GZT-M** Rev: 1.0

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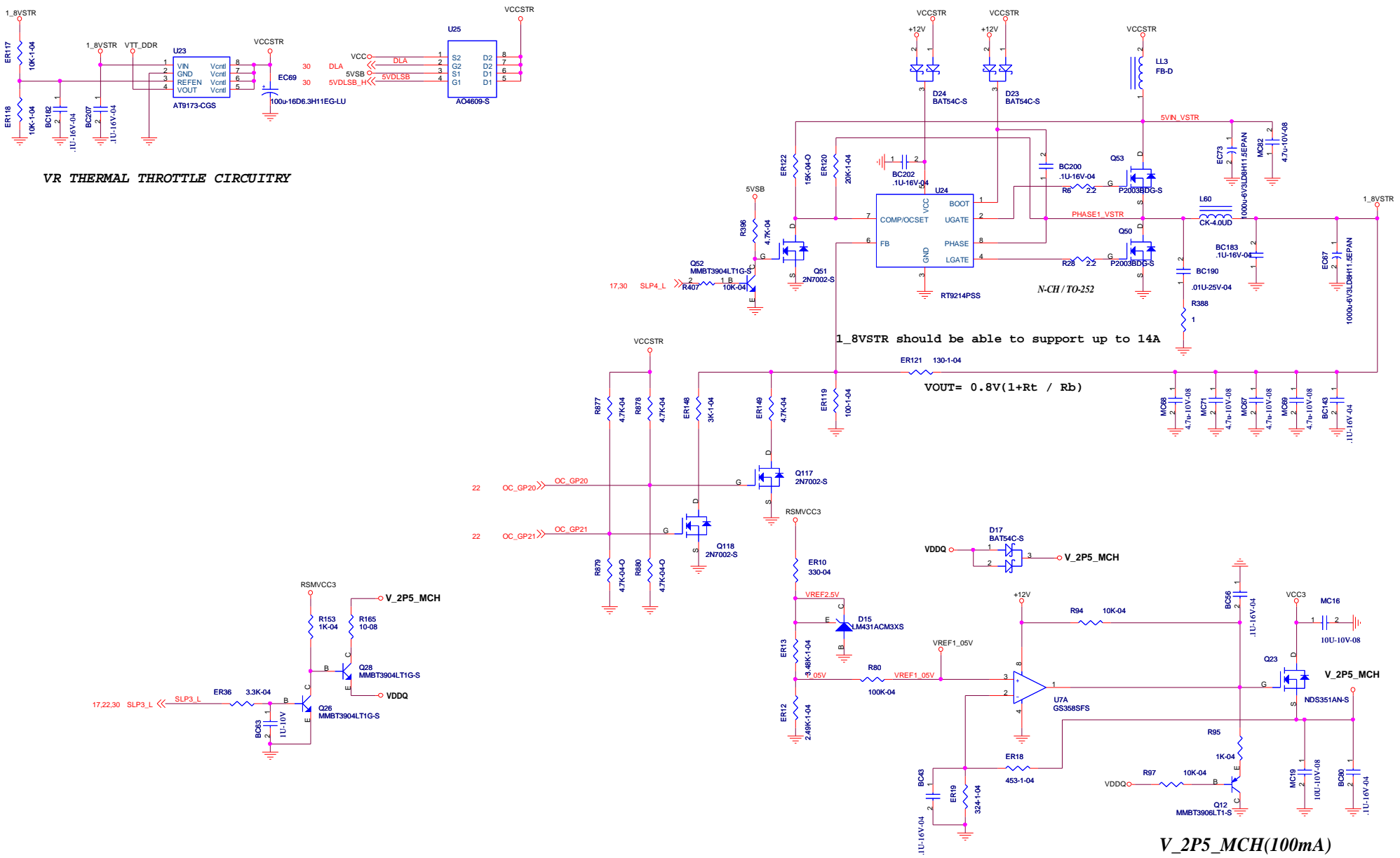
Elitegroup Computer Systems

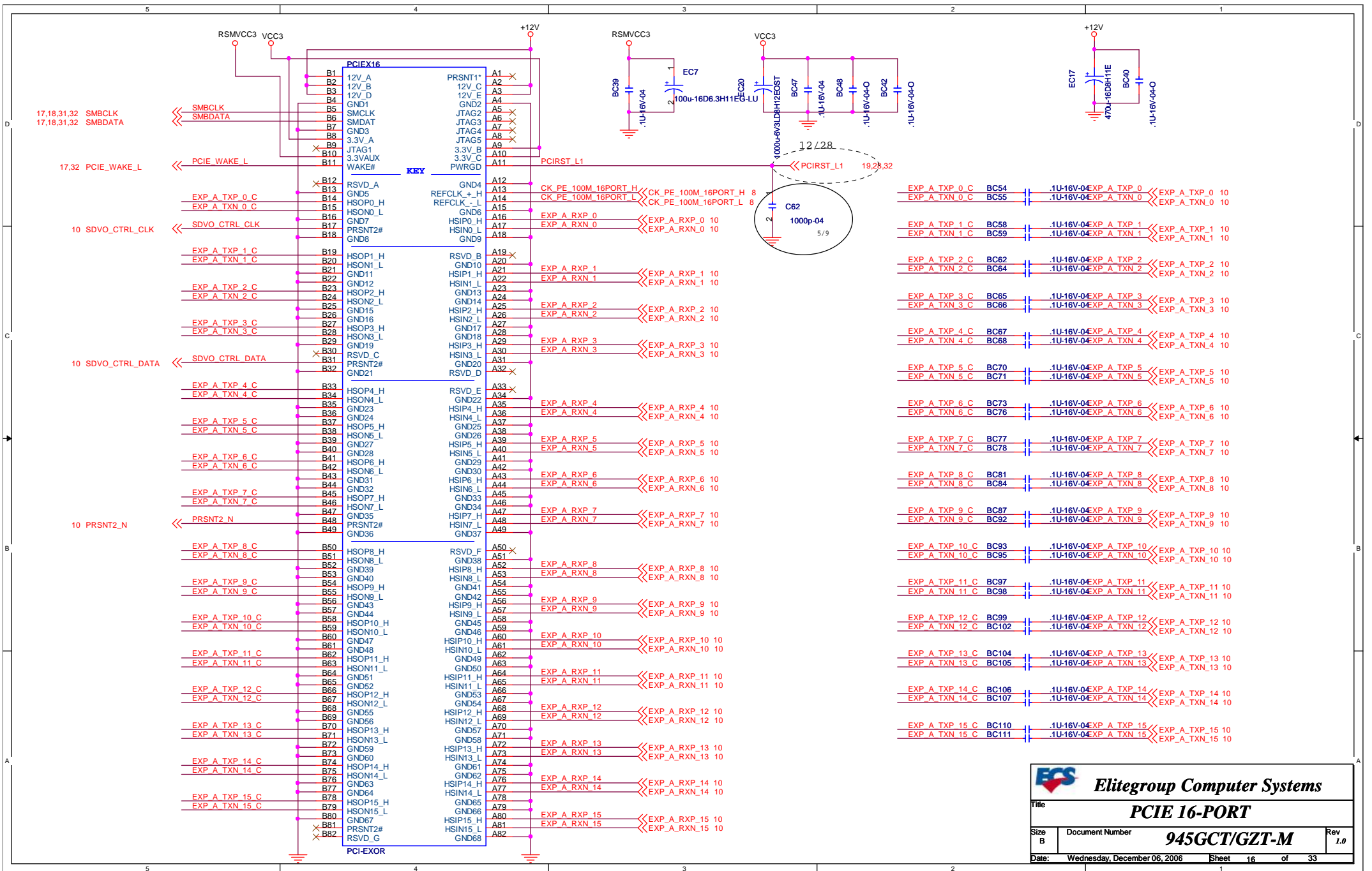
Title: DIMM3&4 (DDR2 SDRAM)

Size: Document Number

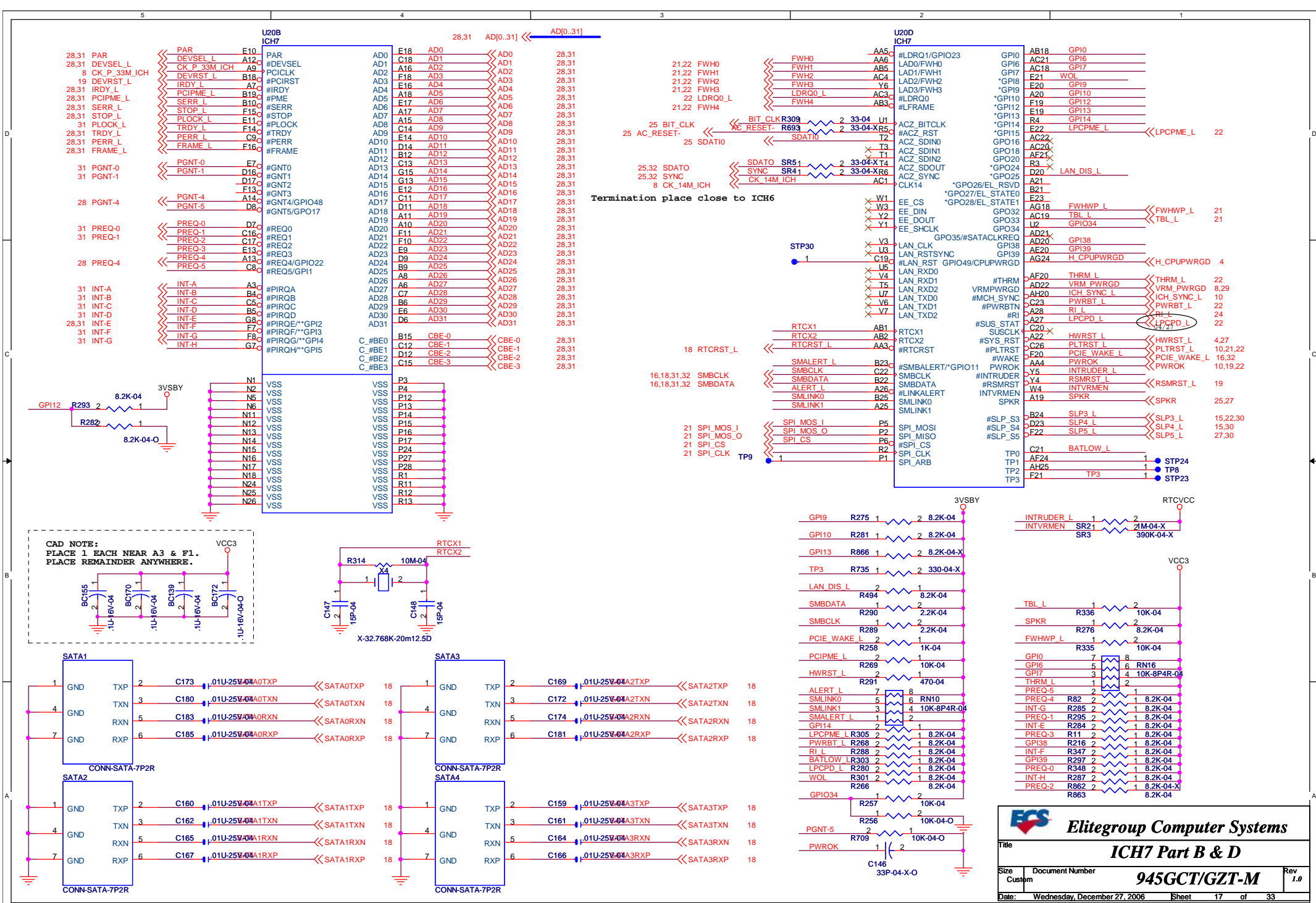
Customer: 945GCT/GZT-M Rev: 1.0

Date: Friday, December 01, 2006 Sheet: 14 of 33

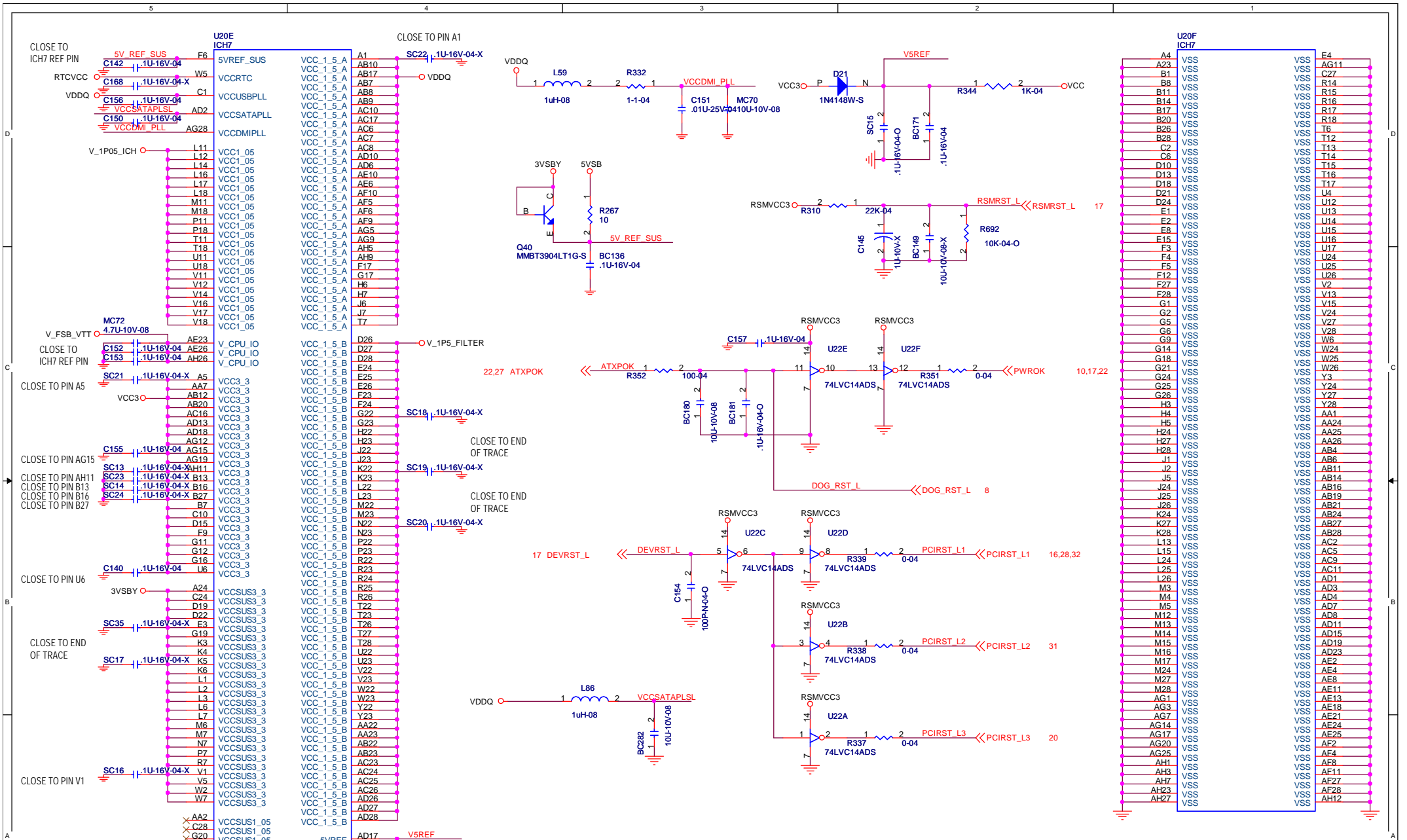





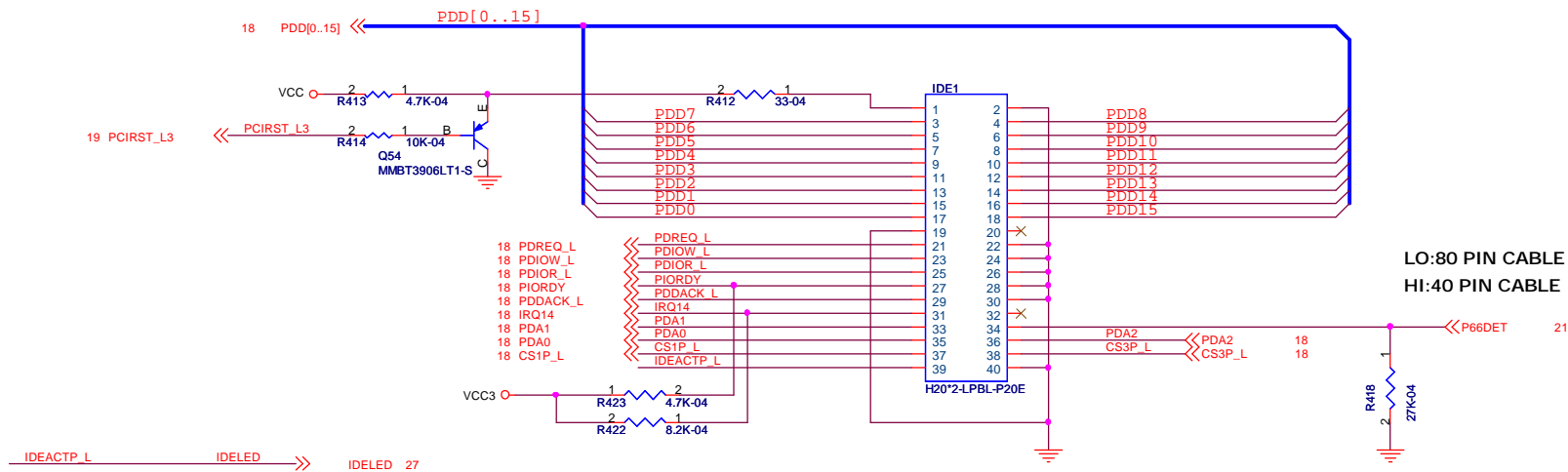
Elitegroup Computer Systems PCI E 16-PORT		
Title PCI E 16-PORT	Document Number 945GCT/GZT-M	Rev 1.0
Size B	Date Wednesday, December 06, 2006	Sheet 16 of 33



Elitegroup Computer Systems
ICH7 Part B & D
Size: Custom | Document Number: 945GCT/GZT-M | Rev: 1.0
Date: Wednesday, December 27, 2006 | Sheet: 17 of 33



 Elitegroup Computer Systems		ICH7 Part E & F	
		Title	Document Number
Size	Custom	945GCT/GZT-M	Rev 1.0
Date:	Friday, December 01, 2006	Sheet	19 of 33

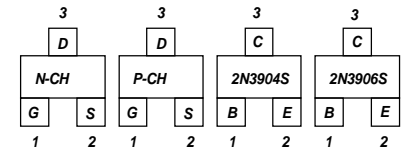
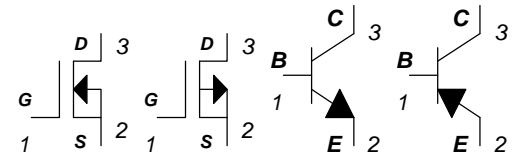


LO:80 PIN CABLE
HI:40 PIN CABLE

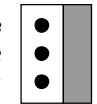
MAX TRACE LENGTH IS 8"

DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR_L , XIORDY_L) WITHIN +/- 250 MIL,
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.

Top View SOT-23

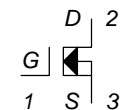


Fan Header

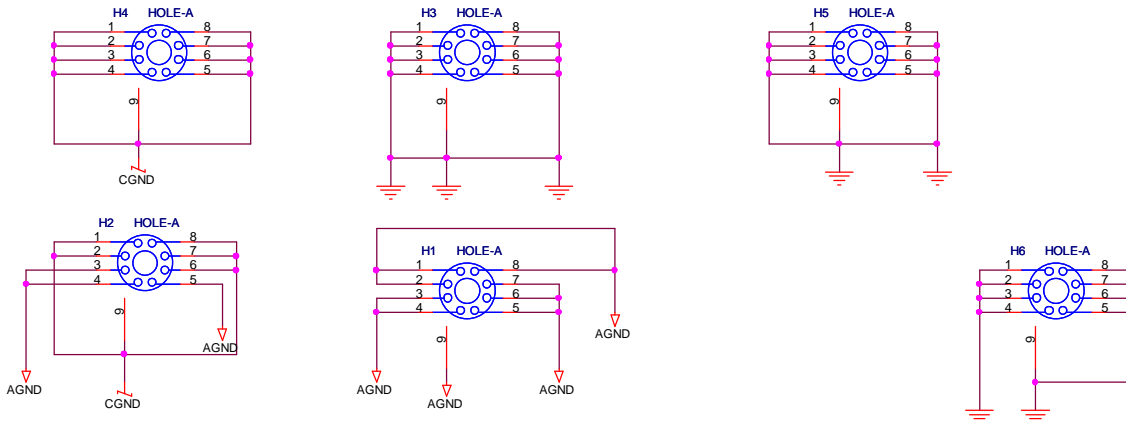
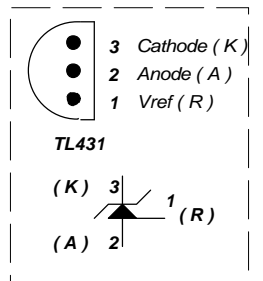


AMP640456-3

TO-263 / TO-252



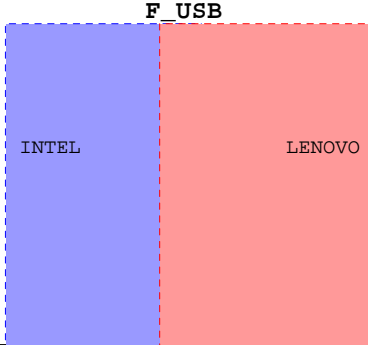
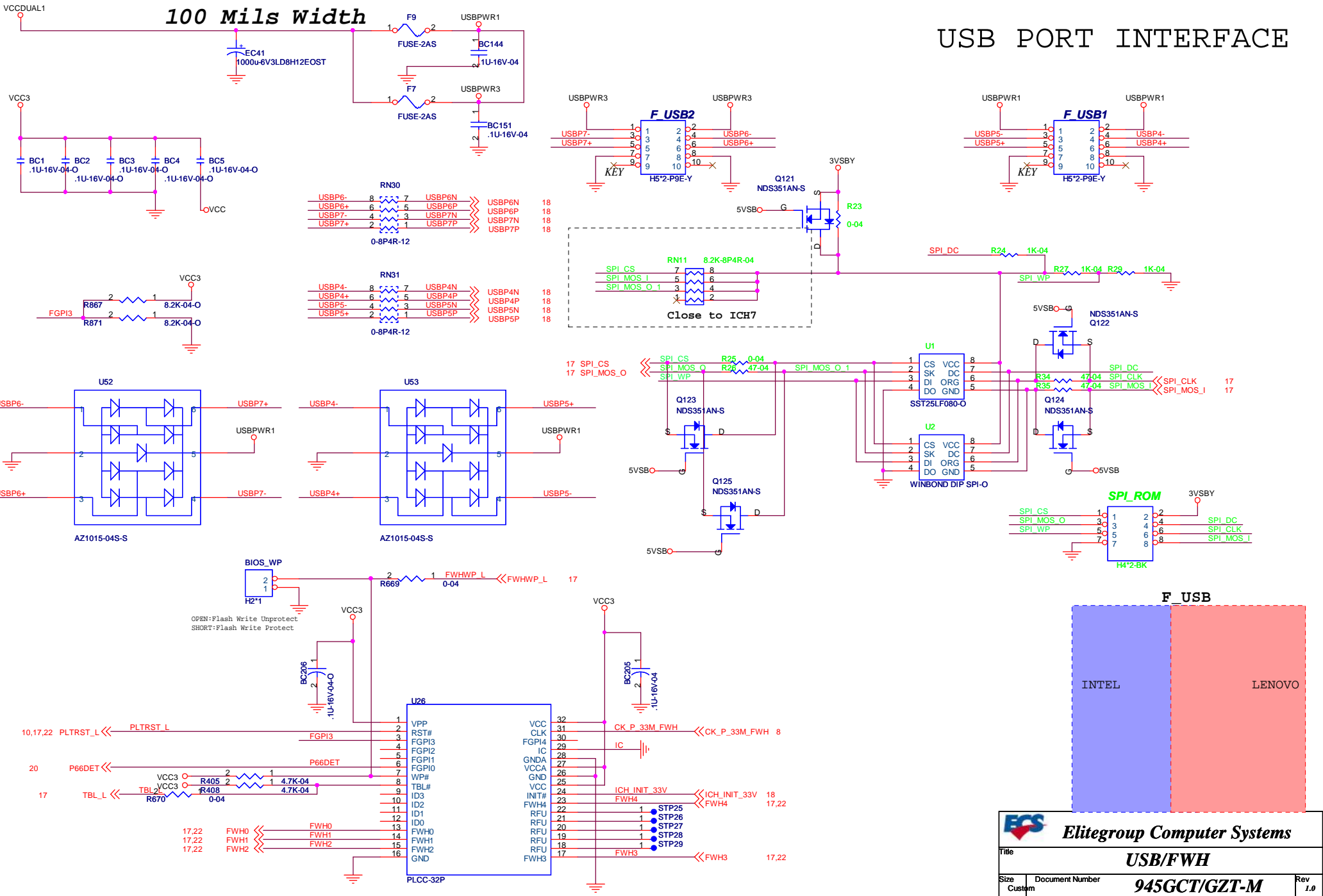
Top View



ECS Elitegroup Computer Systems		
IDE Connector		
Size	Document Number	Rev
Custom	945GCT/GZT-M	1.0
Date:	Thursday, December 07, 2006	Sheet 20 of 33

USB PORT INTERFACE

100 Mils Width

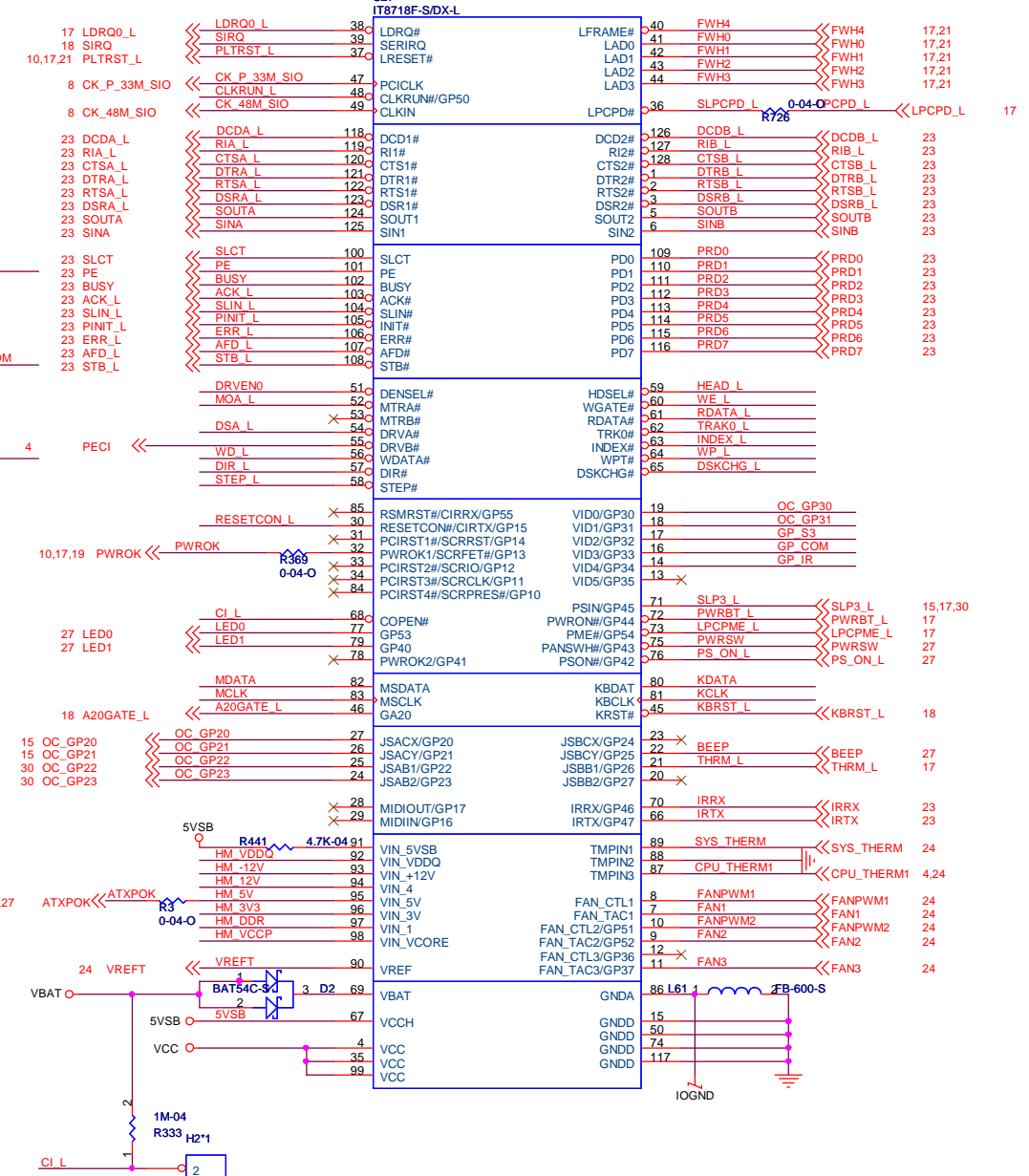
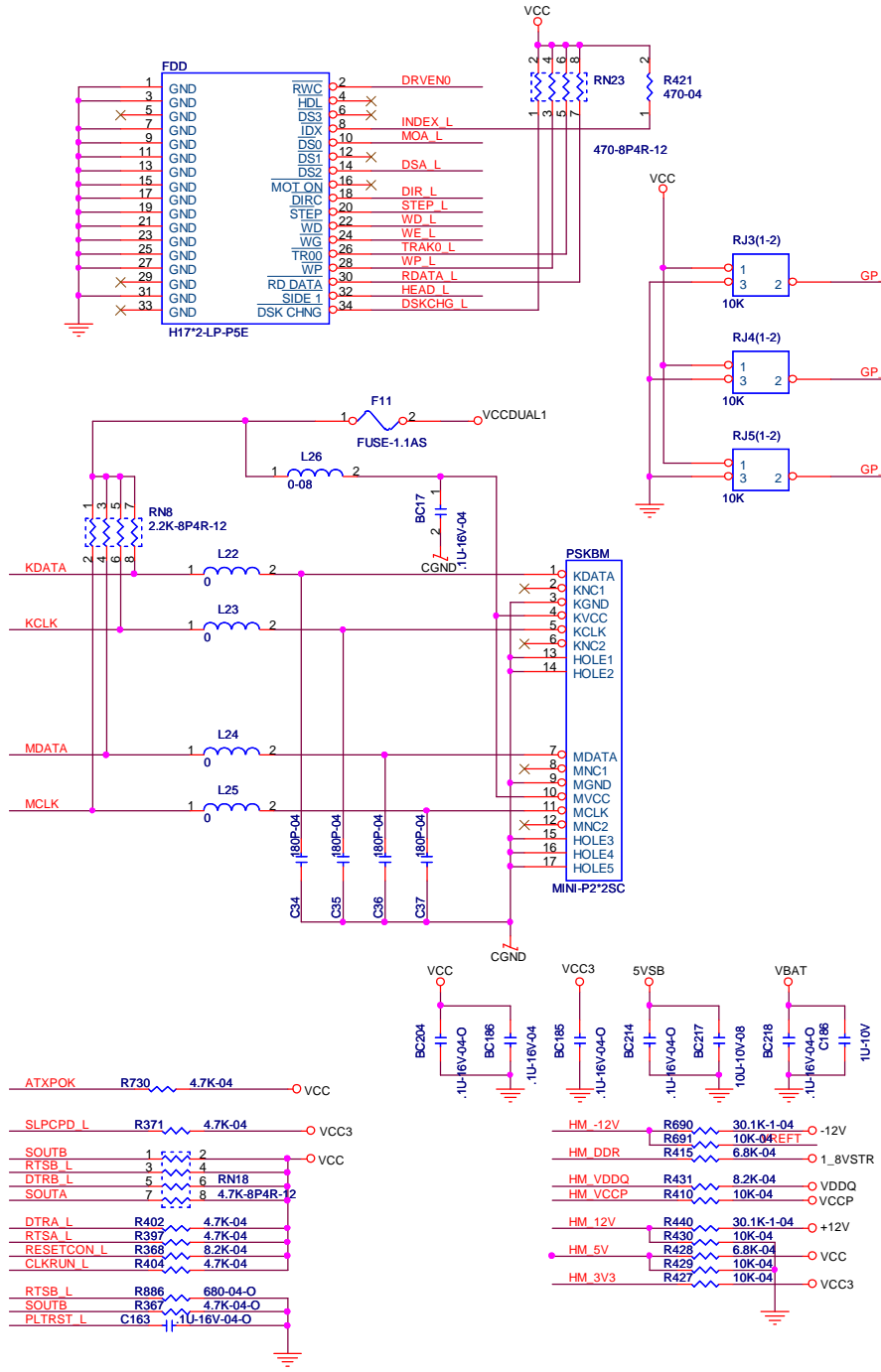


EGS Elitegroup Computer Systems

Title: **USB/FWH**

Size: Custom Document Number: **945GCT/GZT-M** Rev: 1.0

Date: Friday, December 08, 2006 Sheet: 21 of 33

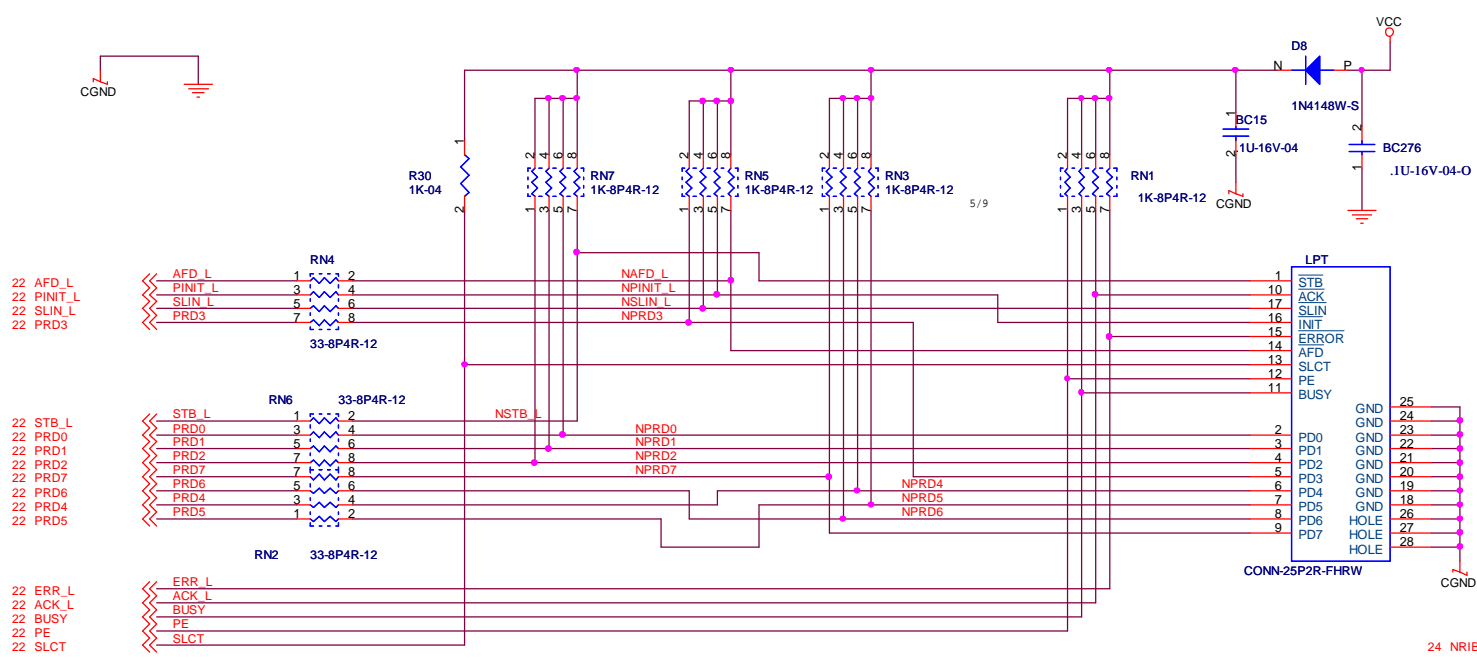
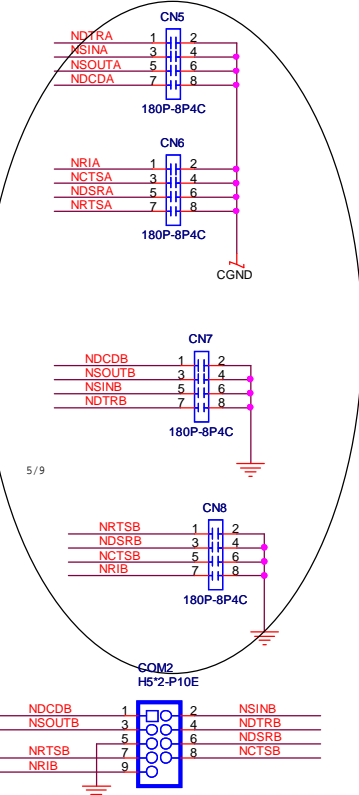
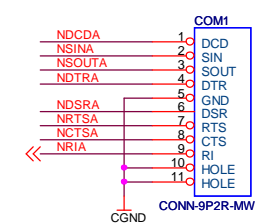
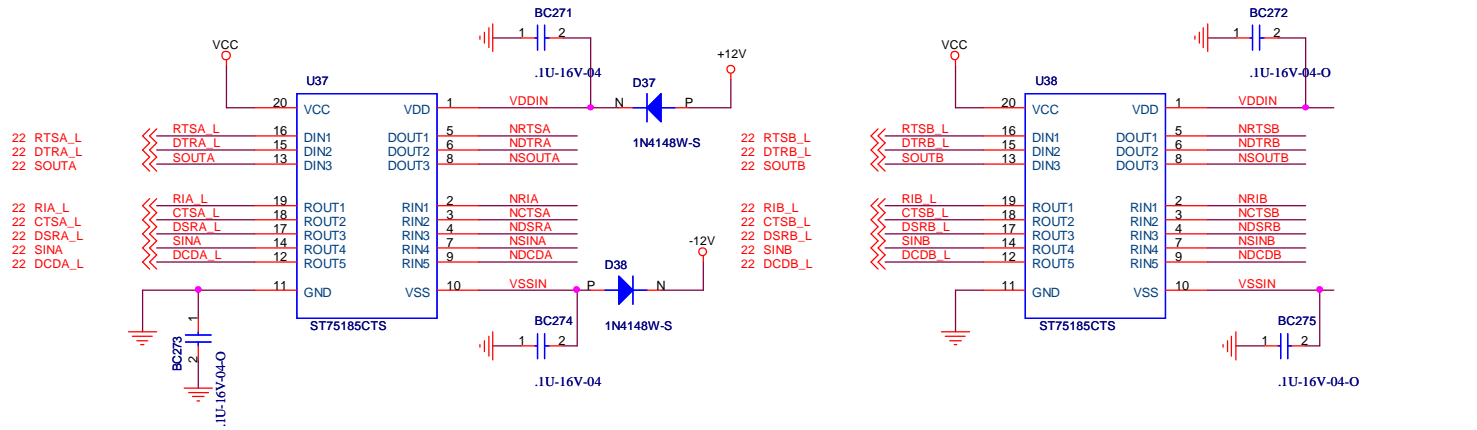


Elitegroup Computer Systems

Title: **LPC_FDD/KB/M**

Size: Custom Document Number: **945GCT/GZT-M** Rev: 1.0

Date: Friday, December 01, 2006 Sheet: 22 of 33

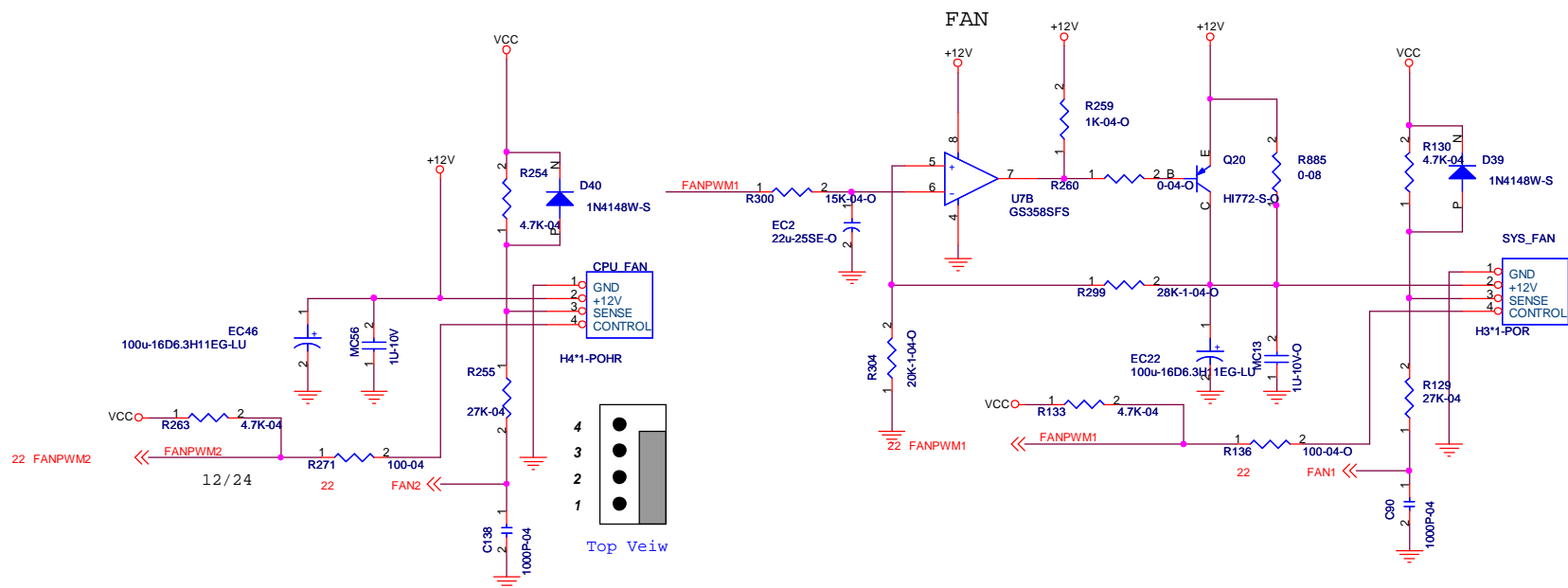


ECS Elitegroup Computer Systems

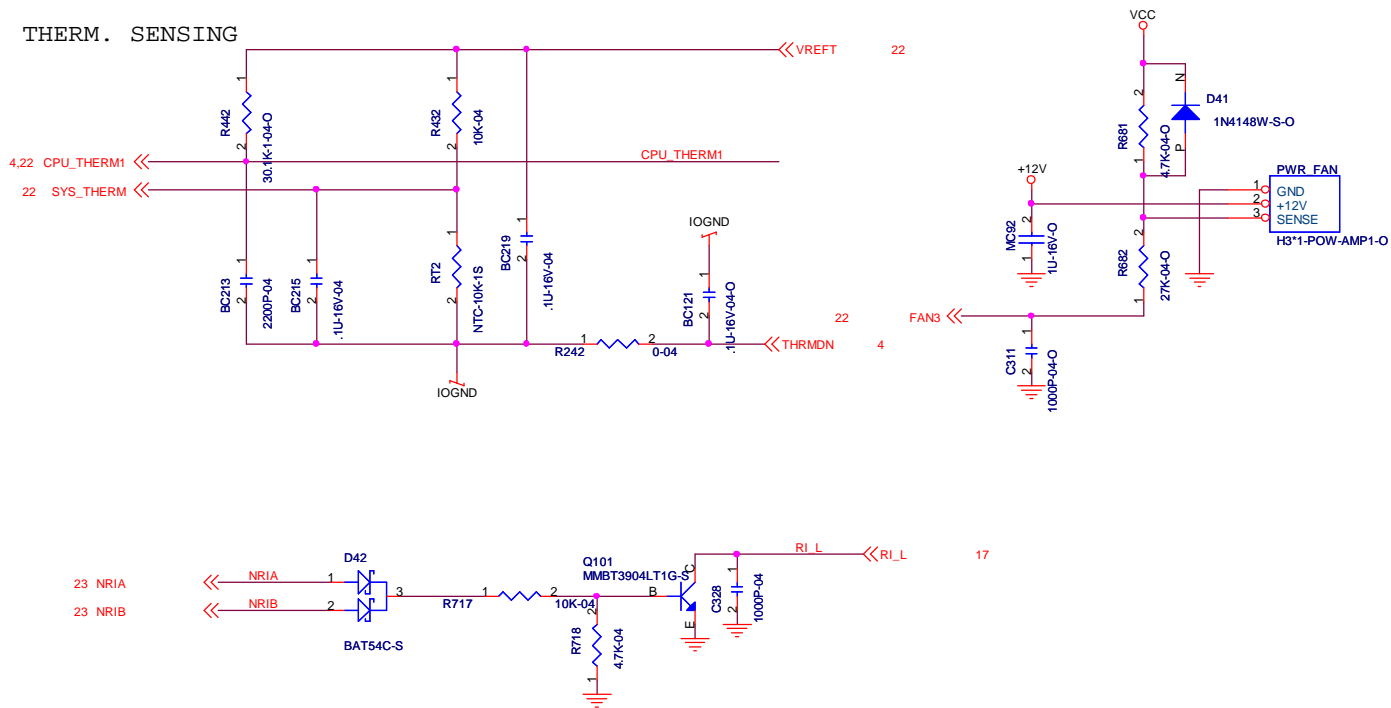
I/O Ports

Size: Custom Document Number: **945GCT/GZT-M** Rev: 1.0

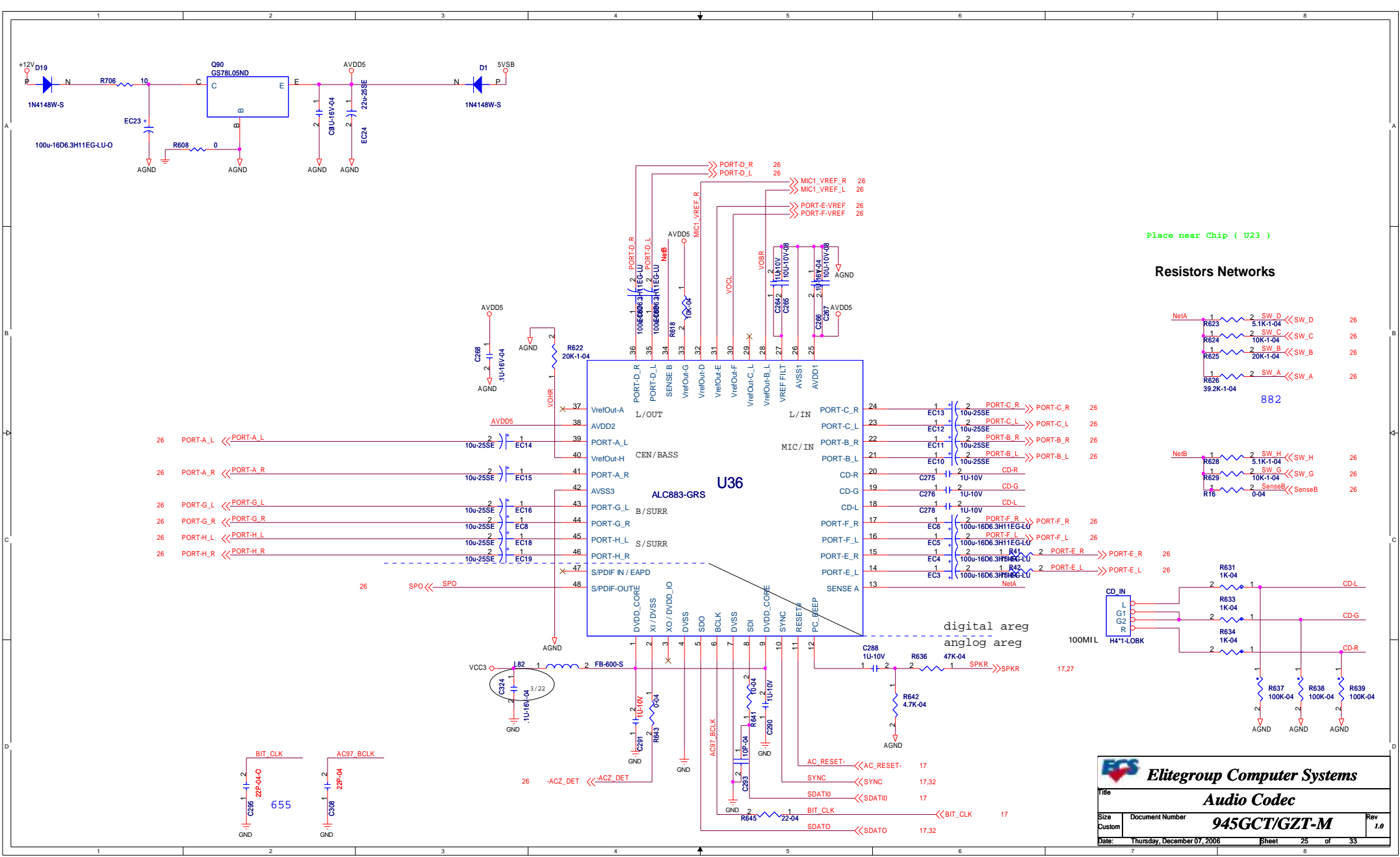
Date: Tuesday, December 05, 2006 Sheet: 23 of 33



THERM. SENSING

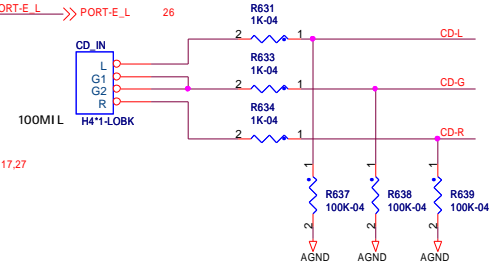
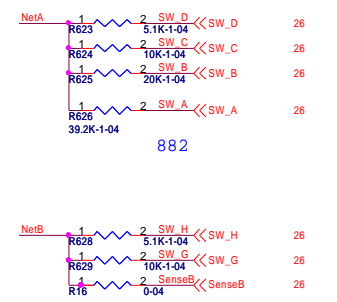


ECS Elitegroup Computer Systems		
Title H/W Monitor		
Size Custom	Document Number 945GCT/GZT-M	Rev 1.0
Date: Tuesday, December 12, 2006	Sheet 24 of 33	



Place near Chip (U23)

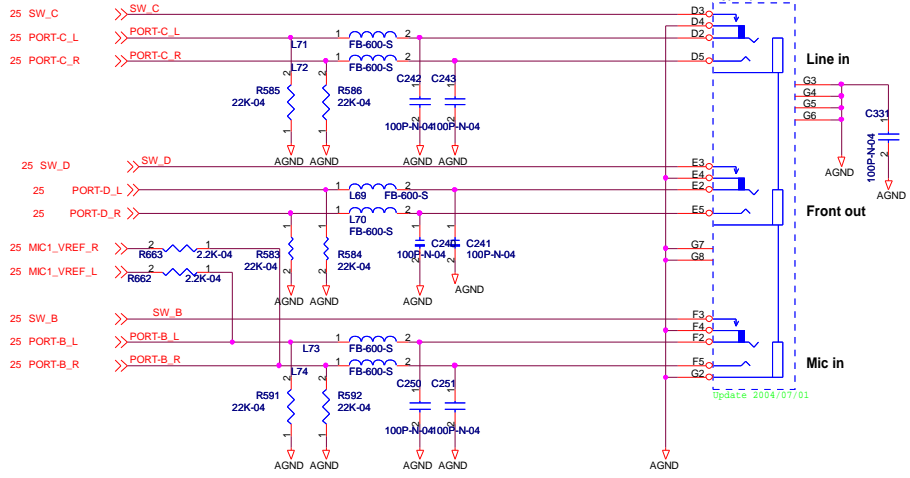
Resistors Networks



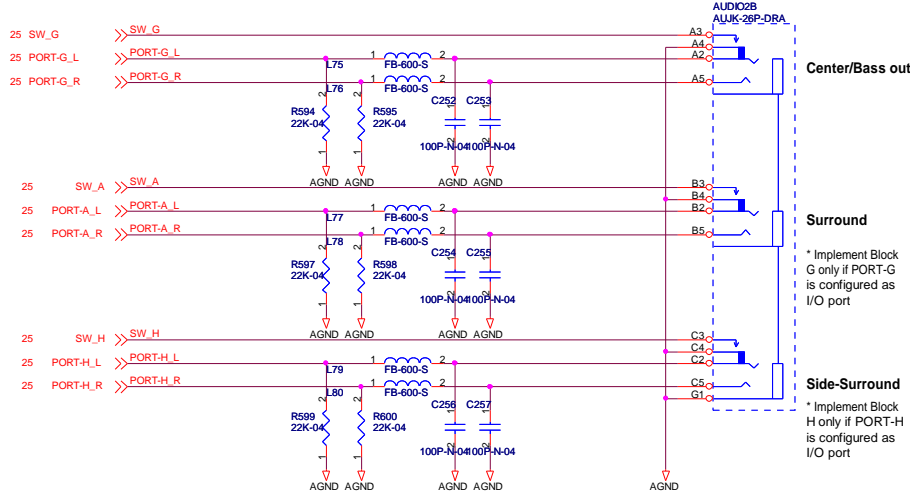
Elitegroup Computer Systems
Audio Codec

Size	Document Number	Rev
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Date:	Thursday, December 07, 2006	Sheet 25 of 33

Rear Panel Onboard Analog I/O



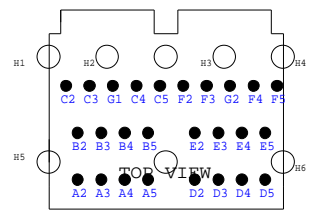
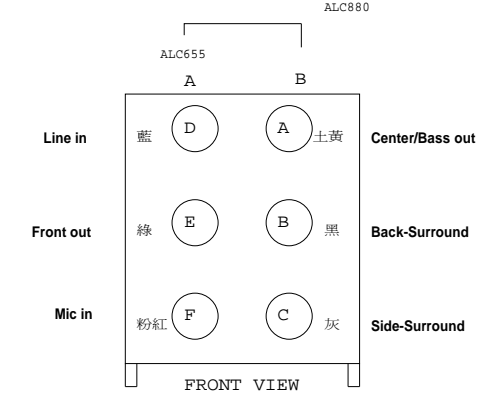
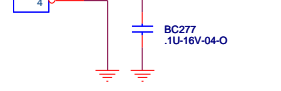
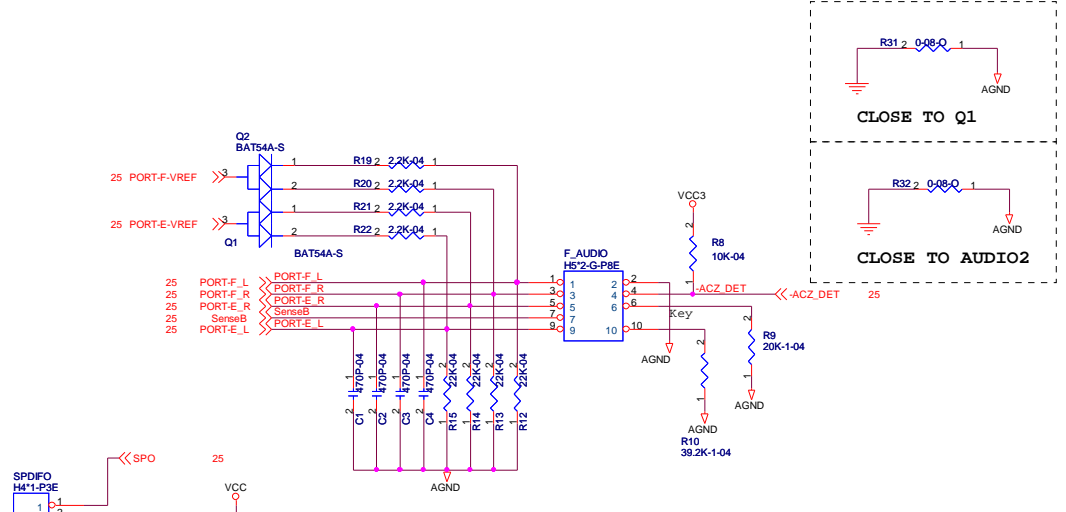
Rear Panel (Optional Rear Audio Panel)

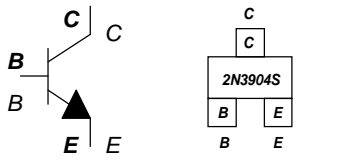
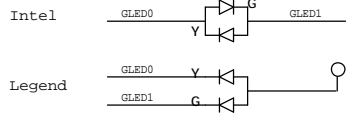
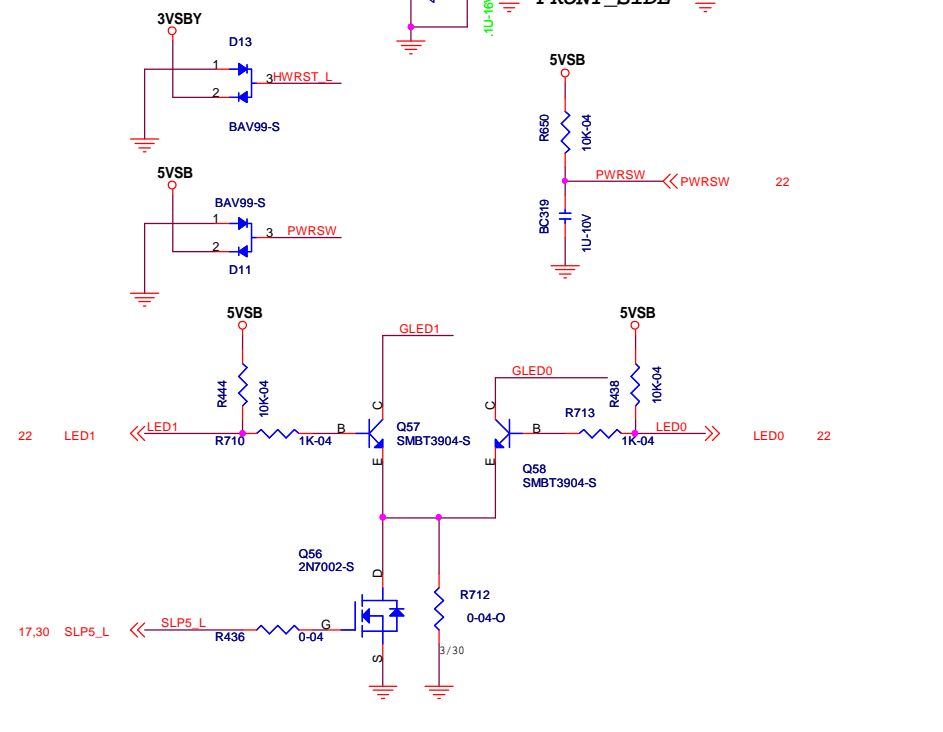
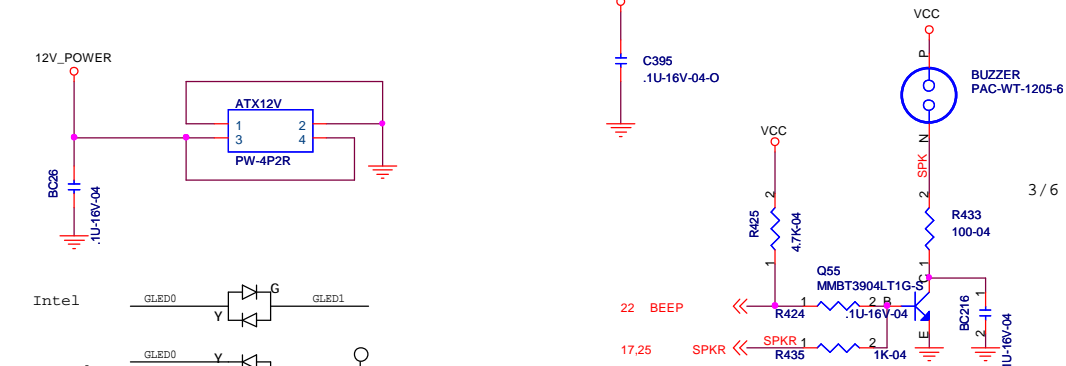
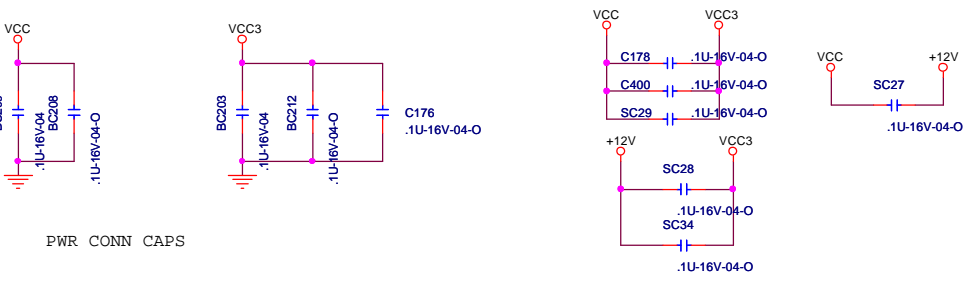
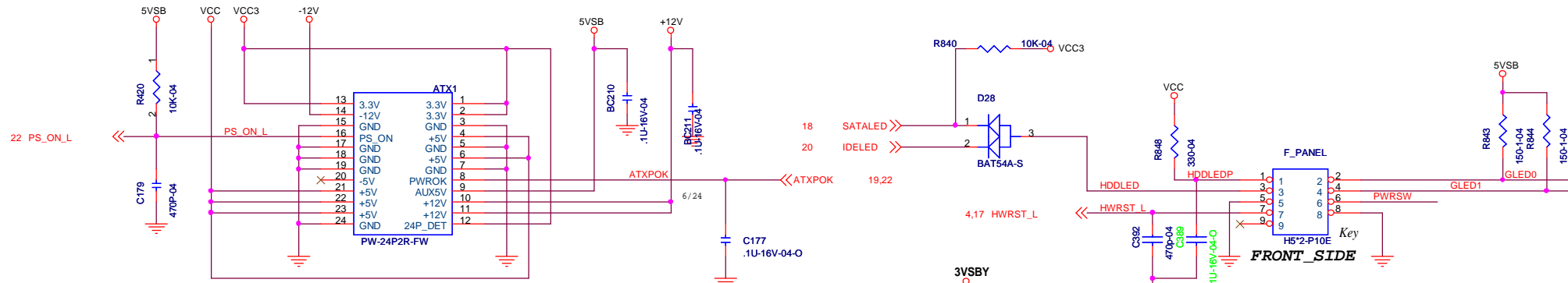


Center/Bass out
Surround
Side-Surround

* Implement Block G only if PORT-G is configured as I/O port
* Implement Block H only if PORT-H is configured as I/O port

The schematic should consist with PINS define of I/O connector.





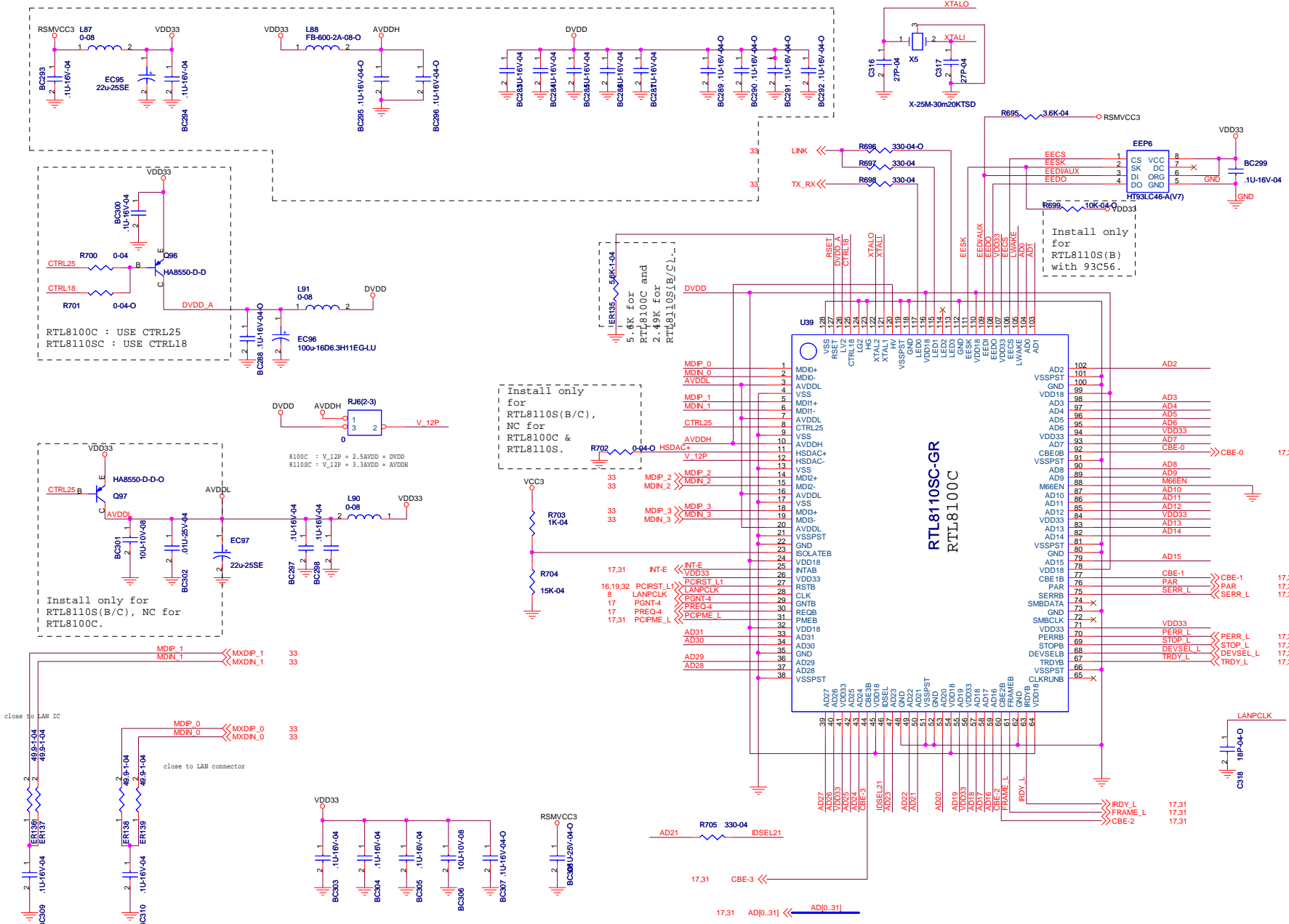
	s0	s1	s3	S4,S5
PANEL1(4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1(3,5,7)	Green	G-blinking	G-blinking	Dark
LSJ1(1,2)	Dark	Dark	Light	Dark
SJ1(1,3)(2,3)	Light	Blinking	Blinking	Dark
GLED0	HIGH	HIGH	LOW	HIGH
GLED1	LOW	SWITCH	SWITCH	HIGH

Elitegroup Computer Systems

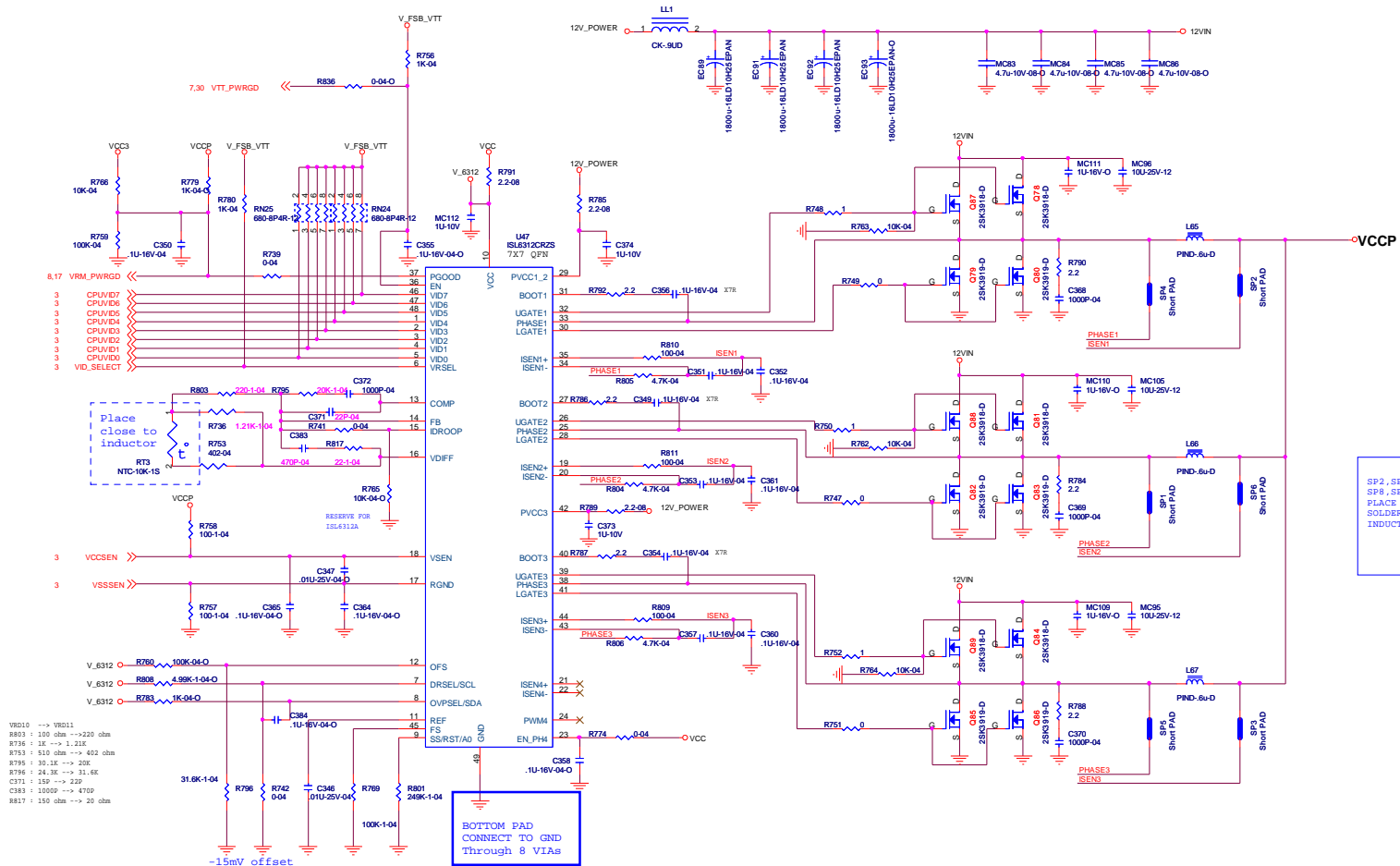
ATX Power & Front Panel

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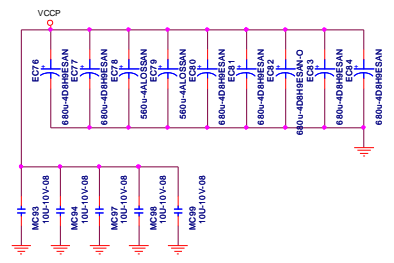
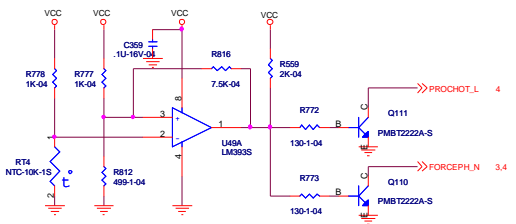
ISL6312/6322CR FOR Intel P4 Broadwater VRD11 POWER CKT - 4 PHASE



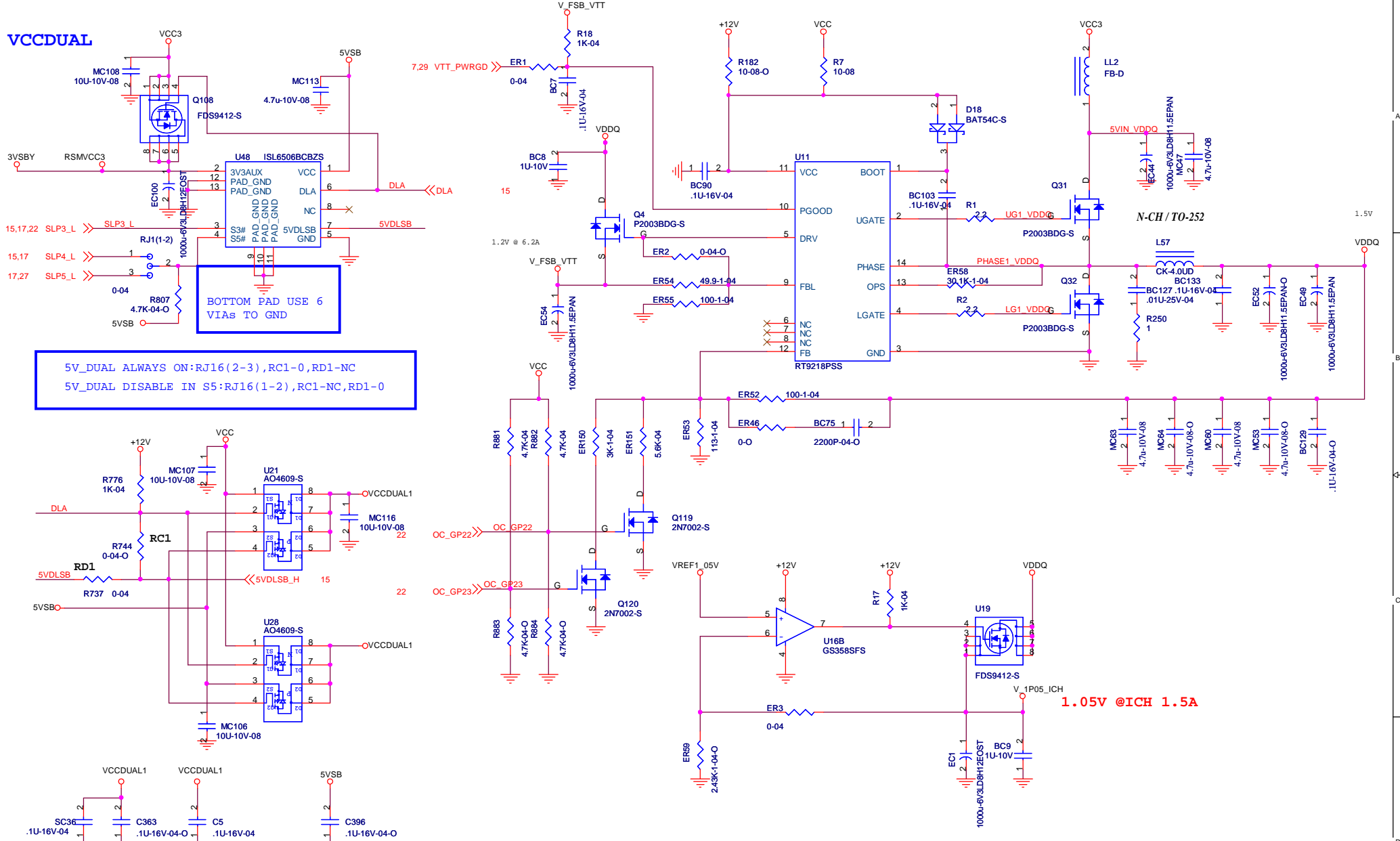
SP2, SP3, SP5, SP6, SP8, SP9, SP11, SP12 PLACE ON THE SOLDER SIDE, CLOSE INDUCTOR

- VRD10 -> VRD11
- R803 : 100 ohm -> 220 ohm
- R736 : 1k -> 1.21k
- R753 : 510 ohm -> 402 ohm
- R795 : 30.1k -> 20k
- R796 : 24.3k -> 31.6k
- C371 : 150 -> 220
- C383 : 1000p -> 470p
- R817 : 150 ohm -> 20 ohm

-15mV offset
Remark: R36,R37,C43,R39,Q10 reserve for ISL6322



VCCDUAL

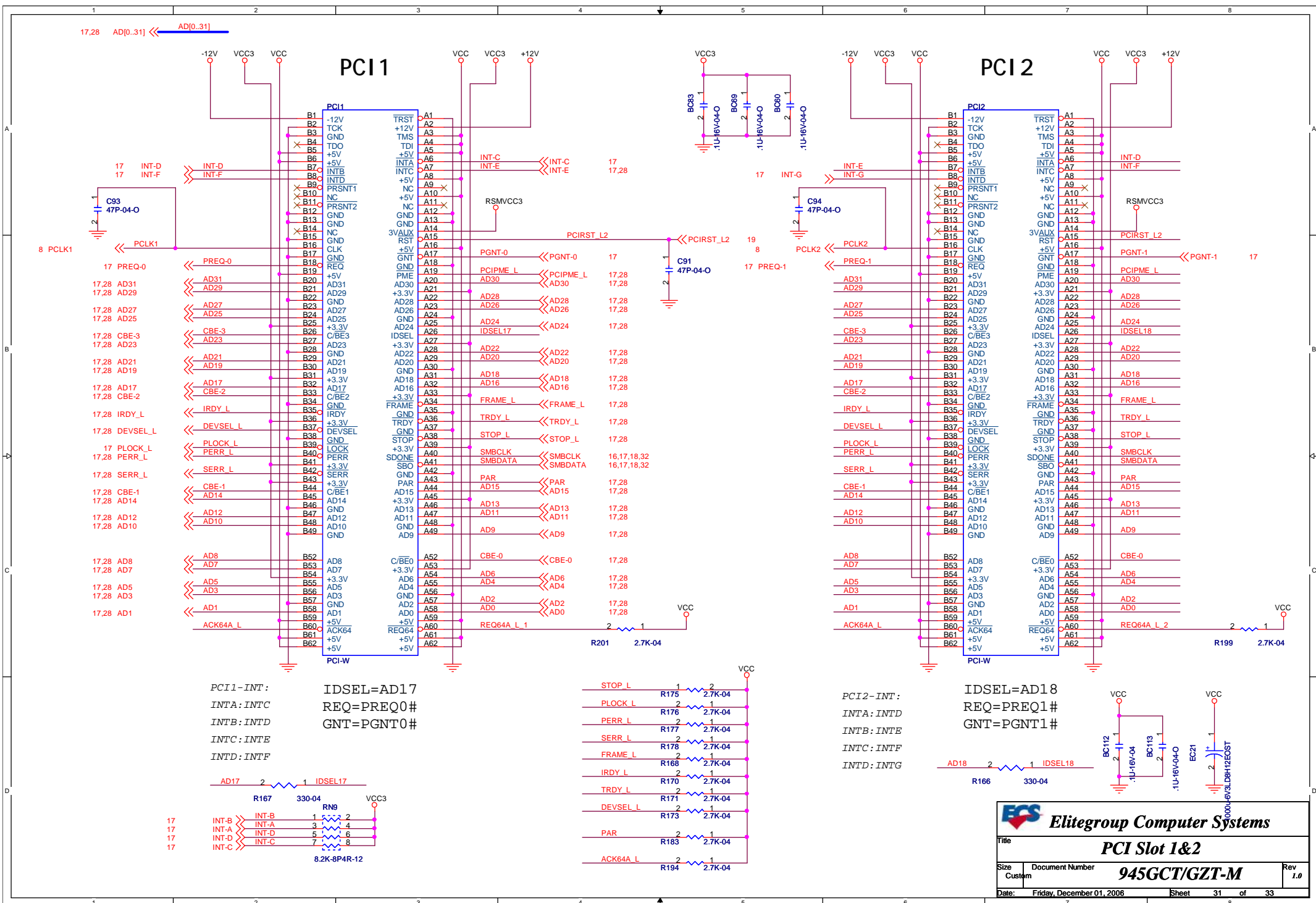


BOTTOM PAD USE 6 VIAS TO GND

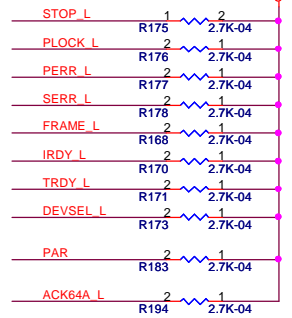
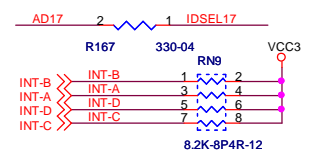
5V_DUAL ALWAYS ON:RJ16(2-3),RC1-0,RD1-NC
5V_DUAL DISABLE IN S5:RJ16(1-2),RC1-NC,RD1-0

1.05V @ ICH 1.5A

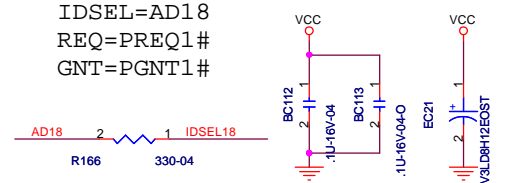
MIS DC-DC			
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PCI1-INT: IDSEL=AD17
 INTA: INT-C
 INTB: INT-D
 INTC: INT-E
 INTD: INT-F
 REQ=PREQ0#
 GNT=PGNT0#



PCI2-INT: IDSEL=AD18
 INTA: INT-D
 INTB: INT-E
 INTC: INT-F
 INTD: INT-G
 REQ=PREQ1#
 GNT=PGNT1#



Elitegroup Computer Systems

Title: **PCI Slot 1&2**

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	SDATO	SYNC
4lane x1	1	1
1lane x4	0	0

17.25 SDATO

17.25 SYNC

16.17,18,31 SMBCLK
16.17,18,31 SMBDATA

16.17 PCIE_WAKE_L

18 HSO_P1
18 HSO_N1

18 HSO_P2
18 HSO_N2

18 HSO_P3
18 HSO_N3

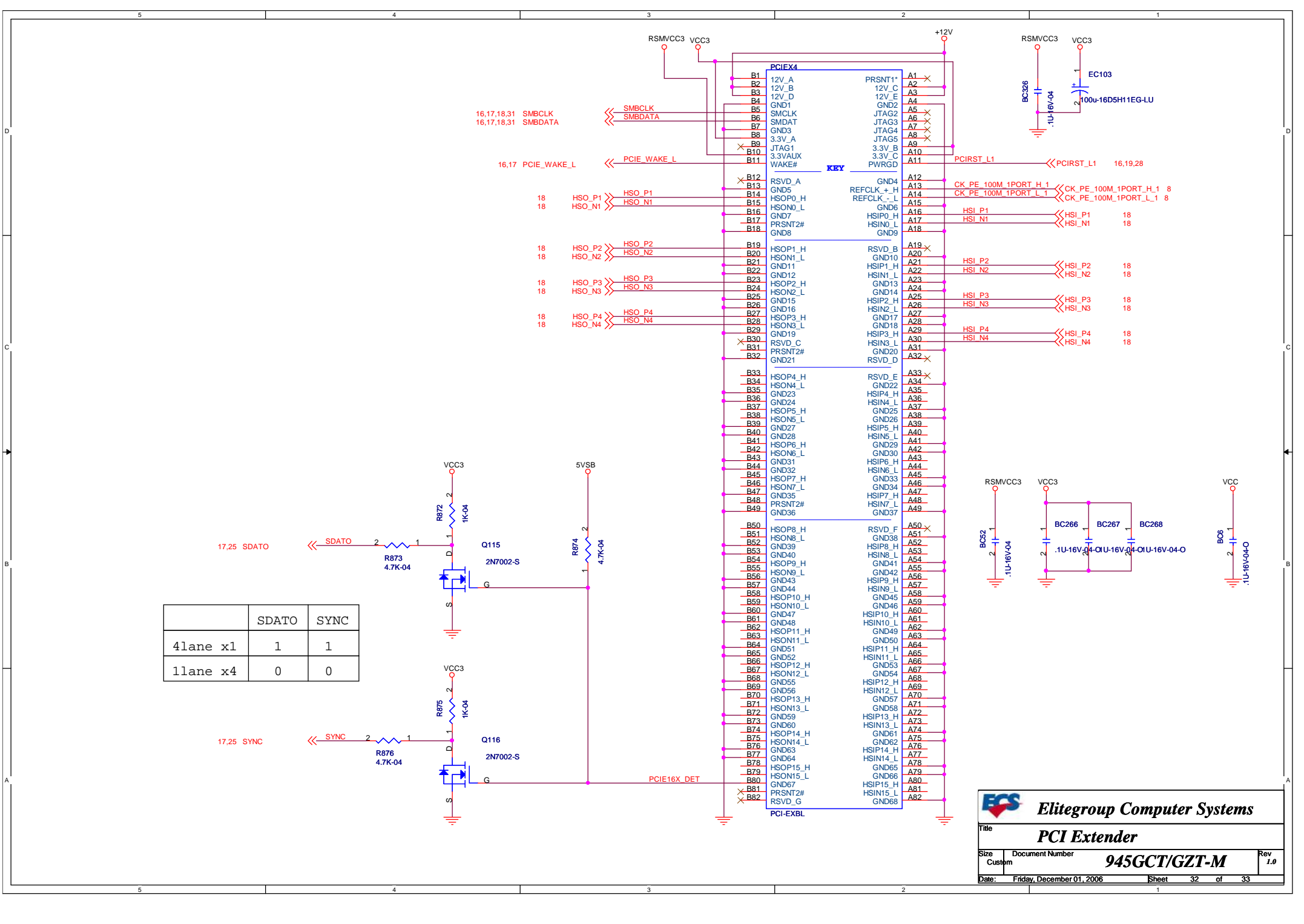
18 HSO_P4
18 HSO_N4

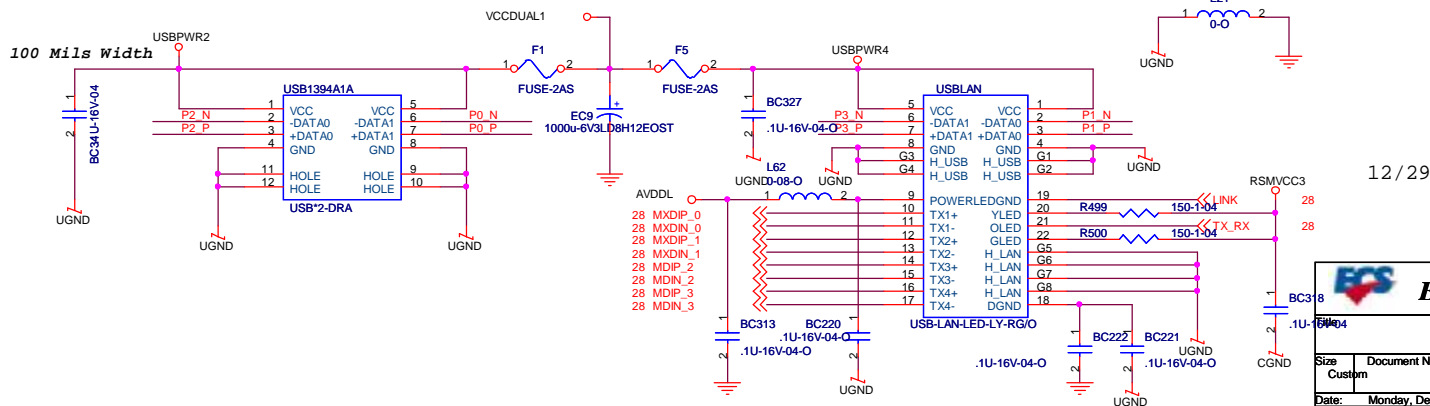
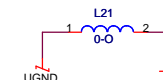
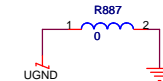
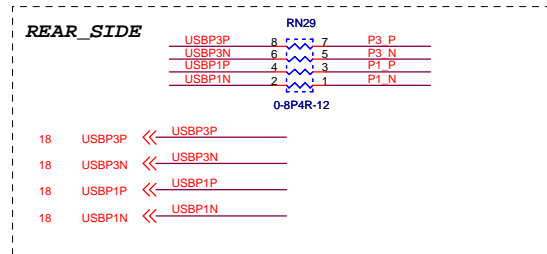
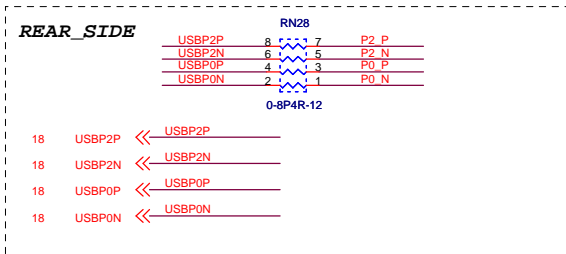
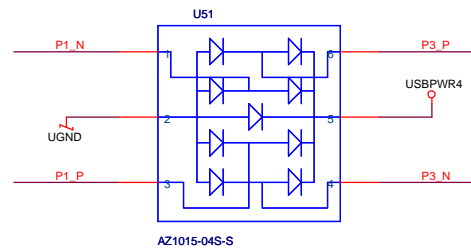
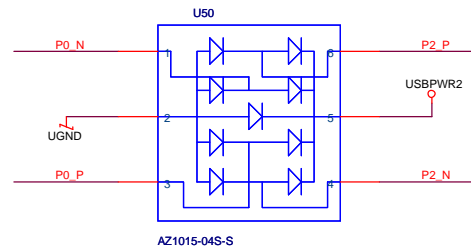
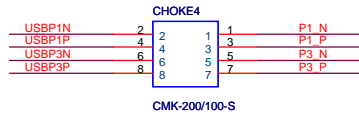
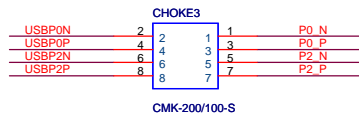
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PCI Extender

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Back I/O

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