

Page	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20
Rev.	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
Data	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21

Page	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
Rev.	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
Data	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21

**Elitegroup Computer Systems**

Title: **BLOCK DIAGRAM**

Size: C Document Number: **558-1-4-01** Rev: 2.0

Date: Thursday, March 24, 2005 Sheet: 1 of 37

Voltage Rails	ON S0-S1	ON S3	ON S4	ON S5	Control signal
12VOUT	X	X	X	X	
3V_591	X	X	X	X	
5VPCU	X	X	X	X	
+3V_SS	X	X	X	X	SS_ON
+1.5V_SS	X	X	X	X	SS_ON
+1.8V/SUS	X	X	X	X	SUS_ON
+3V/SUS	X	X	X	X	SUS_ON
+5V/SUS	X	X	X	X	SUS_ON
+0.9V/SUS	X	X	X	X	SUS_ON
DDR Termination voltage	X	X	X	X	SUS_ON
Core voltage for Processor	X	X	X	X	VR_ON
+0.8V	X				MAINON
+1VCCP	X				MAINON
+1.5V	X				MAINON
+1.8V	X				MAINON
+2.5V	X				MAINON
+3V	X				MAINON
+5V	X				MAINON
+12V	X				MAINON

#### External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus+1394	AD17	1	PIROD/C
Mini-PCI	AD19	2	PIROB/D
10/100M LAN	AD23	3	PIROB

#### EC SM Bus1 address

Device
Smart Battery
THERMAL SENSOR

#### ICH6-M SM Bus address

Device	Address
SODIMM	1010 000x b
Clock Gen	1101 001x b

The region below of Clock Gen. need to place ground plane

Place these termination to close CK410M.

The Crystal must be 20PF => Close to IC chip

CLK\_EN- use to invert VCCP ok

Must be the same length at two targets(48MHz) =>

Smbus address D2

16 STP\_PCI 16.32 STP\_CPU

16 CLK48 USB 25 SIO48M

5.7 CFG1\_FSB 7 CFG2\_FSC

1.1% R340

10uF/10v\_0805\_XSR

SC232 33p/50v\_0402

SC239 10uF/10v\_0805\_XSR

SC236 0.47uF/6.3V\_0402

C405 0.47uF/6.3V\_0402

C401 0.47uF/6.3V\_0402

SR180 33 0402

SR190 33 0402

DOT96 33 0402

DOT96 33 0402

9/22

VCC3

R325 10K\_0402

Q28 2N7002

32 CLK\_EN

VCC3

SR153 4.7K\_0402

R371 4.7K\_0402

R357 10K\_0402

R368 2.49K\_1%\_0402

DOHAN-B

SR153, R371

POP, R488,

R368 DEPOP

DOHAN-B

SR153, R371

POP, R488,

R368 DEPOP

DOHAN-B

SR153, R371

POP, R488,

R368 DEPOP

DOHAN-B

SR153, R371

POP, R488,

R368 DEPOP

DOHAN-B

SR153, R371

POP, R488,

R368 DEPOP

DOHAN-B

SR153, R371

POP, R488,

R368 DEPOP

DOHAN-B

SR153, R371

POP, R488,

R368 DEPOP

DOHAN-B

SR153, R371

POP, R488,

R368 DEPOP

DOHAN-B

SR153, R371

POP, R488,

R368 DEPOP

DOHAN-B

SR153, R371

POP, R488,

R368 DEPOP

DOHAN-B

SR153, R371

POP, R488,

R368 DEPOP

DOHAN-B

SR153, R371

POP, R488,

R368 DEPOP

DOHAN-B

SR153, R371

POP, R488,

R368 DEPOP

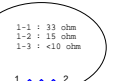
DOHAN-B

SR153, R371

POP, R488,

R368 DEPOP

FSC	FSB	FSA	CPU	SRC	PCI	REF
0	0	0	266	100	33	14.318
0	0	1	133	100	33	14.318
0	1	0	200	100	33	14.318
0	1	1	166	100	33	14.318
1	0	0	333	100	33	14.318
1	0	1	100	100	33	14.318
1	1	0	400	100	33	14.318
1	1	1	RSVD	100	33	14.318

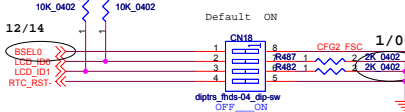


12/07 PCI\_LAN OFF

PULL HIGH TO SET PIN35,36 TO HOST CLK

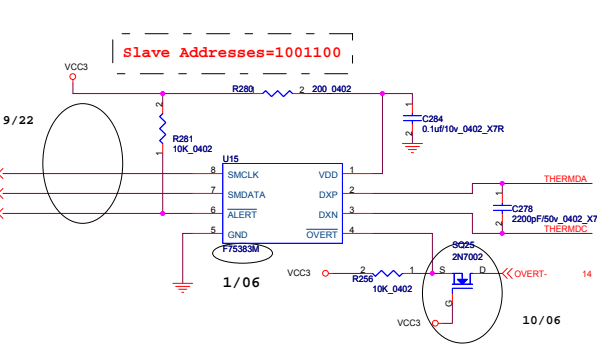
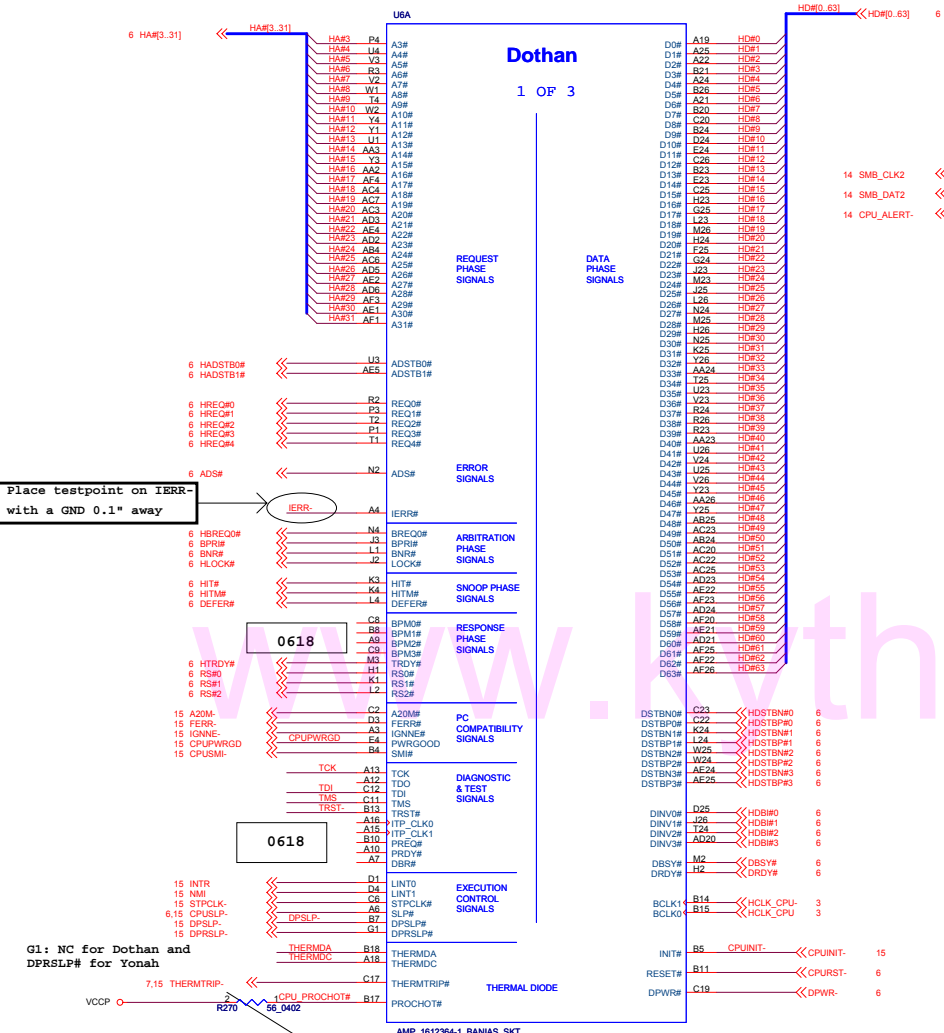
PULL LOW TO SET PIN17,18 TO 96M\_SS CLK

Place these termination to close CK410M.(ICS954201/ICS954206)



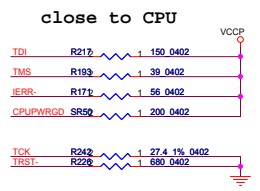
# Dothan

1 OF 3



Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	NC	Within 2.0" of the CPU

Del R682 because no ITP  
Del R672 because no ITP



Place testpoint on IERR- with a GND 0.1" away

0618

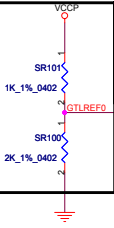
0618

G1: NC for Dothan and DPRSLP# for Yonah

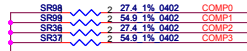
The signal should connect to ICH6 and Alviso w/o T-ing (No stub)

VCC\_CORE  
+VCCP  
+1.8V

Place voltage divider within 0.5" of GTLREF pin



Place pull-down resistors within 0.5" of COMP pins



**Dothan**  
2 OF 3

POWER, GROUND, RESERVED SIGNALS

**VCCORE**

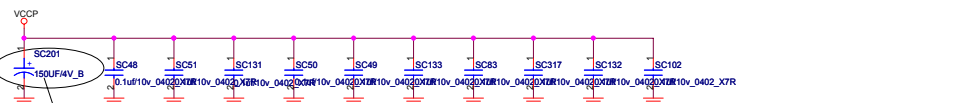
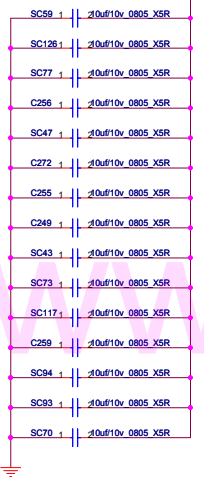
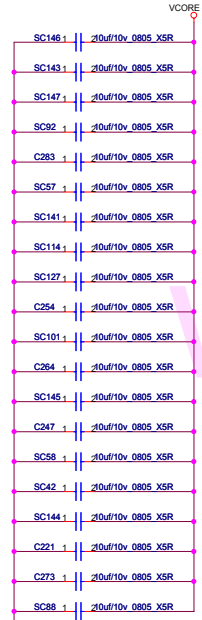
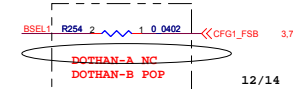
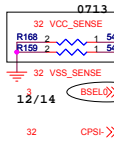
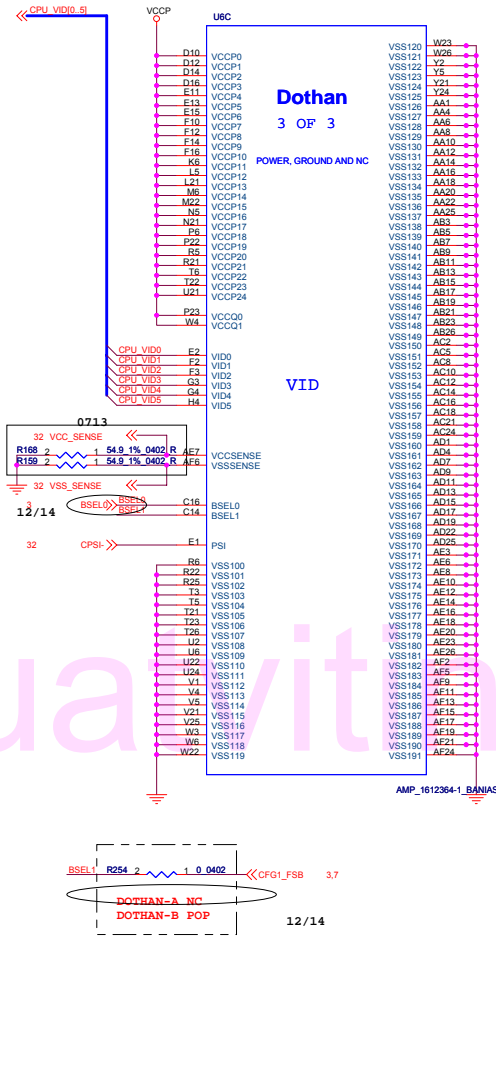
- D6 VCC00
- D8 VCC01
- D18 VCC02
- D20 VCC03
- D22 VCC04
- D24 VCC05
- E7 VCC06
- F3 VCC07
- F5 VCC08
- E19 VCC09
- E21 VCC10
- F8 VCC11
- F18 VCC12
- VSS41 VCC13
- F20 VCC14
- F22 VCC15
- G5 VCC16
- G21 VCC17
- H6 VCC18
- H22 VCC19
- J1 VCC20
- VSS48 VCC21
- K22 VCC22
- VSS40 VCC23
- VSS42 VCC24
- V22 VCC25
- WE VCC26
- W21 VCC27
- Y6 VCC28
- Y22 VCC29
- AA5 VCC30
- AA7 VCC31
- AA9 VCC32
- AA11 VCC33
- AA13 VCC34
- AA15 VCC35
- AA19 VCC36
- AA21 VCC37
- AA23 VCC38
- AB6 VCC39
- AB8 VCC40
- AB10 VCC41
- AB12 VCC42
- AB14 VCC43
- AB16 VCC44
- AB18 VCC45
- AB20 VCC46
- AB22 VCC47
- AC9 VCC48
- AC11 VCC49
- AC13 VCC50
- AC15 VCC51
- VSS79 VCC52
- VSS80 VCC53
- AD10 VCC54
- AD12 VCC55
- VSS84 VCC56
- AD16 VCC57
- AD18 VCC58
- VSS87 VCC59
- AE11 VCC60
- AE13 VCC61
- VSS90 VCC62
- AE15 VCC63
- AE17 VCC64
- AE19 VCC65
- AF8 VCC66
- AF10 VCC67
- AF12 VCC68
- AF14 VCC69
- AF16 VCC70
- AF18 VCC71

Total caps = 2633 uF  
ESR = 15m ohm/5 // 5m ohm/25 // 5m ohm/15

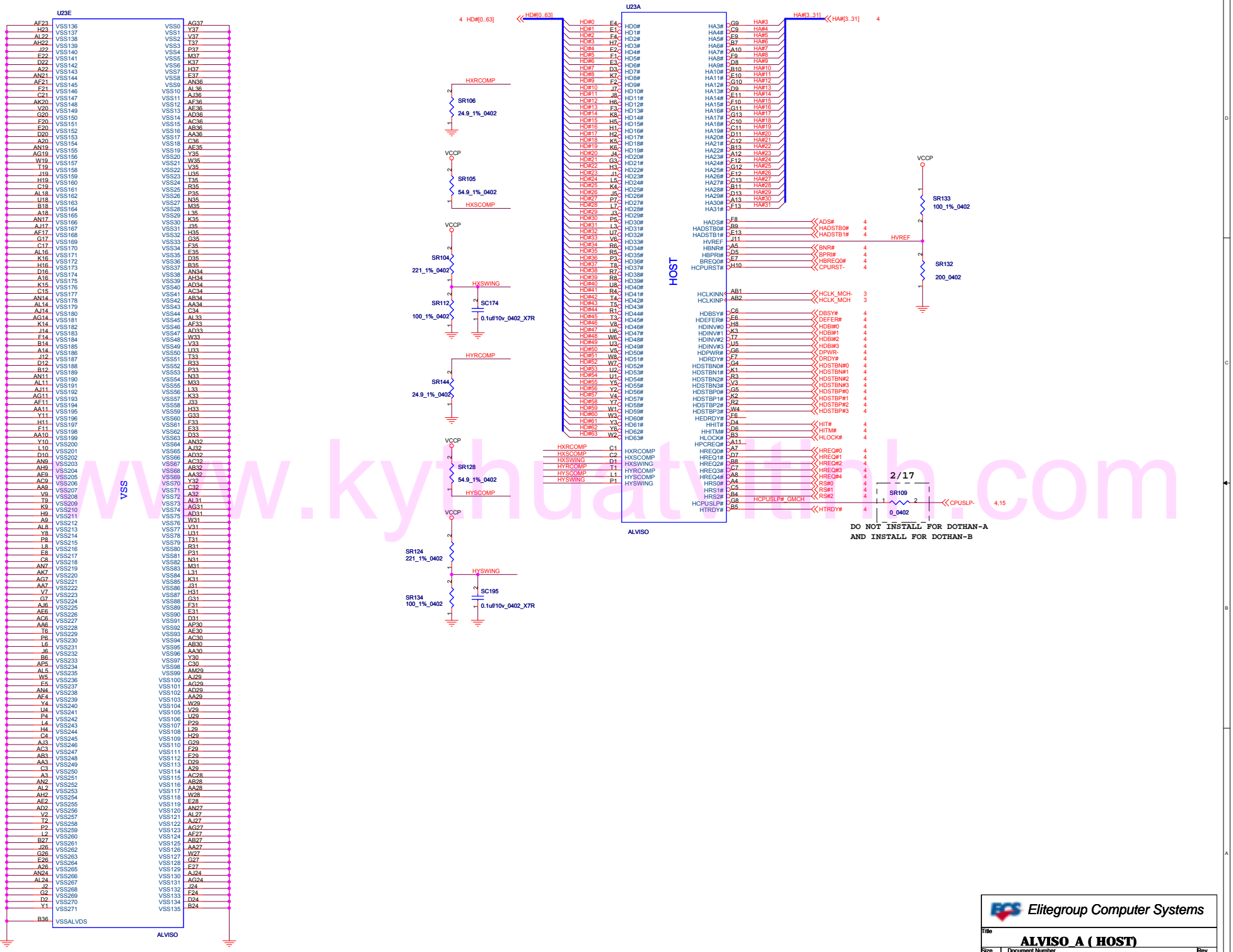
**Dothan**  
3 OF 3

POWER, GROUND AND NC

**VID**



0628



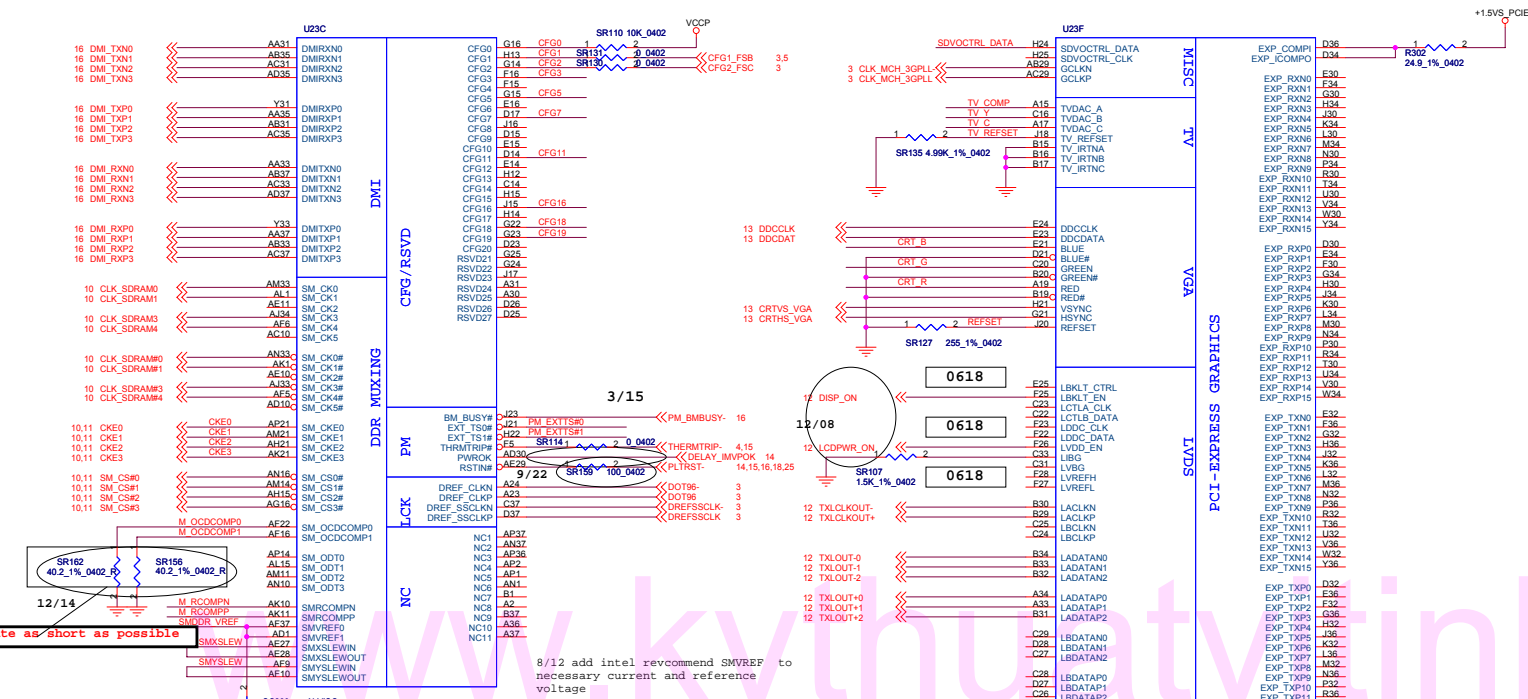
www.kytechuae.com

**ALVISO A (HOST)**

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Route as short as possible

12/14

VCC\_DIMM

VCC2.5V

VCC\_DIMM

2/17

VCC2.5V

VCC2.5V

VCC2.5V

VCC2.5V

VCC2.5V

VCC2.5V

VCC2.5V

VCC2.5V

VCC2.5V

VCC2.5V

VCC2.5V

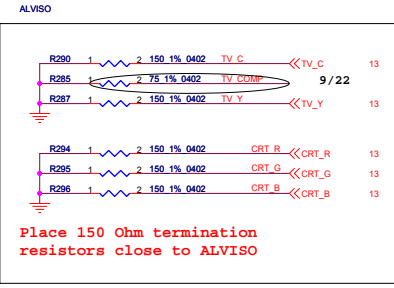
VCC2.5V

001= FOR FSB 533 101= FOR FSB 400	CFG[2:0]	0=Dynamic ODT Disable 1=Dynamic ODT Enable (default)	CFG16
0=DMIx2 1=DMIx4 (default)	CFG5	0= CPU 533 (default) 1= CPU 400	CHECK CFG11
0=DDR2 1=DDR (default)	CFG6	0= 1.05V 1= 1.5V (default) Alviso core voltage	CFG18
0=Mobile Prescott 1=Dothan (default)	CFG7	0= 1.05V (default) 1= 1.2V FSB I/O voltage	CFG19
0=Lane Reversal Enable 1=Normal Operation (default)	CFG9	0= No SDVO device (default) 1= SDVO device present	
01=XOR MODE 10=All ZMODE 11=Normal Operation (Default)	CFG[13:12]		

CFG[17:3] have internal pullup resistors  
CFG[19:18] have internal pulldown resistors

8/12 add intel recommend SMVREF to necessary current and reference voltage

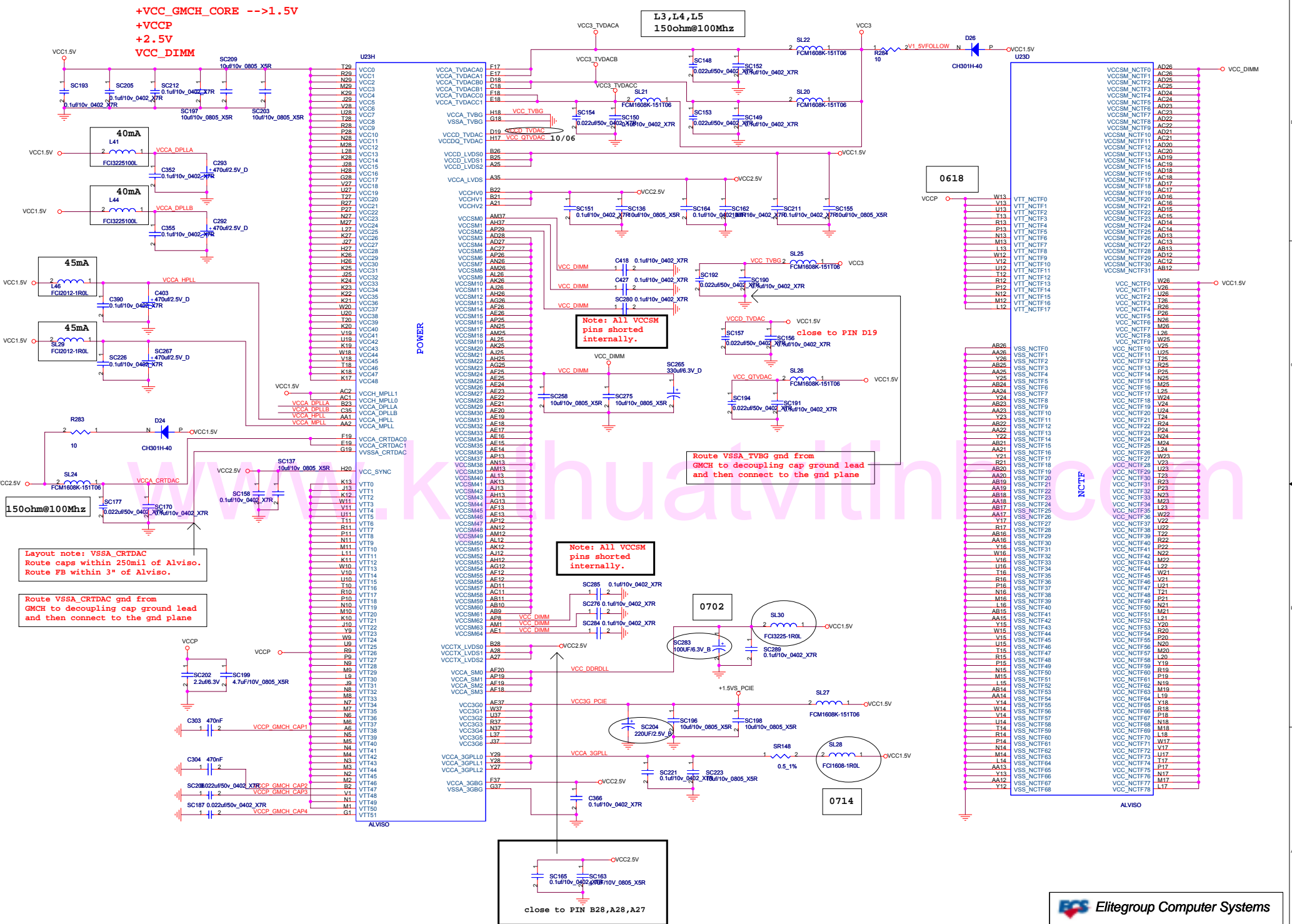
FOR DDR533  
CHECK



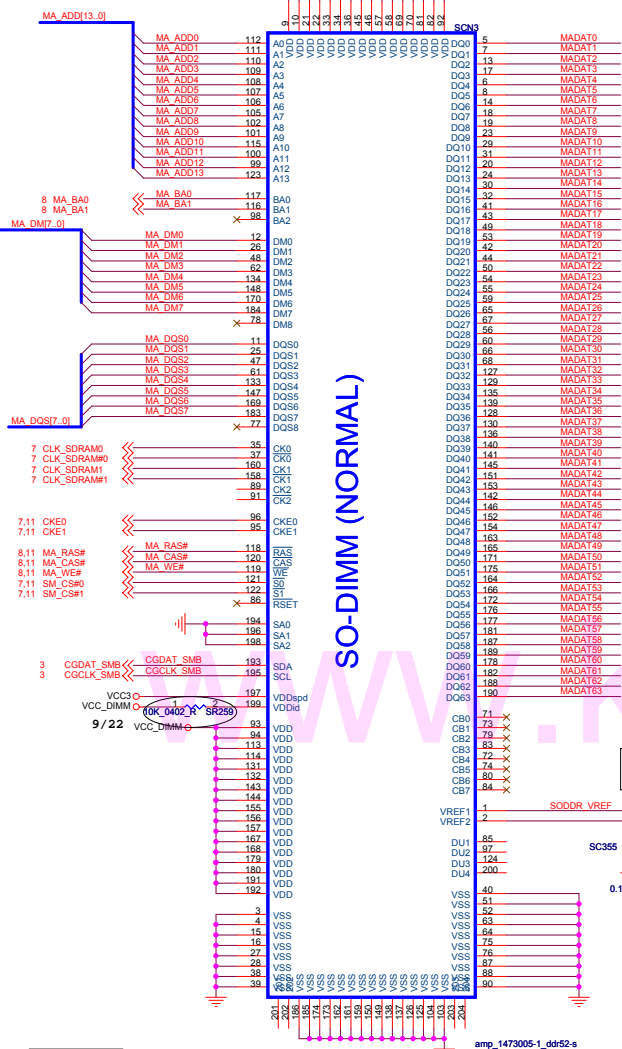
Place 150 Ohm termination resistors close to ALVISO





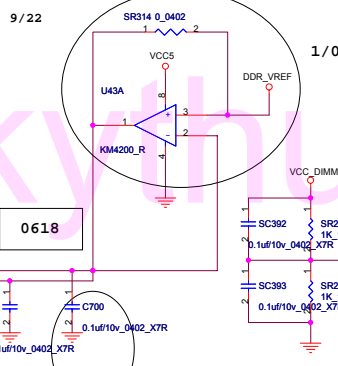


8.11 MA\_ADD[13..0] << MA\_ADD[13..0]  
 8.11 MADAT[63..0] << MADAT[63..0]  
 8.11 MA\_DM[7..0] << MA\_DM[7..0]  
 8.11 MA\_DQS[7..0] << MA\_DQS[7..0]

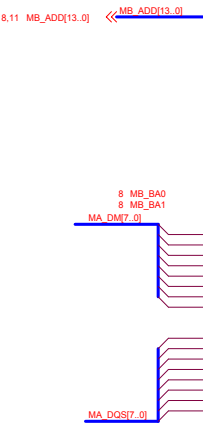


SO-DIMM (NORMAL)

8/12 add intel recommend SMVREF to necessary current and reference voltage

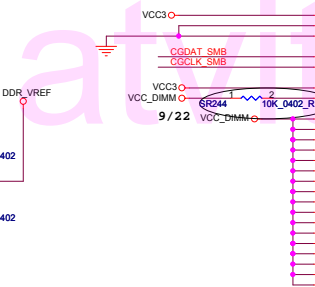


8/12 change location from SC357

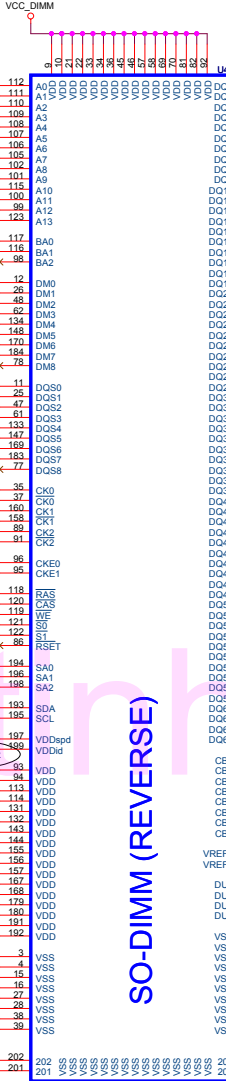


SO-DIMM (NORMAL)

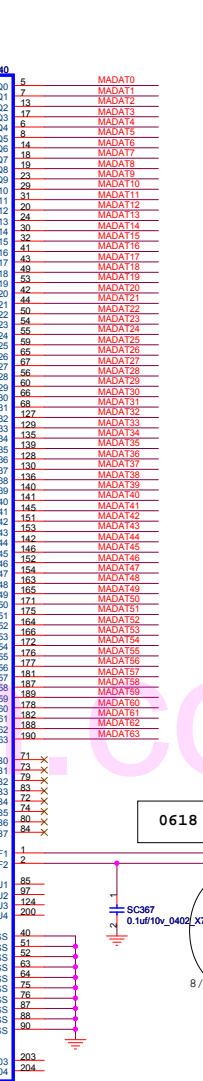
8/12 add intel recommend SMVREF to necessary current and reference voltage



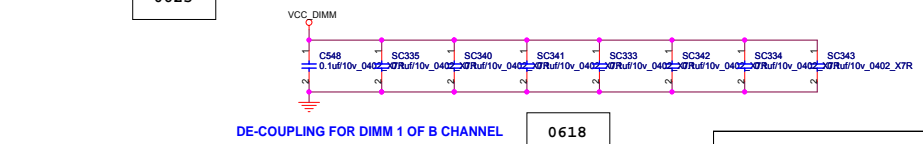
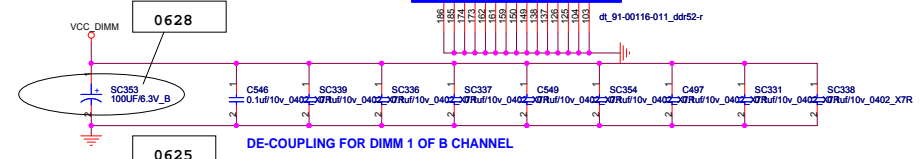
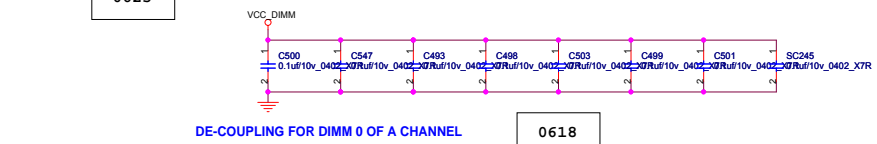
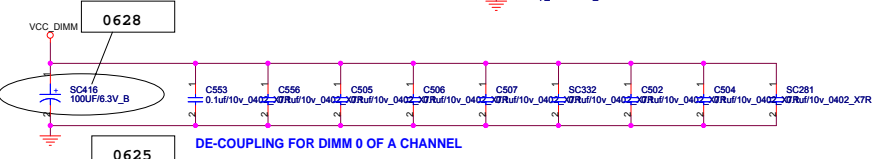
8/12 change location from SC365

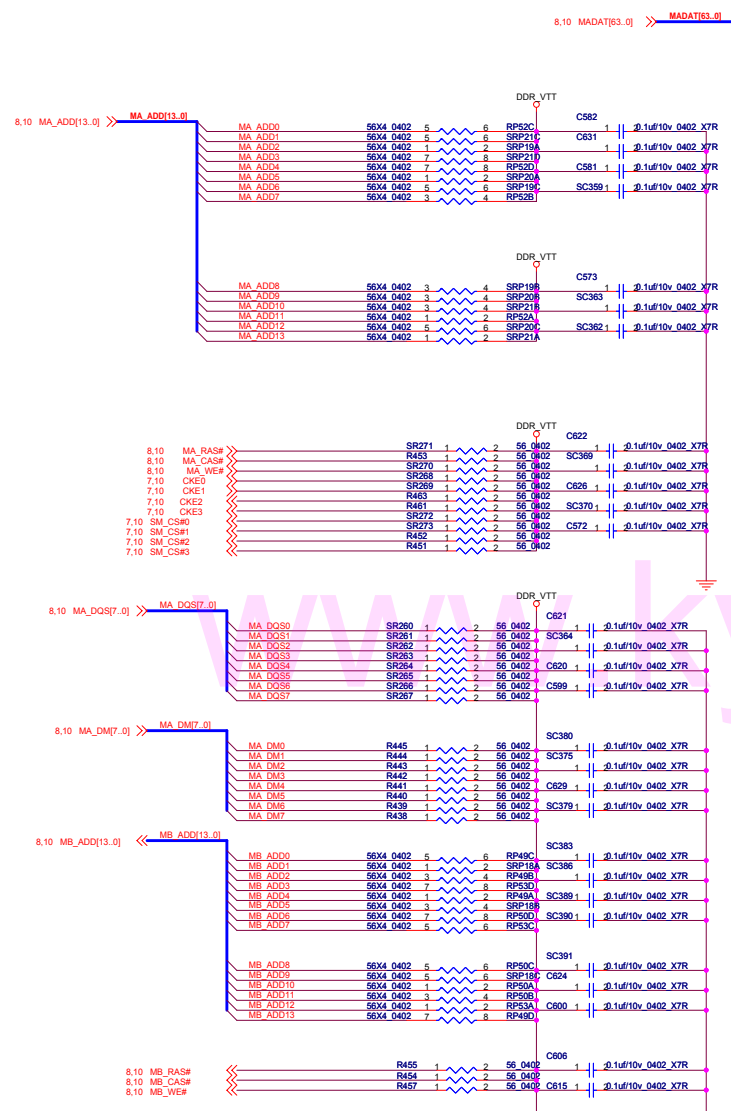


SO-DIMM (REVERSE)

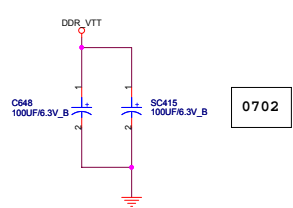


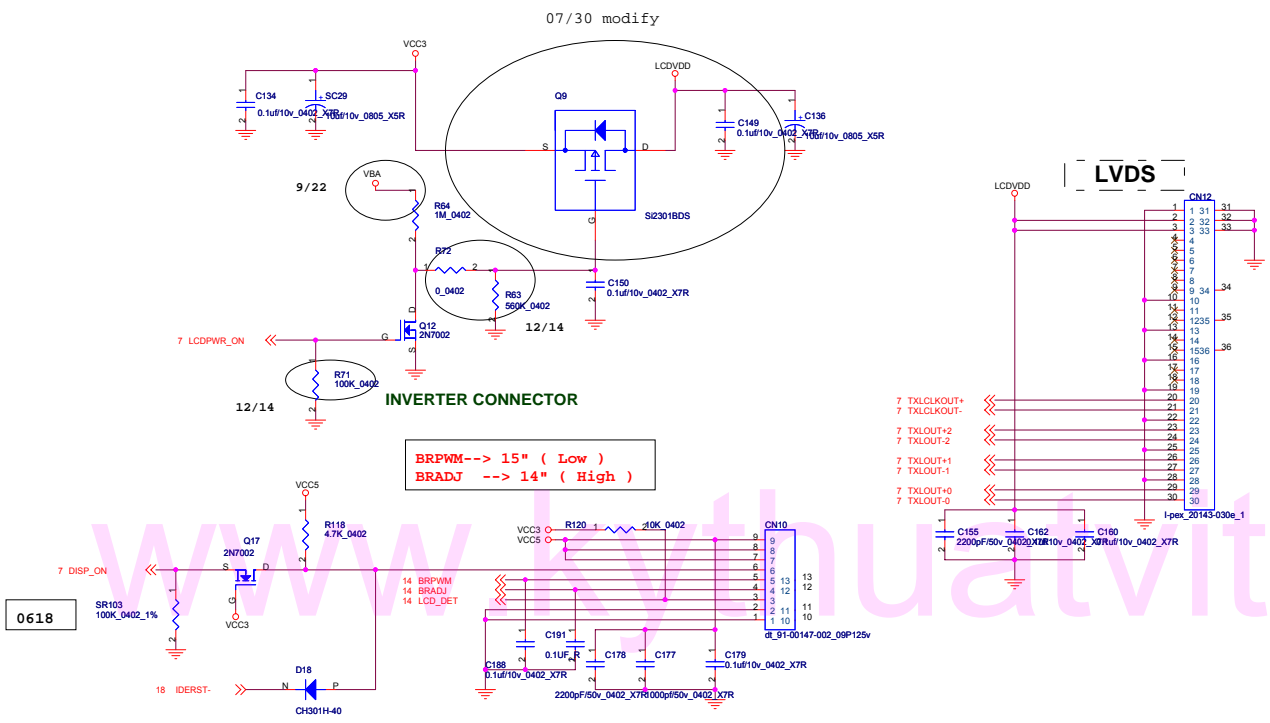
SO-DIMM (REVERSE)





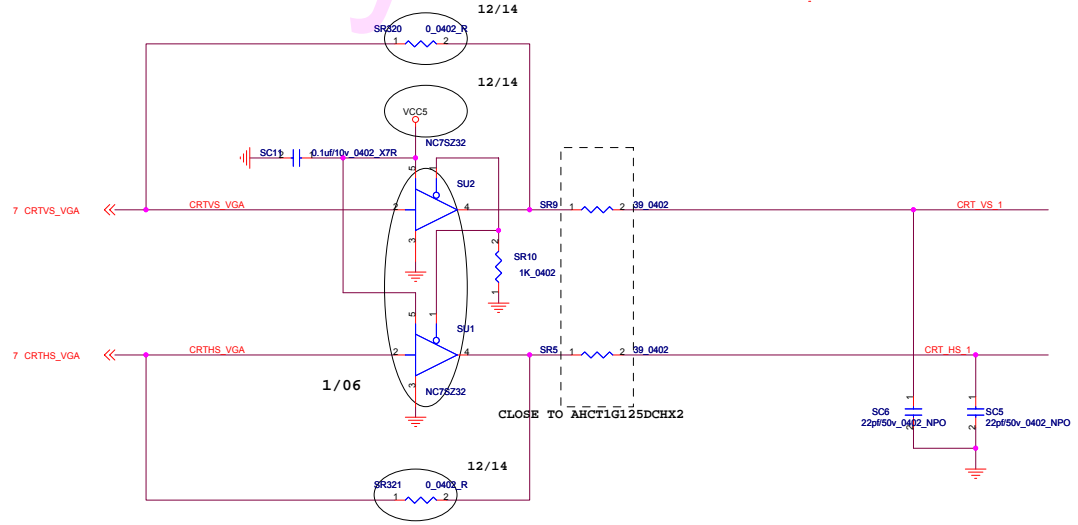
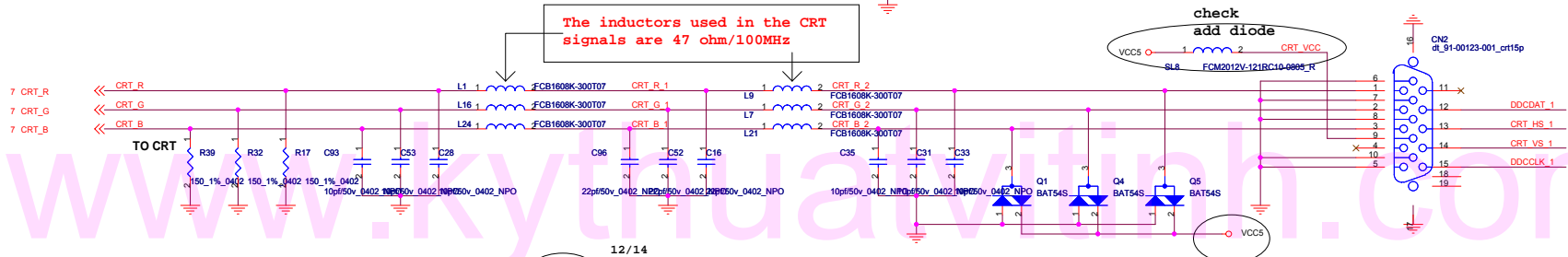
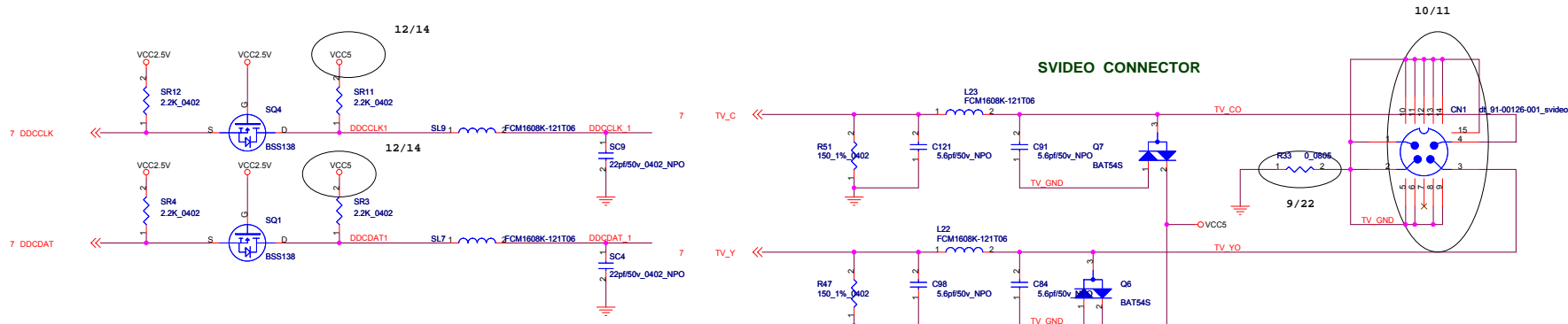
Signal	Bank	Pin	Resistor	Value	Capacitor
MADA0	56X4_0402	7	SRP15D	8	SC361
MADA1	56X4_0402	5	SRP15C	6	C607
MADA2	56X4_0402	3	SRP15B	4	
MADA3	56X4_0402	1	SRP15A	2	
MADA4	56X4_0402	1	RP59A	2	SC372
MADA5	56X4_0402	3	RP59B	4	
MADA6	56X4_0402	5	RP59C	6	SC381
MADA7	56X4_0402	7	SRP50	8	C594
MADA8	56X4_0402	7	SRP50D	8	
MADA9	56X4_0402	5	SRP50C	6	C579
MADA10	56X4_0402	3	SRP50B	4	
MADA11	56X4_0402	1	SRP50A	2	
MADA12	56X4_0402	1	RP55A	2	SC385
MADA13	56X4_0402	3	RP55B	4	
MADA14	56X4_0402	5	RP55C	6	SC384
MADA15	56X4_0402	7	RP55D	8	SC382
MADA16	56X4_0402	7	SRP50D	8	
MADA17	56X4_0402	5	SRP50C	6	SC381
MADA18	56X4_0402	3	SRP50B	4	
MADA19	56X4_0402	1	SRP50A	2	
MADA20	56X4_0402	1	RP60A	2	SC376
MADA21	56X4_0402	3	RP60B	4	
MADA22	56X4_0402	5	RP60C	6	C619
MADA23	56X4_0402	7	RP60D	8	C574
MADA24	56X4_0402	7	SRP17D	8	
MADA25	56X4_0402	5	SRP17C	6	SC373
MADA26	56X4_0402	3	SRP17B	4	
MADA27	56X4_0402	1	SRP17A	2	
MADA28	56X4_0402	1	RP54A	2	SC388
MADA29	56X4_0402	3	RP54B	4	
MADA30	56X4_0402	5	RP54C	6	C634
MADA31	56X4_0402	7	RP54D	8	SC374
MADA32	56X4_0402	7	SRP22D	8	
MADA33	56X4_0402	5	SRP22C	6	SC378
MADA34	56X4_0402	3	SRP22B	4	
MADA35	56X4_0402	1	SRP22A	2	
MADA36	56X4_0402	1	RP48A	2	SC371
MADA37	56X4_0402	3	RP48B	4	
MADA38	56X4_0402	5	RP48C	6	SC366
MADA39	56X4_0402	7	RP48D	8	C633
MADA40	56X4_0402	7	SRP23D	8	
MADA41	56X4_0402	5	SRP23C	6	SC360
MADA42	56X4_0402	3	SRP23B	4	
MADA43	56X4_0402	1	SRP23A	2	
MADA44	56X4_0402	1	RP47A	2	C618
MADA45	56X4_0402	3	RP47B	4	
MADA46	56X4_0402	5	RP47C	6	C605
MADA47	56X4_0402	7	RP47D	8	C628
MADA48	56X4_0402	7	SRP24D	8	
MADA49	56X4_0402	5	SRP24C	6	SC377
MADA50	56X4_0402	3	SRP24B	4	
MADA51	56X4_0402	1	SRP24A	2	
MADA52	56X4_0402	1	RP45A	2	C580
MADA53	56X4_0402	3	RP45B	4	
MADA54	56X4_0402	5	RP45C	6	C596
MADA55	56X4_0402	7	RP45D	8	C601
MADA56	56X4_0402	7	SRP25D	8	
MADA57	56X4_0402	5	SRP25C	6	C617
MADA58	56X4_0402	3	SRP25B	4	
MADA59	56X4_0402	1	SRP25A	2	
MADA60	56X4_0402	1	RP46A	2	C595
MADA61	56X4_0402	3	RP46B	4	
MADA62	56X4_0402	5	RP46C	6	C612
MADA63	56X4_0402	7	RP46D	8	





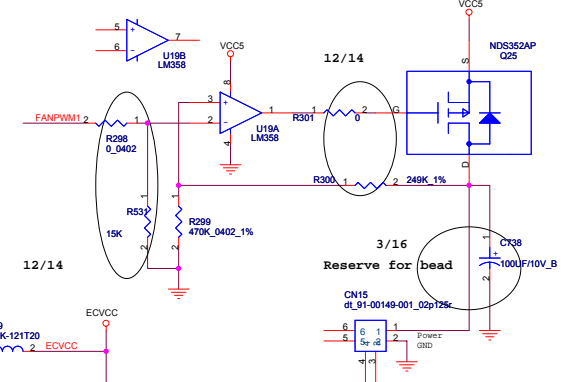
BRPWM--> 15" ( Low )  
BRADJ --> 14" ( High )

0618

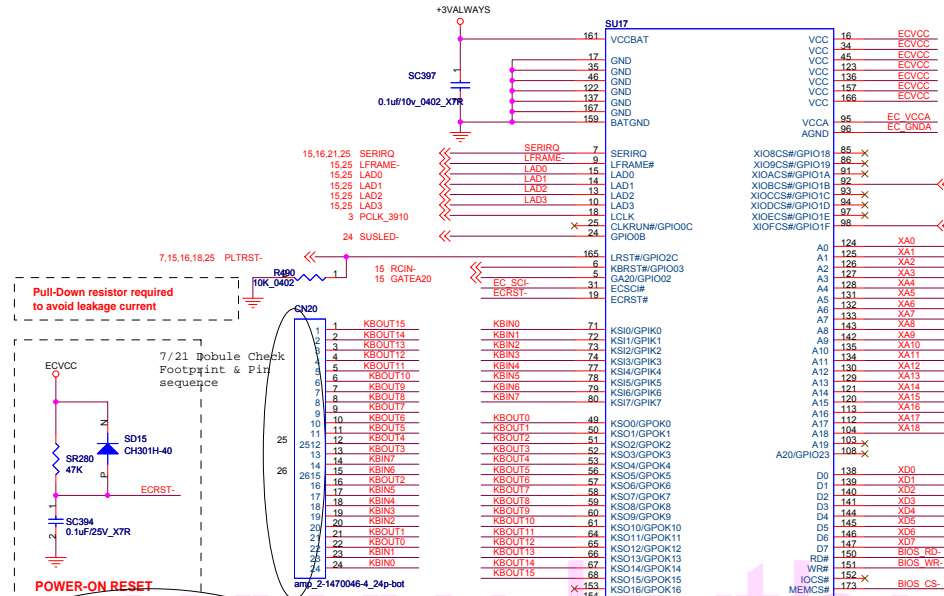
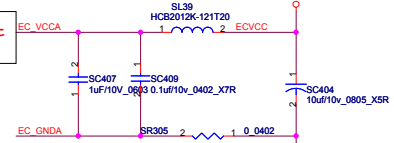


SR285	4.7K_0402	SERIRQ
SR284	4.7K_0402	LFRAME-
SR277	4.7K_0402	LAD0
SR278	4.7K_0402	LAD1
SR282	4.7K_0402	LAD2
SR283	4.7K_0402	LAD3

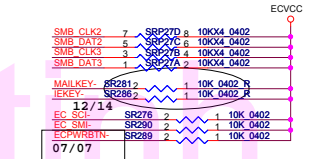
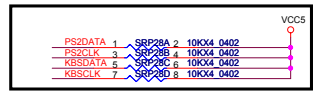
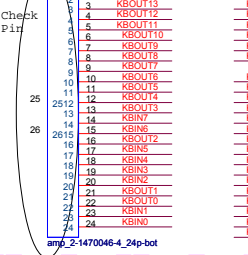
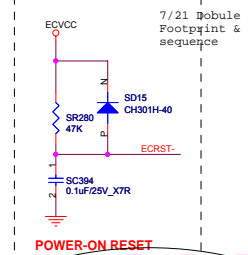
XA0	19	A0	13	XD0
XA1	11	A1	01	XD1
XA2	10	A2	02	XD2
XA3	9	A3	04	XD3
XA4	8	A4	03	XD4
XA5	7	A5	05	XD5
XA6	6	A6	06	XD6
XA7	5	A7	07	XD7
XA8	27	A8		
XA9	26	A9		
XAT0	23	A10		
XAT1	25	A11		
XAT2	4	A12		
XAT3	28	A13		
XAT4	29	A14		
XAT5	29	A15		
XAT6	30	A16		
XAT7	30	A17		
XAT8	30	A18		
BIOS_CS-	2	CE		
BIOS_RD-	24	OE		
BIOS_WR-	31	WE		



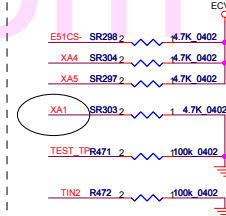
check--> LID SW output to turn-off backlight



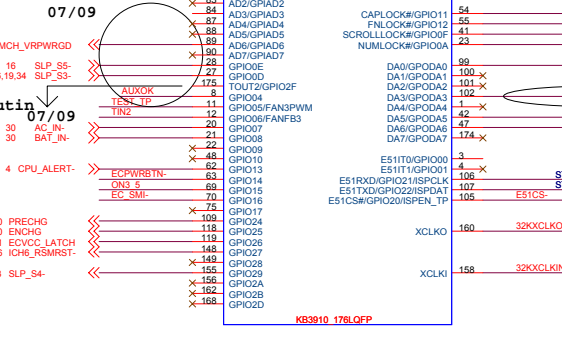
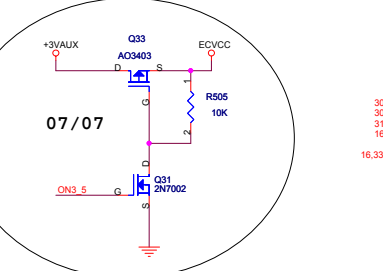
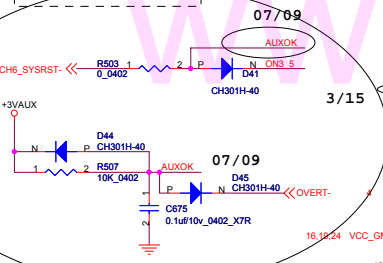
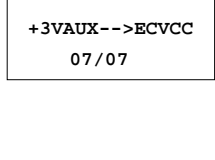
Pull-Down resistor required to avoid leakage current



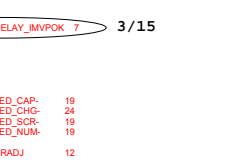
HW STRAP OPTION



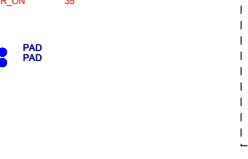
+3VAUX-->ECVCC



DELAY\_INVPOK 7



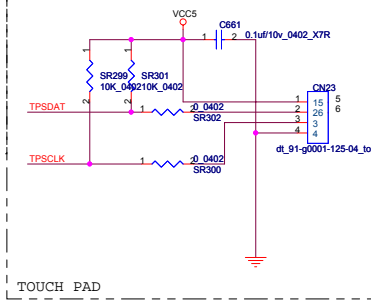
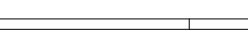
AND\_SBPWROK 16



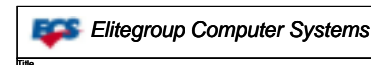
32KXCLKO 160



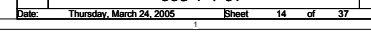
32KXCLKIN 168



TOUCH PAD

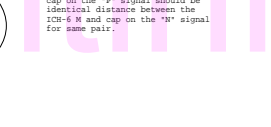
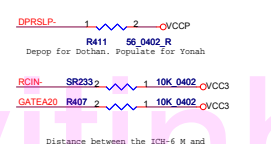
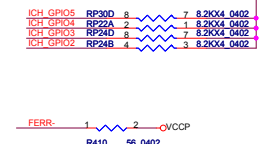
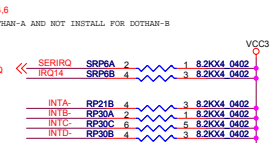
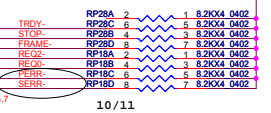
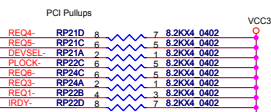
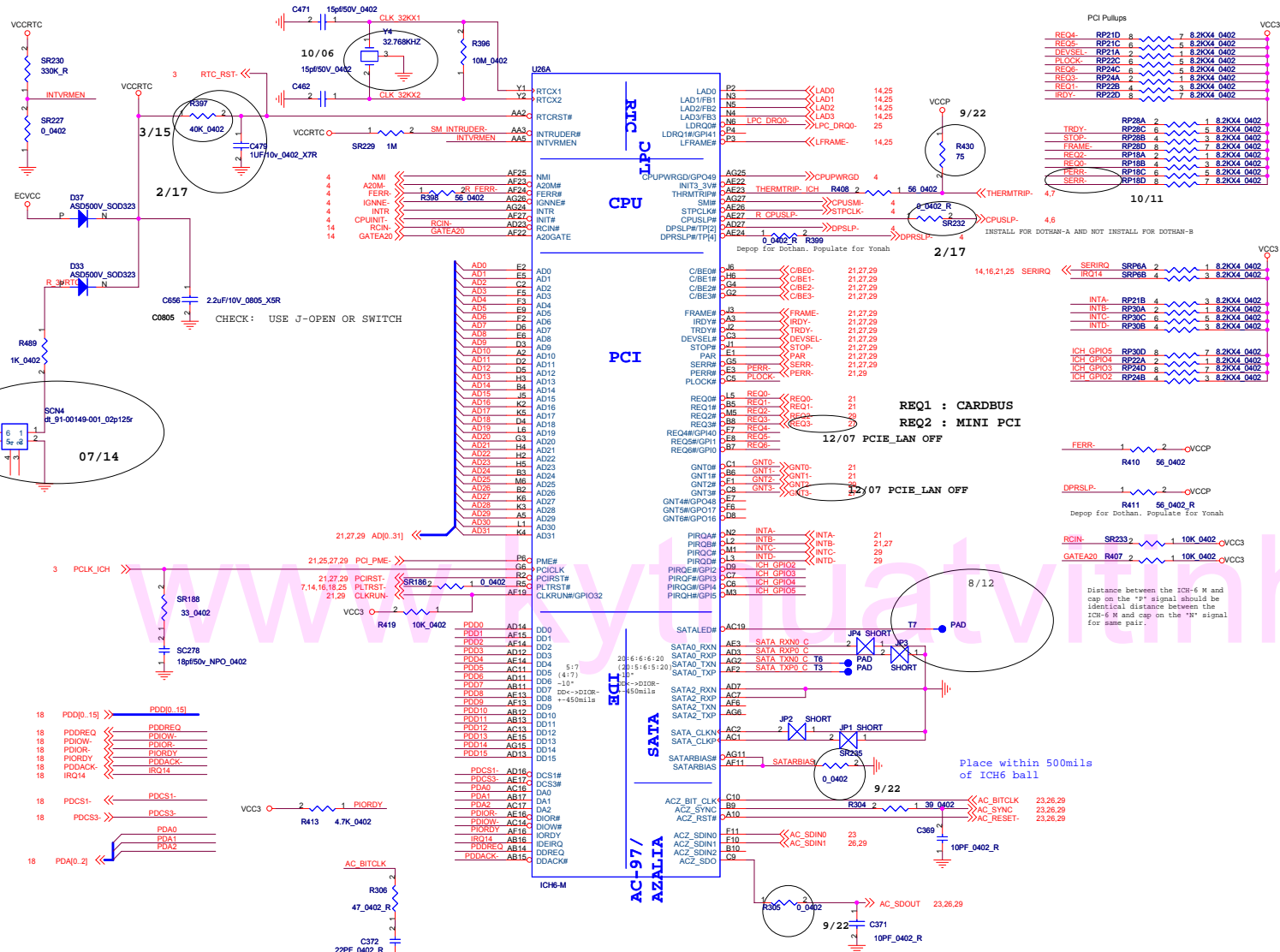


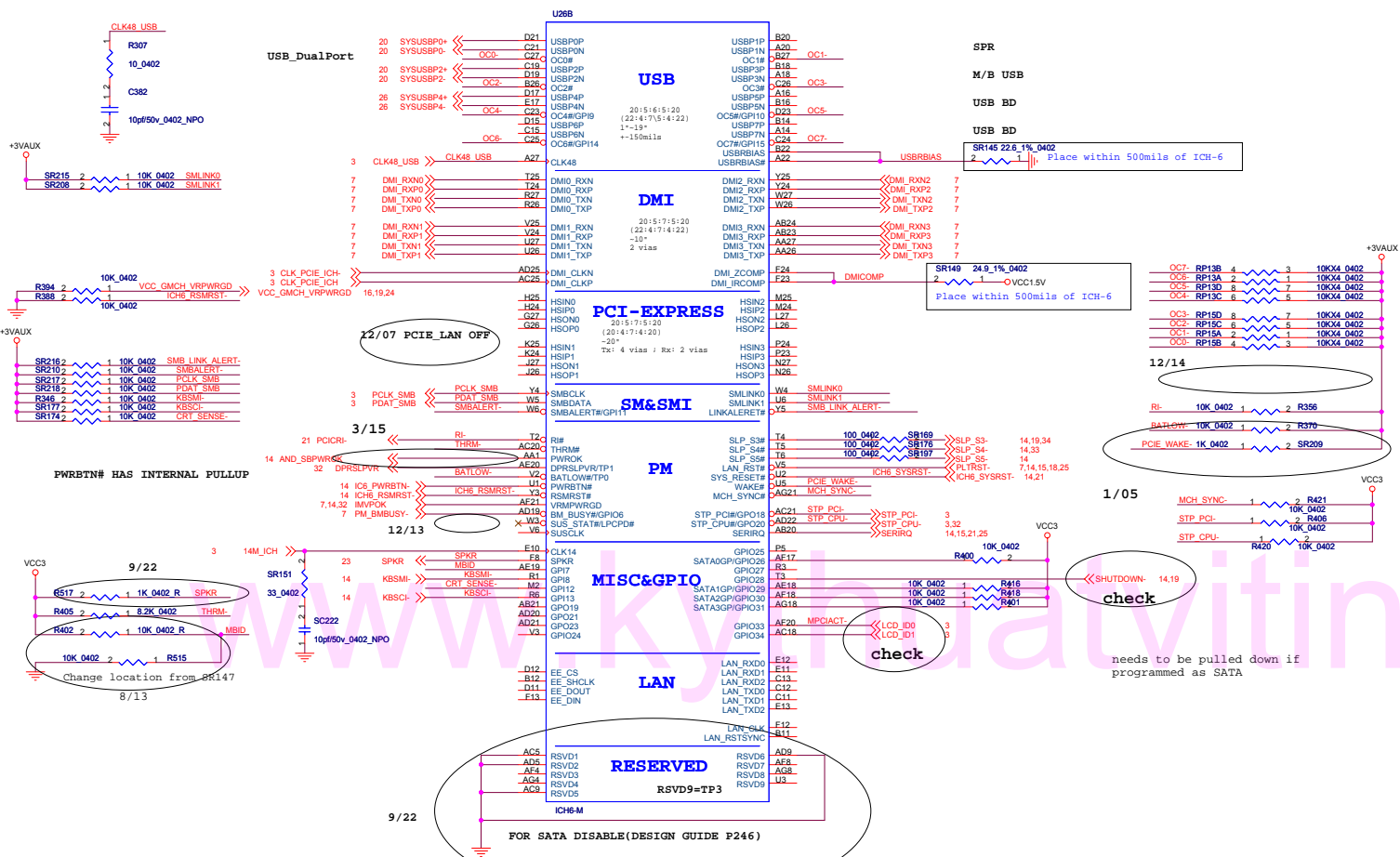
Close to chip



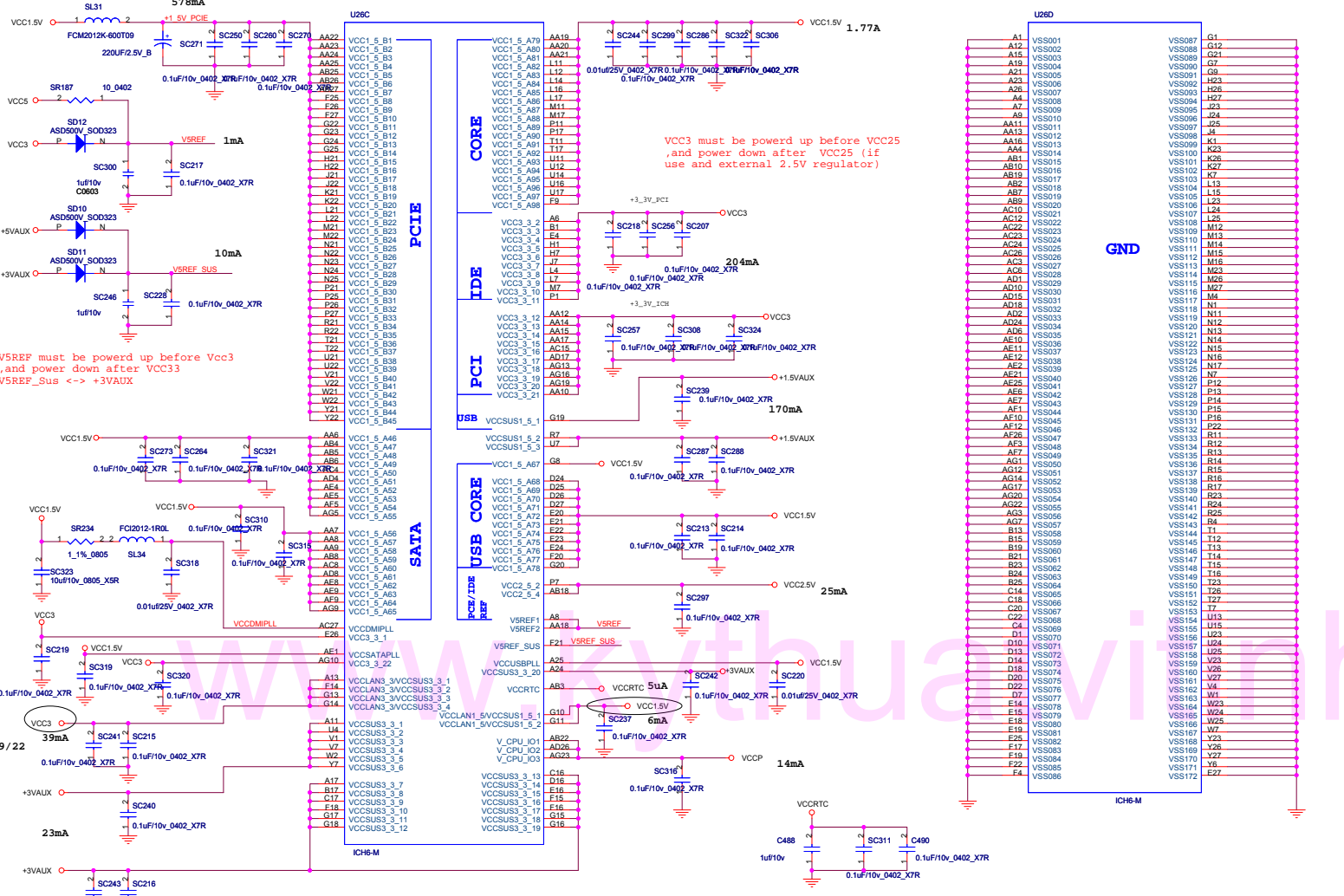
Elitegroup Computer Systems

Title: KBC3910  
 Size: C Document Number: 558-1-4-01  
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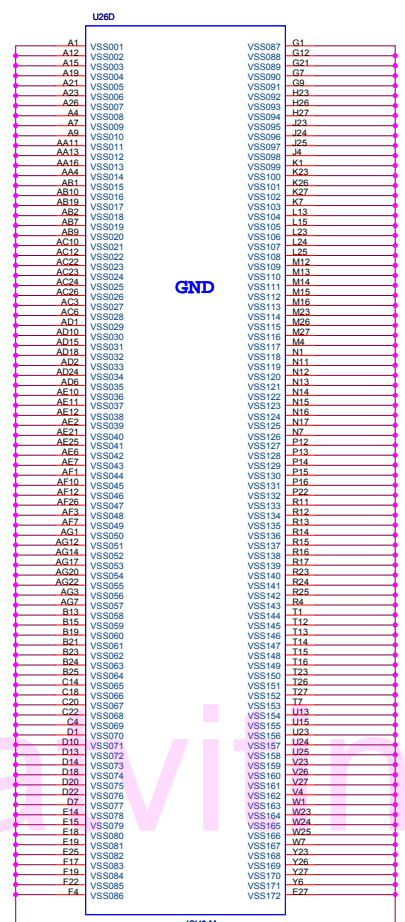


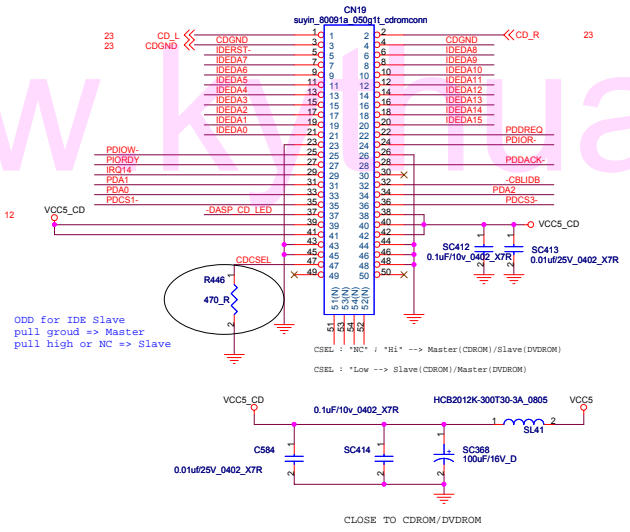
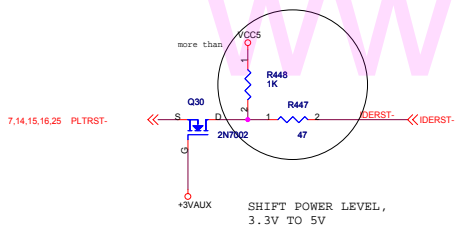
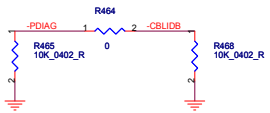
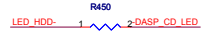
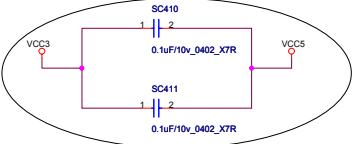
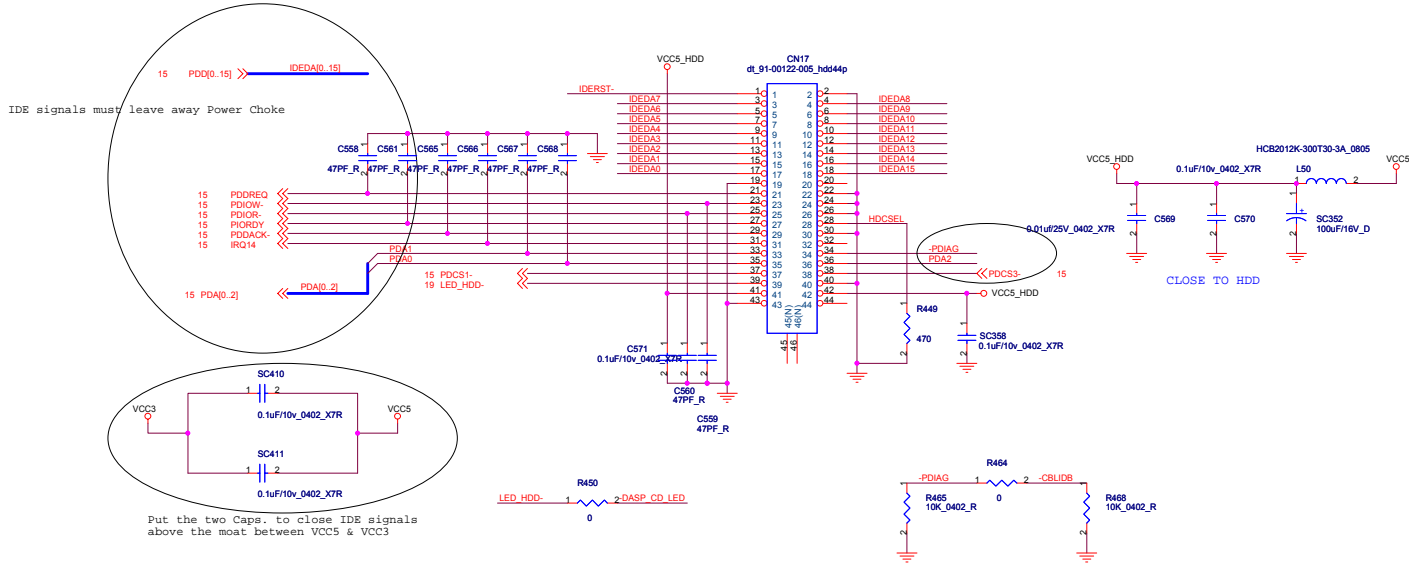
V5REF must be powered up before Vcc3 ,and power down after VCC33  
V5REF\_Sus <-> +3VAUX

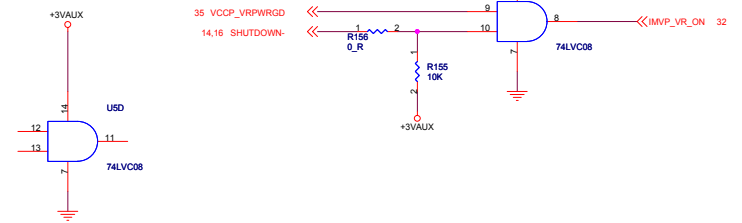
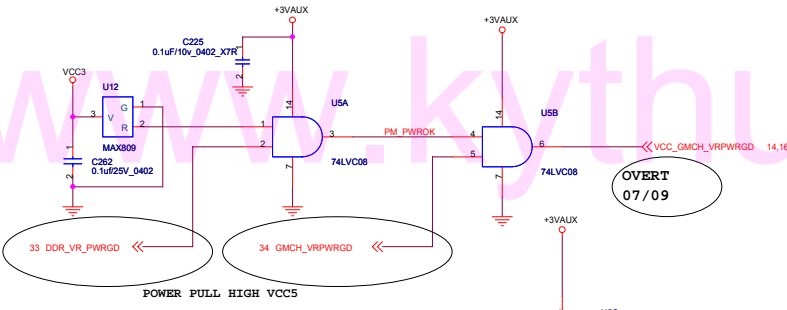
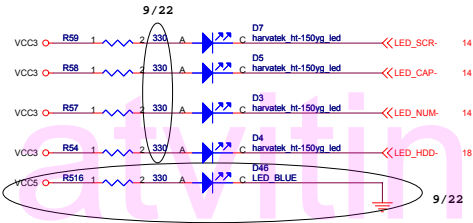
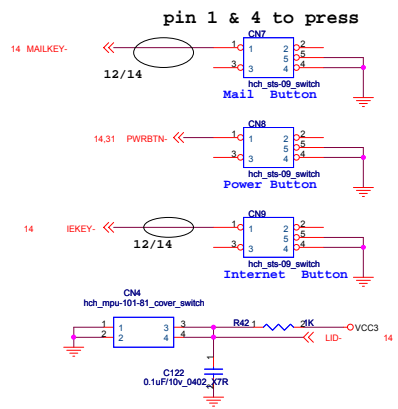
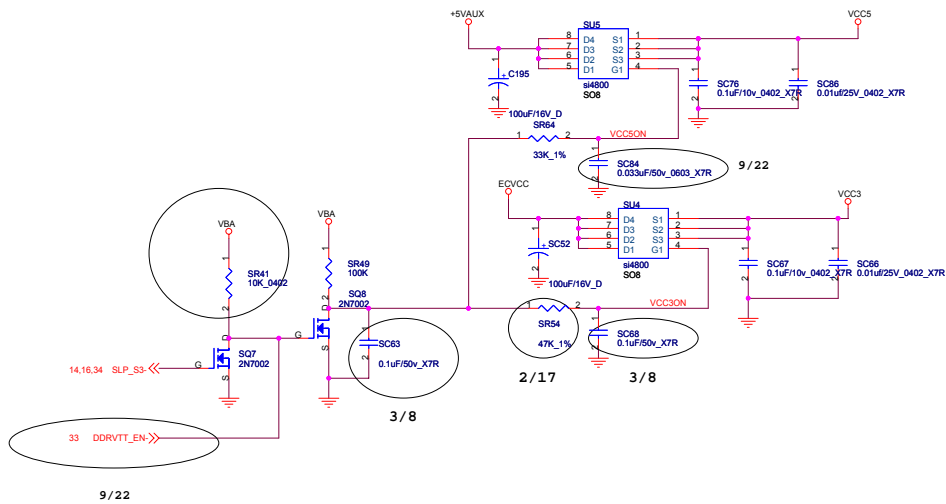
VCC3 must be powered up before VCC25 ,and power down after VCC25 (if use and external 2.5V regulator)

VCC15 must be powered up before VCCP ,and power down after VCCP

+3VAUX must be powered up before +1.5VAUX ,and power down after +1.5VAUX (if use and external 1.5V regulator)  
VccLAN3\_3 <-> VccLAN1\_5





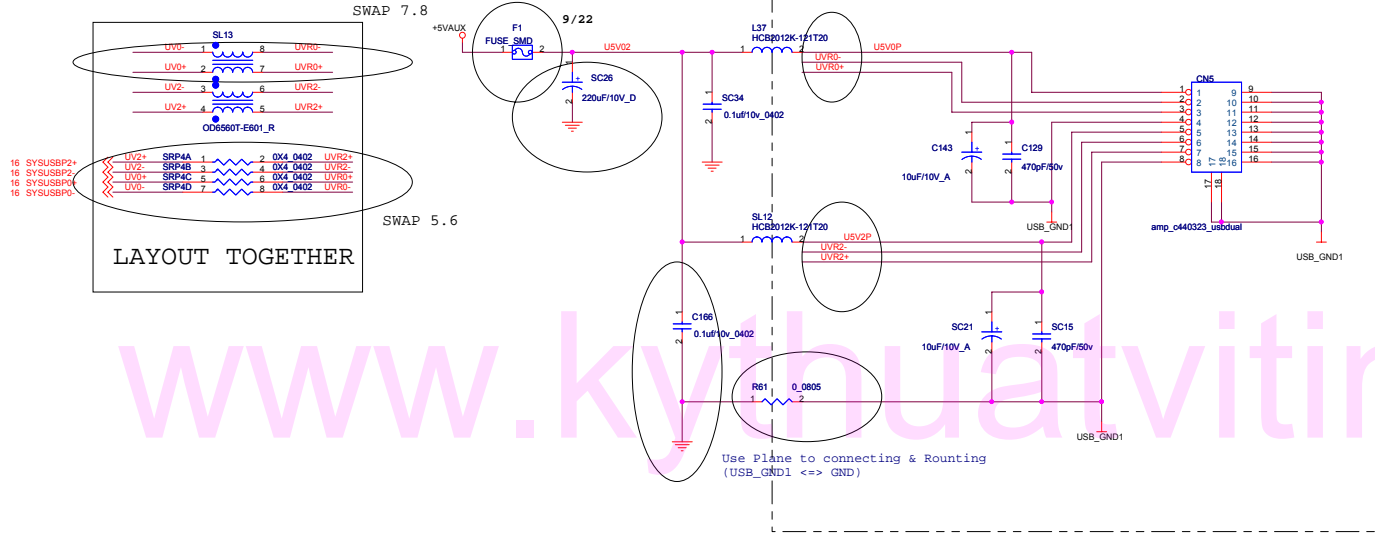


**ALL THESE CLOSE TO CONNECTOR**

8/26 change F1 P/N: from  
16-285-150370 to  
16-200-150010

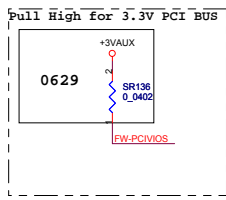
Two ports ,1.5A, at least 60 mils

The dotted line is a moat for layout placement reference.  
Pls Place the components of block into USB moat  
Bead & resistor are bridge



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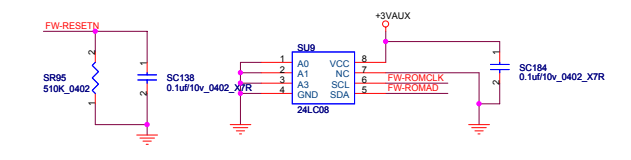
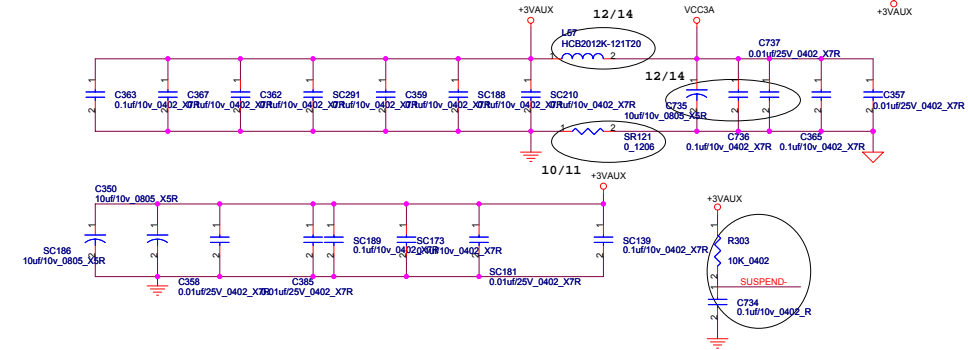
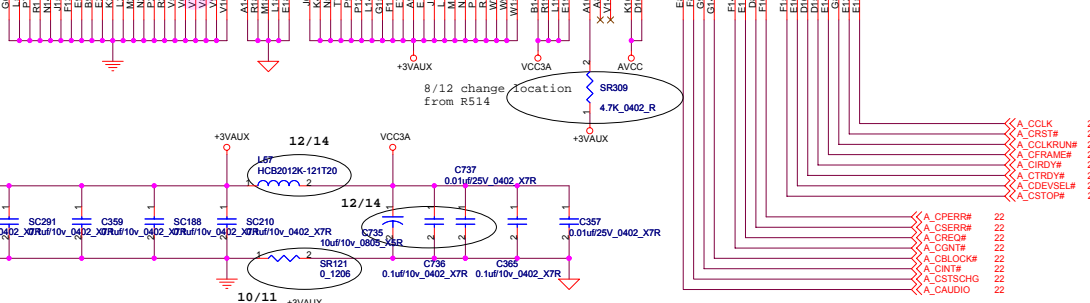
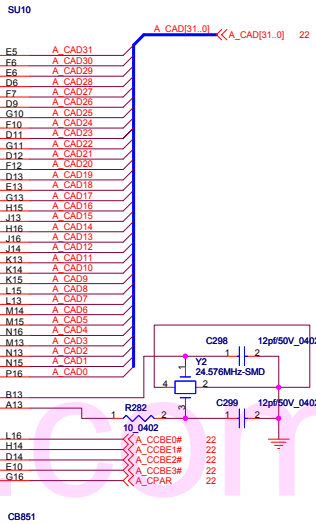
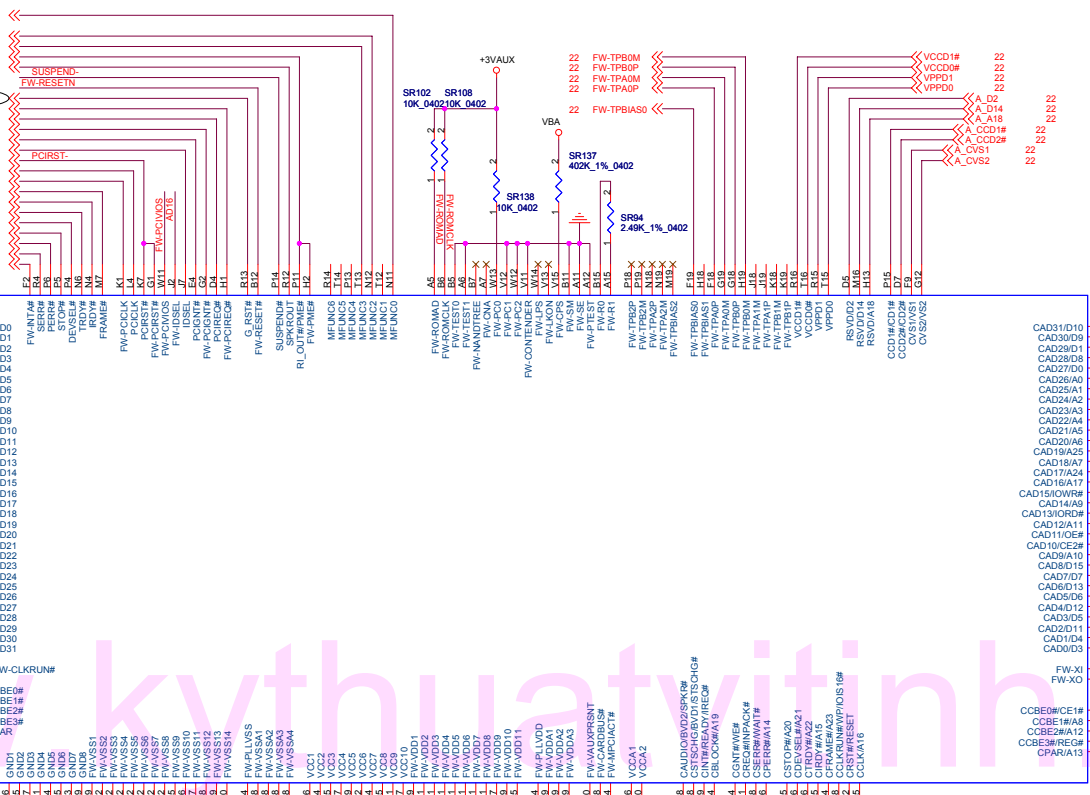
GRST# should connect to Power On reset if support S3

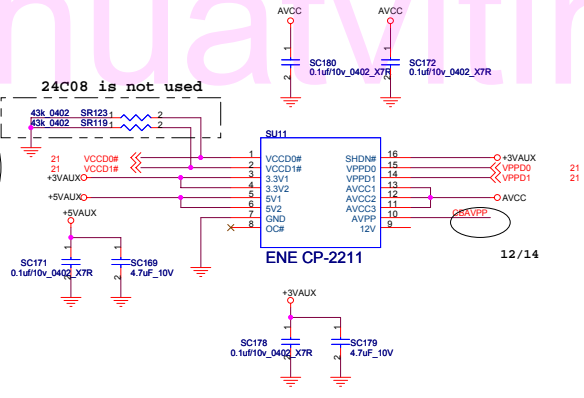
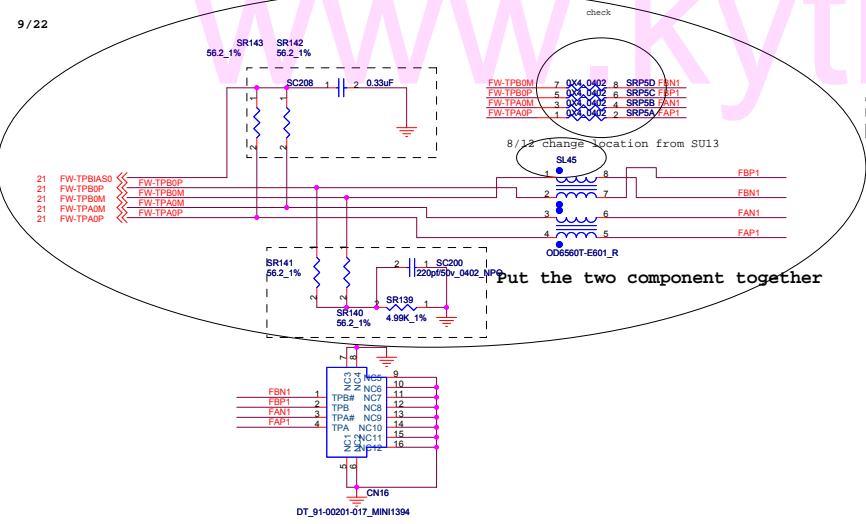
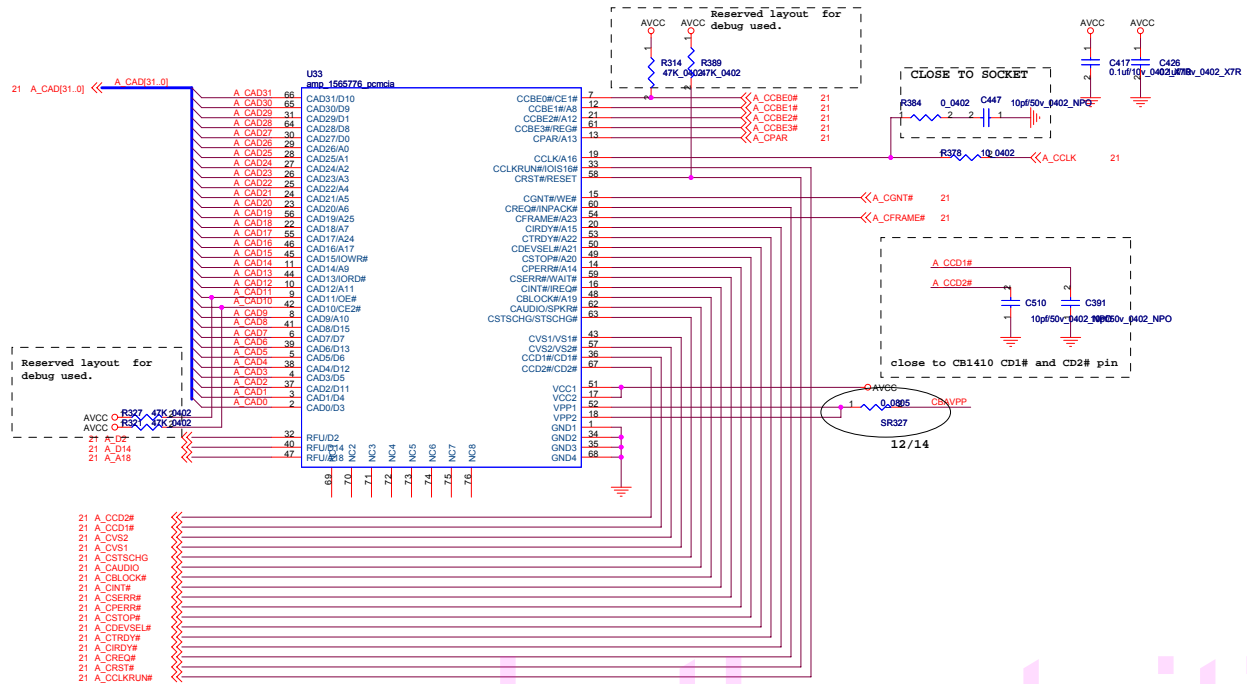


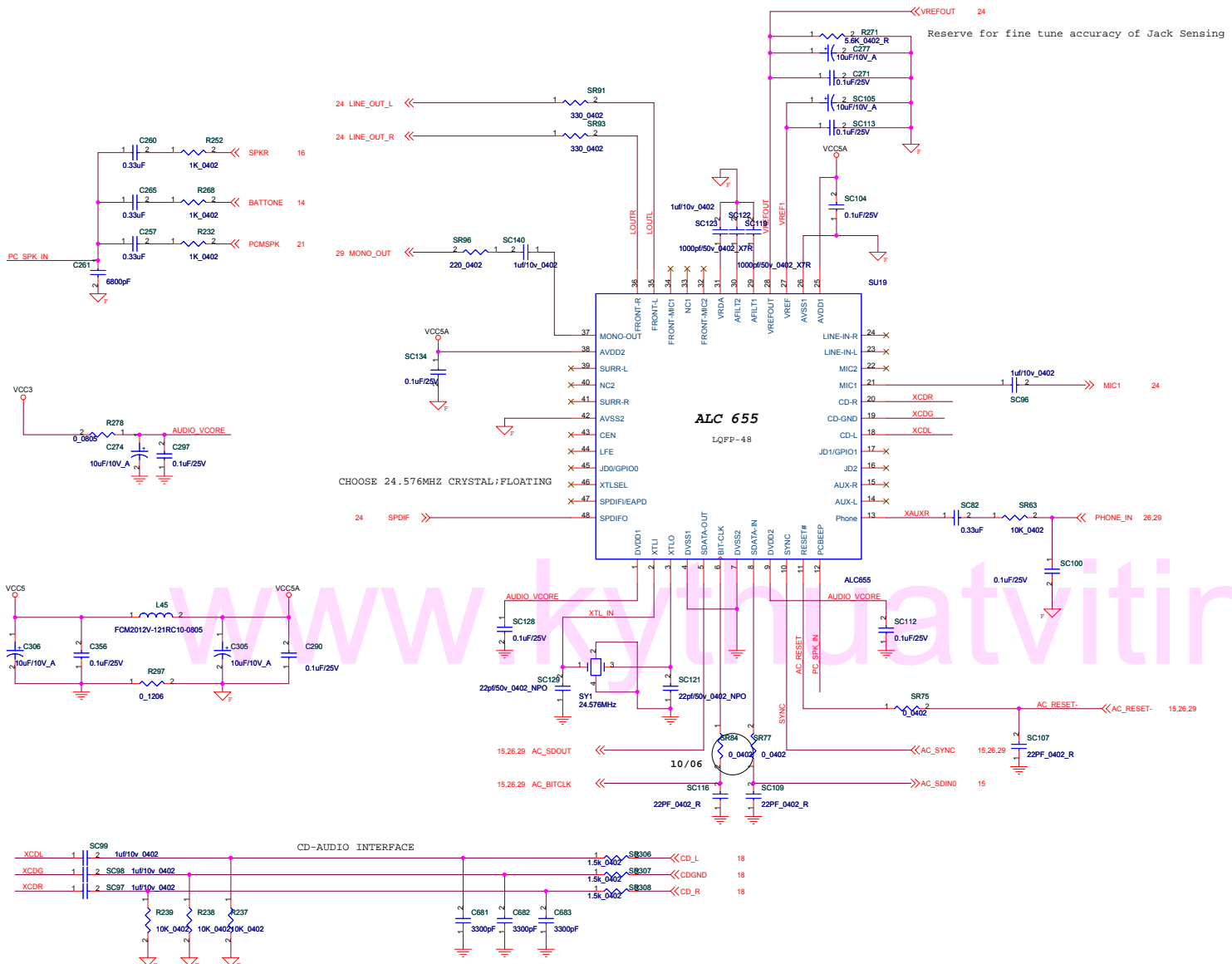
- 15.27 INTB
- 16 PCIOR#
- 14,15,16,26 SERRO
- 15,25,27,29 PCI\_PME
- 23 PCMSPK
- 14,16 ICH6\_SYSTRST
- 15 RED1#
- 15 GNT0#
- 15 GNT1#
- 15,27,29 AD18
- 15,27,29 PCIRST
- 3 PCLK\_CB851
- 3 PCLK\_1394
- 15,27,29 FRAME#
- 15,27,29 IRDY#
- 15,27,29 TRDY#
- 15,27,29 DEVSEL#
- 15,27,29 STOP#
- 15,29 PERR#
- 15,27,29 SERR#
- 15 INTA#

- 15,27,29 AD[31:0] << AD[31:0]
- AD0 T11
- AD1 N10
- AD2 P10
- AD3 T10
- AD4 R10
- AD5 T9
- AD6 R9
- AD7 N9
- AD8 R8
- AD9 N8
- AD10 P8
- AD11 N7
- AD12 R7
- AD13 N7
- AD14 R6
- AD15 N6
- AD16 M6
- AD17 T4
- AD18 T7
- AD19 L6
- AD20 K6
- AD21 K5
- AD22 J4
- AD23 J5
- AD24 H5
- AD25 H6
- AD26 H7
- AD27 G4
- AD28 G5
- AD29 G7
- AD30 F4
- AD31 F5

- 15,29 CLKRUN# << F1 FW-CLKRUN#
- 15,27,29 CBE0# << T8 CBE0#
- 15,27,29 CBE1# << M6 CBE1#
- 15,27,29 CBE2# << R4 CBE2#
- 15,27,29 CBE3# << R4 CBE3#
- 15,27,29 PAR << R4 PAR

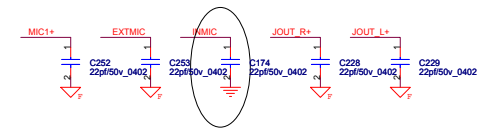
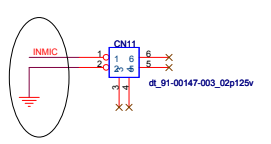
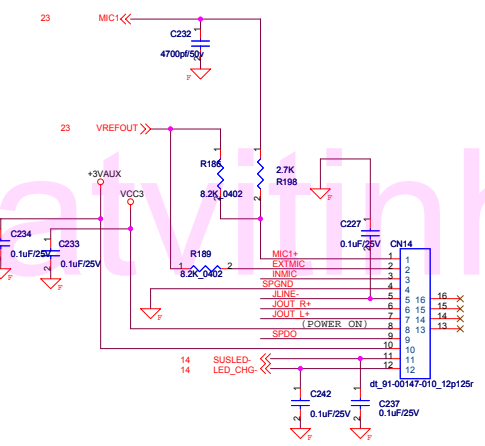
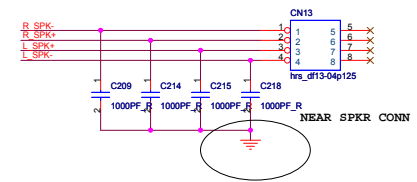
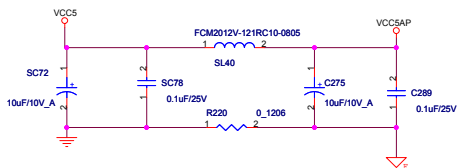
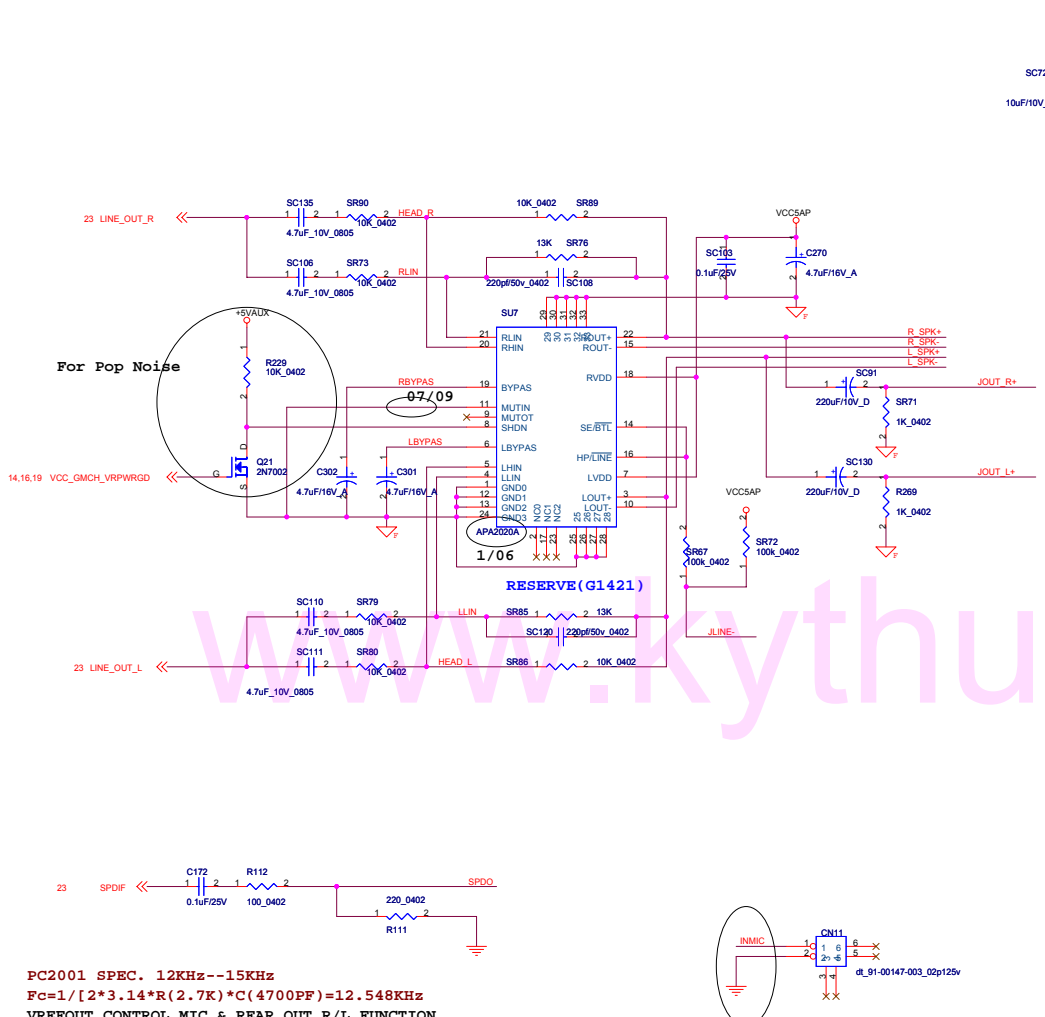




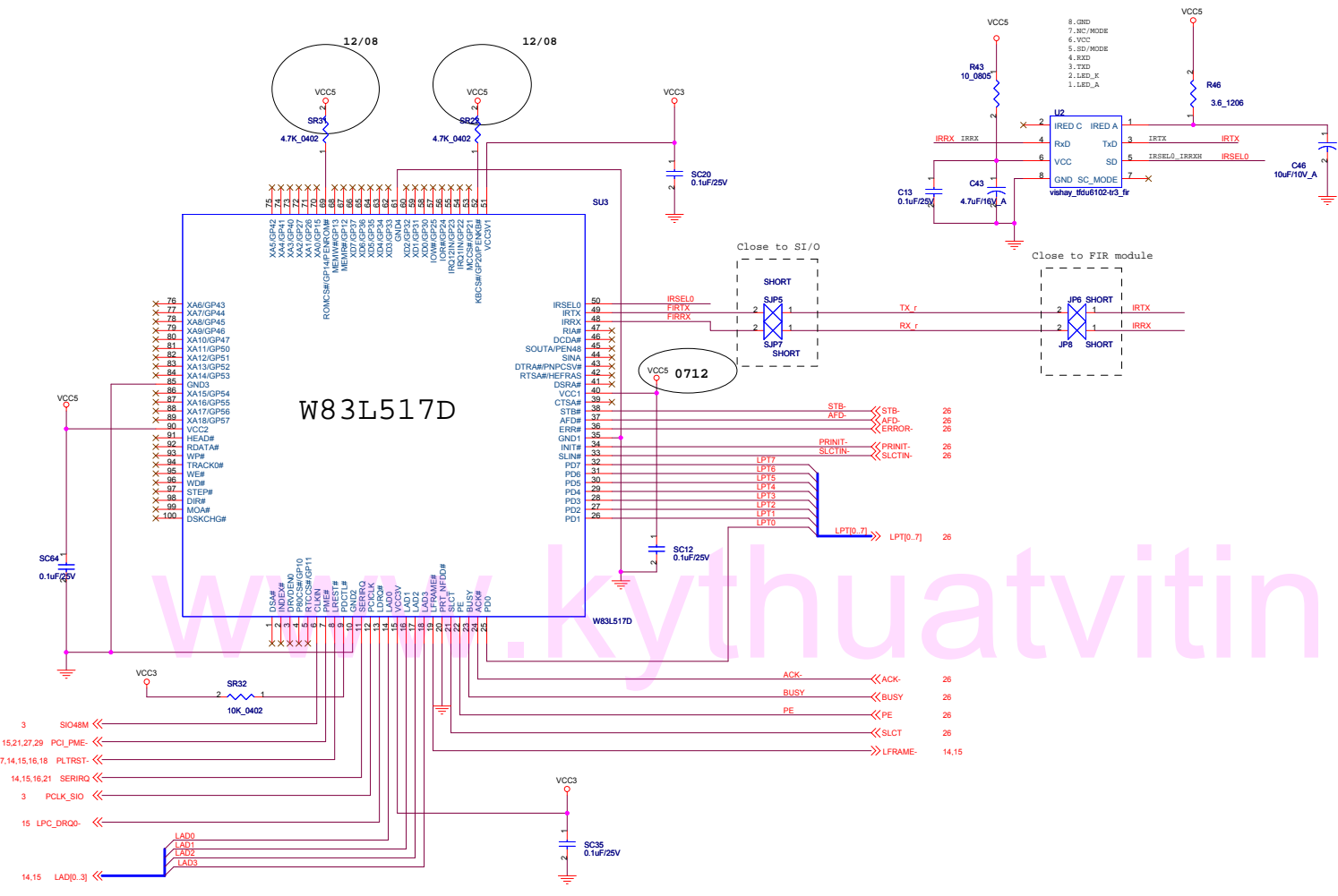


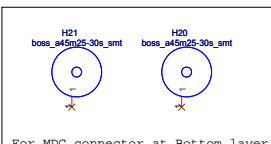
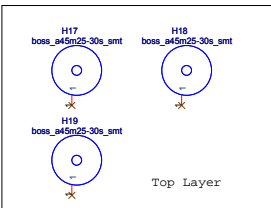
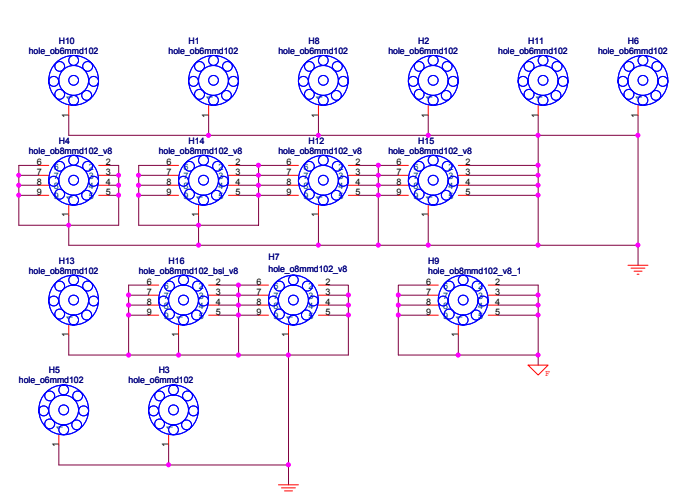
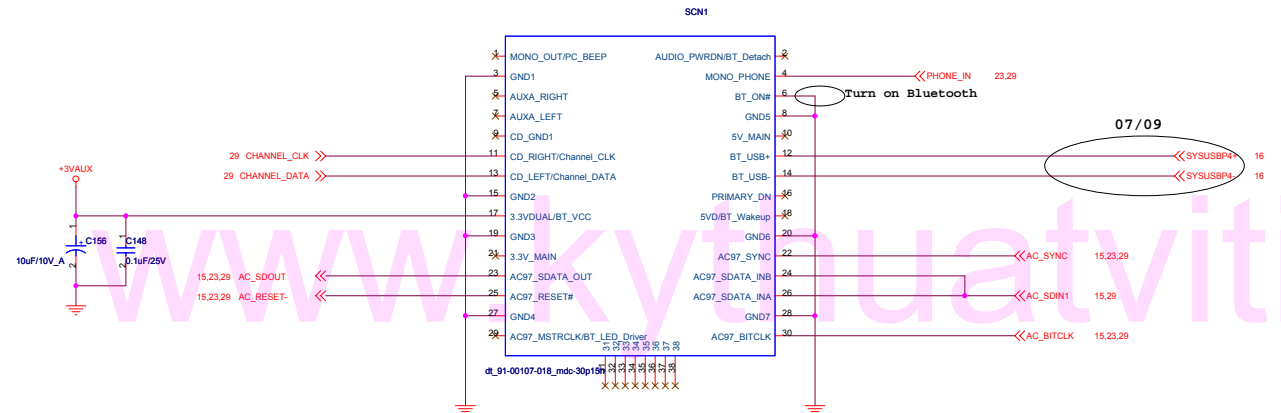
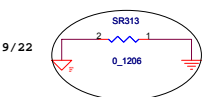
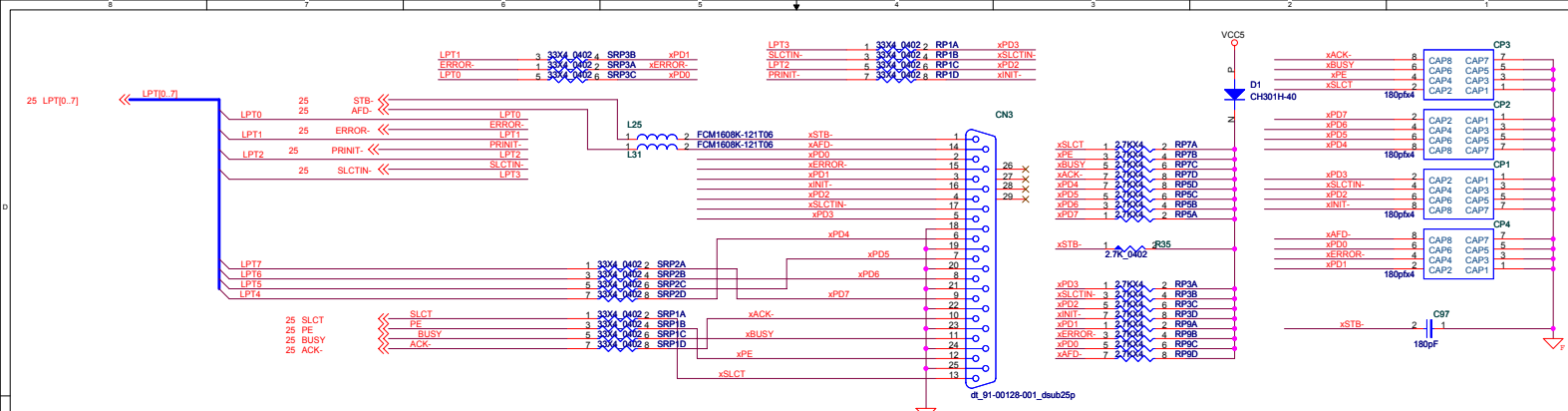
Reserve for fine tune accuracy of Jack Sensing

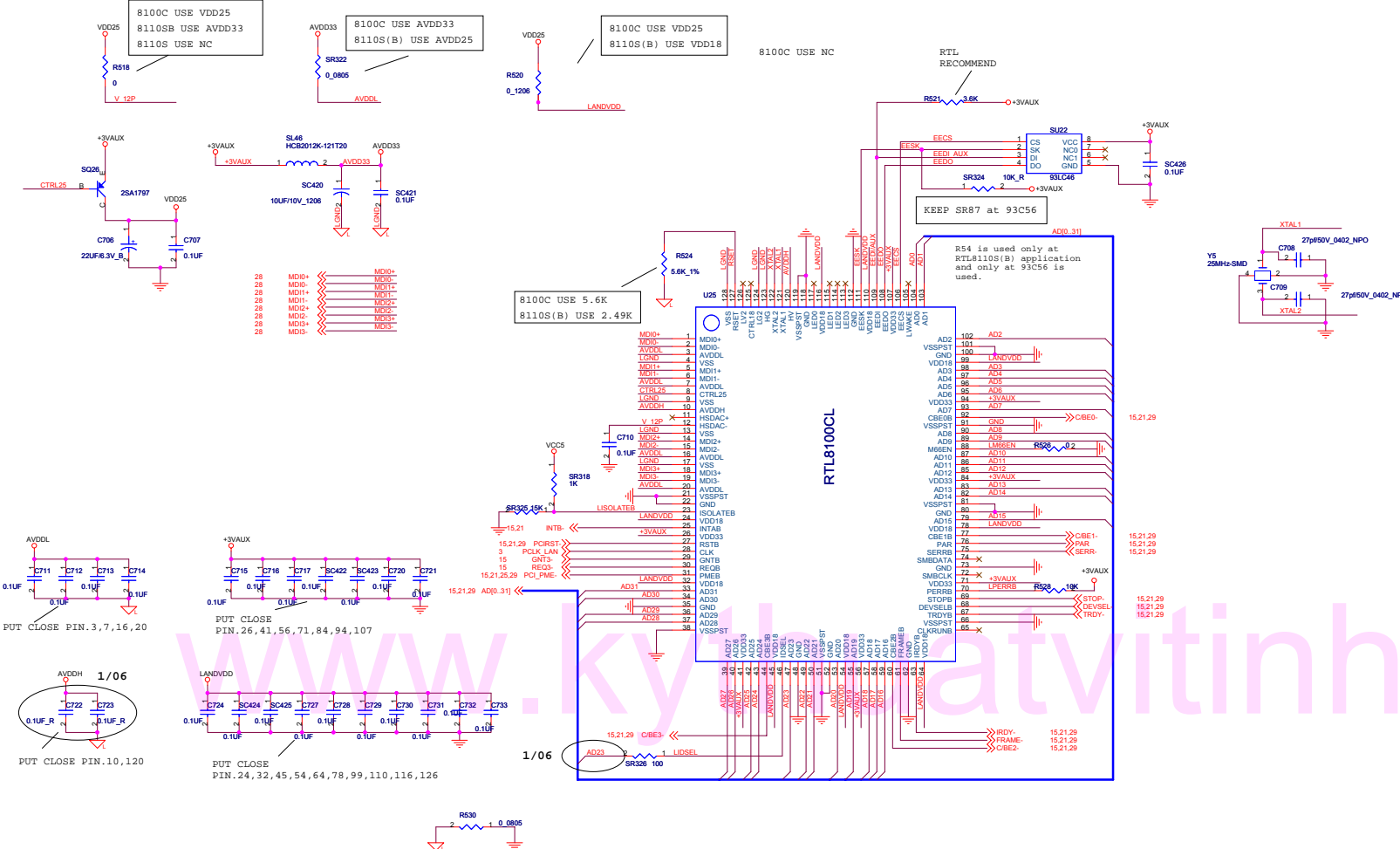
CHOOSE 24.576MHZ CRYSTAL; FLOATING





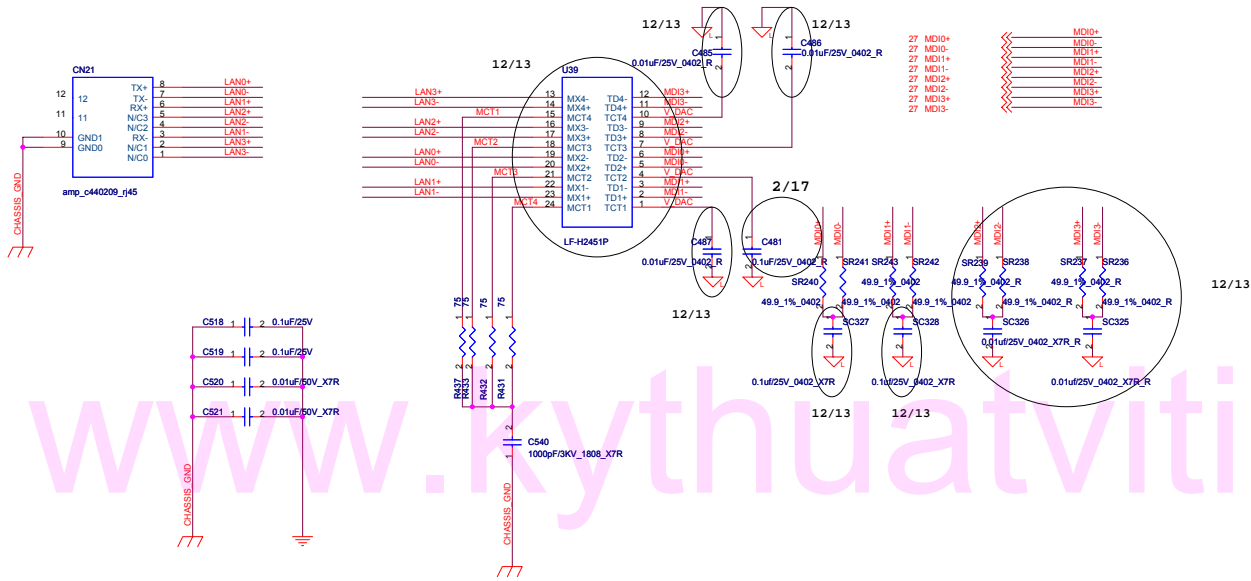






(GLAN)Broadcom Modified by 12/08

<b>LAN CHIP</b>	
Doc No:	558-1-4-01
Date:	Thursday, March 24, 2005
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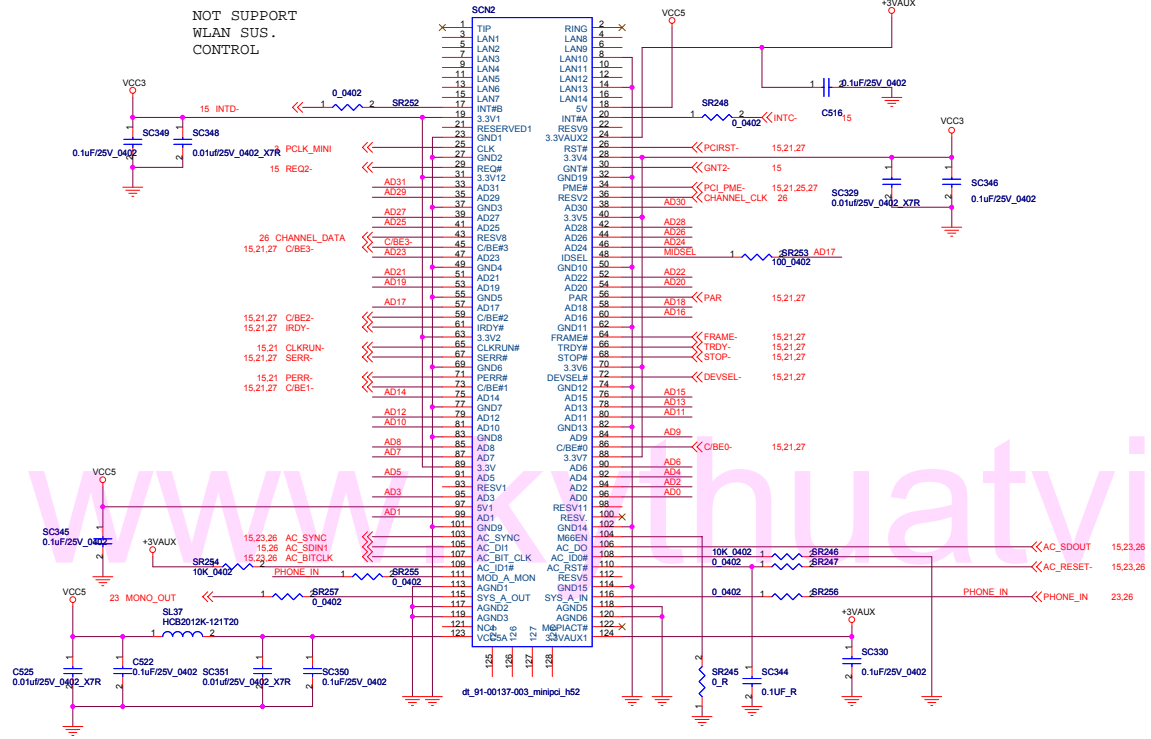


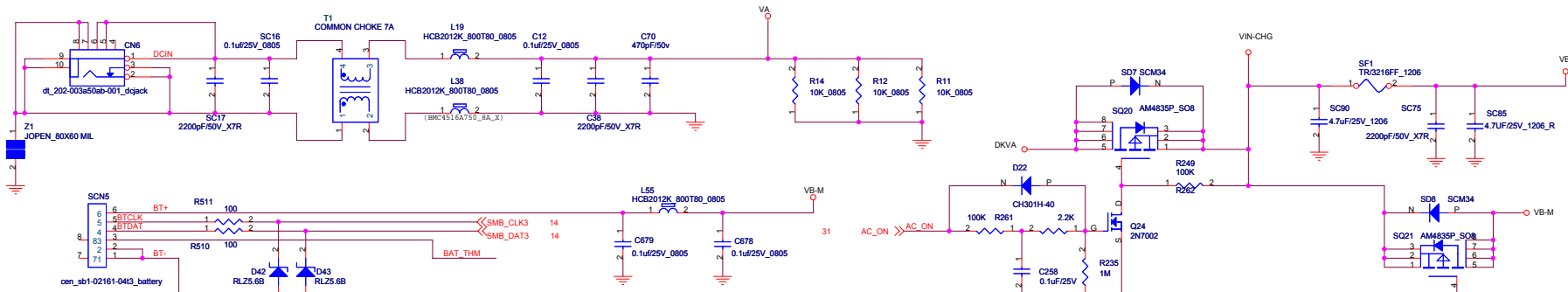
15.21.27 AD[0..31]

AD[0..31]

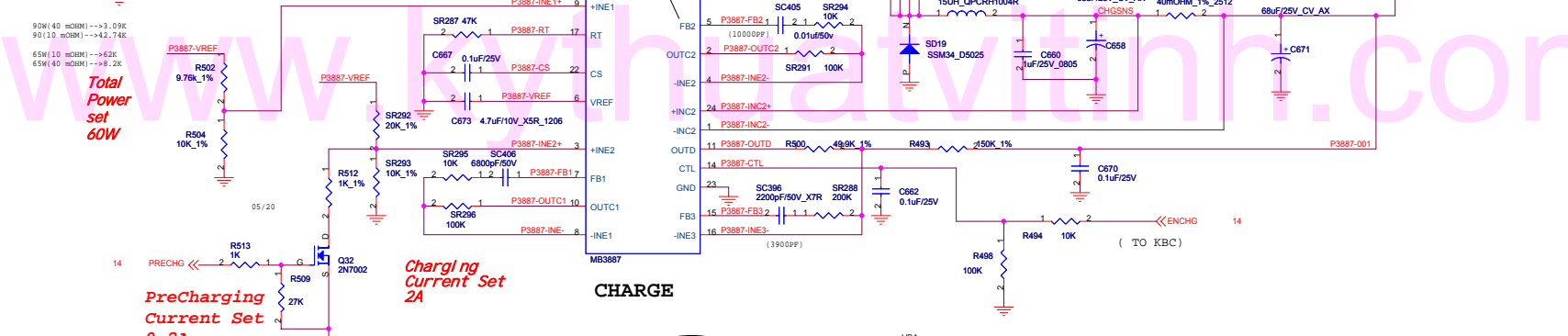
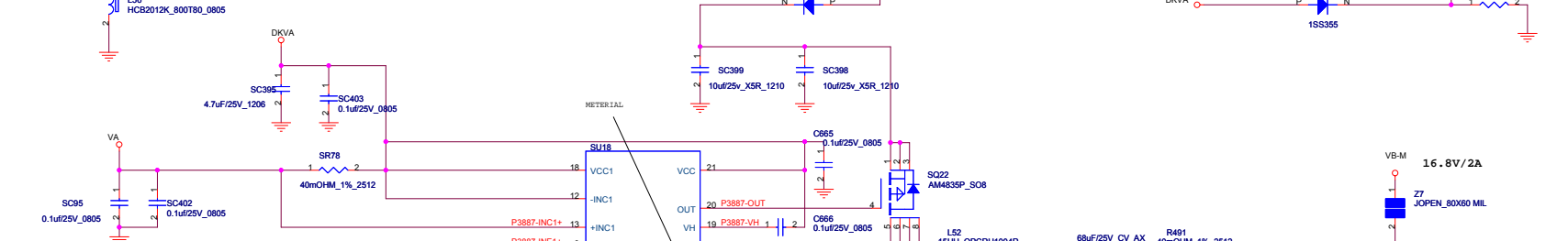
NOT SUPPORT  
WLAN SUS.  
CONTROL

### MINI PCI SOCKET





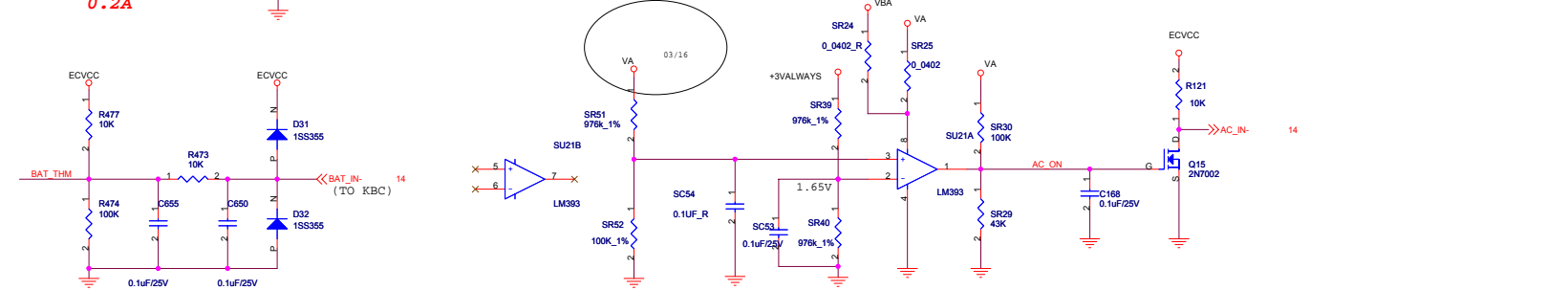
**ADAPTER/BATTERY SELECT**

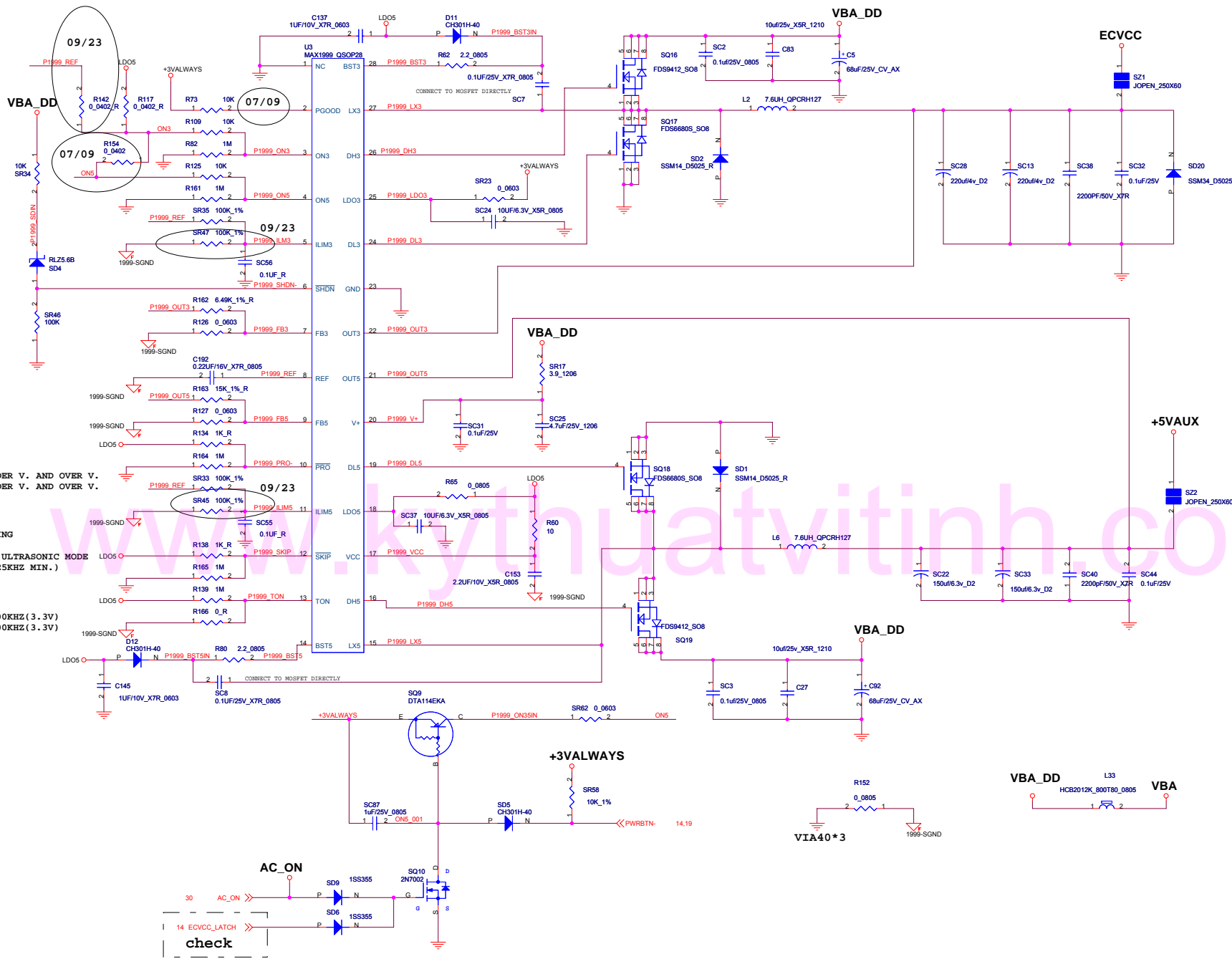


**Total Power set 60W**

**PreCharging Current Set 0.2A**

**Charging Current Set 2A**

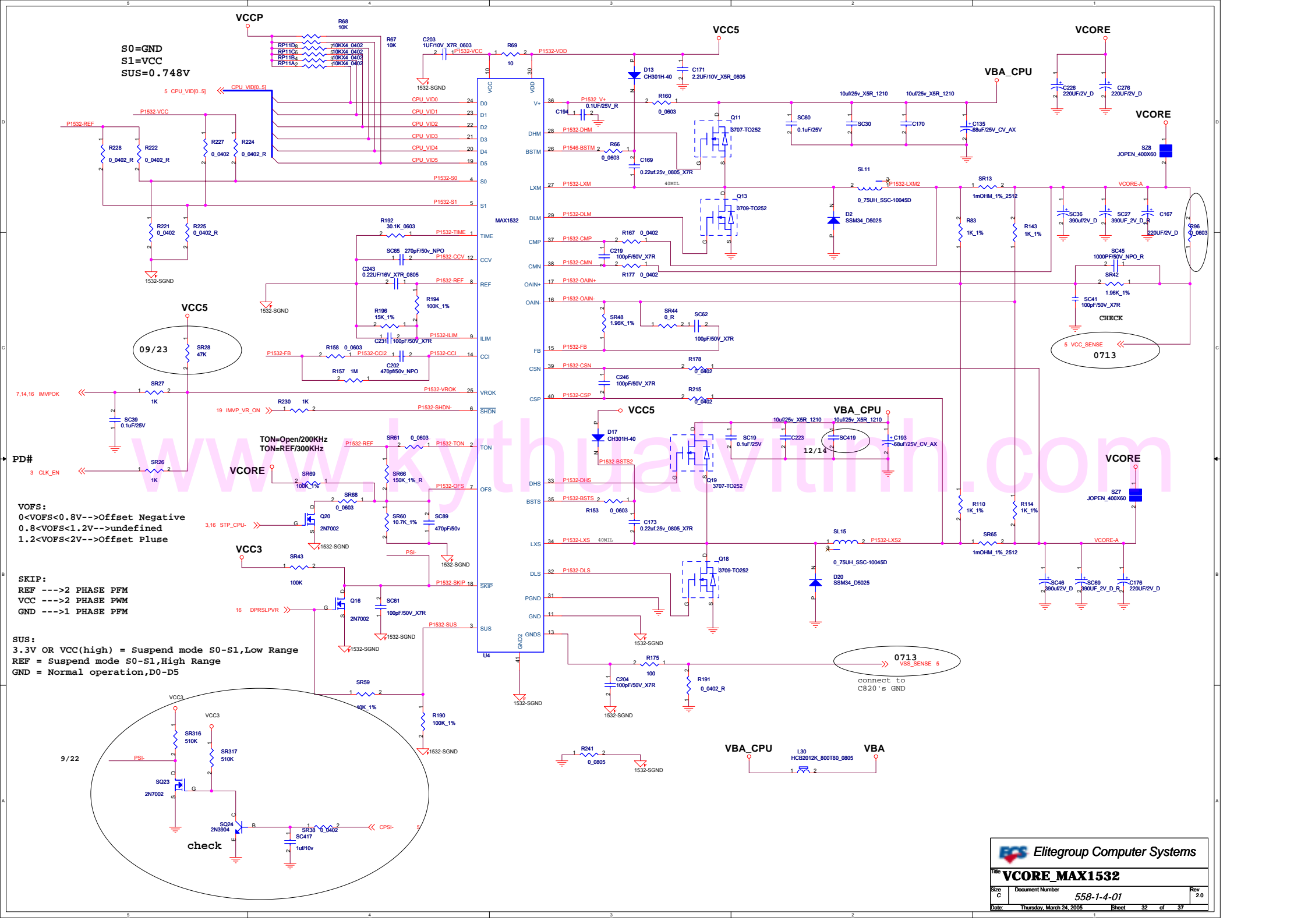




/PRO:  
 VCC: DISABLE UNDER V. AND OVER V.  
 GND: ENABLE UNDER V. AND OVER V.

/SKIP:  
 GND: PULSE-SKIPPING  
 VCC: PWM MODE  
 REF OR FLOATING: ULTRASONIC MODE  
 (PULSE SKIPPING, 25KHZ MIN.)

TON:  
 VCC: 200KHZ (5V), 300KHZ (3.3V)  
 GND: 400KHZ (5V), 500KHZ (3.3V)



S0=GND  
S1=VCC  
SUS=0.748V

VCC5  
09/23  
SR28  
47K

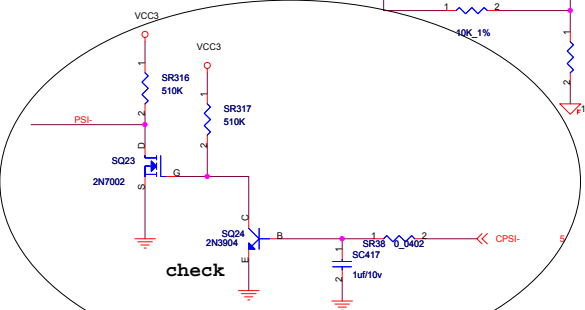
7.14.16 IMVPOK

PD#  
3 CLK\_EN

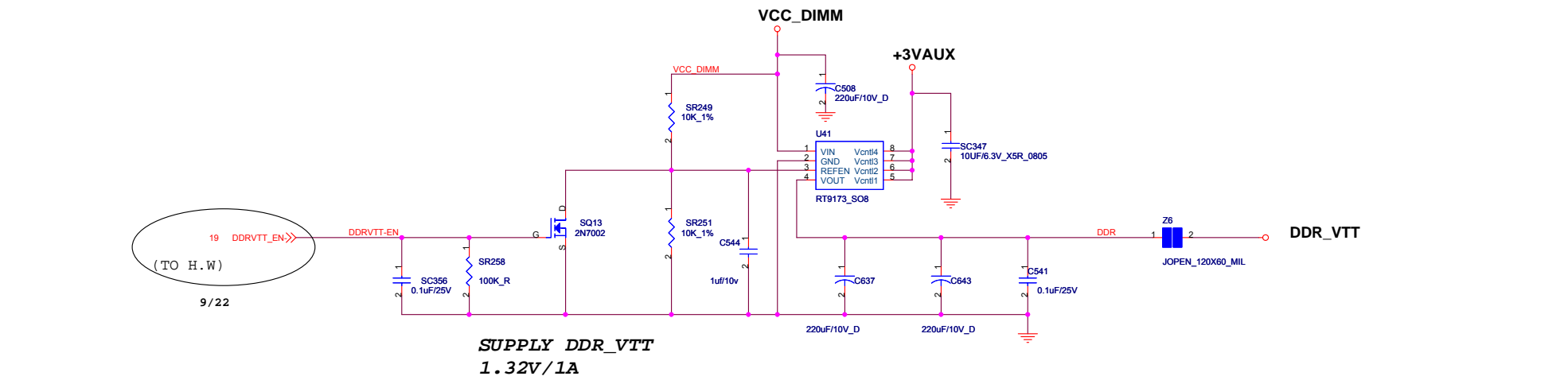
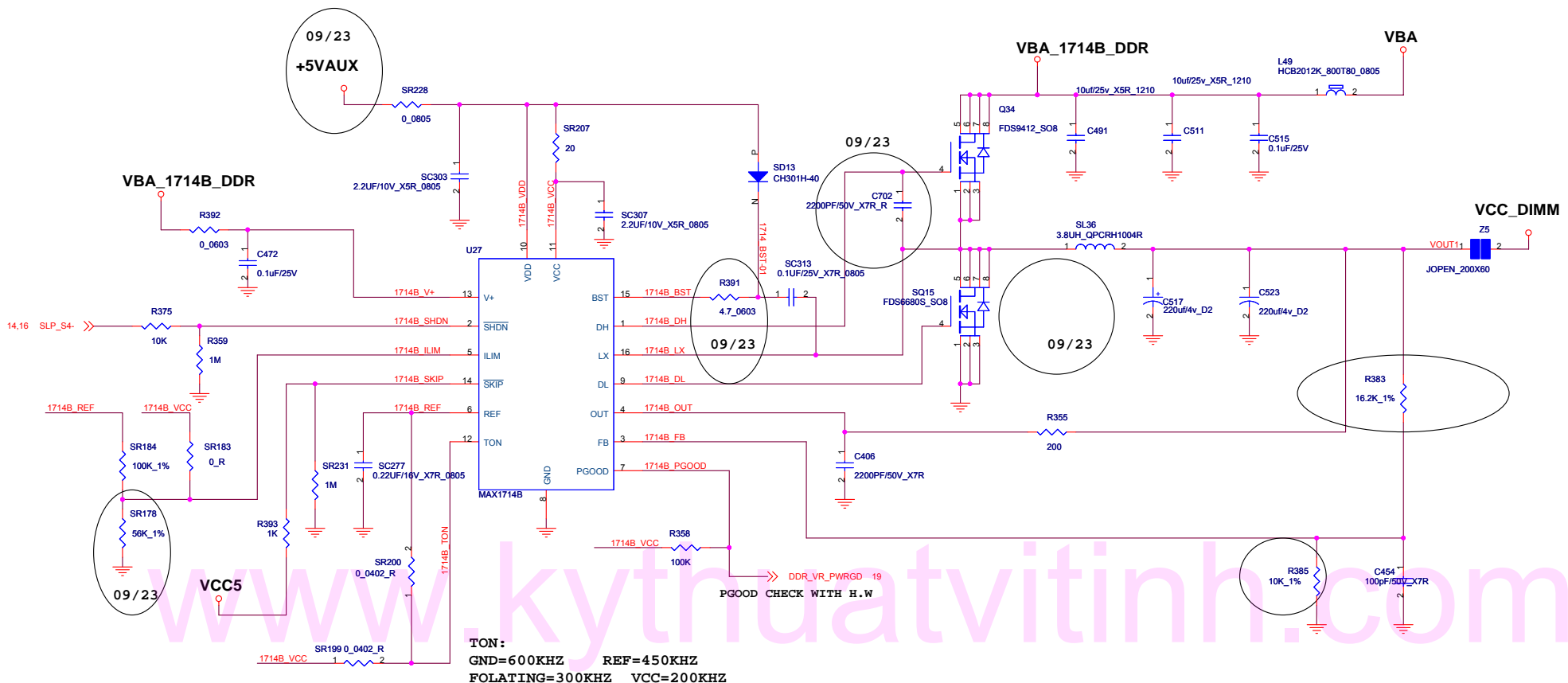
VOFS:  
0<VOFS<0.8V-->Offset Negative  
0.8<VOFS<1.2V-->undefined  
1.2<VOFS<2V-->Offset Plus

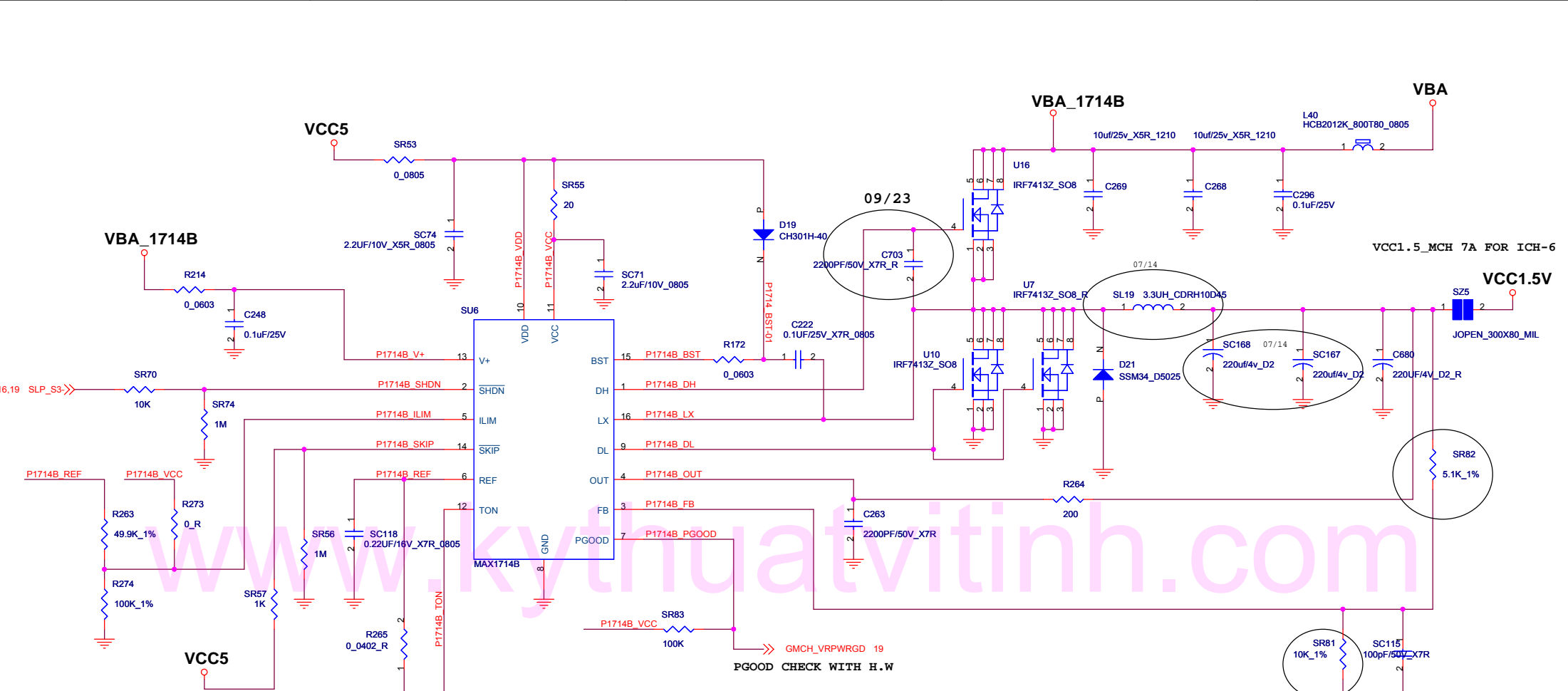
SKIP:  
REF ---->2 PHASE PFM  
VCC ---->2 PHASE PWM  
GND ---->1 PHASE PFM

SUS:  
3.3V OR VCC(high) = Suspend mode S0-S1,Low Range  
REF = Suspend mode S0-S1,High Range  
GND = Normal operation,D0-D5





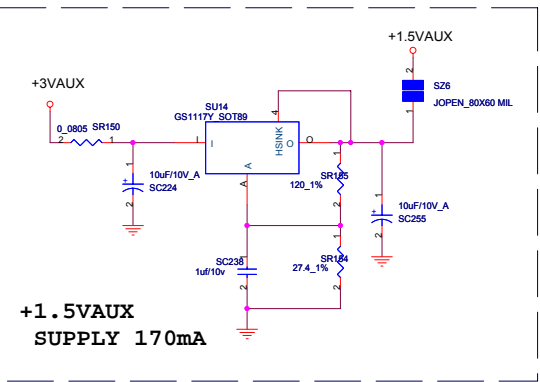
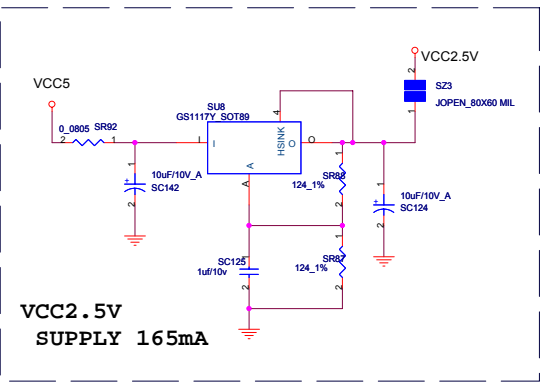
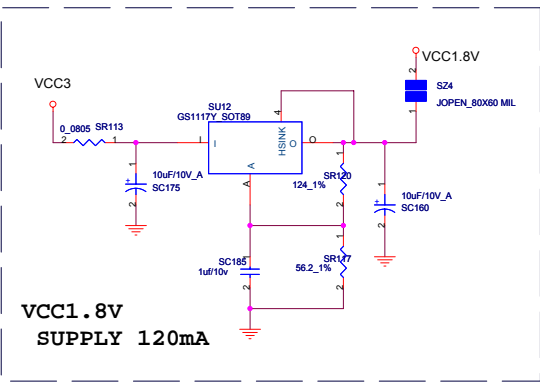
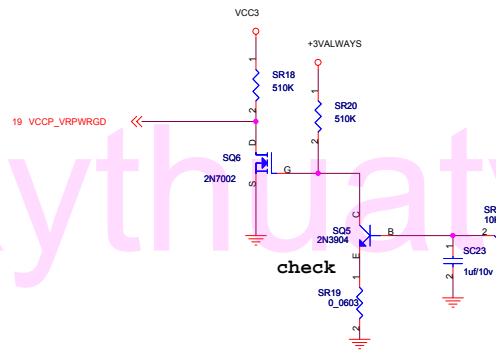
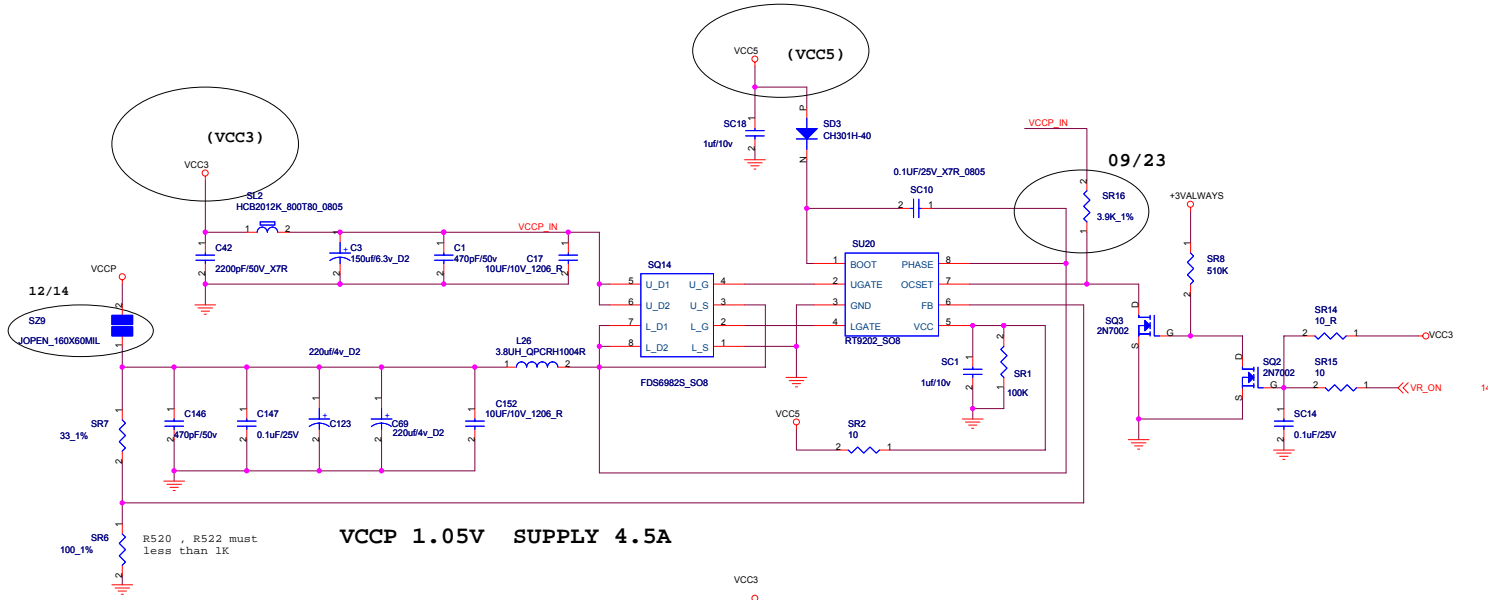




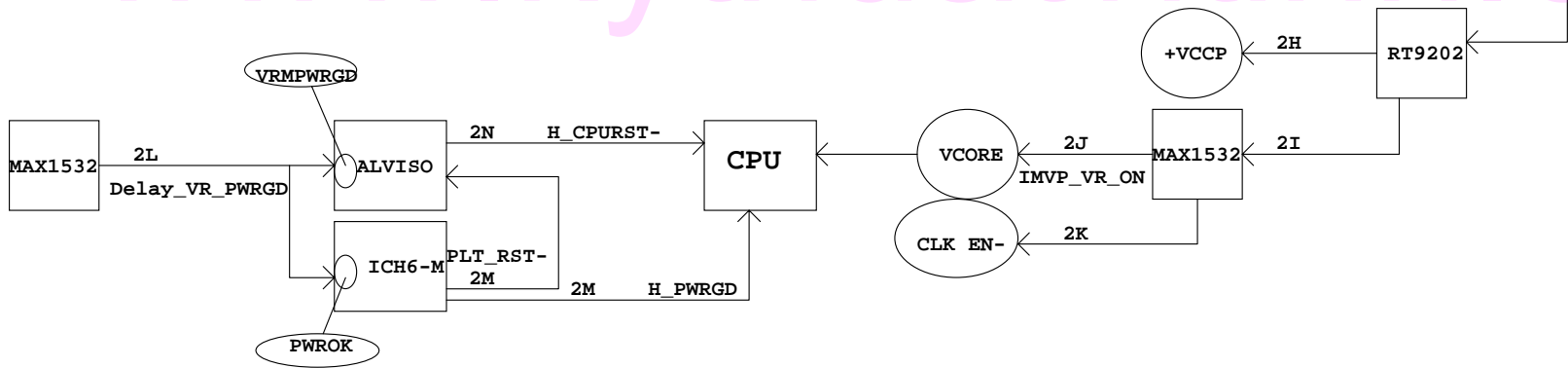
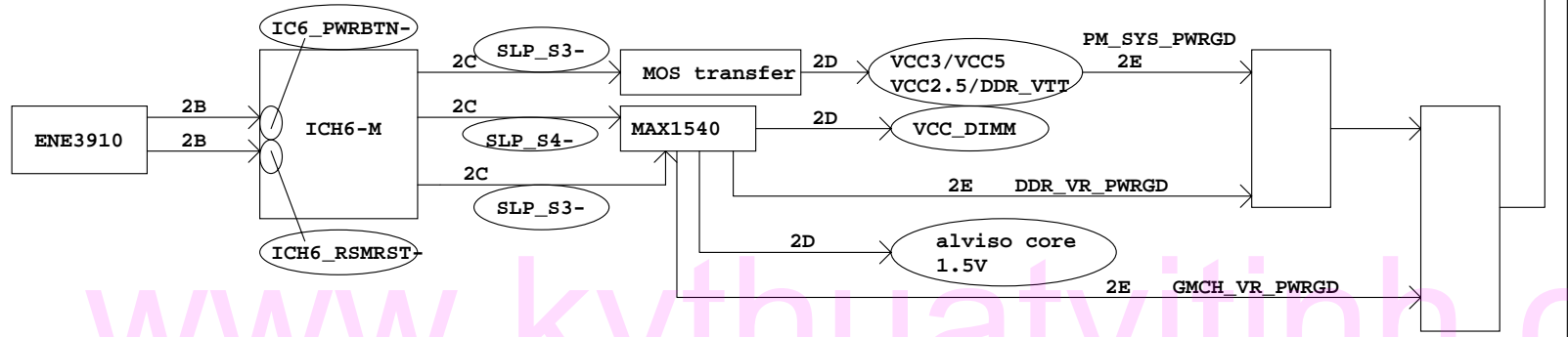
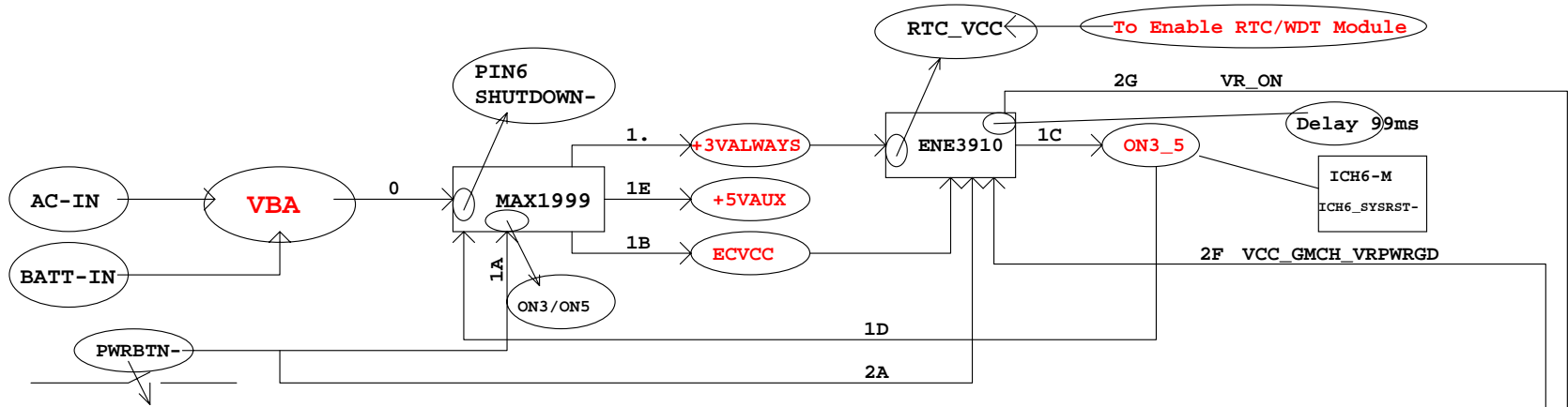
**TON:**  
**GND=600KHZ      REF=450KHZ**  
**FOLATING=300KHZ      VCC=200KHZ**

PGOOD CHECK WITH H.W

<b>Title    VCC1.5V_MAX1714B</b>		
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