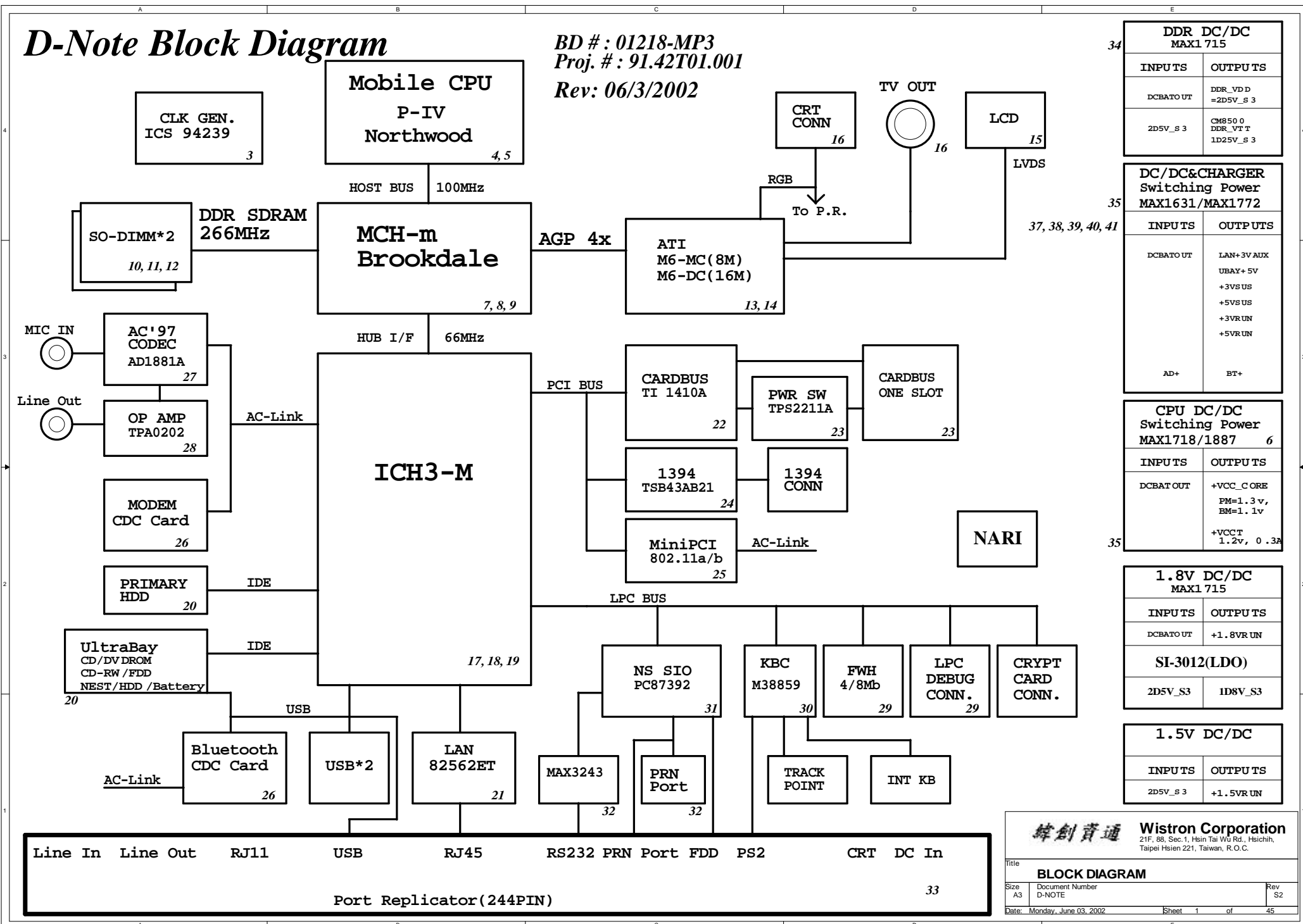


# D-Note Block Diagram

BD #: 01218-MP3  
 Proj. #: 91.42T01.001  
 Rev: 06/3/2002



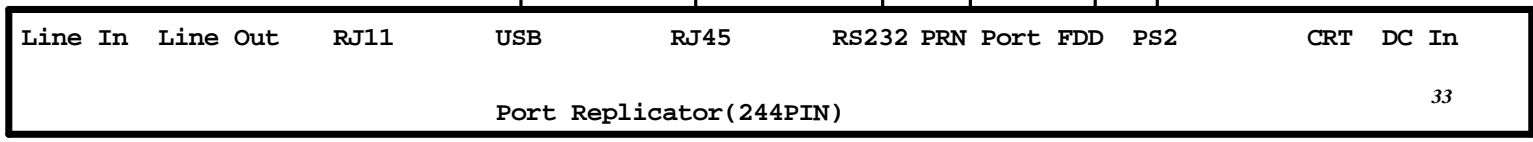
DDR DC/DC MAX1715	
INPUTS	OUTPUTS
DCBATO UT	DDR_VD D =2D5V_S 3
2D5V_S 3	CM850 0 DDR_VT T 1D25V_S 3

DC/DC&CHARGER Switching Power MAX1631/MAX1772	
INPUTS	OUTPUTS
DCBATO UT	LAN+ 3V AUX UBAY+ 5V +3VSUS +5VSUS +3VR UN +5VR UN
AD+	BT+

CPU DC/DC Switching Power MAX1718/1887	
INPUTS	OUTPUTS
DCBAT OUT	+VCC_C ORE PM=1.3 v, BM=1.1 v
	+VCC T 1.2v, 0.3A

1.8V DC/DC MAX1715	
INPUTS	OUTPUTS
DCBATO UT	+1.8VR UN
SI-3012(LDO)	
2D5V_S3	1D8V_S3

1.5V DC/DC	
INPUTS	OUTPUTS
2D5V_S 3	+1.5VR UN



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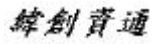
**BLOCK DIAGRAM**

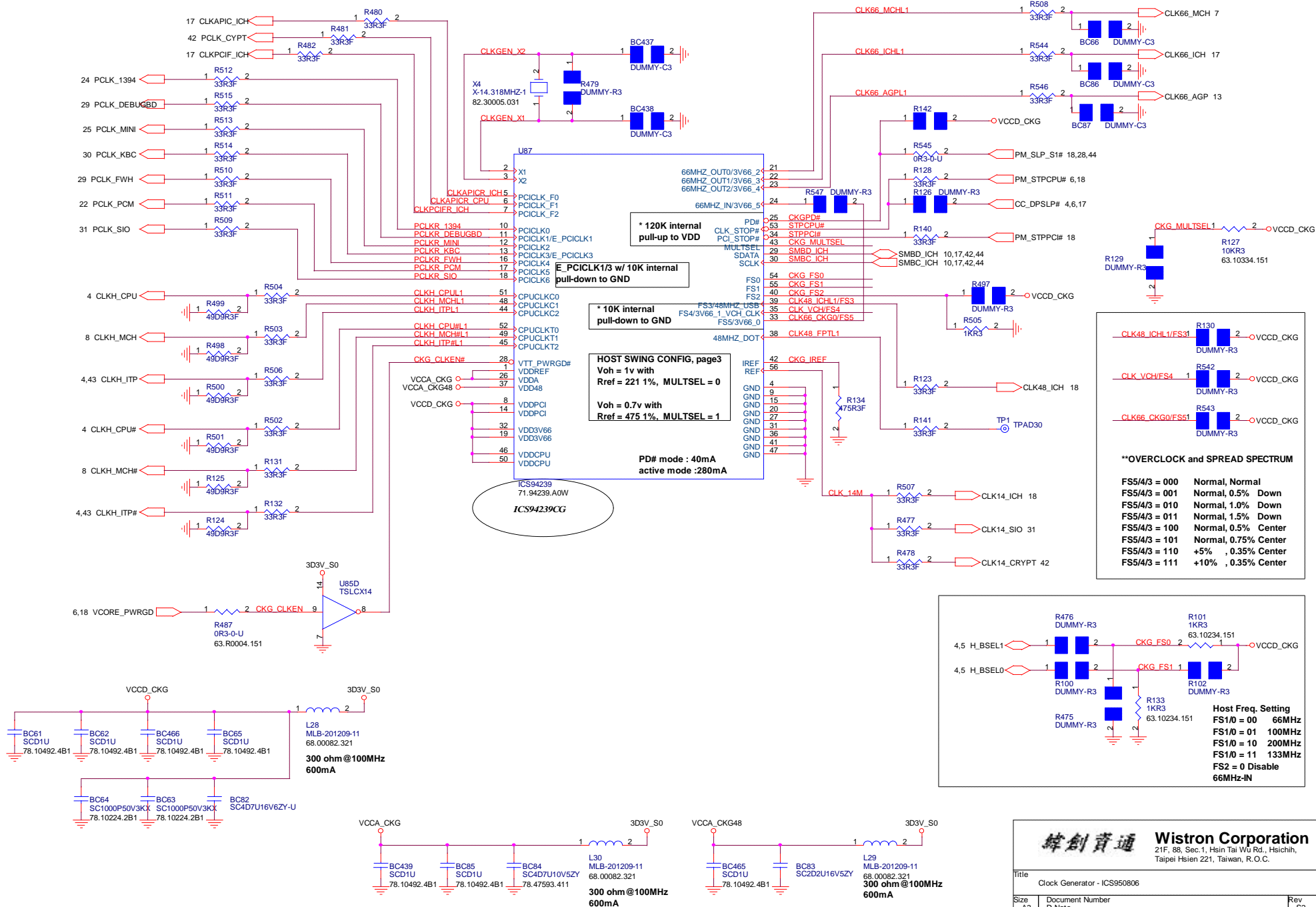
Size A3	Document Number D-NOTE	Rev S2
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1D5V_S0	↔	1D5V_S0	8,9,14,29,36	LCD_DCBATO	↔	LCD_DCBAT	15
1D8V_LANAC	↔	1D8V_LANAC	19,36	LIGHT_PWR	↔	LIGHT_PWR	15
1D8V_S5	↔	1D8V_S5	19,35	SLOTVCC	↔	SLOTVCC	22,23
1D8V_S0	↔	1D8V_S0	8,9,17,19,34,36	SLOTVPP	↔	SLOTVPP	22,23
3D3VRTC	↔	3D3VRTC	18	1394_AVDD	↔	1394_AVDD	24
3D3V_LANAC	↔	3D3V_LANAC	17,19,21,25,33,36	1394_PLLVDD	↔	1394_PLLVDD	24
3D3V_S0	↔	3D3V_S0	3,4,5,6,7,10,13,14,15,16,17,18,19,20,24,25,26,27,29,30,31,34,36,42,43,45	MOD_5VAD	↔	MOD_5VAD	25
3D3V_S3	↔	3D3V_S3	10,13,14,15,20,22,23,26,30,36,38	USB0_VCC	↔	USB0_VCC	26
3D3V_S5	↔	3D3V_S5	15,17,18,19,22,26,35,36,44	AUD_VREF	↔	AUD_VREF	28
5V_S0	↔	5V_S0	6,15,16,17,19,20,25,27,28,29,30,31,32,36,38,42,43,44	OP+5V	↔	OP+5V	28
5V_S3	↔	5V_S3	15,16,23,26,28,30,34,36,41,43,45	TP_VCC	↔	TP_VCC	30
5V_S5	↔	5V_S5	15,19,20,33,35,36	M1772_LDO	↔	M1772_LDO	37
UBAY+5V	↔	UBAY+5V	20	DC+5V	↔	DC+5V	35
5VA	↔	5VA	27,28	DC+3V	↔	DC+3V	35
3D3V_LANACAUX	↔	3D3V_LANACAUX	25,26				
USB1_VCC	↔	USB1_VCC	26,33				
LCDVDD	↔	LCDVDD	15				
AC97_3V	↔	AC97_3V	26				
CRT_VCC	↔	CRT_VCC	16,33				
AD+	↔	AD+	40,41,44				
DCBATOUT	↔	DCBATOUT	6,15,34,35,36,37,39,40,41				
ICH_VBIAS	↔	ICH_VBIAS	18				
VCC_RTC	↔	VCC_RTC	17,18,19,42				
AD+_IN	↔	AD+_IN	33,41				
MAX1631_VL	↔	MAX1631_VL	35				
BT_VCC	↔	BT_VCC	26				
FAN1_VCC	↔	FAN1_VCC	42				

### PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
TI 1394	AD19	Auto	REQ2# / GNT2#
MINIPCI SLOT	AD21	C,E	REQ3# / GNT3#
PCMCIA TI 1410	AD25	B,D	REQ1# / GNT1#
AGP	AD17 (Int.)	A,B	
LAN	AD24 (Int.)	E	
USB	AD29	A,D,C	
Hub-to-PCI	AD30		
LPC Bridge/ IDE/AC97/ SMBus	AD15		

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Title Table of Content	
Size A3	Document Number D-Note
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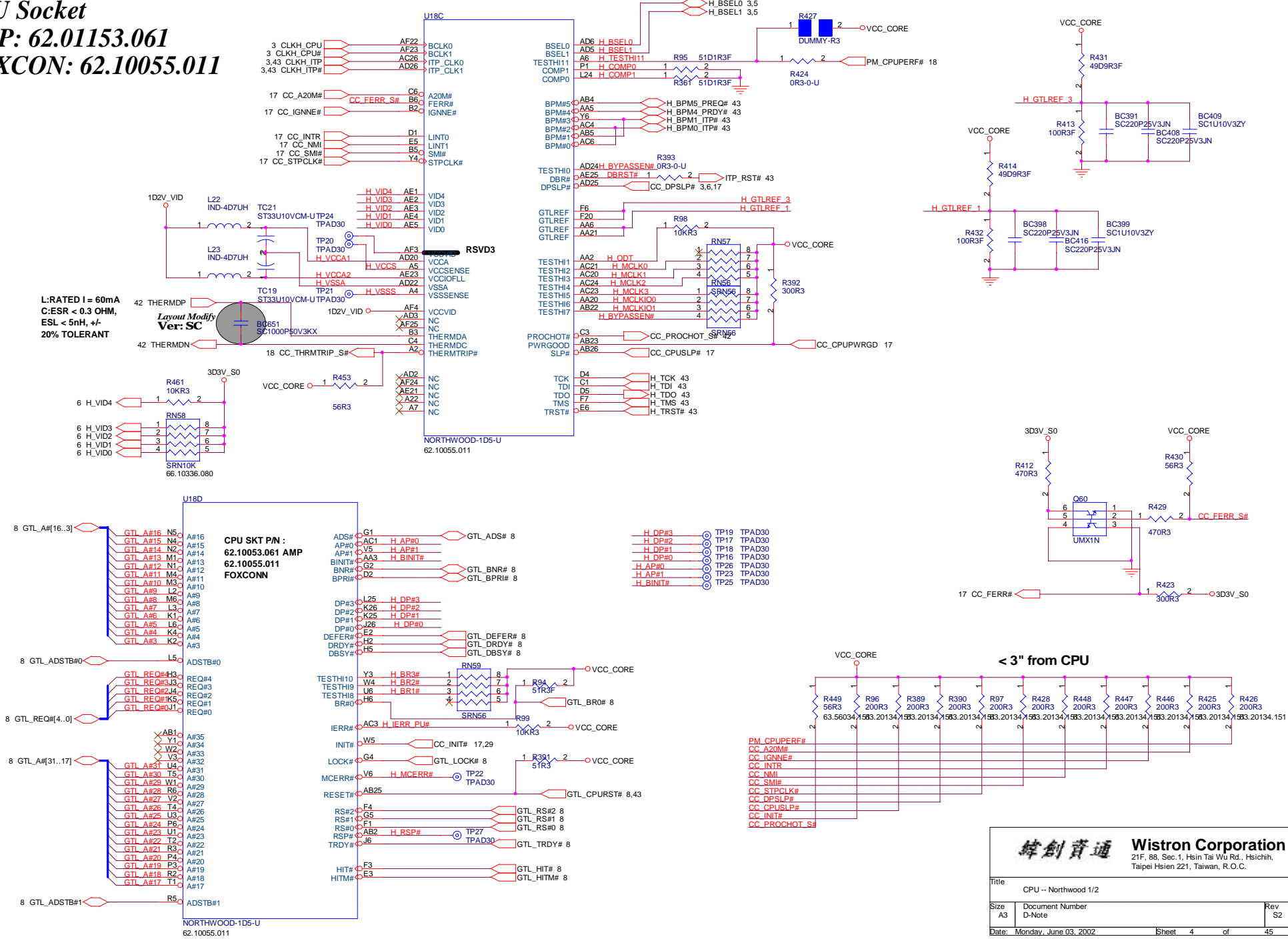
# CPU Socket

## AMP: 62.01153.061

### FOXCON: 62.10055.011

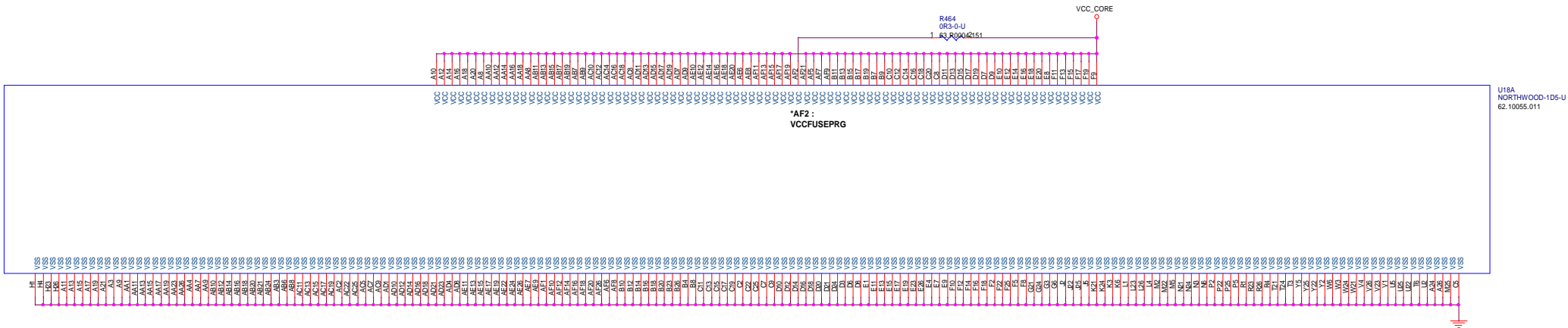
L-RATED I = 60mA  
 C:ESR < 0.3 OHM,  
 ESL < 5nH, +/-  
 20% TOLERANT

Layout Modify  
 Ver: SC

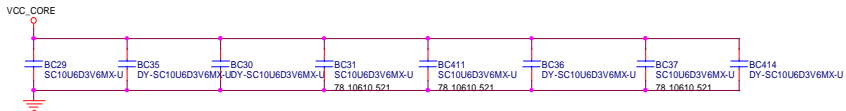


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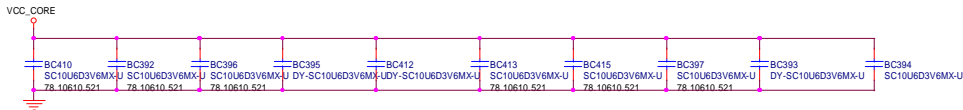
Title CPU - Northwood/1/2		
Size A3	Document Number D-Note	Rev S2
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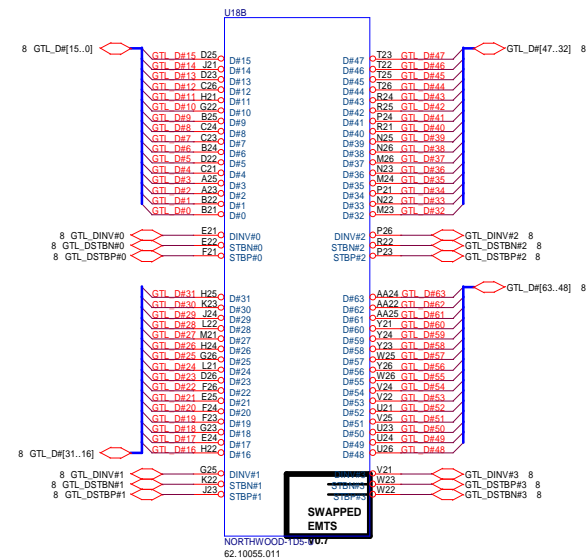
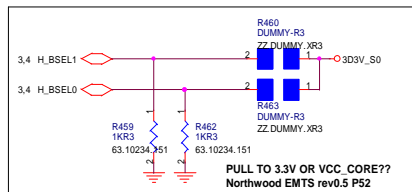
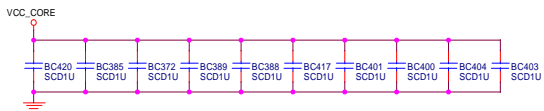
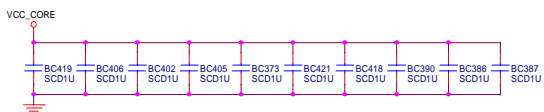
**10U/X7R 1206 DECOUPLING CAPS  
8X IN SOCKET CAVITY  
10X IN CRB**



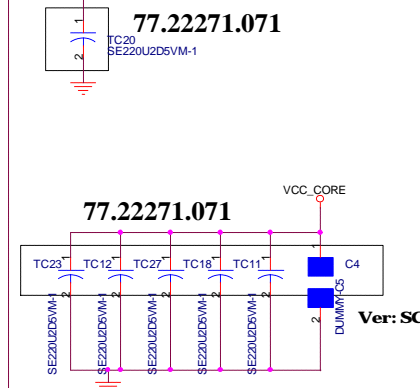
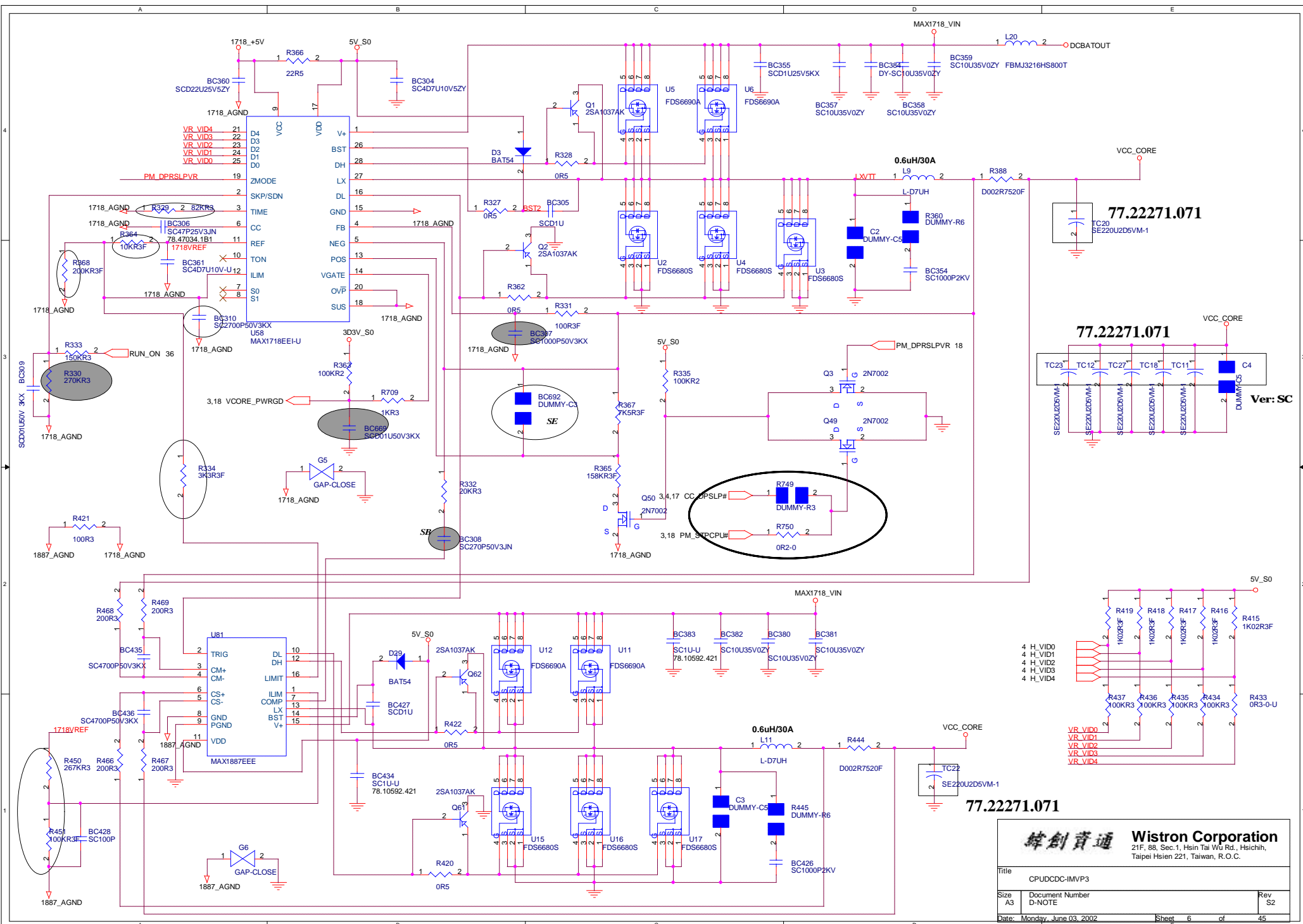
**10U/X7R 1206 DECOUPLING CAPS  
10X AROUND SOCKET  
28X IN CRB**



**0.1U/X5R 0603 DECOUPLING CAPS  
20X AROUND SOCKET  
0.47U/X5R 0603 10X IN CRB**

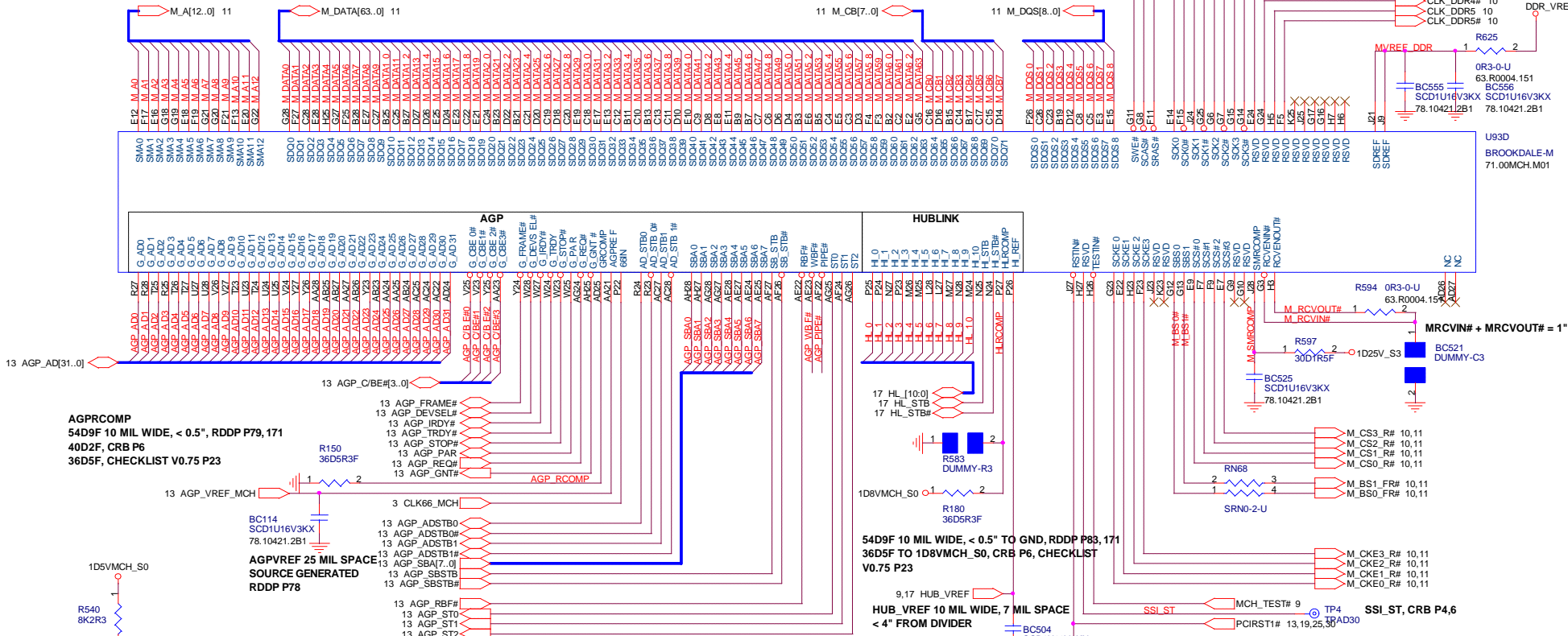
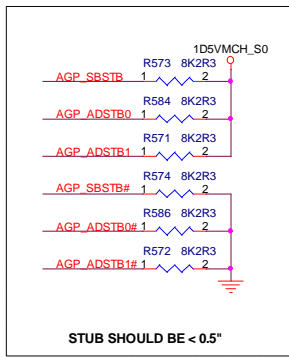
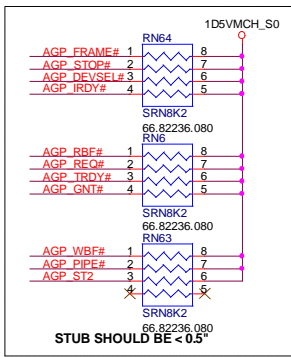


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77.22271.071

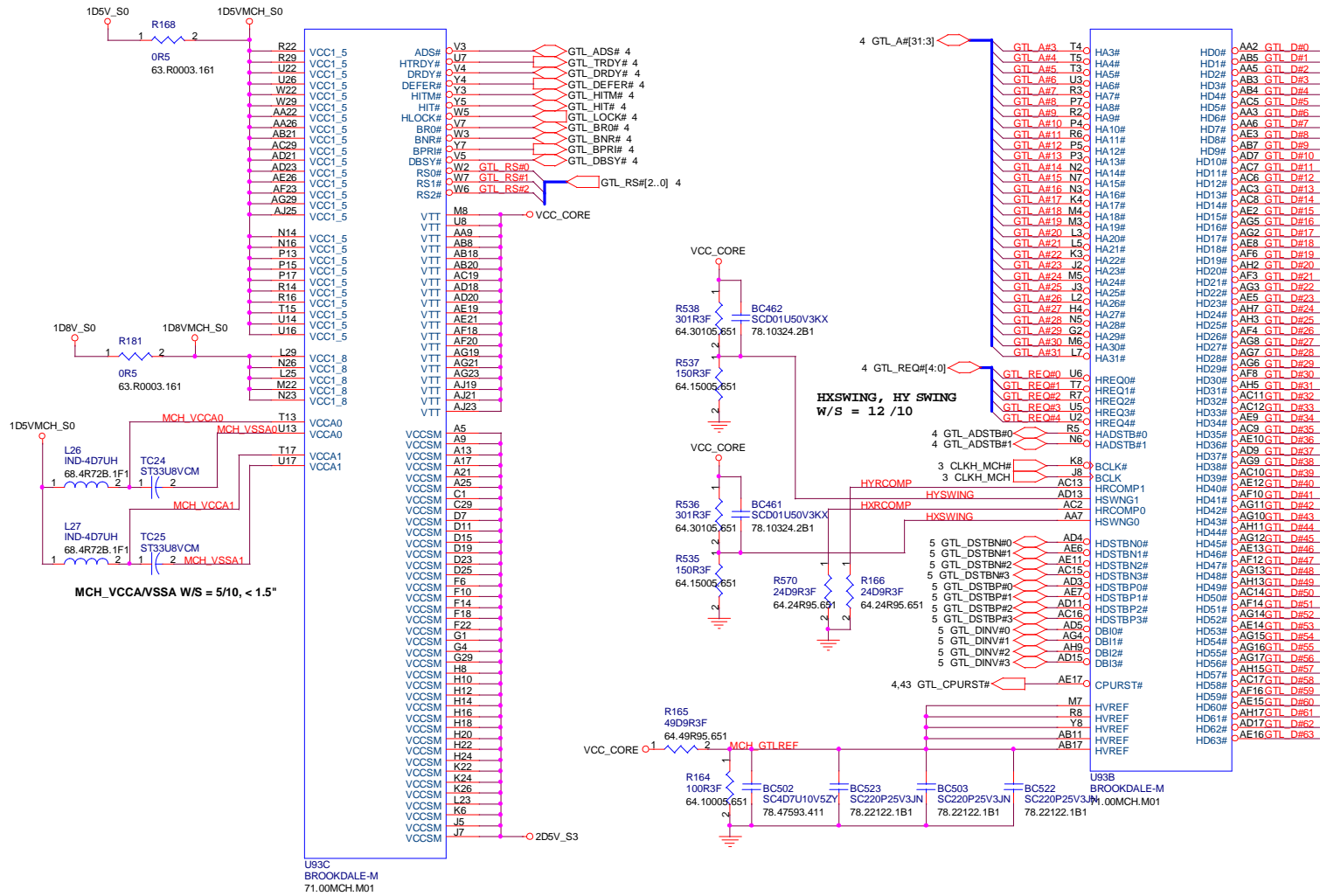
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPUDCC-IMV/P3
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ST1	ST0	MCH STRAP
X	0	DDR
X	1	SDR
0	X	533 MHz
1	X	400 MHz

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Title: Brookdale 1/3  
 Size: A3 Document Number: D-Note Rev: S2  
 Date: Monday, June 03, 2002 Sheet: 7 of 45

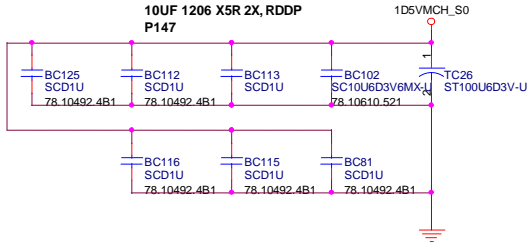


GTL\_D#[63..0] 5

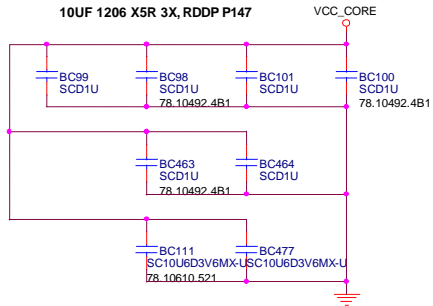
Title Brockdale 2/3		
Size A3	Document Number D-Note	Rev S2
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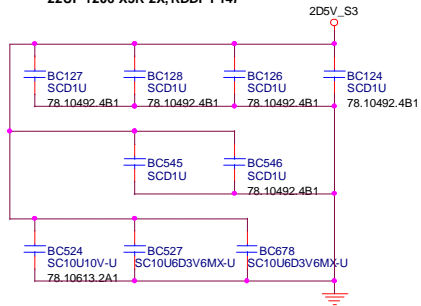
**AGP HF DECOUPLING CAPS**  
**0.1UF 0603 X7R 6X**  
**10UF 1206 X5R 2X, RDDP**  
**P147**



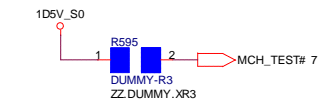
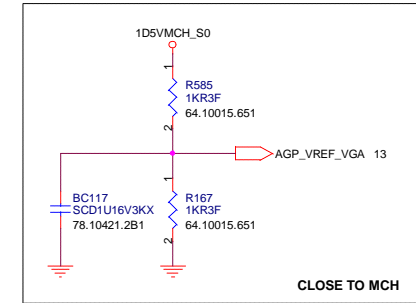
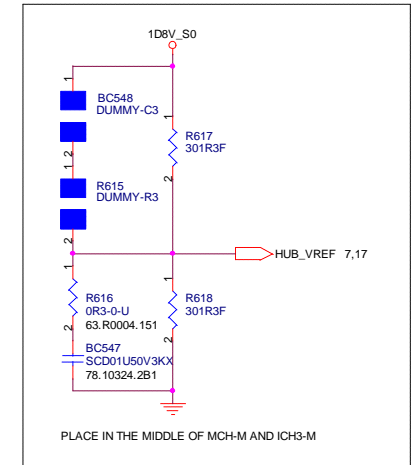
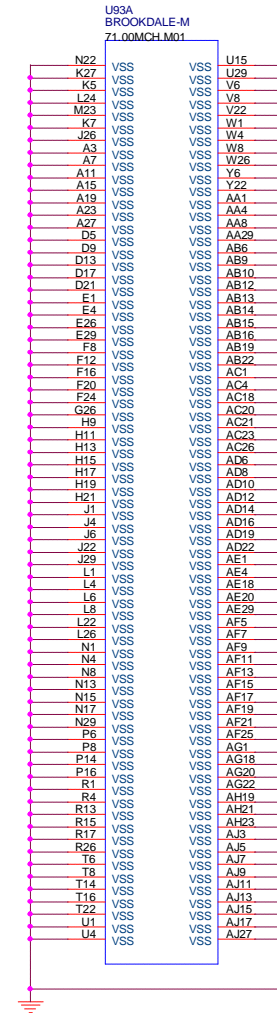
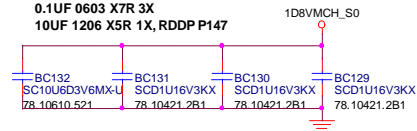
**AGTL+ HF DECOUPLING CAPS**  
**0.1UF 0603 X7R 10X**  
**10UF 1206 X5R 3X, RDDP P147**



**DDR HF DECOUPLING CAPS**  
**0.1UF 0603 X7R 6X IN RDDP, 14X IN CRB-P8**  
**22UF 1206 X5R 2X, RDDP P147**

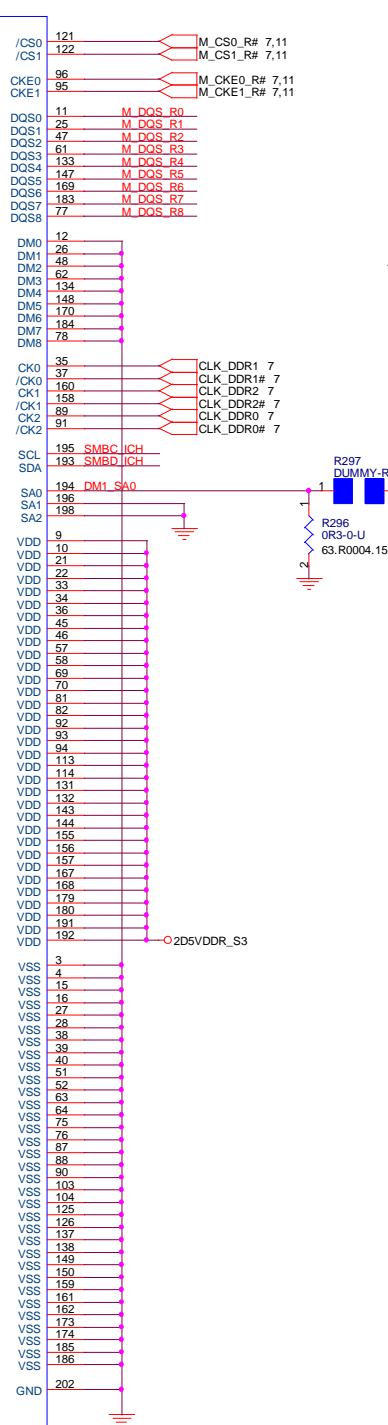


**HUBLINK HF DECOUPLING CAPS**  
**0.1UF 0603 X7R 3X**  
**10UF 1206 X5R 1X, RDDP P147**

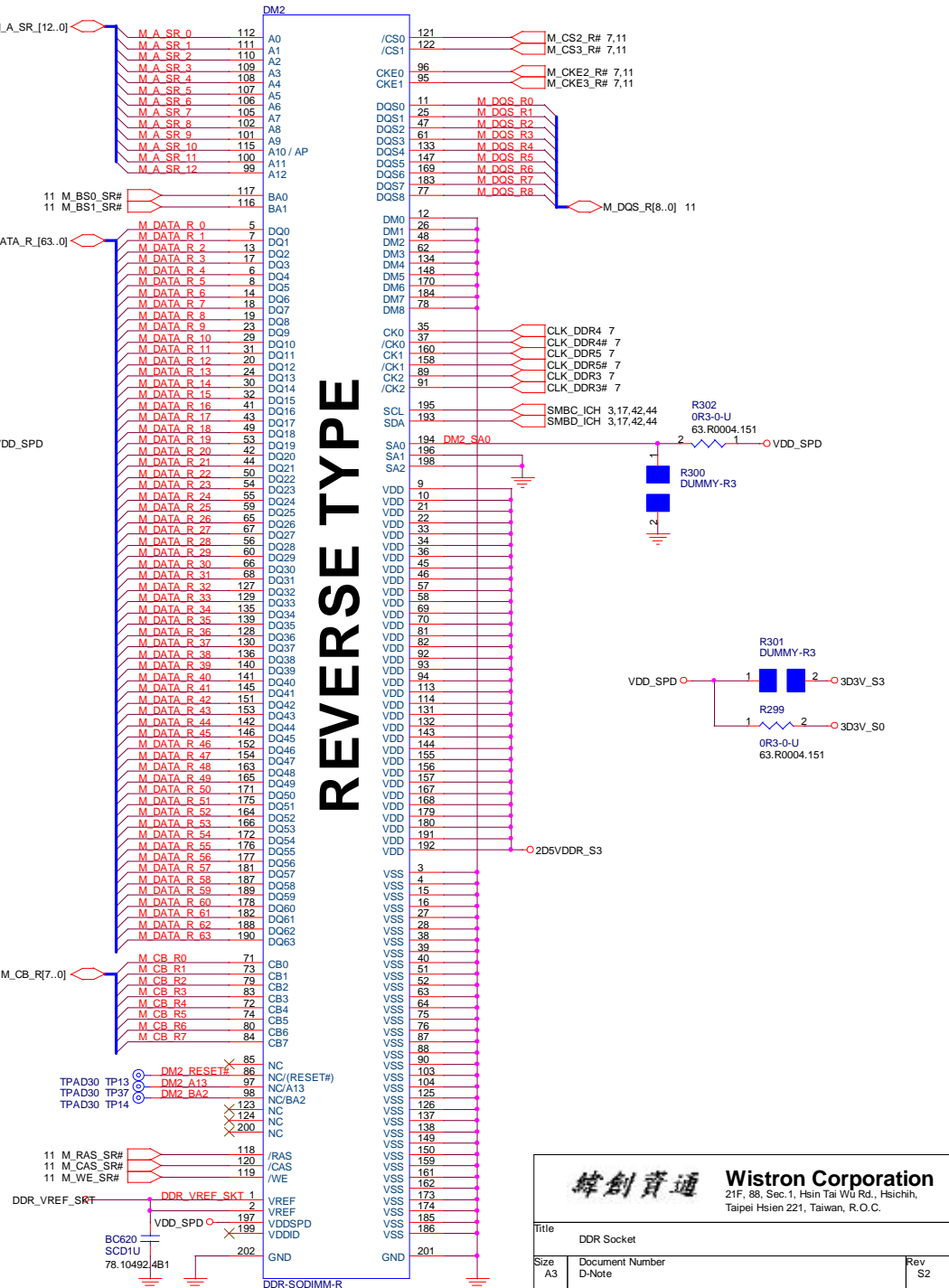




# NORMAL TYPE



# REVERSE TYPE

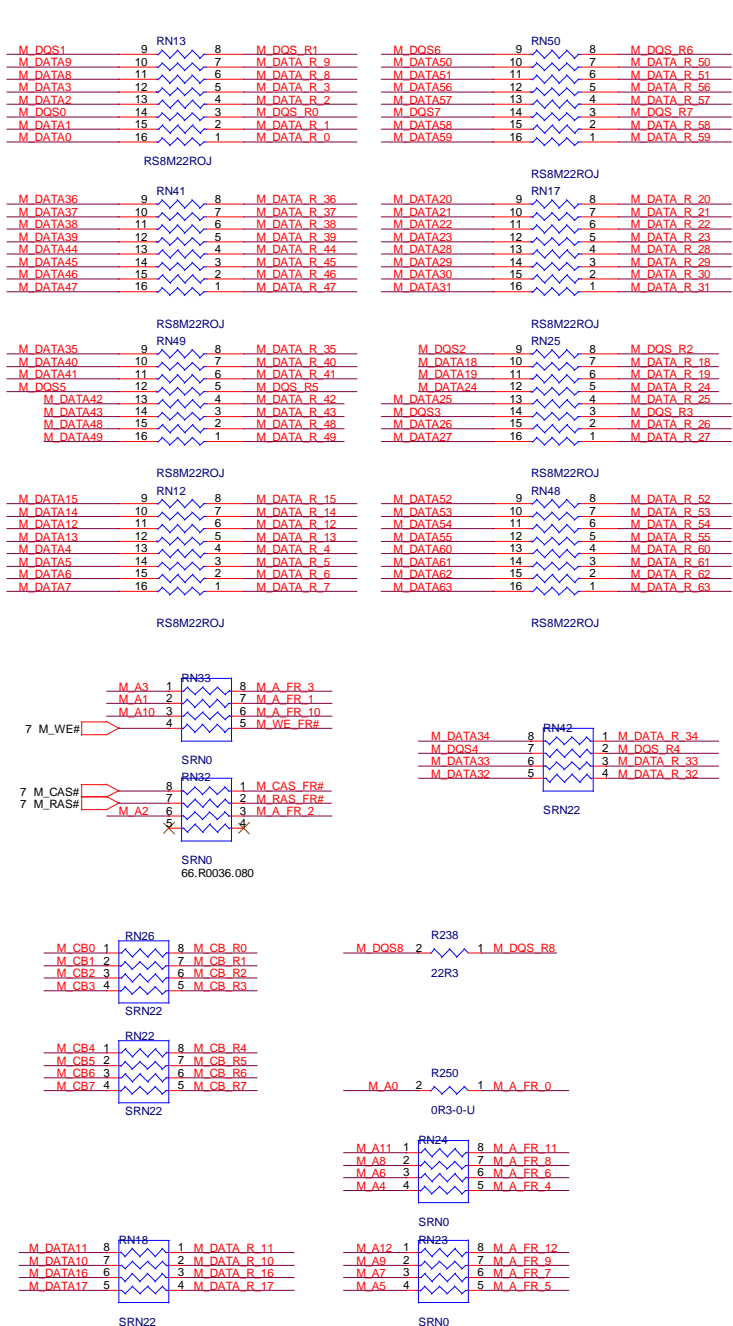


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Title	DDR Socket	
Size	Document Number	Rev
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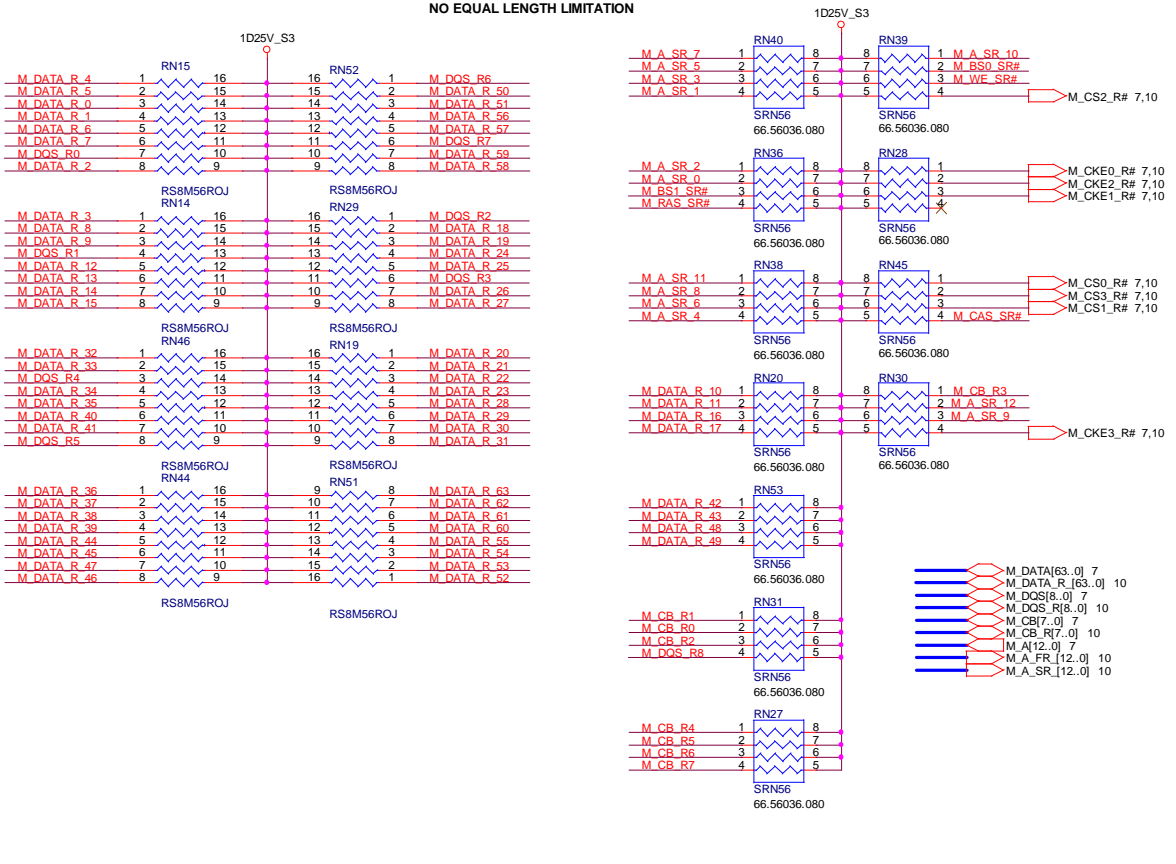
# SERIES DAMPING

PLACE RNs CLOSE TO DM1, < 0.75"  
STRICT EQUAL LENGTH LIMITATION WITH DQS, CB PINS

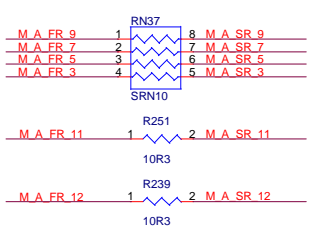
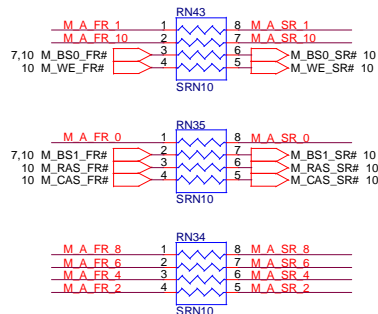


# PARALLEL TERMINATION

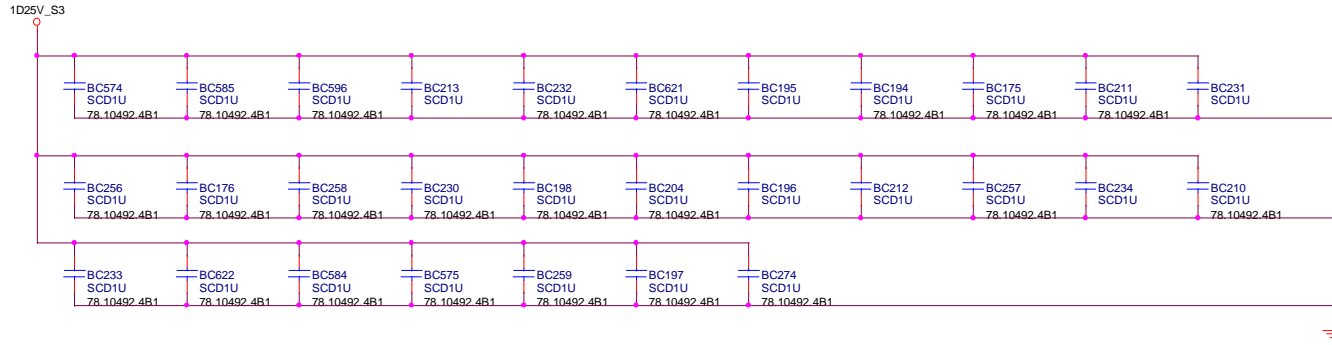
PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO DM2  
NO EQUAL LENGTH LIMITATION



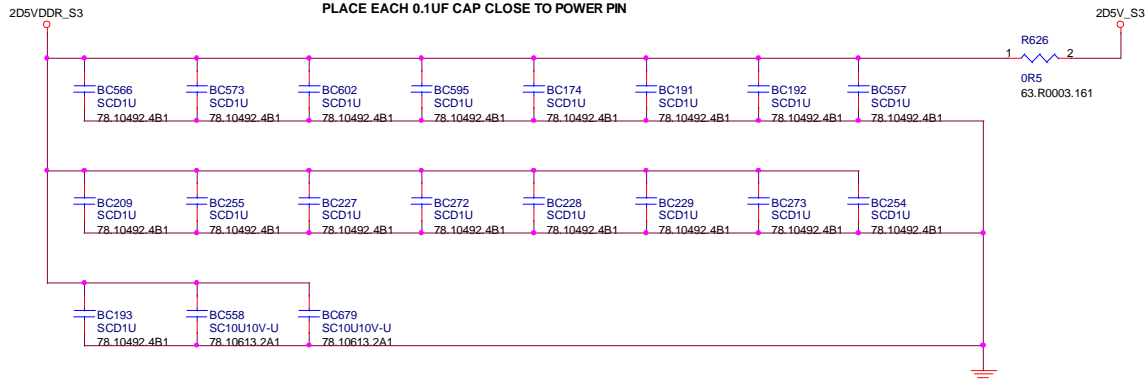
PLACE BETWEEN DM1, DM2  
CLOSE TO DM2 < 0.2", TO DM1 < 1.1"  
EQUAL LENGTH LIMITATION WITH  
SCK/SCK#



PLACE ONE CAP CLOSE TO EVERY 2 PULL-UP TERMINATION RESISTORS, CRB-P13  
 DATA(64)+ADD(13)+DQS(9)+CB(8)+CMD(13)=107  
 0.1UF 0603 Y5V 27X



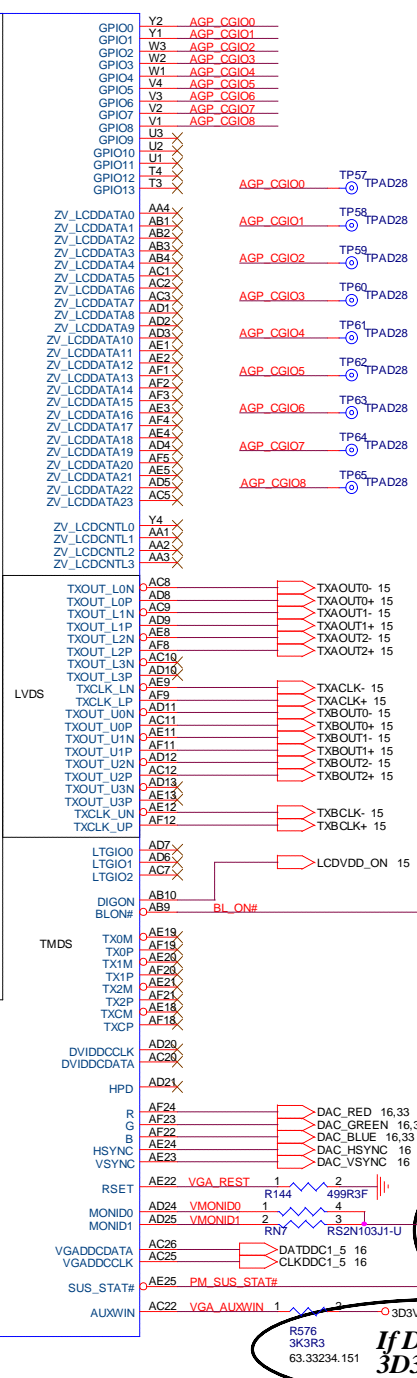
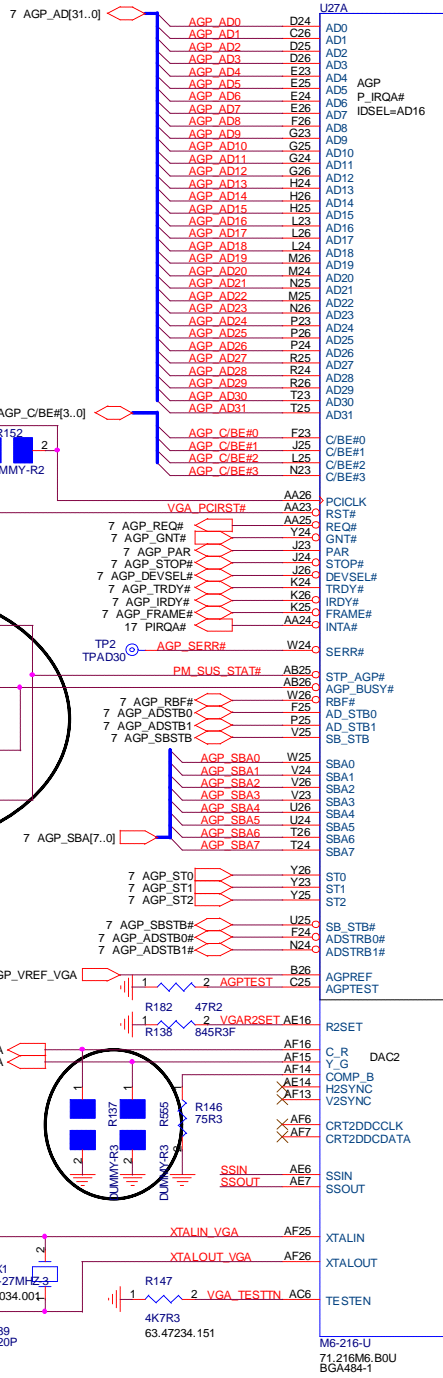
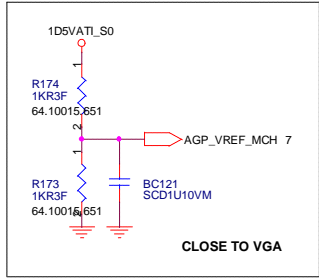
PLACE CAPS BETWEEN AND NEAR DDR SKTS  
 PLACE EACH 0.1UF CAP CLOSE TO POWER PIN



緯創資通

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Title		DDR Decoupling
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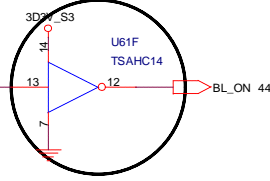


### SPREAD SPECTRUM SETTING

	SPECTRUM	NO SPECTRUM
SSIN	FLOATING	20KR2_0ND
SSOUT	FLOATING	20KR2_0ND
MK1705	MOUNT	DUMMY
R163	33R3	DUMMY
BCY1	SC1000P5V	DUMMY
SS_SEL0	TABLE	DUMMY
SS_SEL1	TABLE	DUMMY

SLEW	SLEW1	Spread %
0	0	1.25
1	0	0.5
0	1	test
1	1	1.0

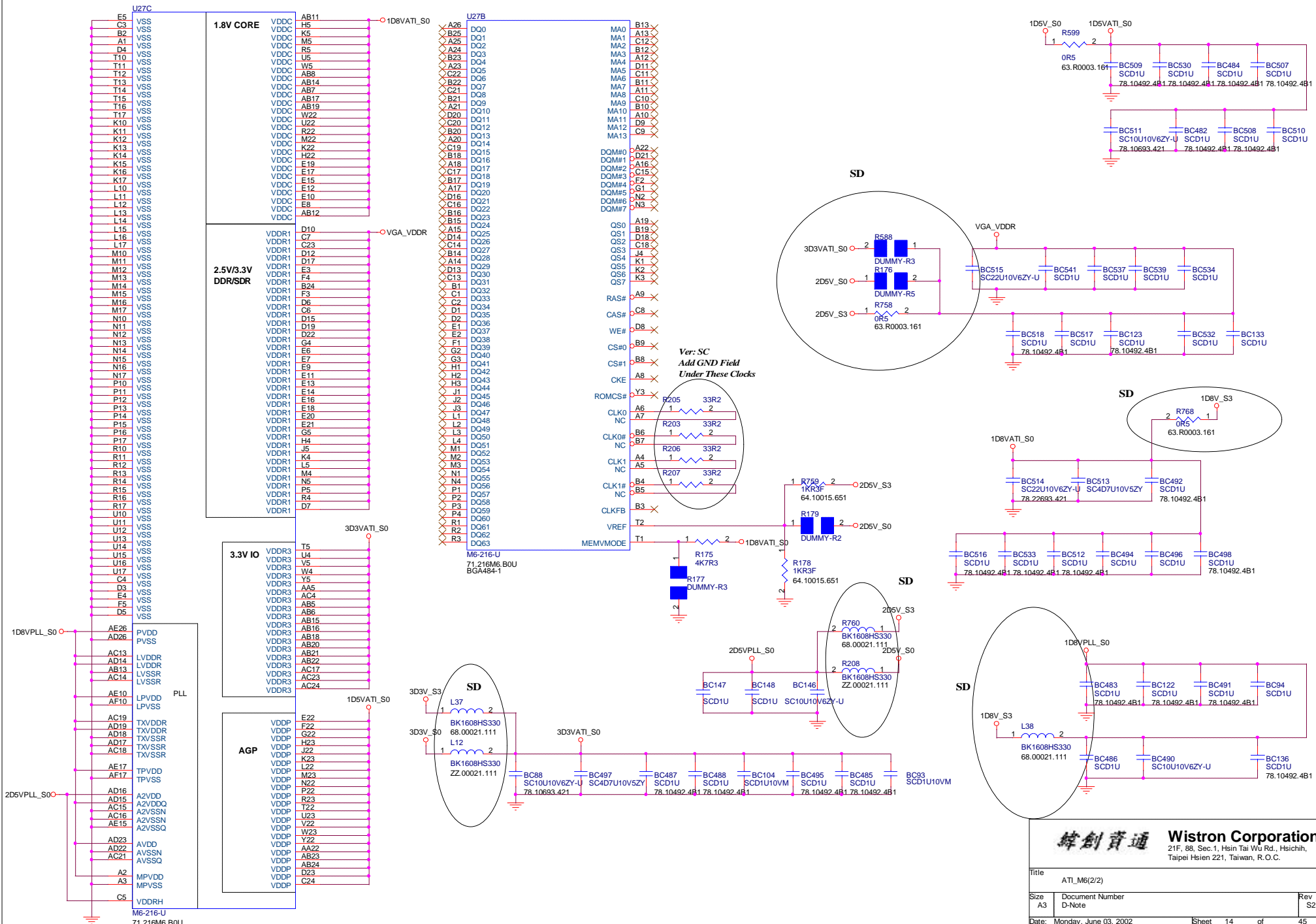
**ATI-M6C(8M) : 71.216M6.C0U**  
**ATI-M6C(16M) : 71.216M6.B0U**



*If D3(hot) is support,  
3D3VATI\_S0 is S3*

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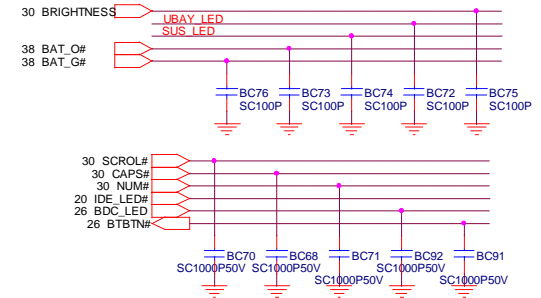
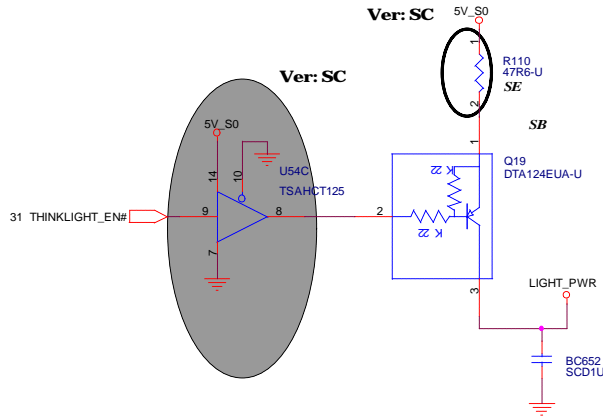
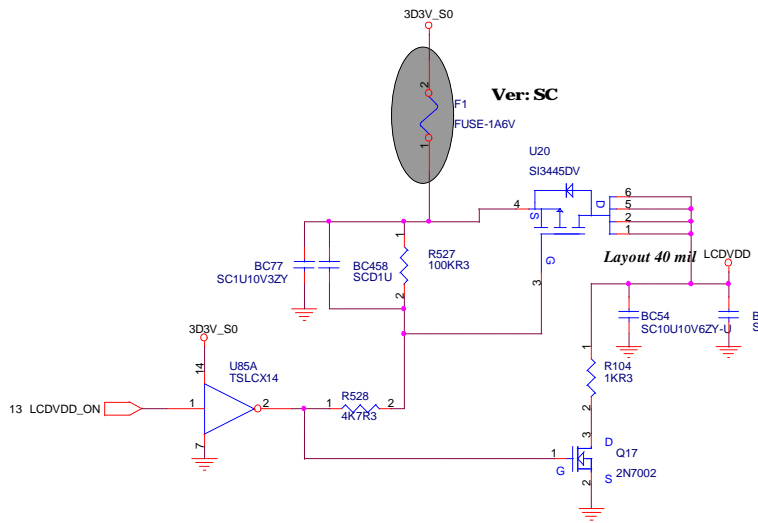
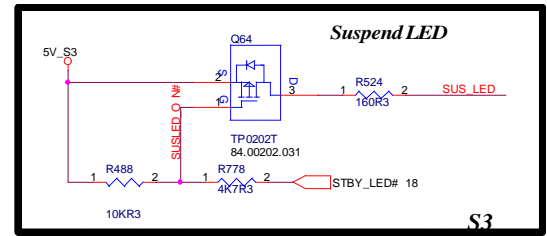
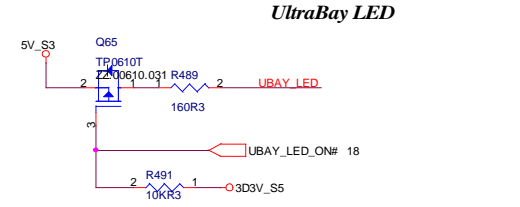
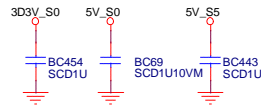
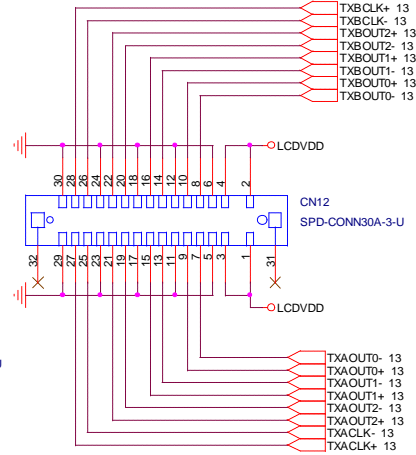
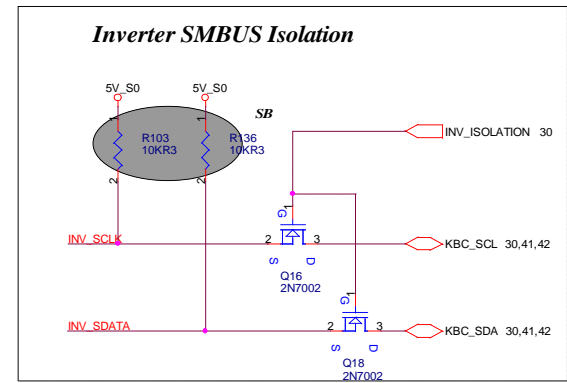
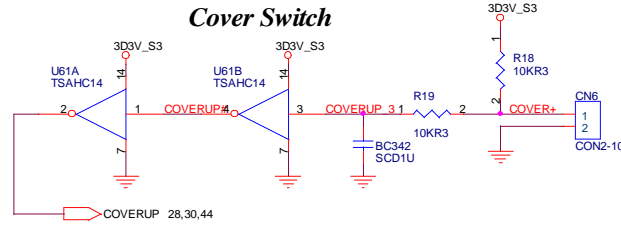
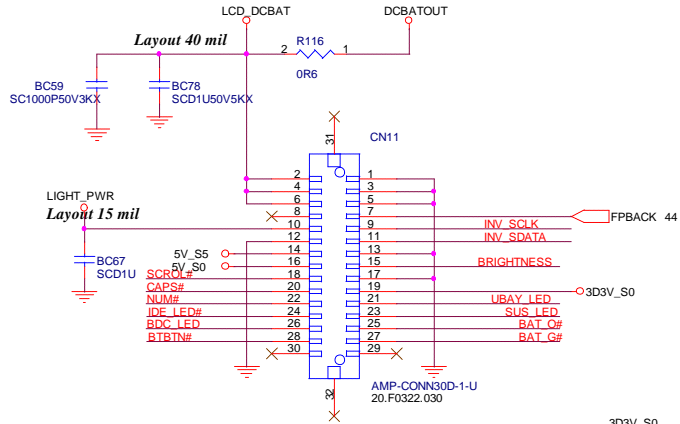
Title	ATI-M6 (1/2)	
Size	A3	Document Number D-Note
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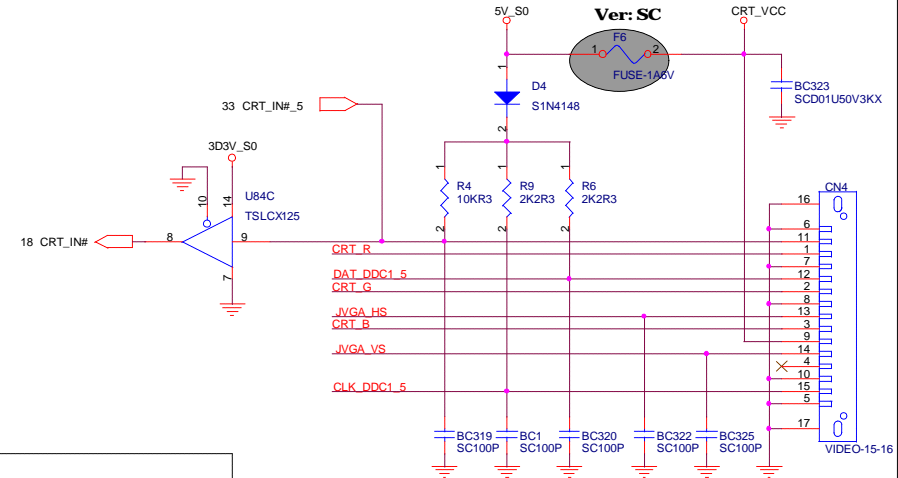
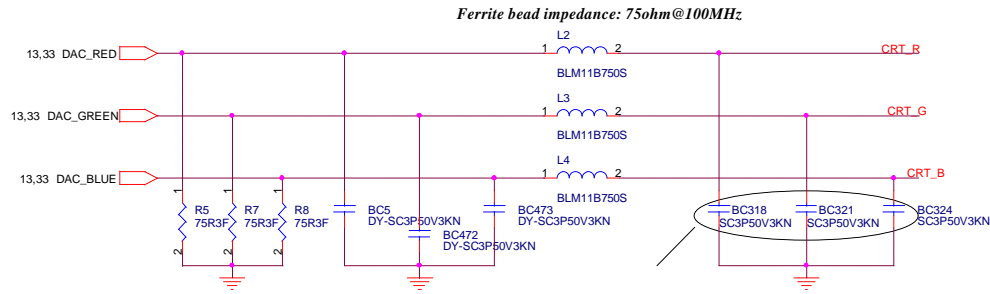

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Title ATL_M6(2/2)		
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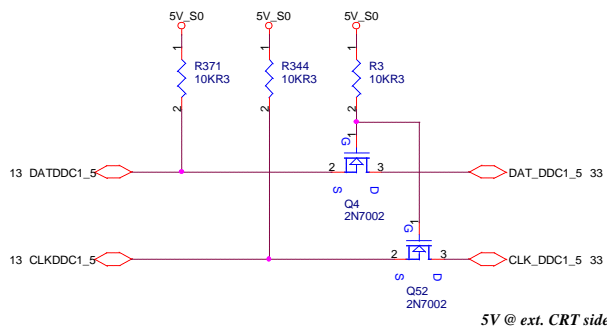
# LCD /INVERTER INTERFACE



# CRT I/F & CONN



## DDC\_CLK & DATA level shift



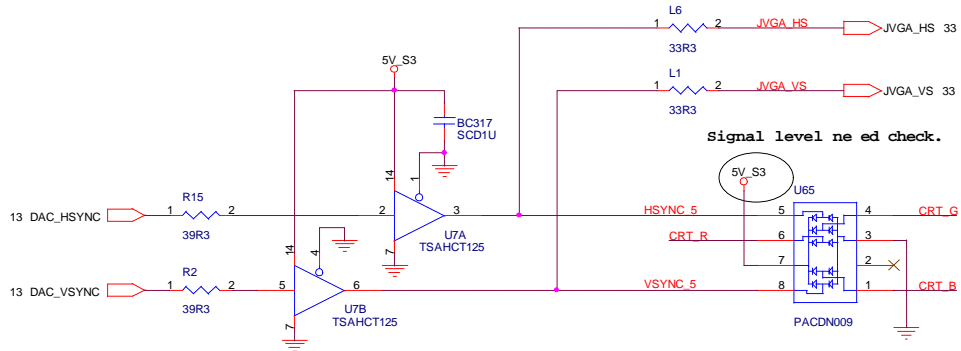
## Layout Note:

- \* Must be a ground return path between this ground and the ground on the VGA connector.
- \* 37.4\_1% resistors must be placed at the same place as the RGB 75 Ohm pull-down resistors.

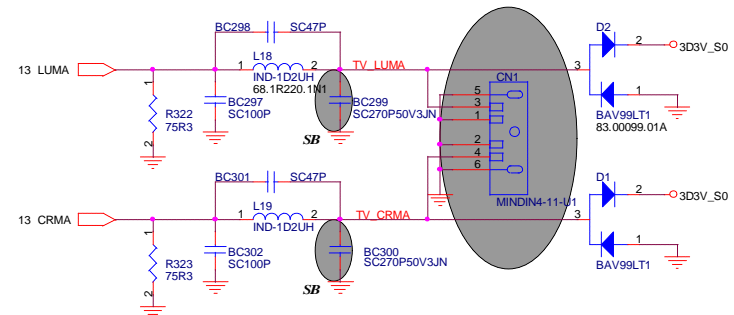
*Pi-filter & 75 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.*

RDDP 1.0

## Hsync & Vsync level shift



## Geometry Change from 440453-1-U1 --> 440453-1-U2

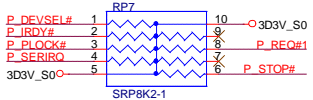


**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

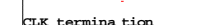
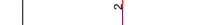
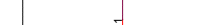
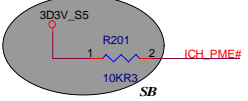
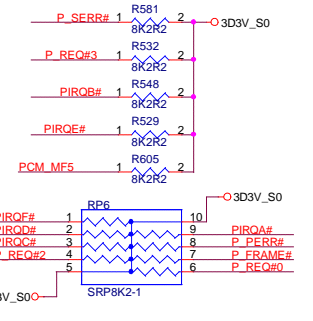
Title TV/CRT Connector		
Size A3	Document Number D-Note	Rev S2
Date: Monday, June 03, 2002	Sheet 16	of 45



### Interrupt I/F Pullups



### PCI I/F Pullups

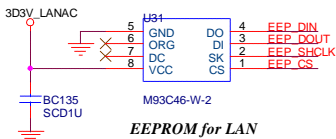
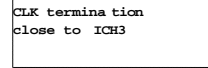


22,24,25 P\_AD[0..31]  
22,24,25 P\_C/BE[0..3]

### ICH3-M

U84A ICH3-M-U 71.0ICH3.M03	P_AD0 J2 PCI AD0	P_AD1 K1 PCI AD1	P_AD2 J4 PCI AD2	P_AD3 K3 PCI AD3	P_AD4 H5 PCI AD4	P_AD5 K4 PCI AD5	P_AD6 H3 PCI AD6	P_AD7 L1 PCI AD7	P_AD8 L2 PCI AD8	P_AD9 G2 PCI AD9	P_AD10 L4 PCI AD10	P_AD11 M4 PCI AD11	P_AD12 M4 PCI AD12	P_AD13 J3 PCI AD13	P_AD14 M5 PCI AD14	P_AD15 J1 PCI AD15	P_AD16 F5 PCI AD16	P_AD17 N2 PCI AD17	P_AD18 G4 PCI AD18	P_AD19 P2 PCI AD19	P_AD20 G1 PCI AD20	P_AD21 P1 PCI AD21	P_AD22 F2 PCI AD22	P_AD23 P3 PCI AD23	P_AD24 F3 PCI AD24	P_AD25 R1 PCI AD25	P_AD26 E2 PCI AD26	P_AD27 N4 PCI AD27	P_AD28 D1 PCI AD28	P_AD29 P4 PCI AD29	P_AD30 E1 PCI AD30	P_AD31 P5 PCI AD31	
	P_C/BE#0 K2 PCI C/BE#0	P_C/BE#1 K5 PCI C/BE#1	P_C/BE#2 N1 PCI C/BE#2	P_C/BE#3 R2 PCI C/BE#3																													
	P_GNT#0 A4 PCI GNT#0	P_GNT#1 E3 PCI GNT#1	P_GNT#2 D2 PCI GNT#2	P_GNT#3 B4 PCI GNT#3	P_GNT#4 B4 PCI GNT#4																												
	P_REQ#0 D3 PCI REQ#0	P_REQ#1 F4 PCI REQ#1	P_REQ#2 A3 PCI REQ#2	P_REQ#3 R4 PCI REQ#3	P_REQ#4 E4 PCI REQ#4																												
	22,24,25 P_DEVSEL# M3 PCI DEVSEL#	22,24,25 P_FRAME# F1 PCI FRAME#	22,24,25 P_IRQA# D4 PCI GPIO0/REQA#	22,24,25 P_IRQB# B3 PCI GPIO1/REOB#/REQB#	22,24,25 P_IRQC# C5 PCI GPIO17/GNTB#/GNTS#	22,24,25 P_IRQD# N3 PCI IRDY#	22,24,25 P_PERR# G6 PCI PERR#	22,25 ICH_PME# W1 PCI PME#	19 PCIRST#_3 L5 PCI RST#	22,24,25 P_SFERR# H2 PCI SERR#	22,24,25 P_STOP# H2 PCI STOP#	22,24,25 P_TRDY# H1 PCI TRDY#																					

Part Number Change to 71.0ICH3.M01



### System Management I/F

SM_INTRUDER# Y6	INTRUDER# 42
SMLINK0 AC3	SMLINK0
SMLINK1 AB2	SMLINK1
SMB_CLK AC4	SMB_CLK
SMB_DATA AB5	SMB_DATA
SMB_ALERT#/GPIO11 AC5	SMB_ALERT#/GPIO11

CPU_A20GATE Y22	ICH_A20GATE 30
CPU_A20M# V23	CC_A20M# 4
CPU_DPLSP# AB22	CC_DPLSP# 3,4,6
CPU_FERR# J22	CC_FERR# 4
CPU_IGNNE# AB23	CC_IGNNE# 4
CPU_INTR# AA21	CC_INTR# 4
CPU_NMI Y21	CC_NMI 4
CPU_PWRGOOD W23	CC_CPUPWRGD 4
CPU_RCIN# W21	CC_RCIN# 30
CPU_SLP# Y23	CC_SLP# 4
CPU_SMI# Y23	CC_SMI# 4
CPU_STPCLK# U23	CC_STPCLK# 4

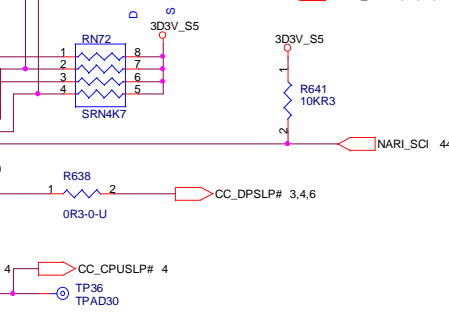
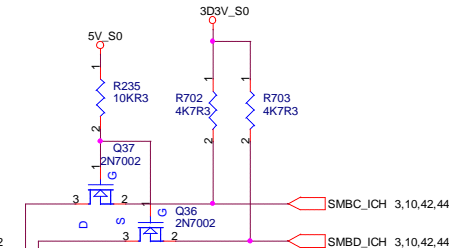
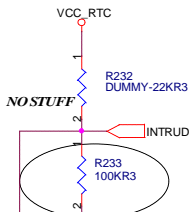
HUB_PD0 L22	HL_0
HUB_PD1 M21	HL_1
HUB_PD2 N20	HL_2
HUB_PD3 P21	HL_4
HUB_PD4 HUB_PD3	HL_5
HUB_PD5 HUB_PD4	HL_6
HUB_PD6 R20	HL_6
HUB_PD7 TP3	HL_7
HUB_PD8 M19	HL_8
HUB_PD9 P19	HL_9
HUB_PD10 N19	HL_10

CLK66 CLK66_ICH T19	CLK66_ICH
HUB_PAR R19	HUB_PAR
HL_STB# N22	HL_STB# 7
HL_STB# K19	HL_STB# 7
HUB_RCOMP L20	HUB_RCOMP ICH3
HUB_VREF L19	HUB_VSWING

INT_APICCLK J19	APICCLK_ICH
INT_APICD0 J20	APICD0
INT_APICD1 J21	APICD1
INT_PIRQA# B1	PIRQA# 13
INT_PIRQB# C1	PIRQB# 22
INT_PIRQC# A2	PIRQC# 25
INT_PIRQD# A6	PIRQD#
INT_PIRQA#/GPIO3 C5	PIRQA#/GPIO3
INT_PIRQB#/GPIO3 C5	PIRQB#/GPIO3
INT_PIRQC#/GPIO3 C5	PIRQC#/GPIO3
INT_PIRQD#/GPIO3 C5	PIRQD#/GPIO3
INT_IRQ14# AB14	IRQ14 20
INT_IRQ15# W19	IRQ15 20
INT_IRQ16# H22	IRQ16 20

EPPROM I/F	EPP_CS E9	EPP_CS
	EPP_DIN D8	EPP_DIN
	EPP_DOUT E8	EPP_DOUT
	EPP_SHCLK D10	EPP_SHCLK

LAN I/F	LAN_RXD0 C8	LAN_RXD0 21
	LAN_RXD1 A8	LAN_RXD1 21
	LAN_RXD2 A9	LAN_RXD2 21
	LAN_RXD3 B9	LAN_RXD3 21
	LAN_TXD0 C10	LAN_TXD0 21
	LAN_TXD1 A10	LAN_TXD1 21
	LAN_TXD2 A10	LAN_TXD2 21
	LAN_JCLK C9	LAN_JCLK
	LAN_RSTSYNC D7	LAN_RSTSYNC 21



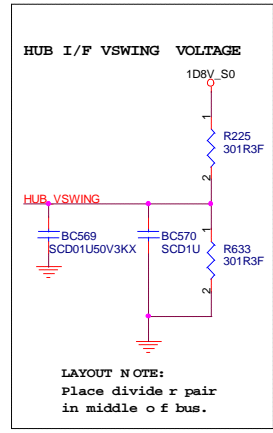
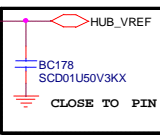
#### HUB INTERFACE LAYOUT

Route signals with 5/20 trace/ space routing.  
Signals must match +/- 0.1" of HUB\_STB/STB# signals.

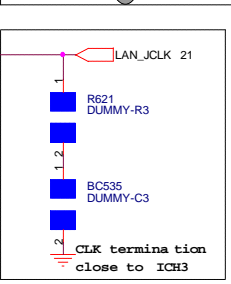
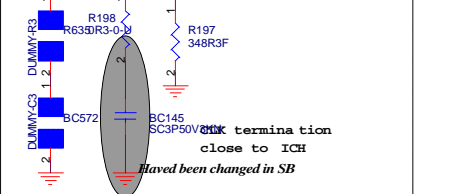
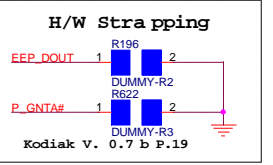
Kodiak Ver. 0.7

PLACE RCOMP resistor within 0.5" of ICH pad using a thick trace  
RCOMP should be 2/3 board impedance

SC-30 62

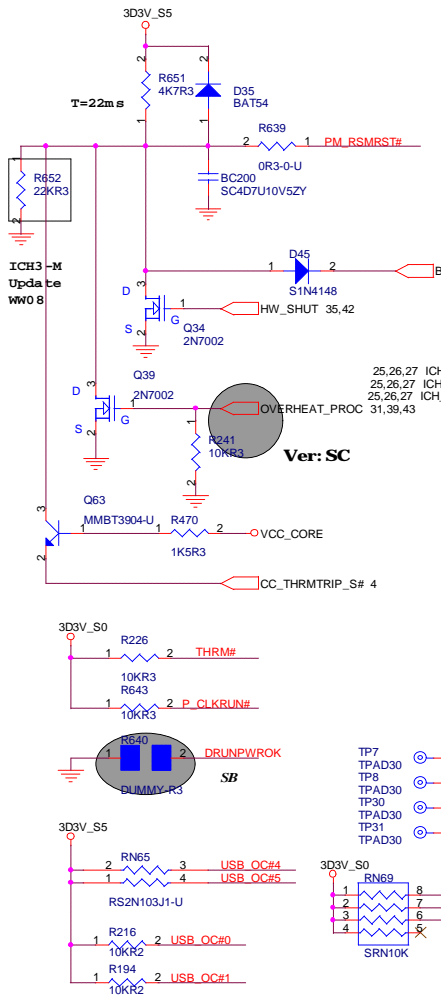


LAYOUT NOTE:  
Place divider pair in middle of bus.



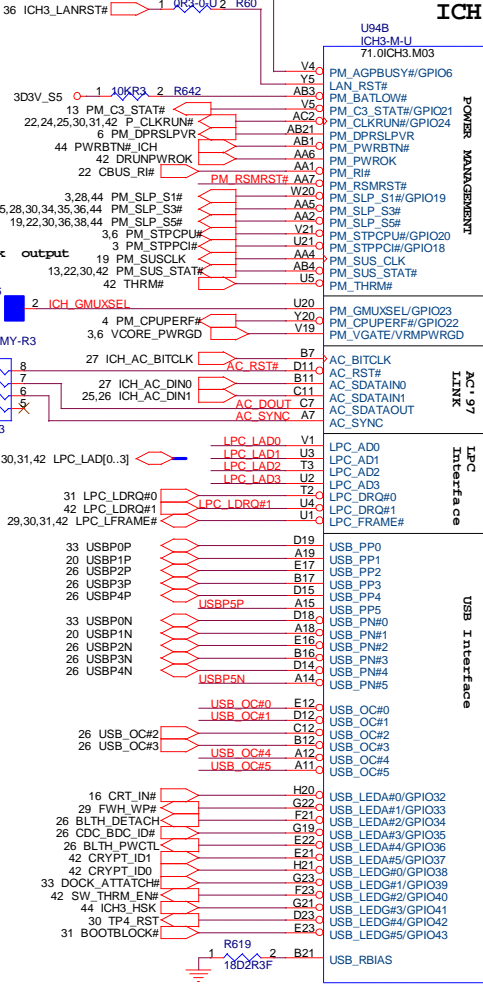
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**BIOS NOTE:**  
BIOS should disable PM\_STPCP U# on CK\_Titan.  
(Use H\_DPSLP# i nstead)

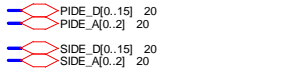
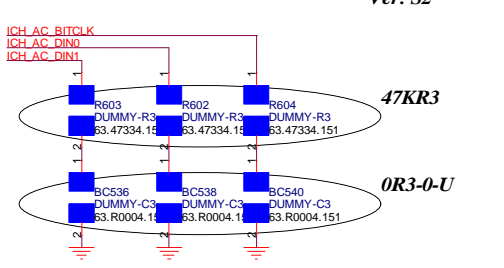


**ICH3 Integrated Pull-up and Pull-down Resistors**

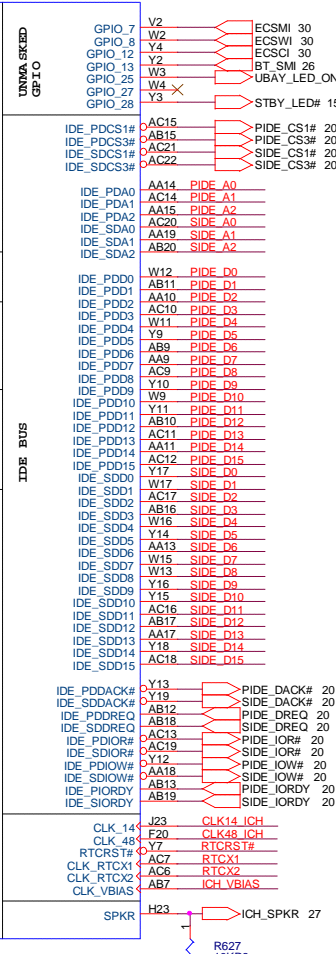
EE_DIN , EE_DOUT , LDRQ[1:0] , PME#	FM-1882 P 4-1,2
GNT[B:A]#/GNT[5]#/G PIO[17:16] , LAD[3:0]#/FWH [3:0]# , PWRBTN#	ICH3 internal 24K pull-ups
LAN_RXD[2:0]	ICH3 internal 9K pull-ups
AC_BITCLK , AC_SDIN[0] , AC_SDOUT , AC_SDIN[1] / GP IO[9] , AC_SYNC ,	ICH3 internal 20K pull-downs
SPKR	ICH3 internal 24K pull-downs
PDD[7]/SDD [7] , PDDREQ / SD DREQ	ICH3 internal 5.9K pull-downs
DPSLP VR	ICH3 internal TBD K pull-downs



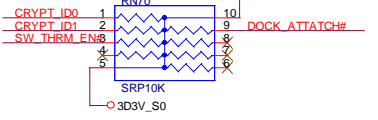
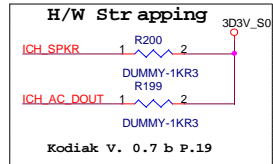
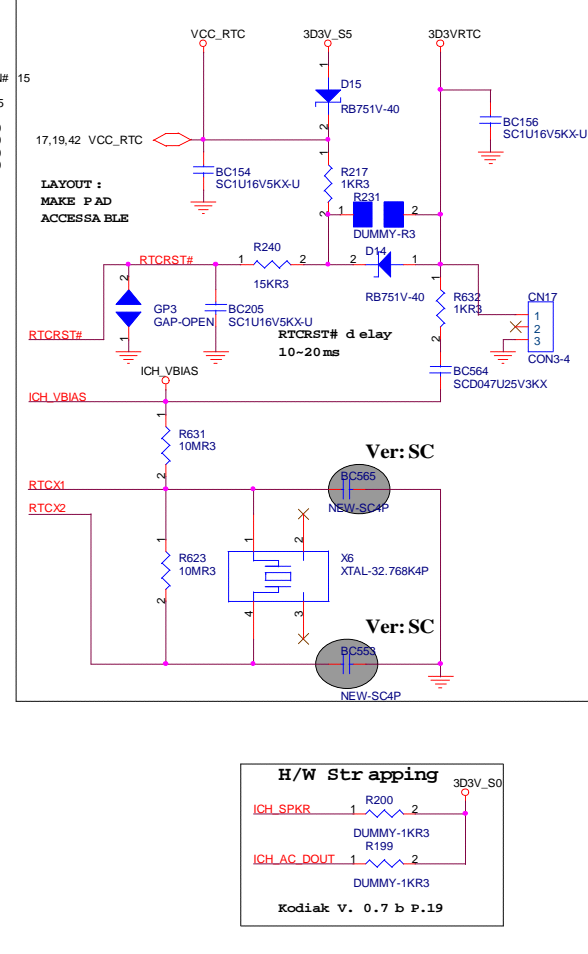
**AC97 AC terminations Ver: S2**



**ICH3-M**

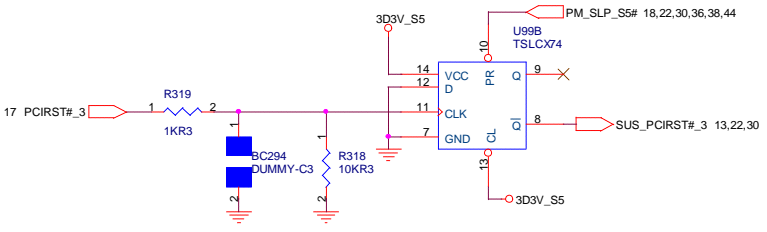
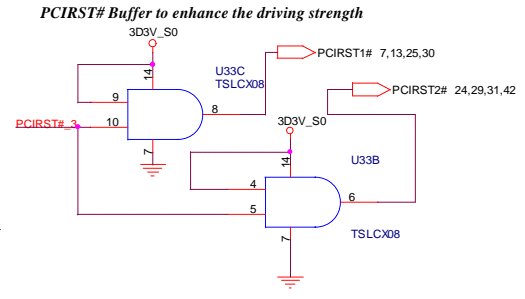
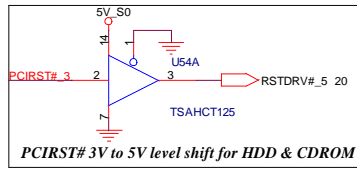
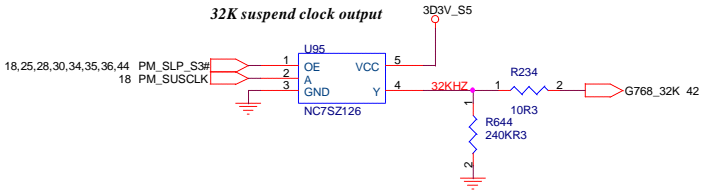
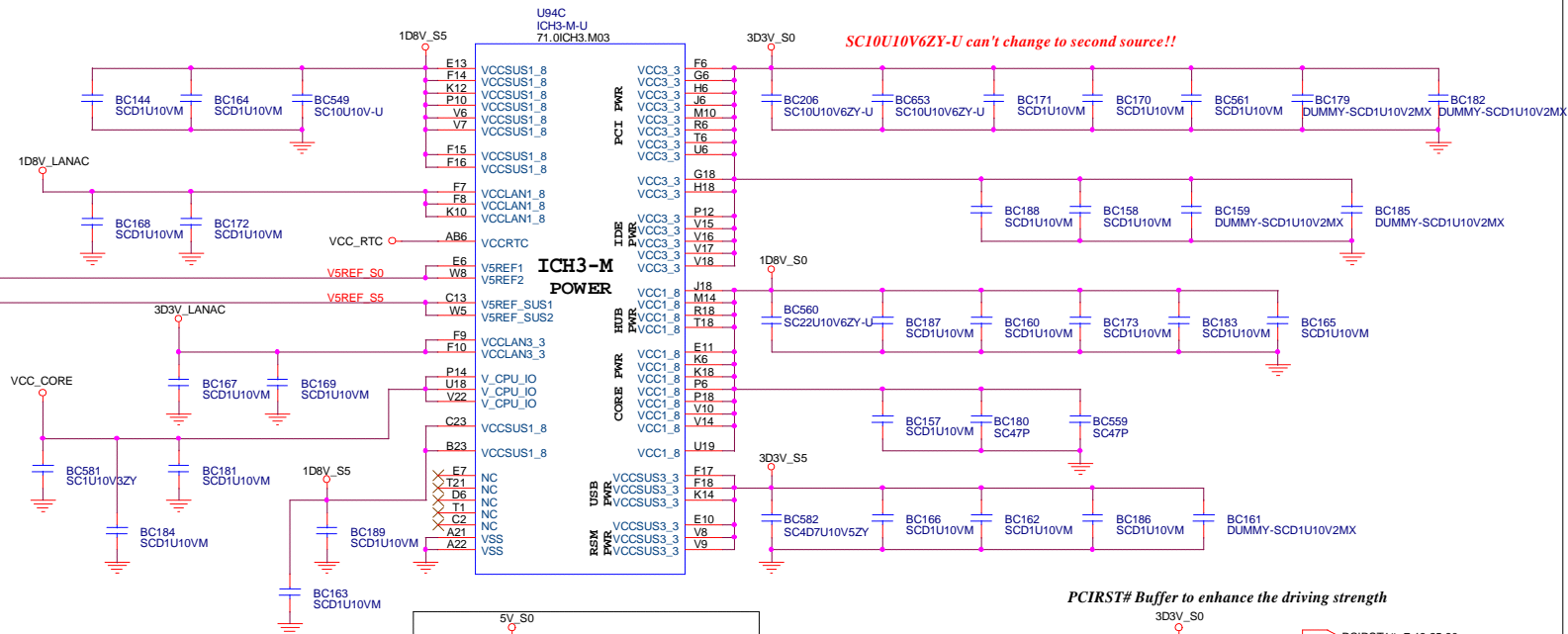
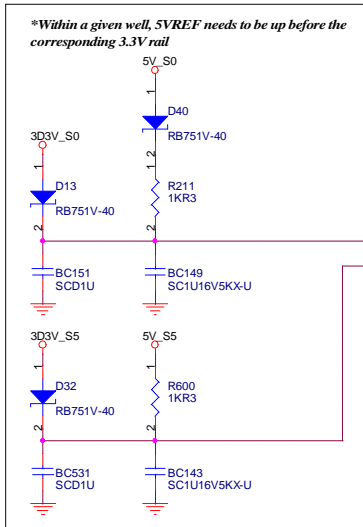


**RTC Circuitry**

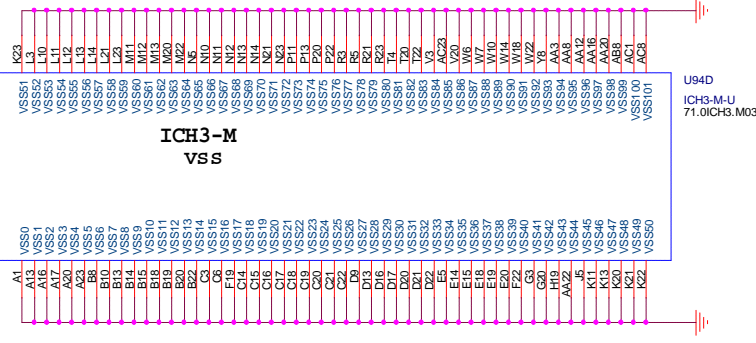


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Title: ICH3-M (2/3)  
Size: A3 Document Number: D-Note Rev: S2  
Date: Monday, June 03, 2002 Sheet: 18 of 45



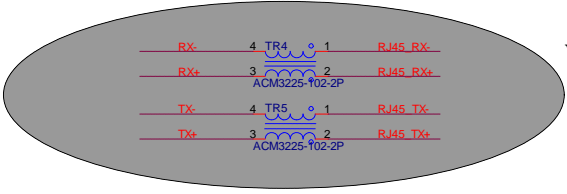
ICH3 H/W Pin Straps		FM-1882	
AC_SDOOUT	SAFE MODE	Rising Edge of PWR OK	This signal has a weak int. pull-down. If the signal is sampled high, the ICH3 will set the CPU speed strap pins for safe mode.
EE_DOUT	Reserved		System designers should include a placeholder for a pull-down resistor on EE_DOUT but do not populate the resistor.
GNT[A] #	TOP-SWAP OVERRIDE	Rising Edge of PWR OK	This signal has a weak int. pull-up. If the signal is sampled low, this indicates that the system is strapped to the "TOP-SWAP" mode (ICH3 will invert A16 for all cycles targeting FWH BIOS spacing). Note that SW will not be able to clear the Top-Swap bit until the system is rebooted w/o GNT[A]# being pulled down.
DPRS_LV	HUB INTERFACE TERMINATION SCHEME (PARALLEL vs. SOURCE)	Rising Edge of PWR OK	If this signal is sampled low (default due to weak int. pull-down), the termination scheme will be set to source. If this signal is sampled high (via an ext. pull-up to Vcc1_8), the termination scheme will be set to parallel.
SPKR	NO REBOOT	Rising Edge of PWR OK	This signal has a weak int. pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (ICH3 will disable the TXO Timer system reboot feature).



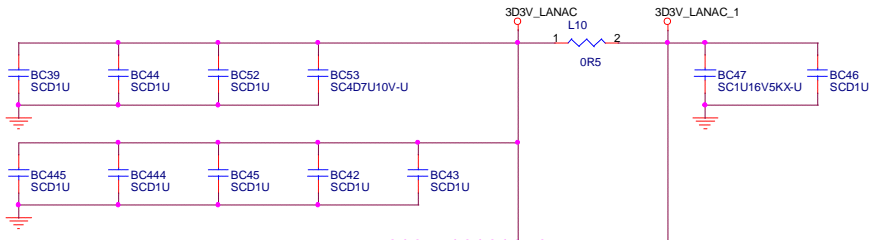
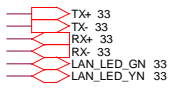
**Decoupling Recommendation**

Voltage	Capacitor Value	Capacitor Value	Capacitor Value
+1.5VRUN	0.1uF * 2	1uF / 16V * 1	Kenora Bulk X
1.8VRUN	0.1uF * 5	47pF * 2	100uF*1+22 uF*1
1.8VVSUS	0.1uF * 3		10uF * 1
1.8V_ICH LAN	0.1uF * 2		22uF * 1
3.3VRUN	0.1uF * 13	47pF * 5	22uF * 2
3.3VVSUS	0.1uF * 8		22uF * 1
3.3V_ICH LAN	0.1uF * 2		22uF * 1

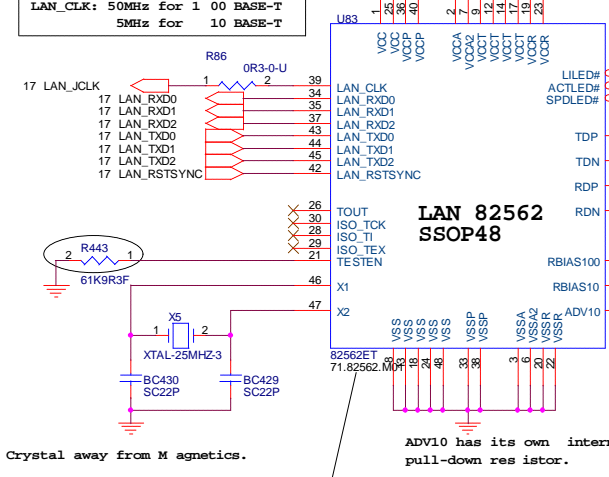




Ver: SC



LAN\_CLK: 50MHz for 1 00 BASE-T  
 5MHz for 10 BASE-T

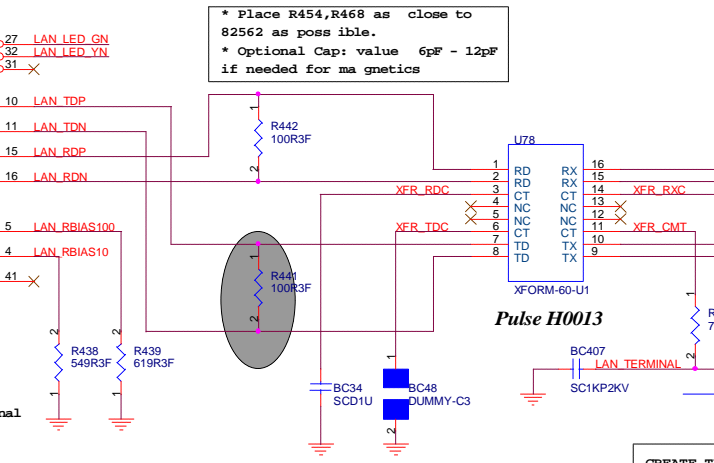


Crystal away from Magnetics.

Symbol is 82562EM,  
 Note 2 use it to replace 82562ET

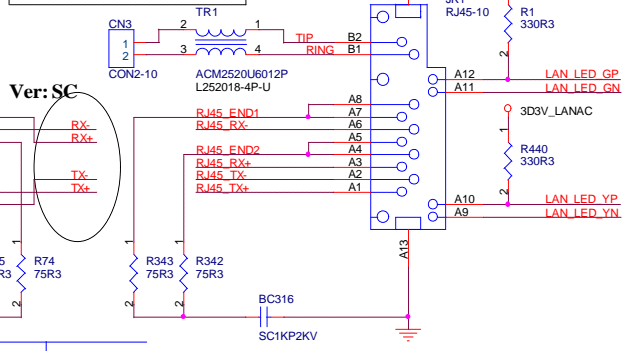
ADV10 has its own internal pull-down resistor.

\* Place R454, R468 as close to 82562 as possible.  
 \* Optional Cap: value 6pF - 12pF if needed for magnetics



For Modem Cable from MDC

Ver: SC

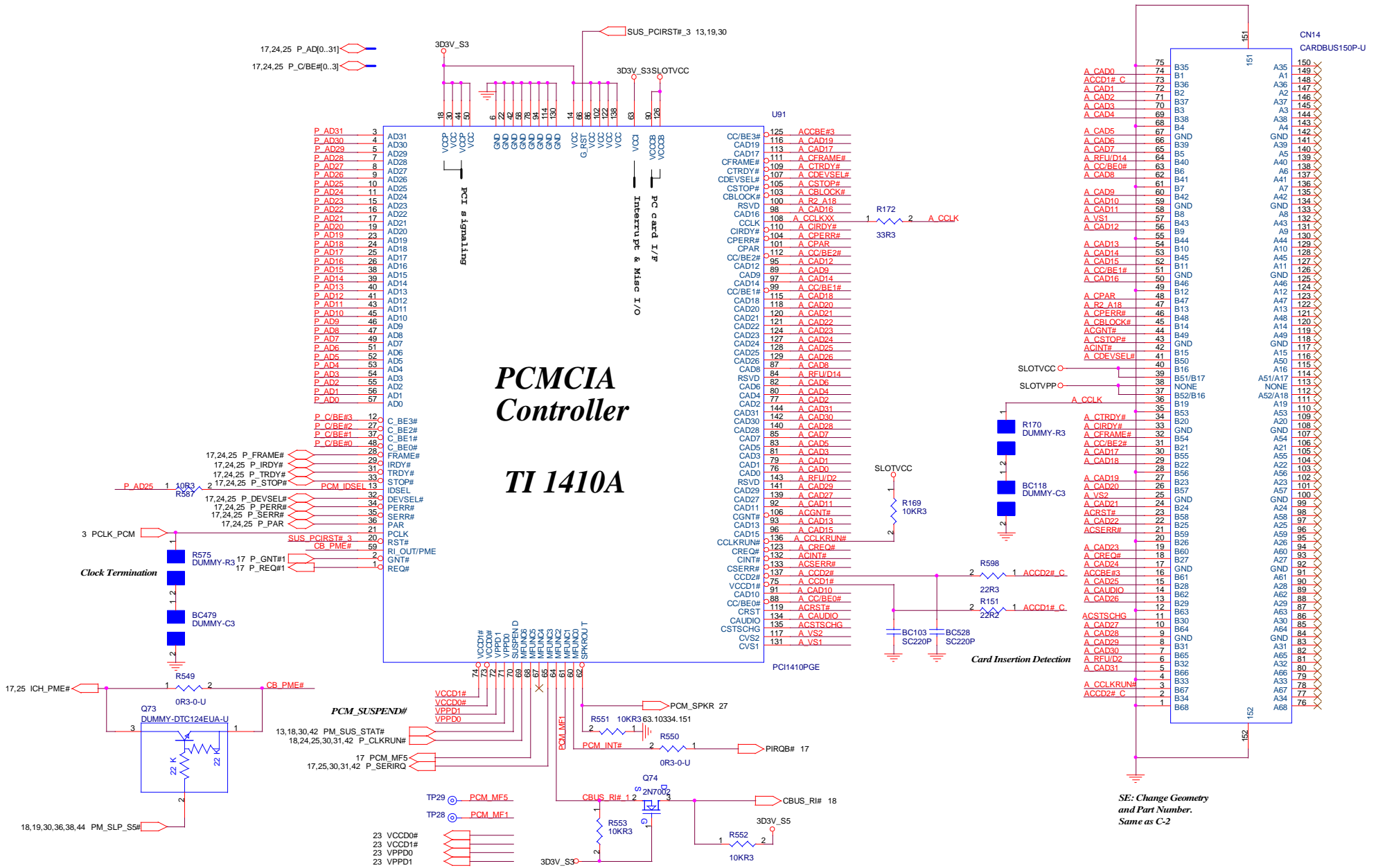


CREATE TERMINATION PLANE - 1500pF - reference to chassis GND

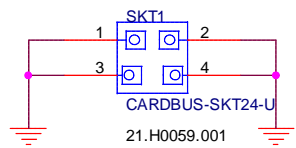
Chassis GND should cover part of magnetics

**Bob Smith Termination**  
 A floating termination plane is cut out from power plane layer which acts as a plane of capacitance with an adjacent ground plane.

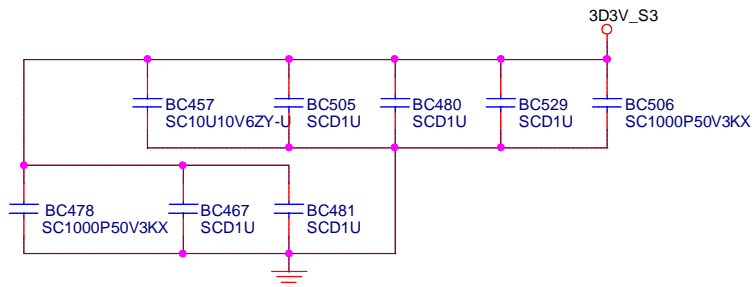
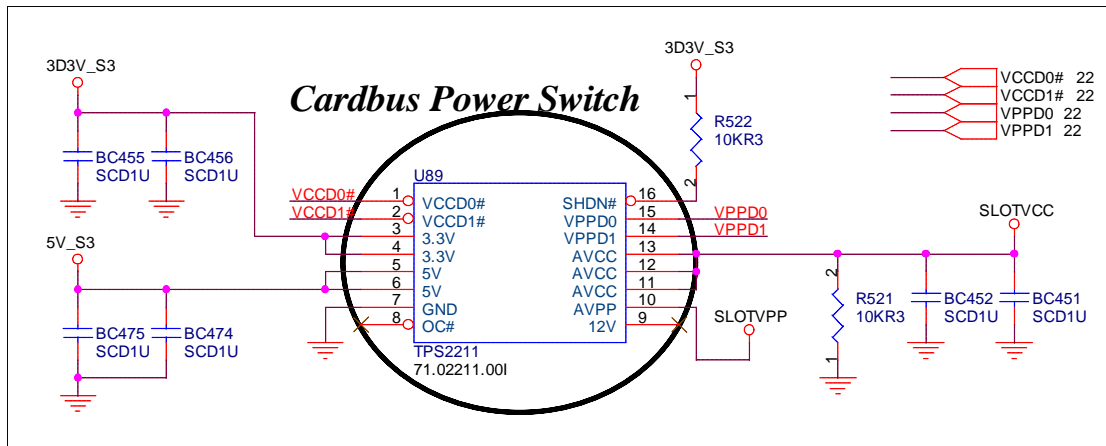
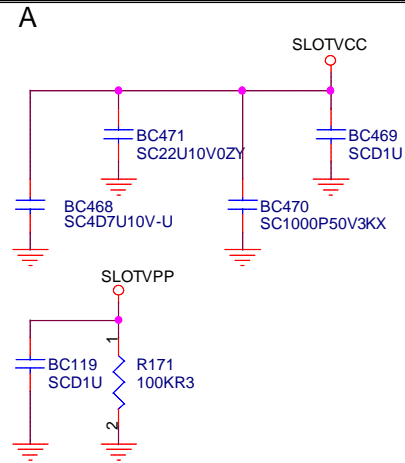
# PCMCIA Controller TI 1410A



SE: Change Geometry and Part Number. Same as C-2



### PCMCIA CAGE



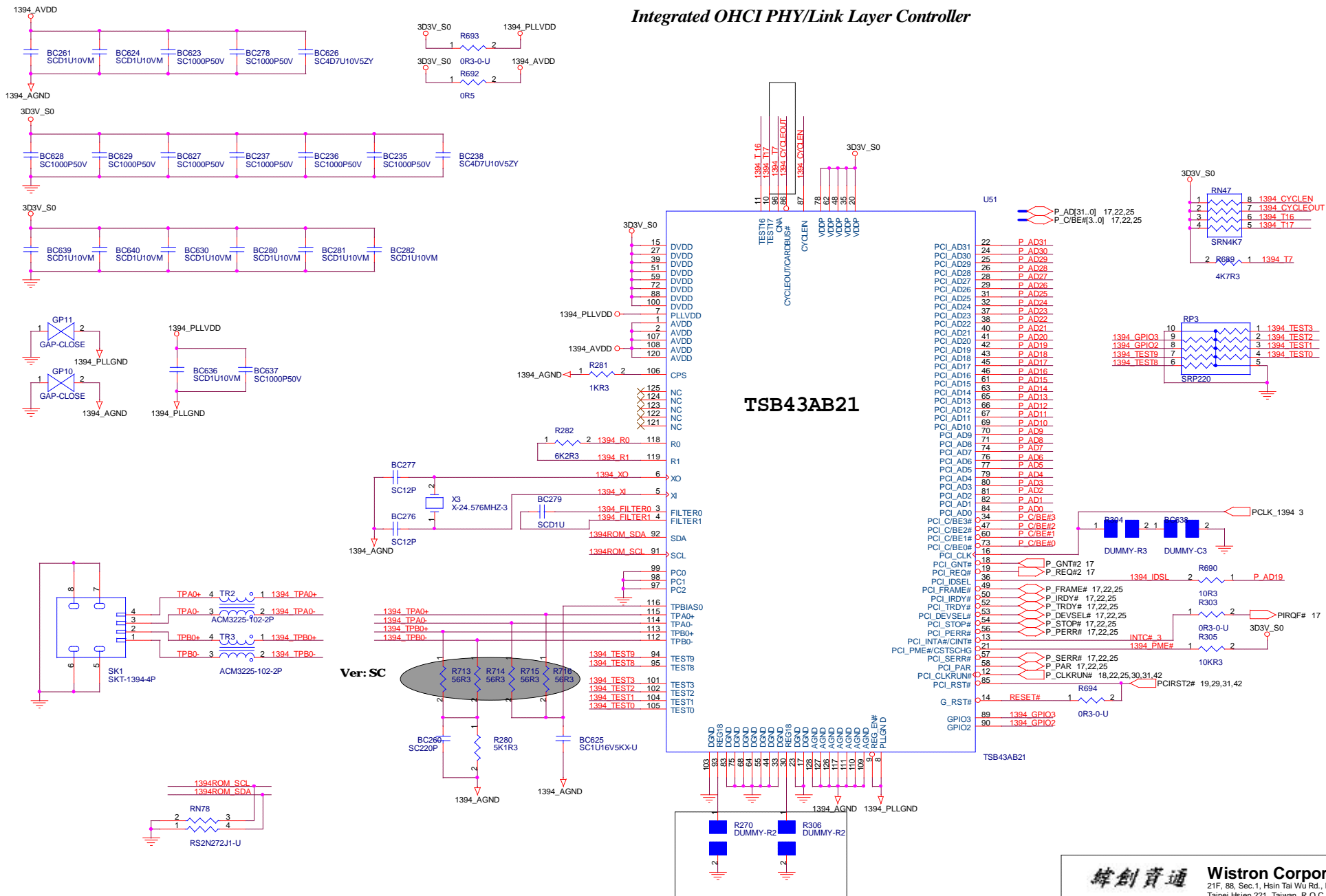
緯創資通

**Wistron Corporation**

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Taipei Hsien 221, Taiwan, R.O.C.

Title PCM Socket Power		
Size A4	Document Number D-Note	Rev S2
Date: Monday, June 03, 2002	Sheet 23	of 45

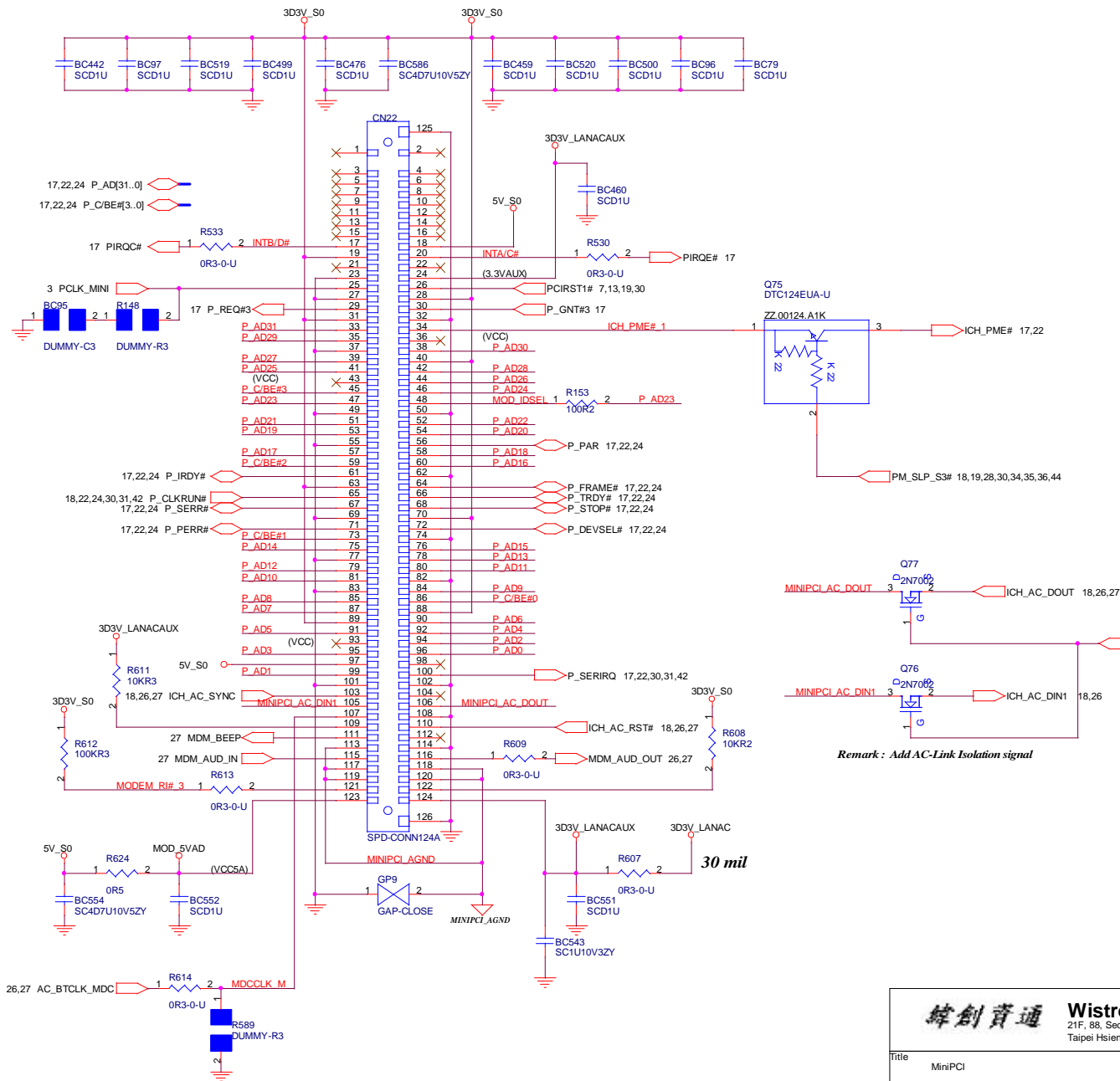
# Integrated OHCI PHY/Link Layer Controller





# MiniPCI Socket

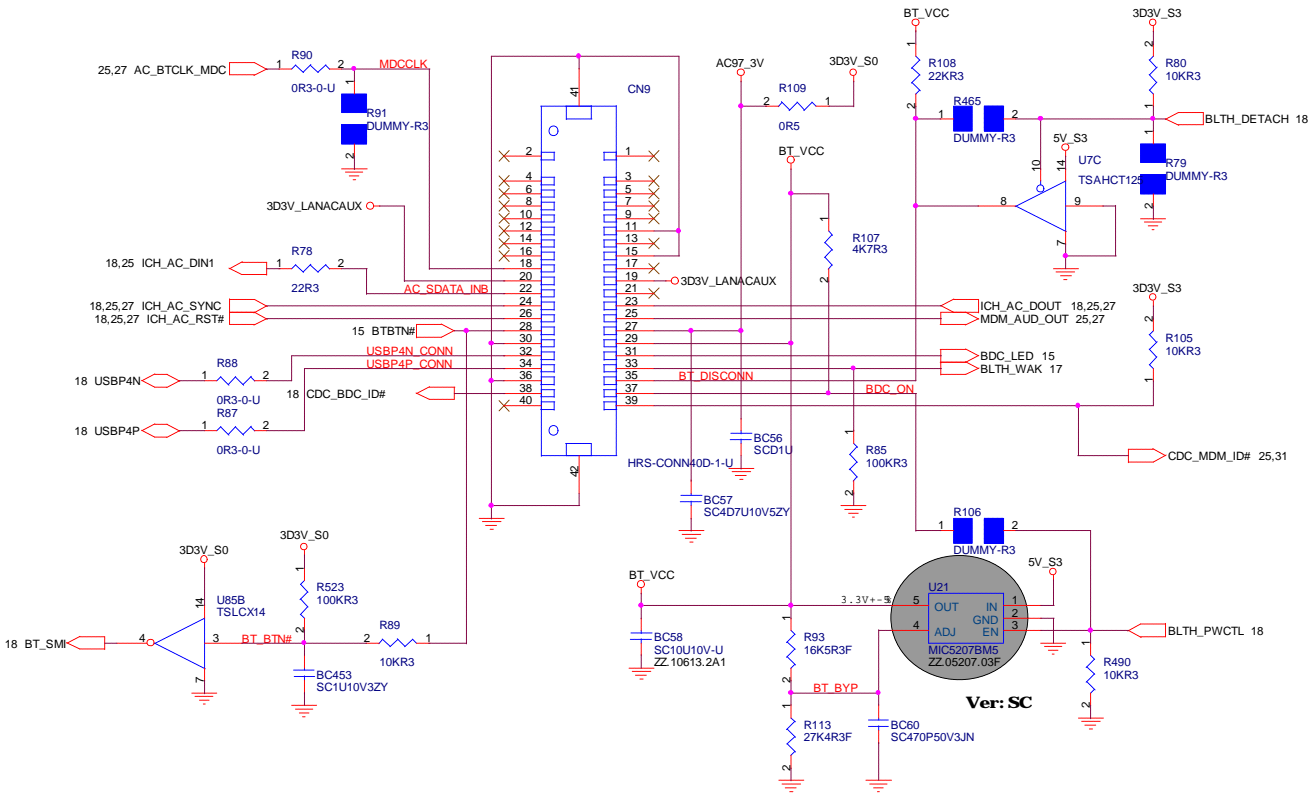
20.F0222.124 4/18



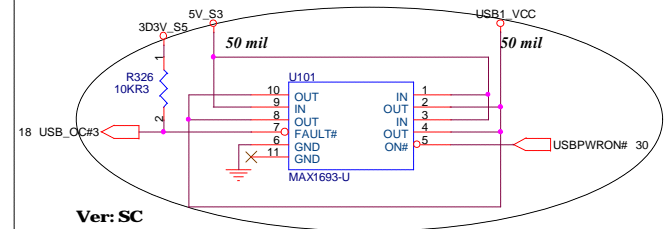
緯創資通 **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title	MiniPCI	
Size	Document Number	Rev
A3	D-Note	S2
Date:	Monday, June 03, 2002	Sheet 25 of 45

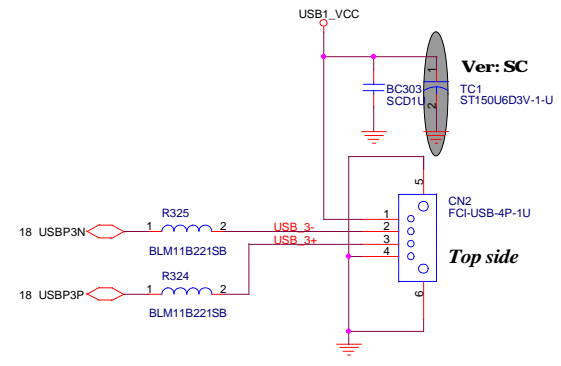
# CDC Connector



# USB PORT

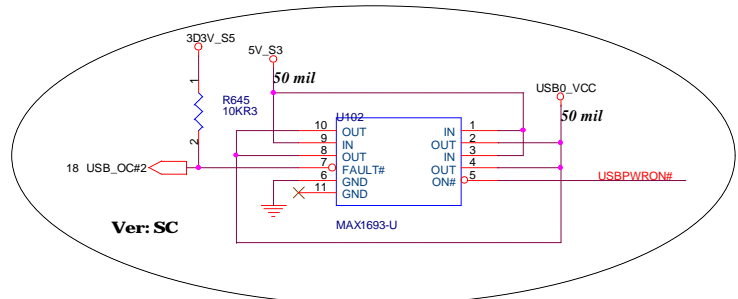


Ver: SC

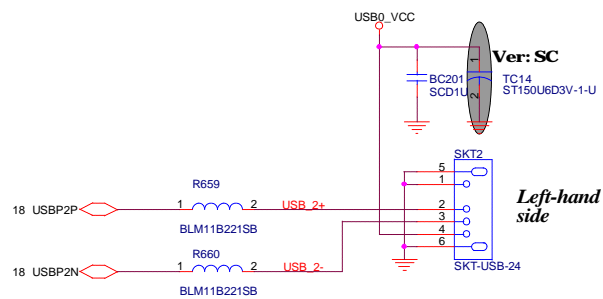


Ver: SC

Top side



Ver: SC



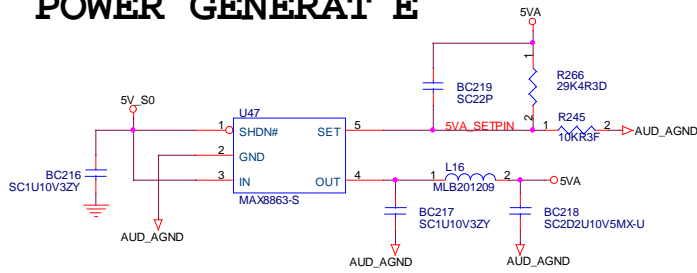
Ver: SC

Left-hand side

<b>緯創資通 Wistron Corporation</b>		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	USB and CDC I/F	
Size	Document Number	Rev
A3	D-Note	S2
Date:	Monday, June 03, 2002	Sheet 26 of 45

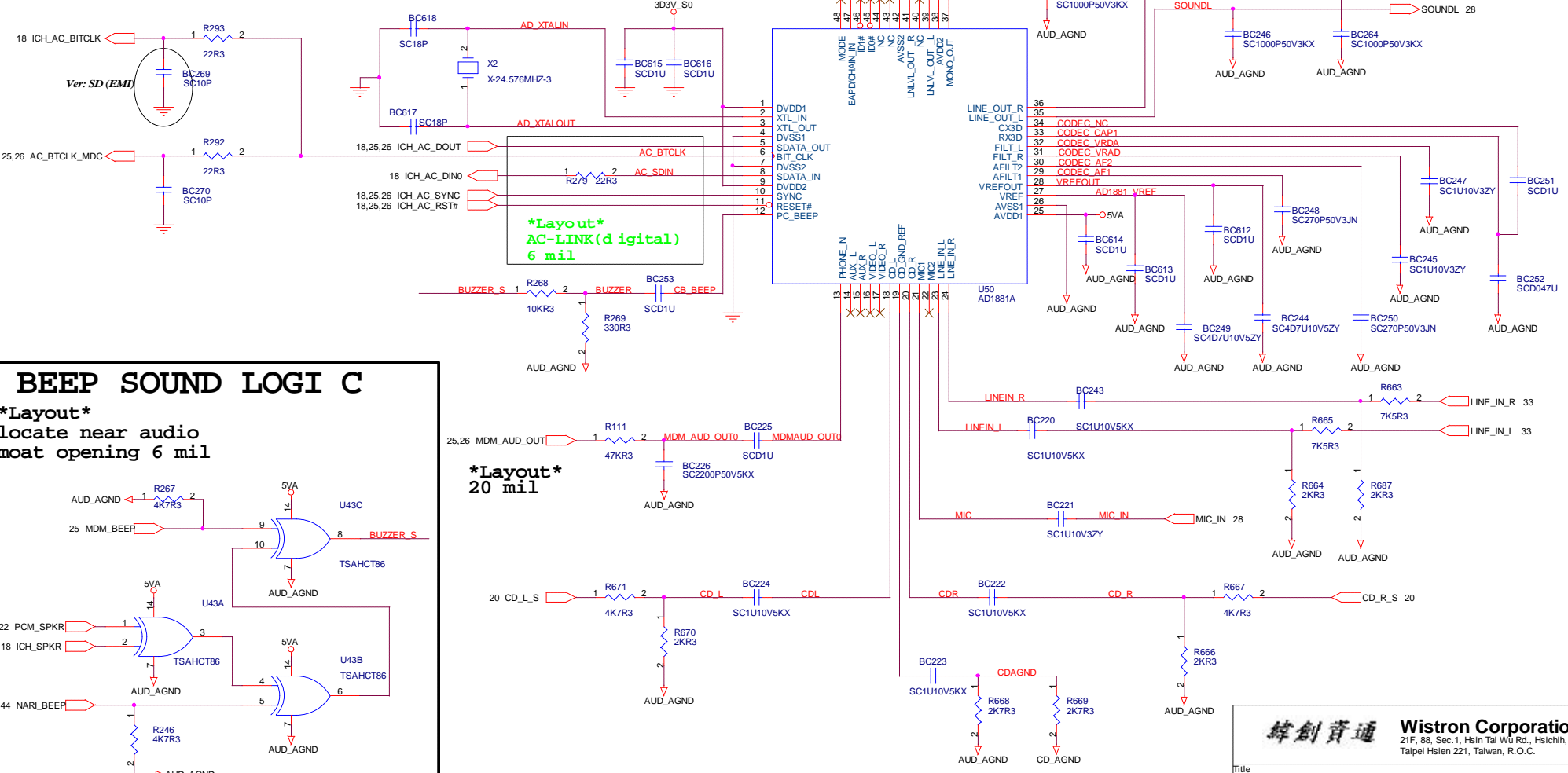
# POWER GENERAT E

**\*Layout\***  
20 mil



# AD1881A AC97 A UDIO CODEC

**\*Layout\***  
AUDIO(analog)  
(10,10) mil

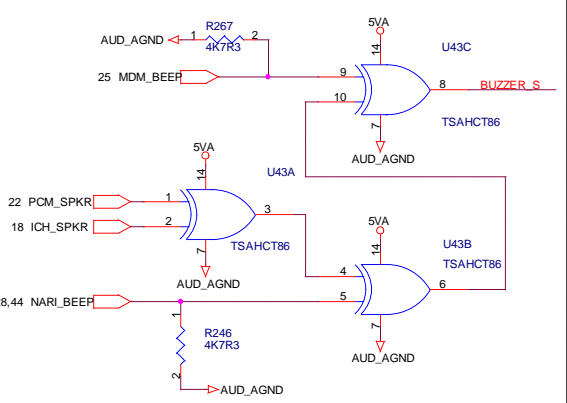


**\*Layout\***  
AC-LINK(d igital)  
6 mil

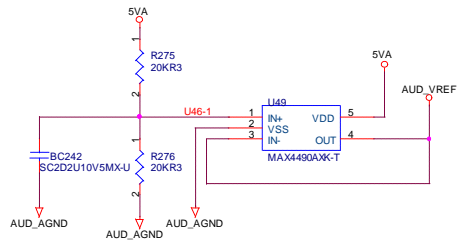
**\*Layout\***  
20 mil

## BEEP SOUND LOGI C

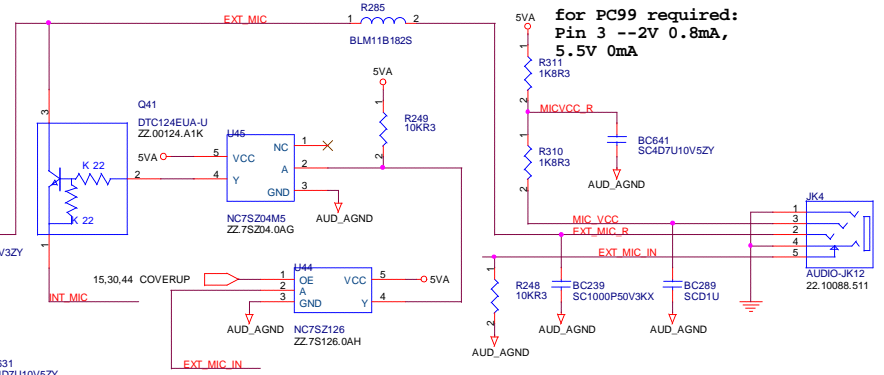
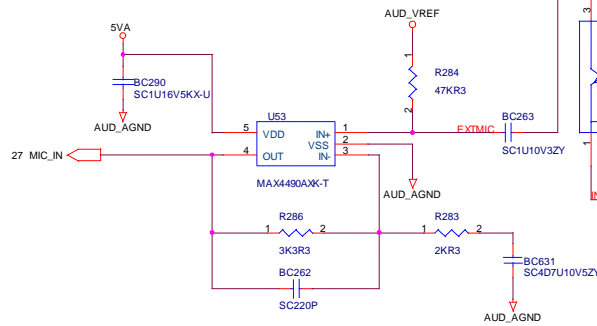
**\*Layout\***  
locate near audio  
moat opening 6 mil



# AUDIO VREF GENERATE

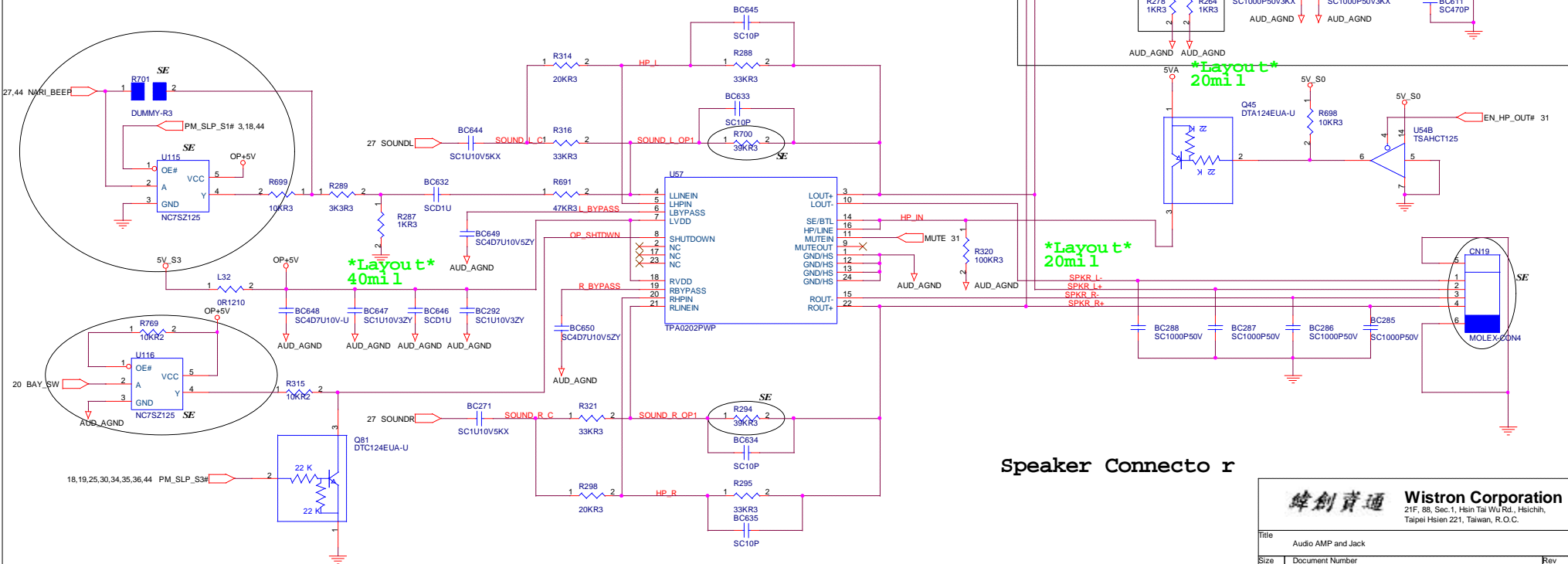


# EXT. MICROPHONE IN



for PC99 required:  
Pin 3 --2V 0.8mA,  
5.5V 0mA

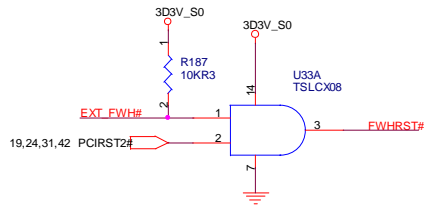
# AUDIO OP AMPLIFIER



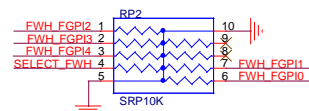
# Speaker Connector

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

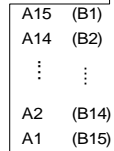
Title		Audio AMP and Jack
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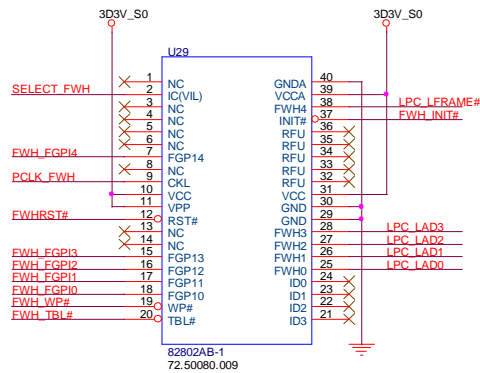
Unused FGPI pins must not be float



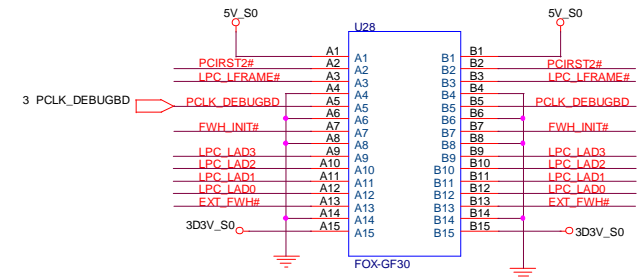
TOP VIEW



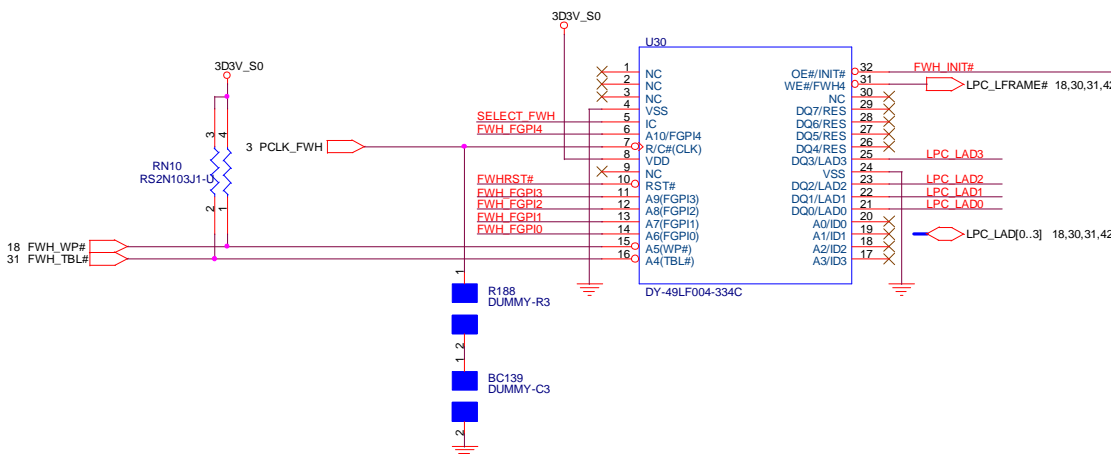
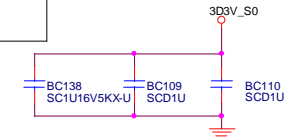
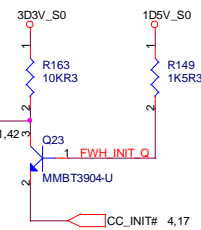
(BOTTOM VIEW)

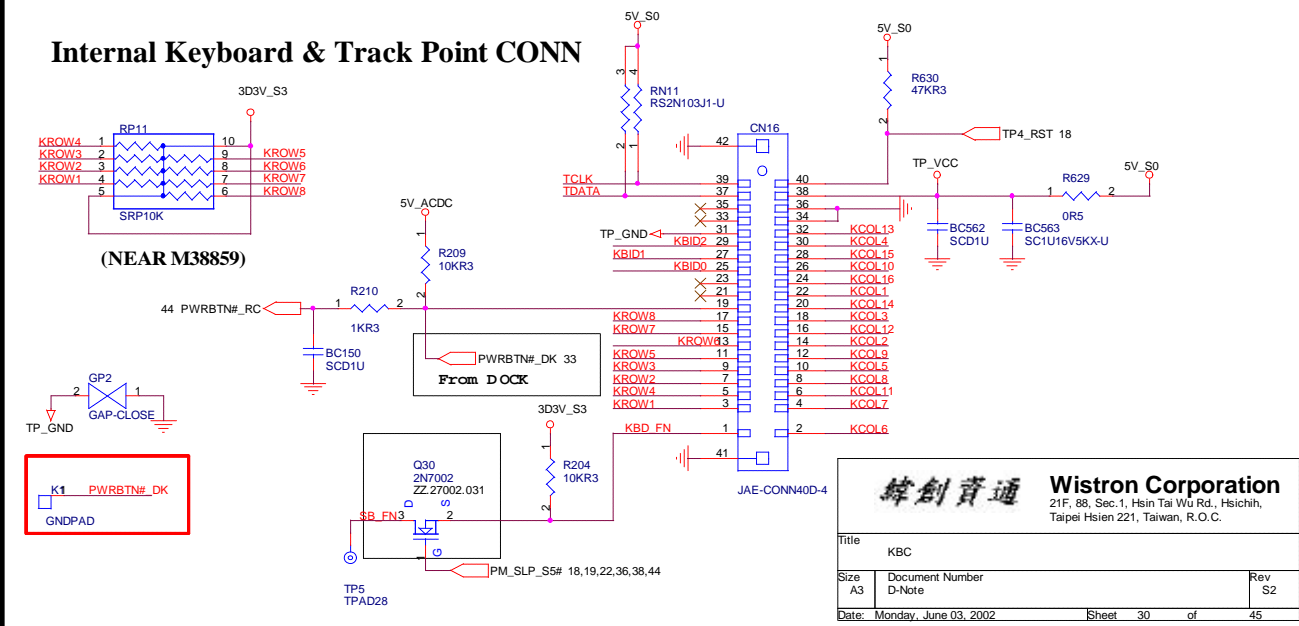
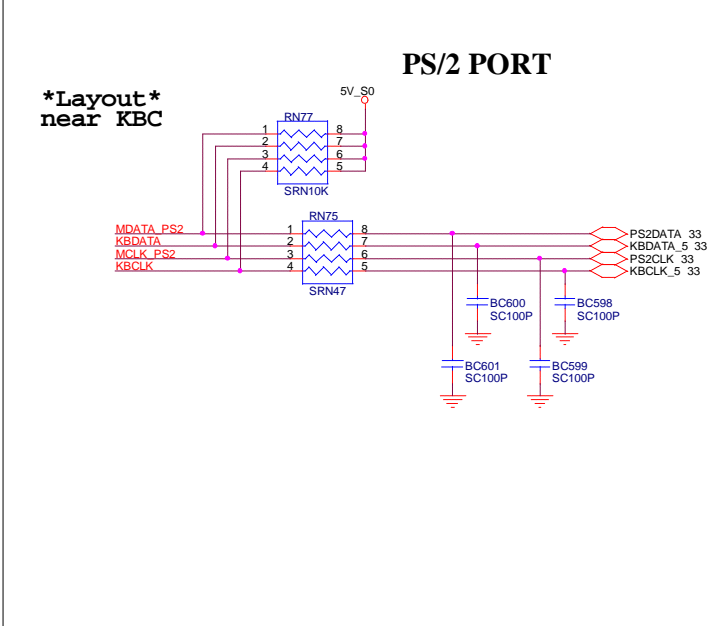
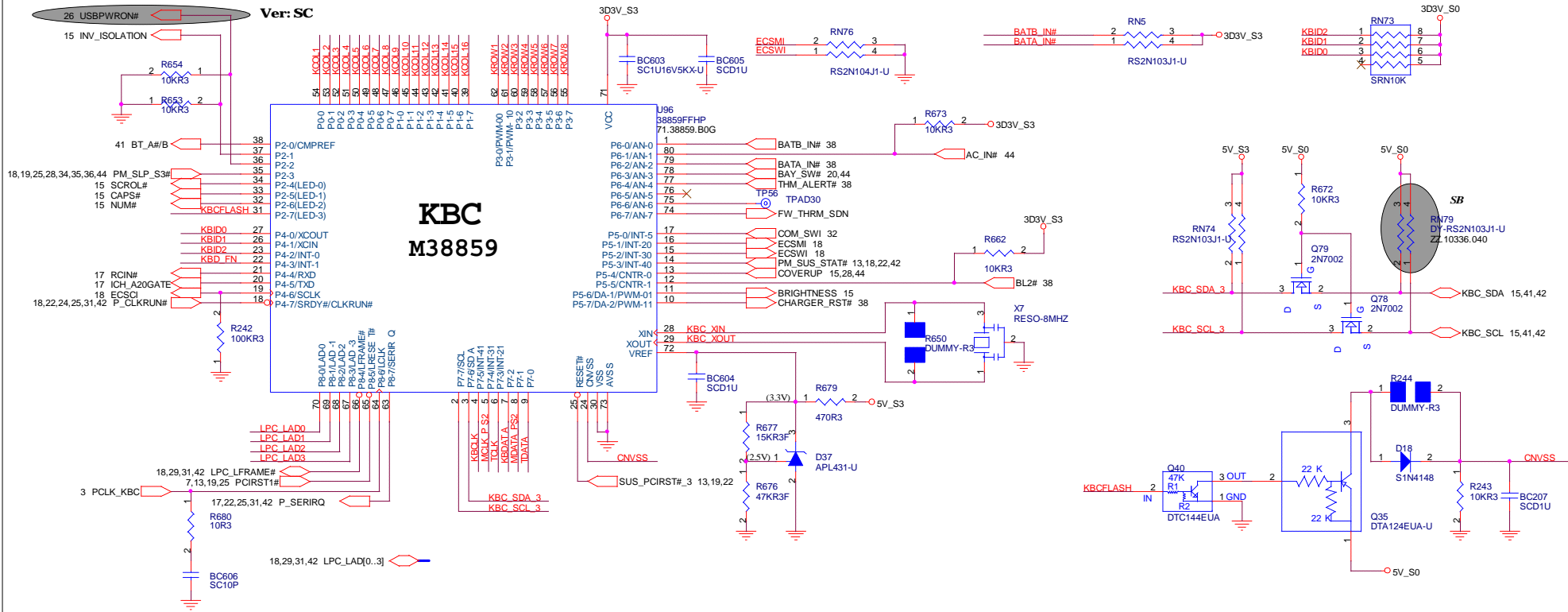


GOLDEN FINGER FOR DEBUG BOARD

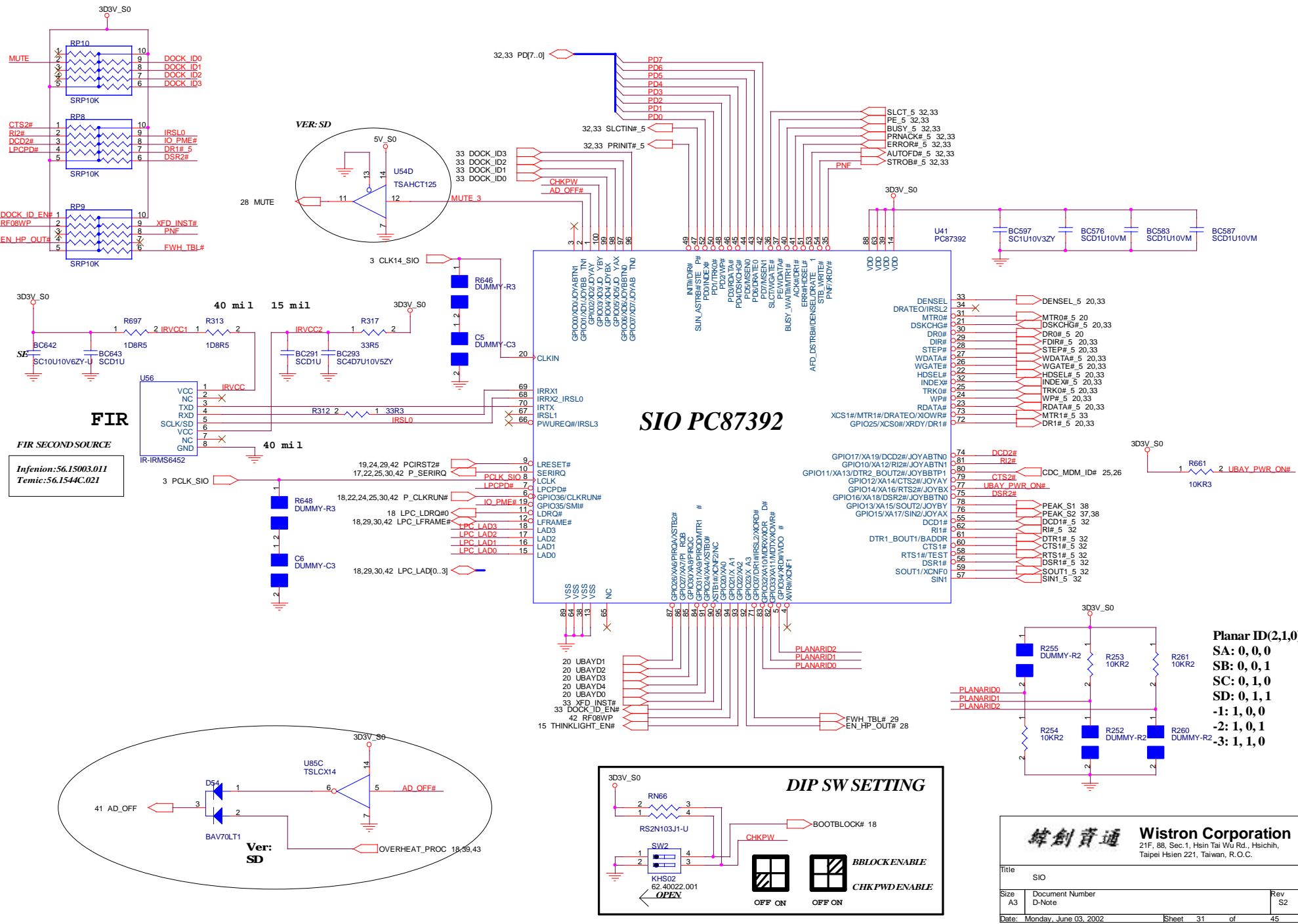


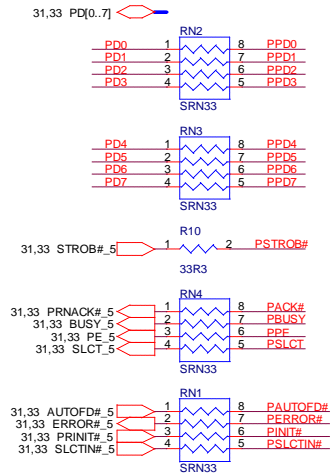
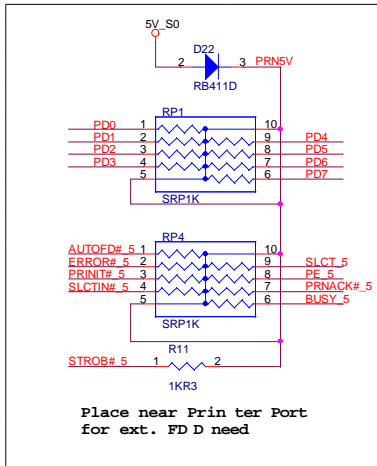
Boot Device must have ID [3:0] = 0000  
Has internal pull-down resistors  
All may be left floated  
FPET7 Elec. P3-46



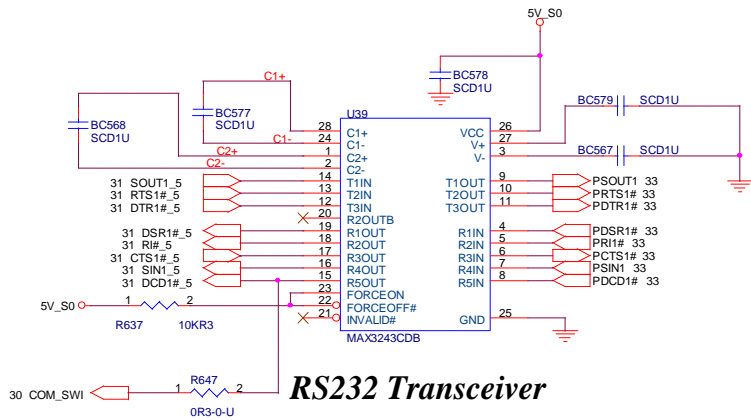
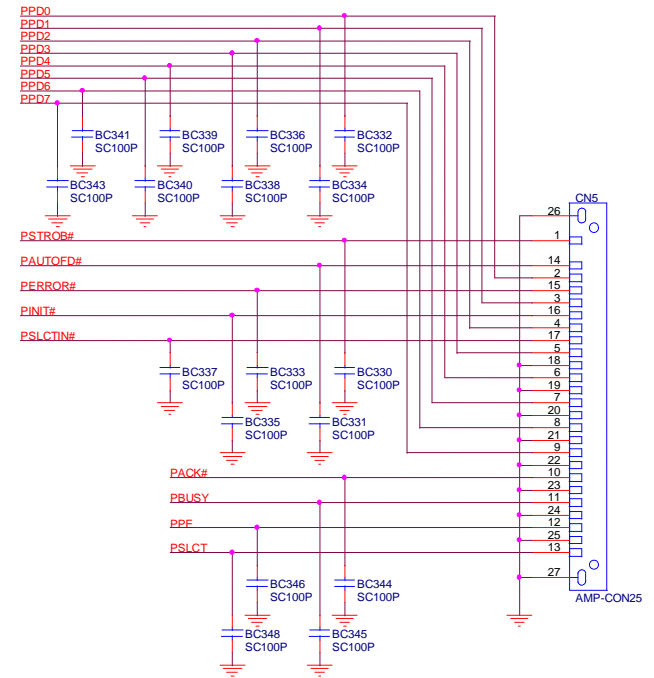


<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: KBC			
Size: A3	Document Number: D-Note	Rev: S2	
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### Printer Port



### RS232 Transceiver

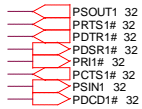
RS232 SECOND SOURCE

MAXIM:74.03243.0F9  
TI :74.03243.FF9

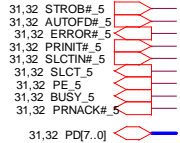
<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Serial/Parallel Port			
Size A3	Document Number D-Note	Rev S2	
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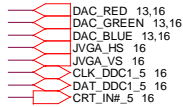
**SERIAL PORT I/F**



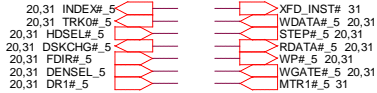
**LPT I/F**



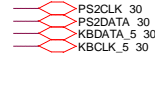
**CRT I/F**



**FDD I/F Signal**



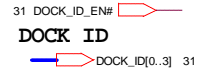
**KBC PS/2 I/F**



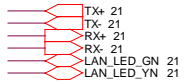
**AUDIO I/F**



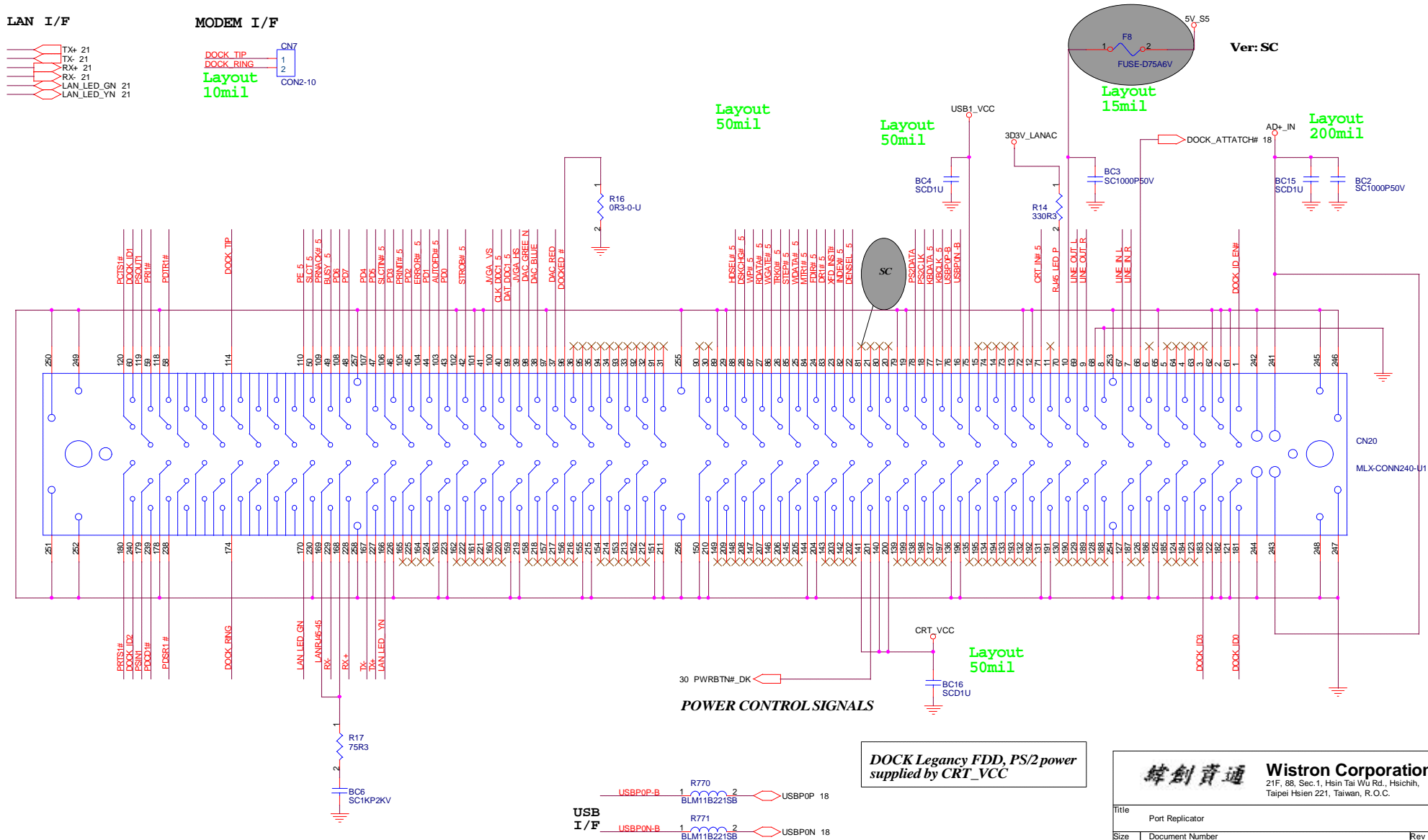
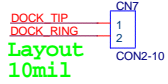
**DOCK CONTR OL SIGNAL**



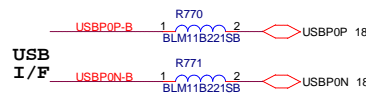
**LAN I/F**



**MODEM I/F**



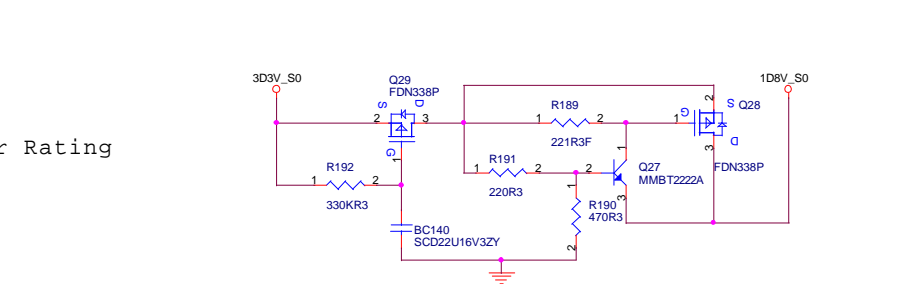
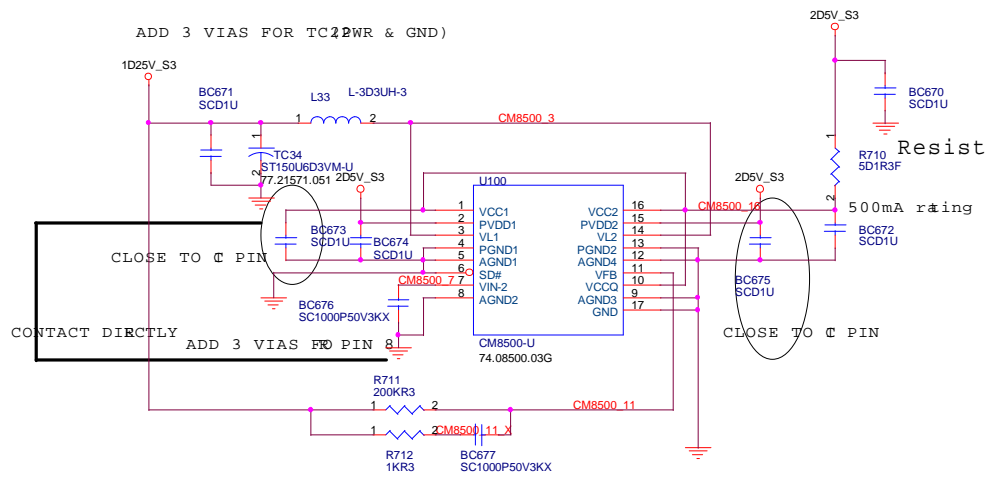
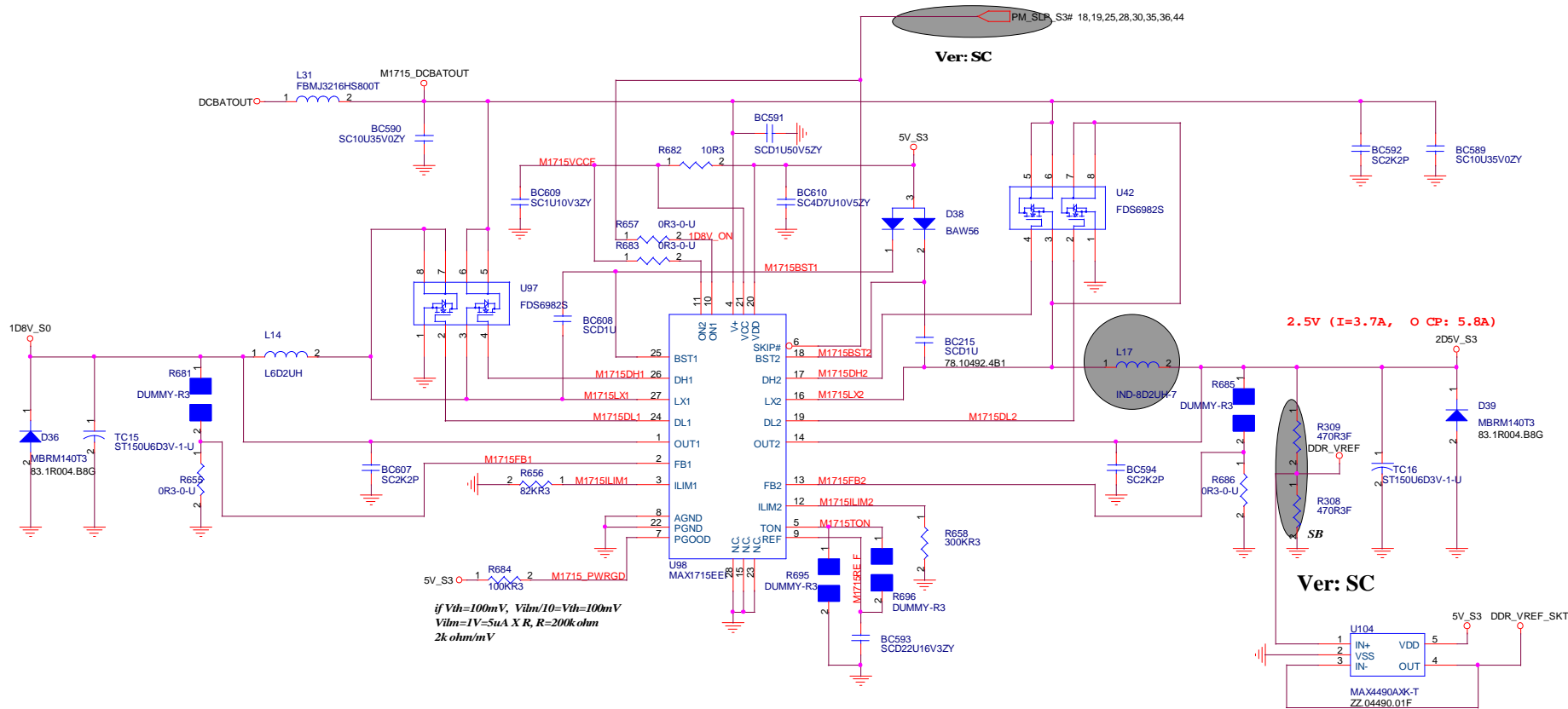
**POWER CONTROL SIGNALS**



**DOCK Legacy FDD, PS/2 power supplied by CRT\_VCC**

**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

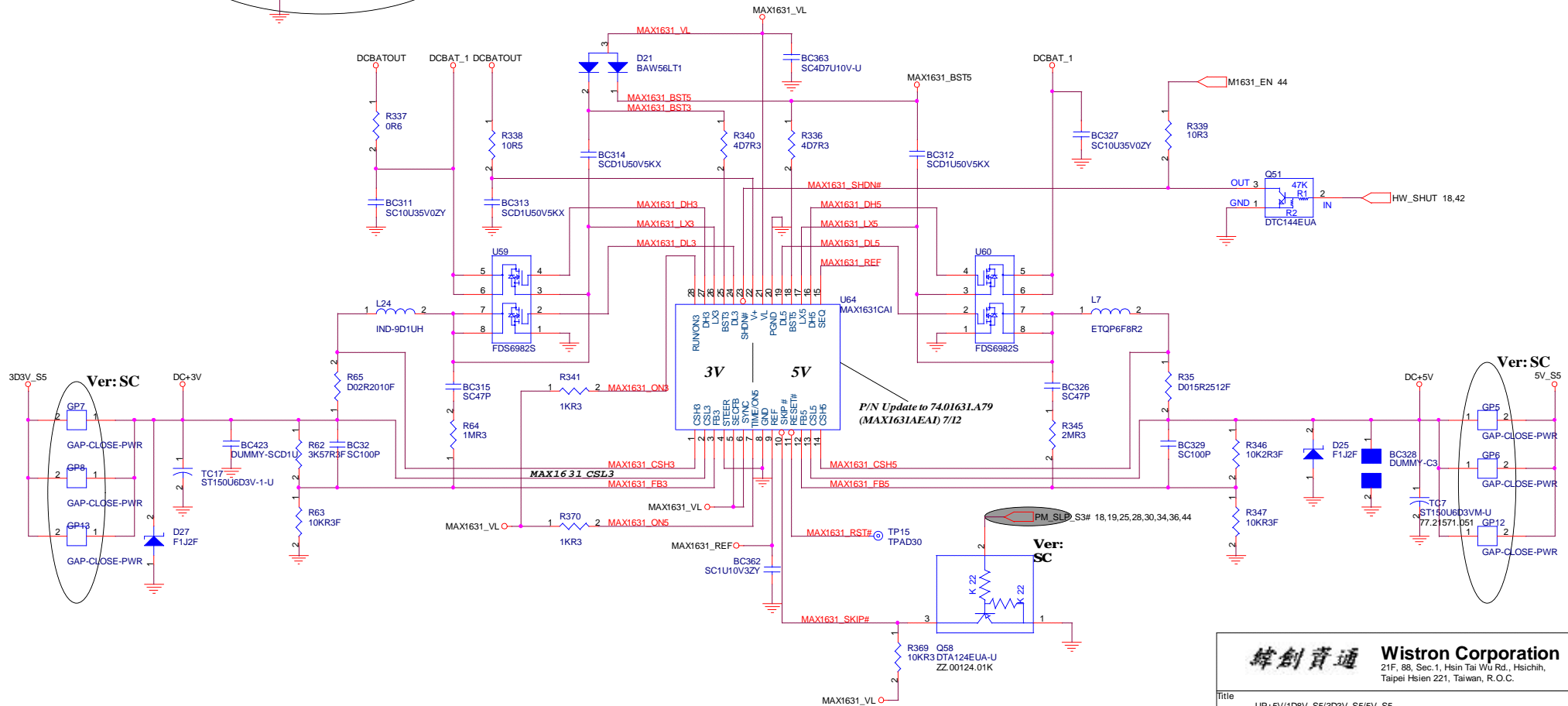
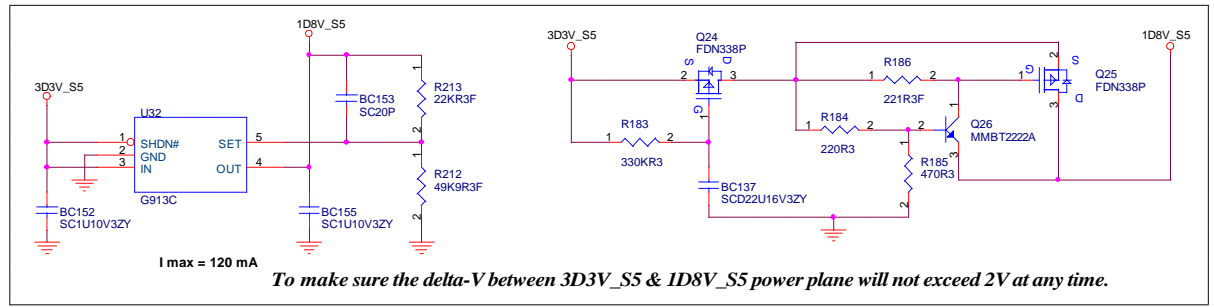
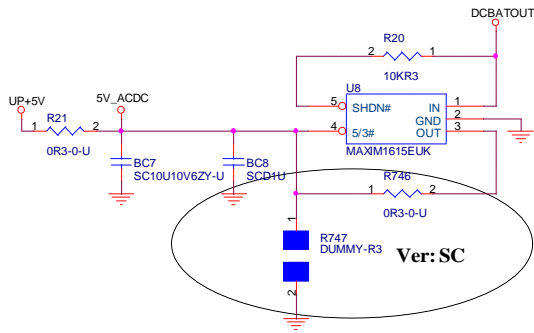
Title	Port Replicator	
Size	Document Number	Rev
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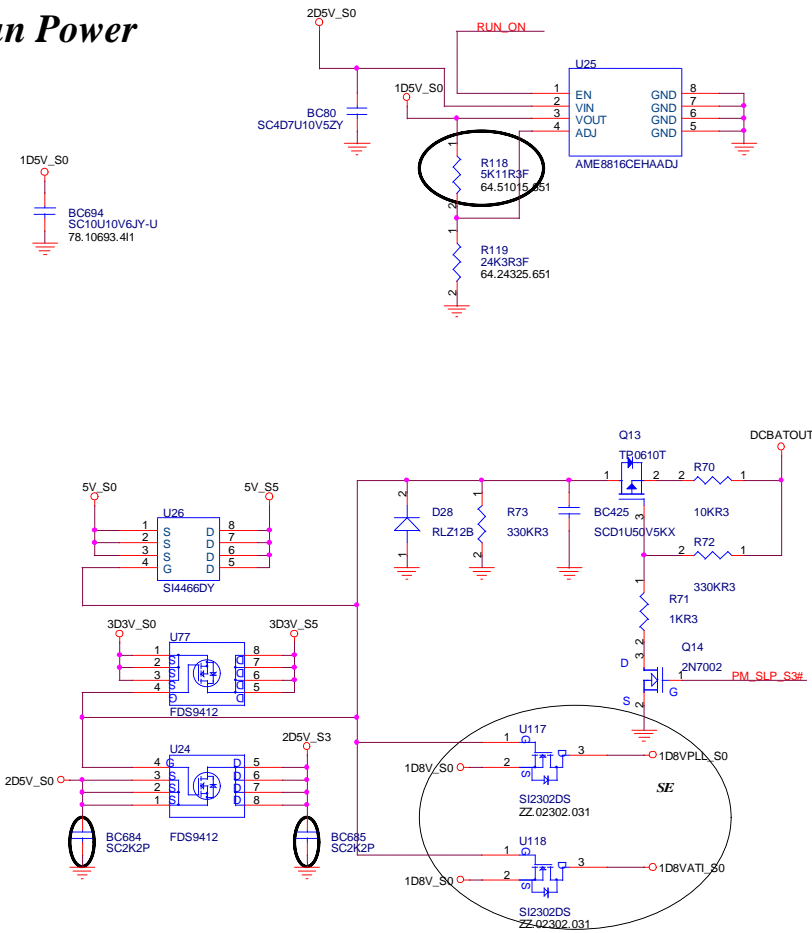
<b>緯創資通 Wistron Corporation</b>		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.		
Title	2D5V_S3/1D25V_S3/1D8V_S0	
Size	Document Number	Rev
A3	D-Note	S2
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# SYSTEM DC/DC

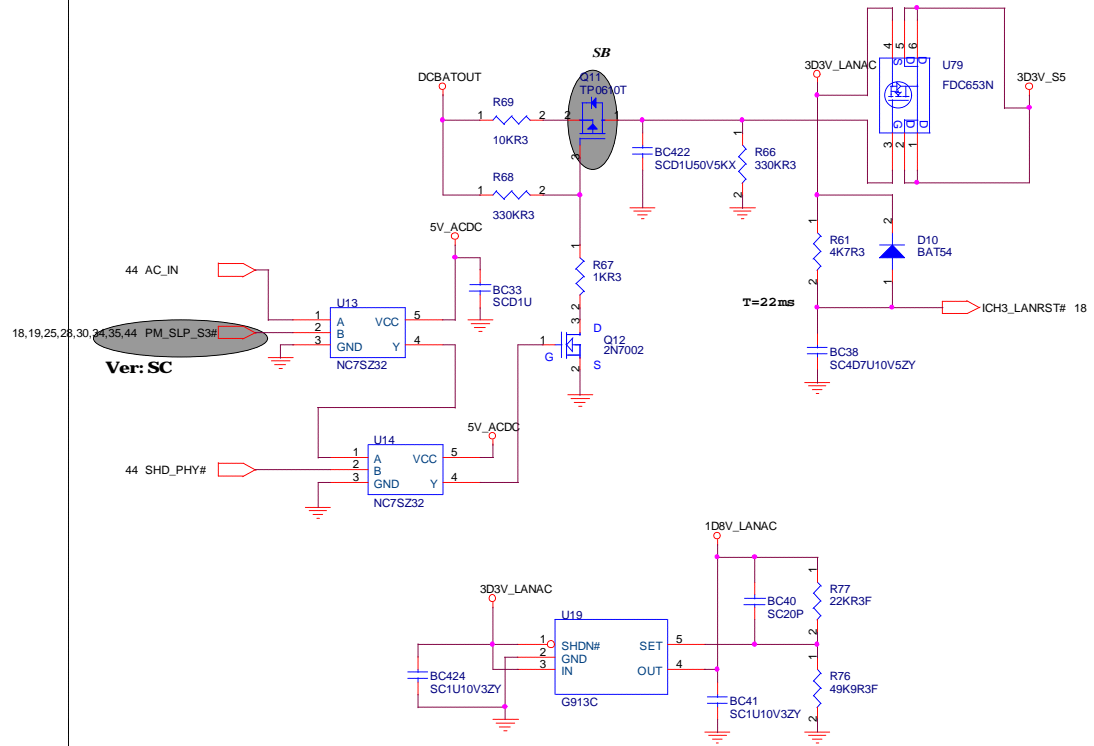
## 3D3V\_S5/5V\_S5/1D8V\_S5/UP+5V



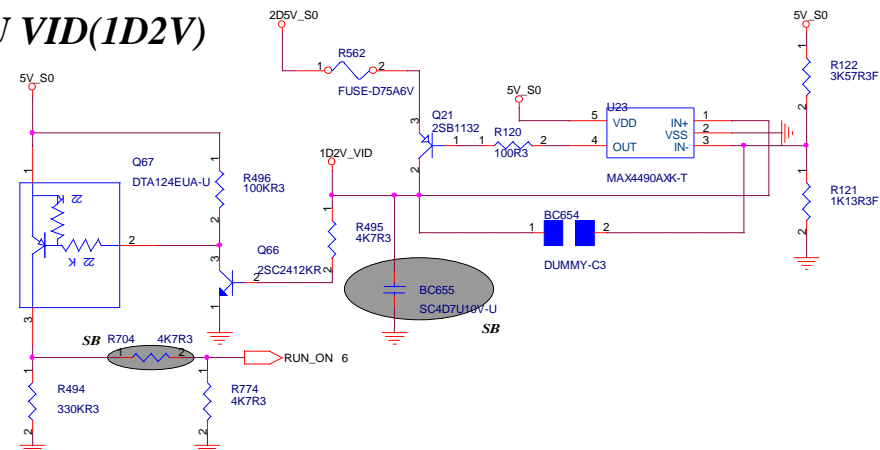
# Run Power



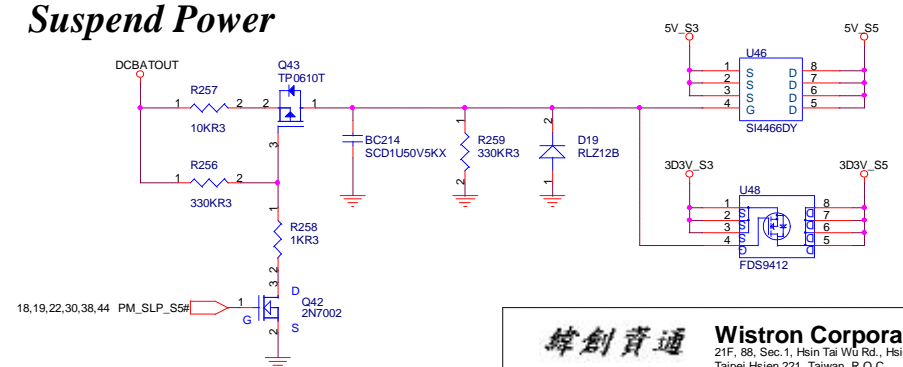
# 3D3V\_S5 → FDC653N → 3D3V\_LANAC → LDO G913C → 1D8V\_LANAC



# CPU VID(1D2V)



# Suspend Power



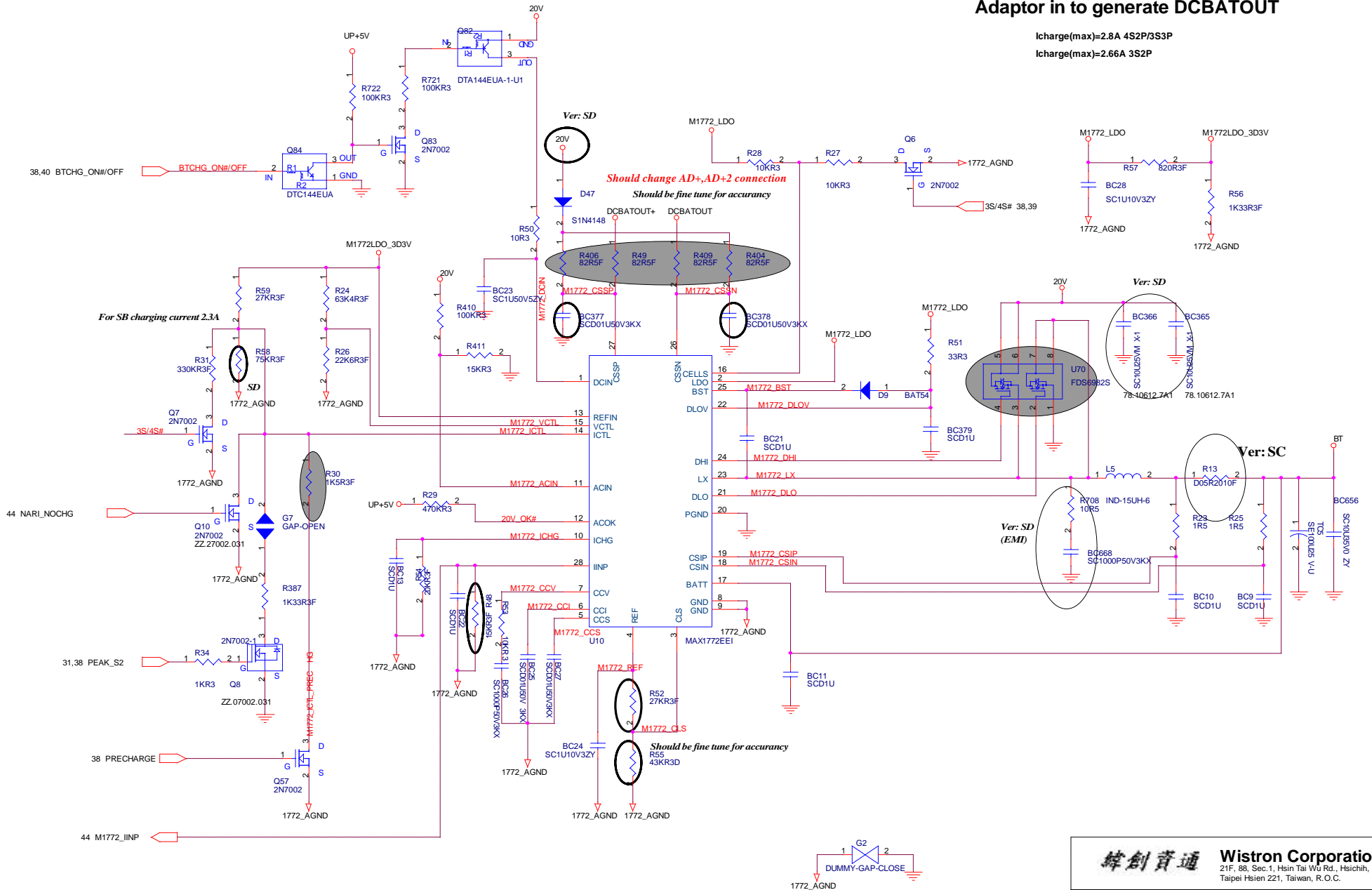
**緯創資通 Wistron Corporation**

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Title			PWR Plane
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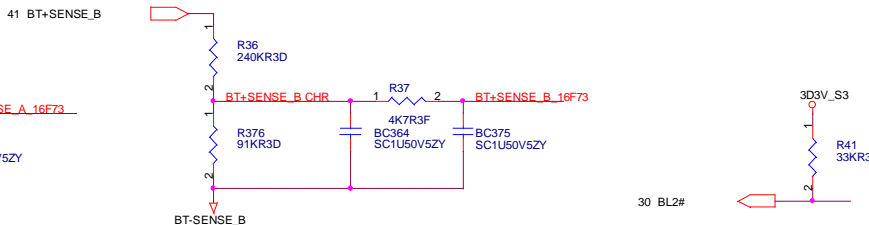
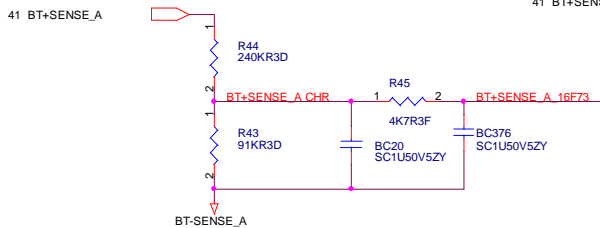
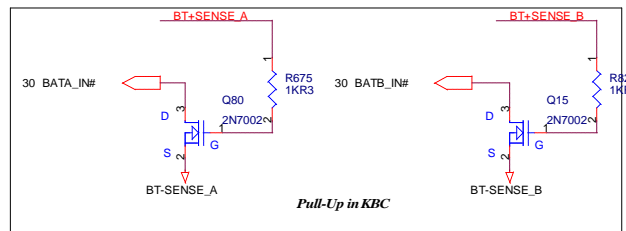
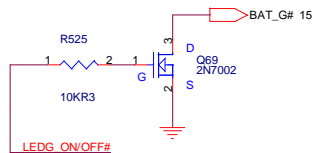
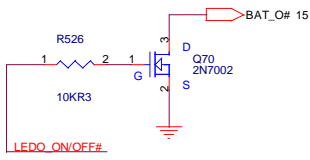
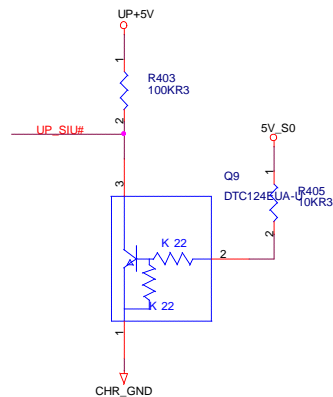
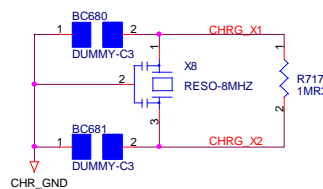
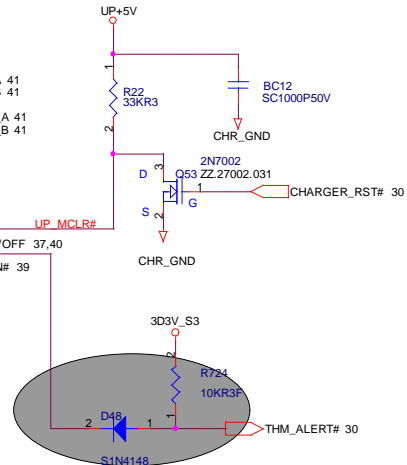
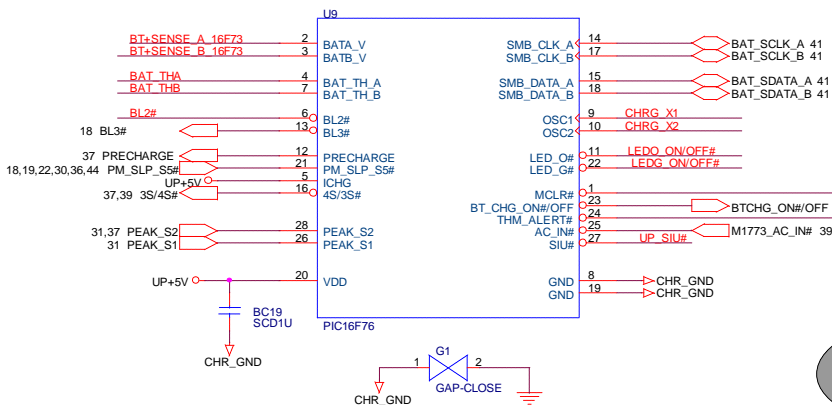
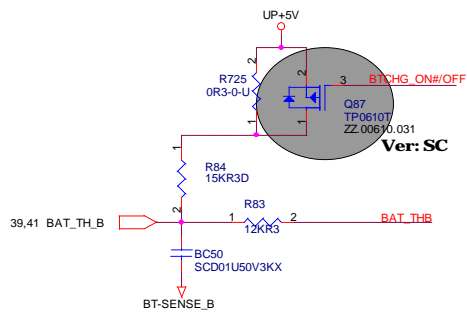
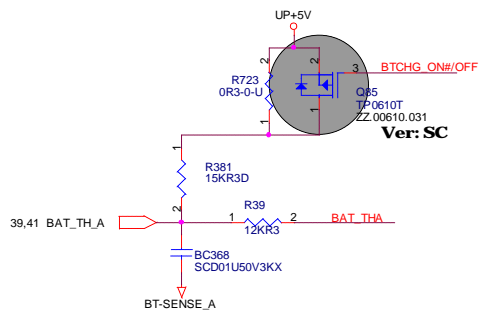
# Adaptor in to generate DCBATOUT

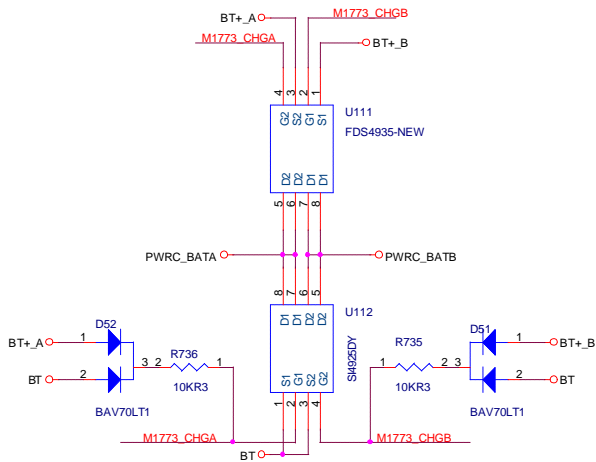
Icharge(max)=2.8A 4S2P/3S3P  
Icharge(max)=2.66A 3S2P



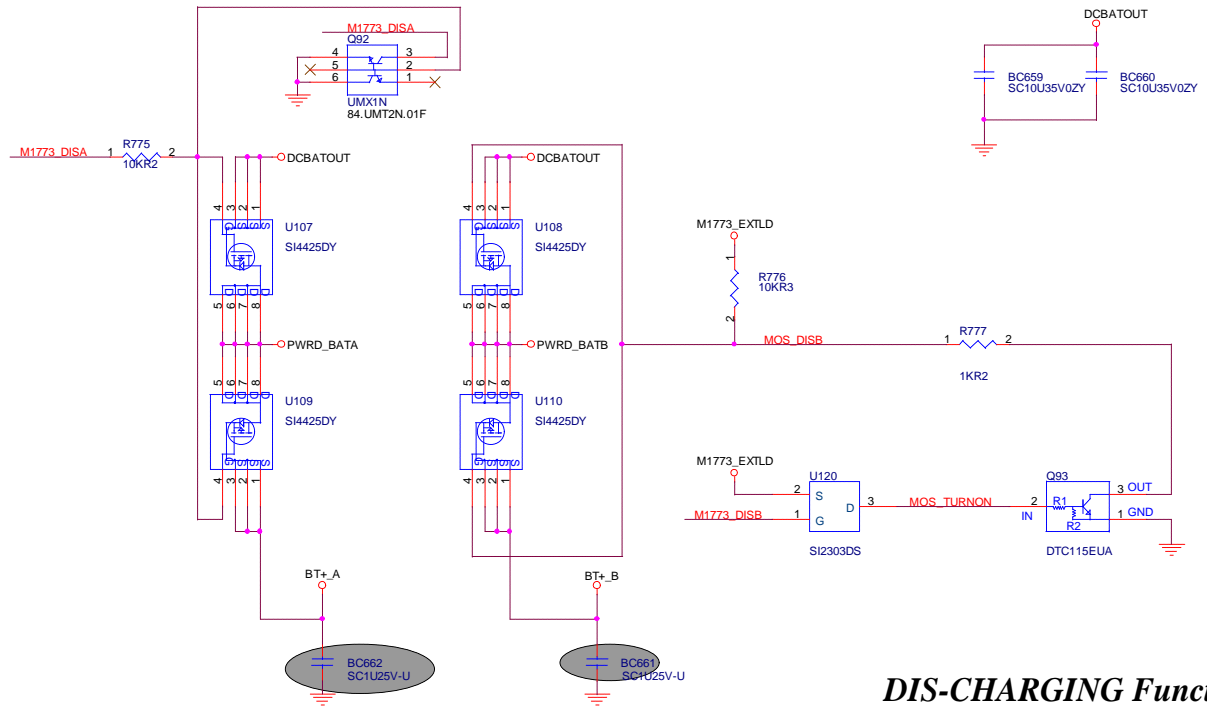
**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title MAX1772		
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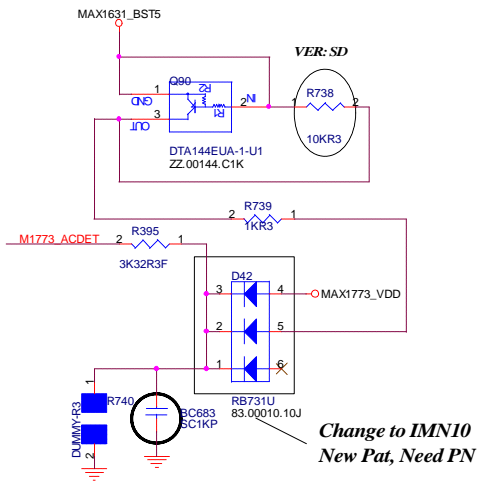




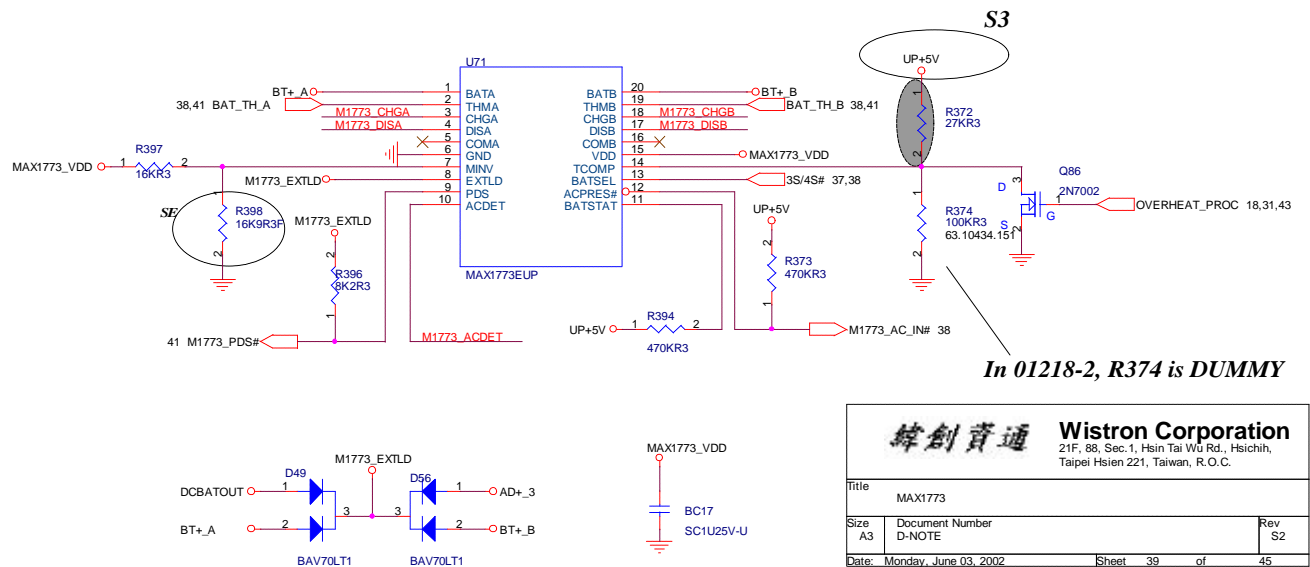
**CHARGING Function**



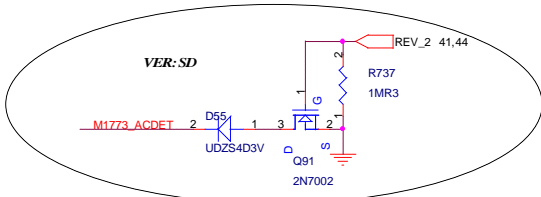
**DIS-CHARGING Function**



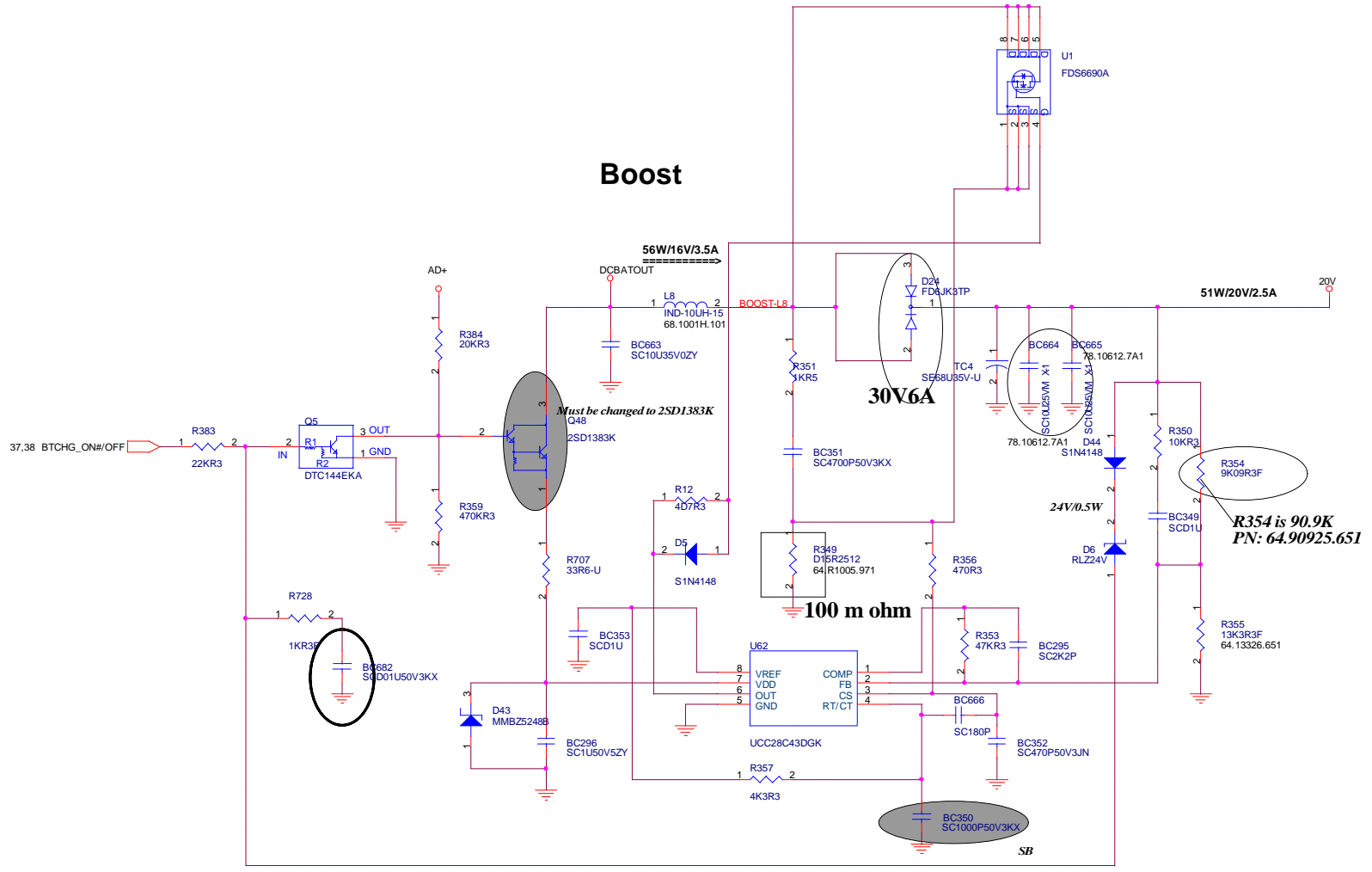
Change to IMN10  
New Pat, Need PN



In 01218-2, R374 is DUMMY



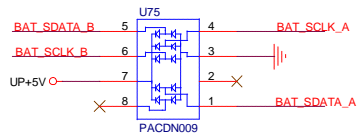
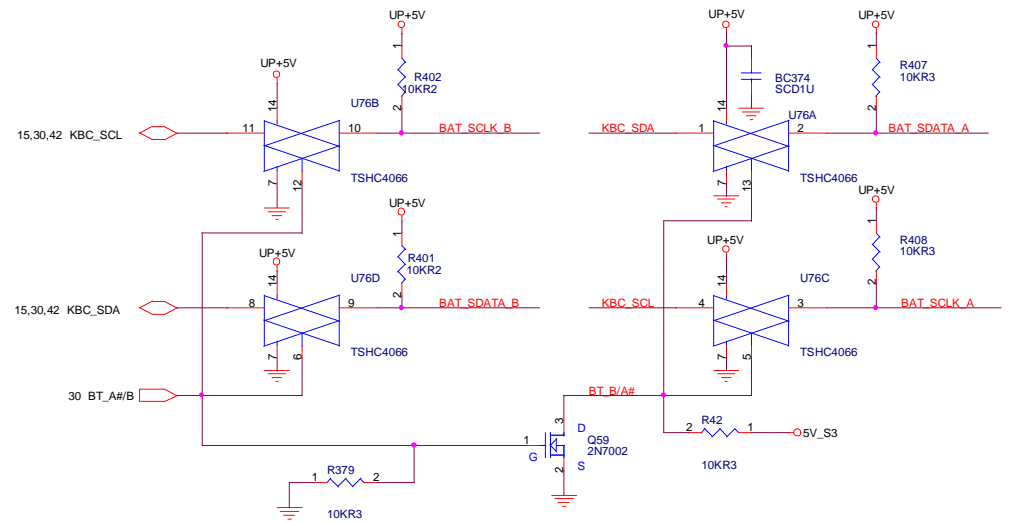
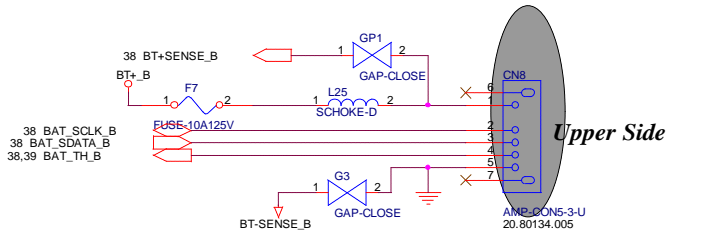
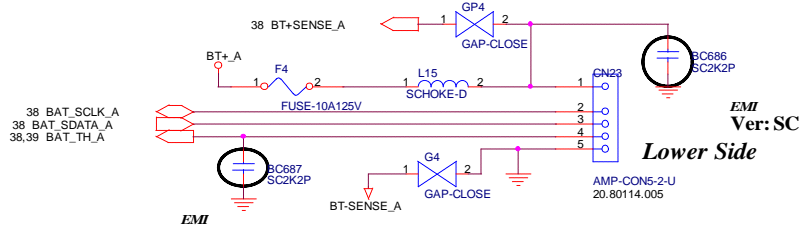
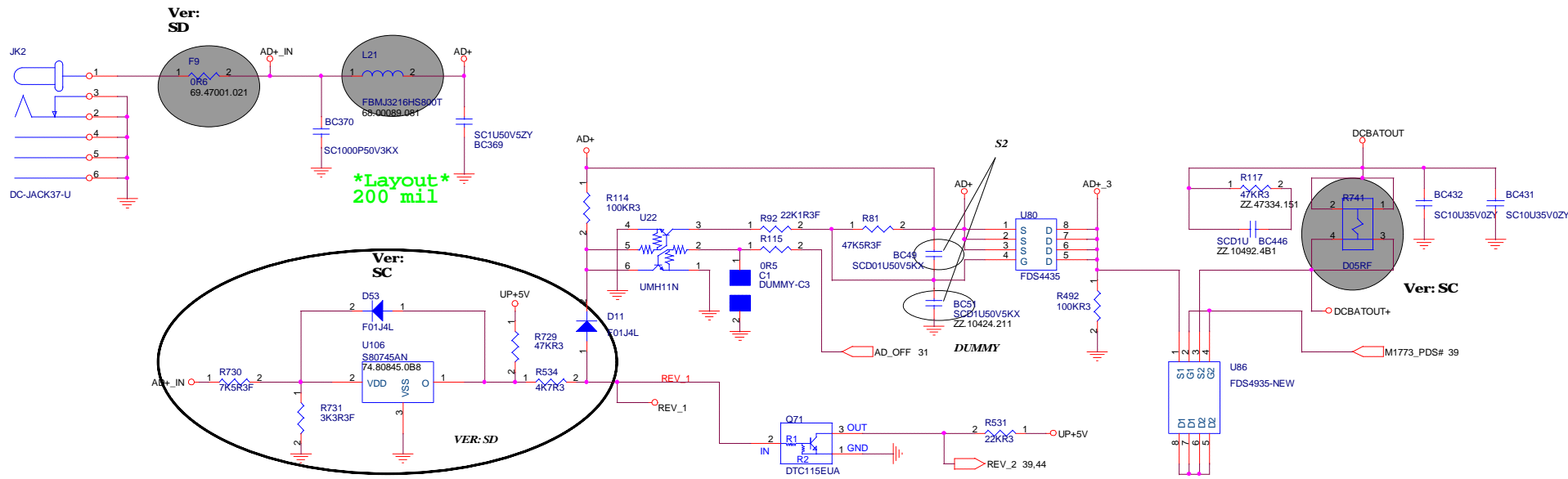
<b>緯創資通 Wistron Corporation</b>	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: MAX1773	
Size: A3	Document Number: D-NOTE
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**緯創資通** Wistron Corporation  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title		BOOST CIRCUIT	
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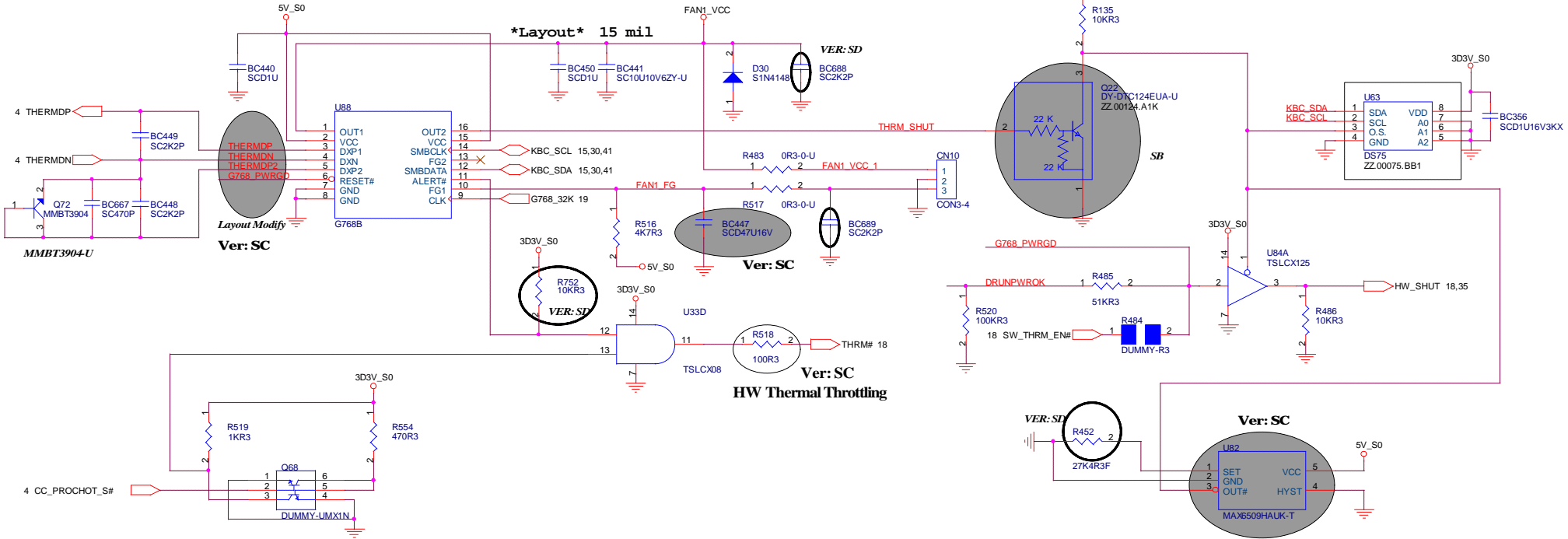
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DCJACK/BATTERY CONNECTORS

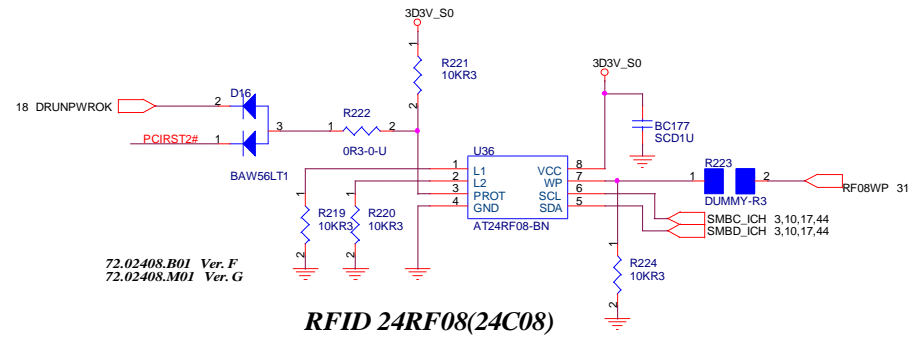
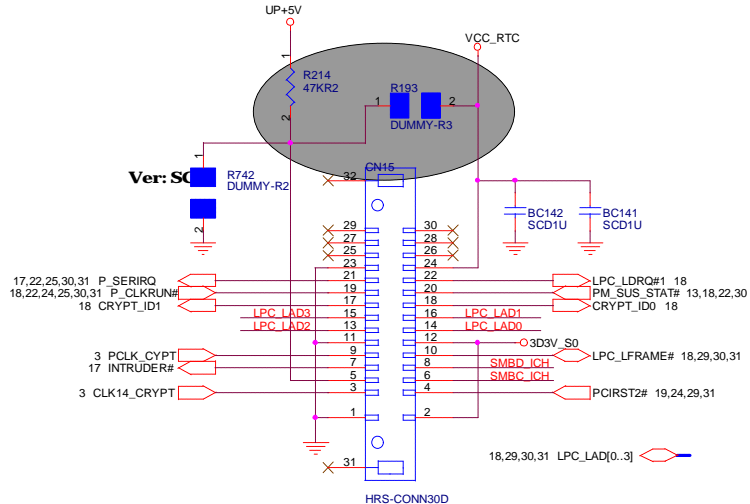
Size: A3 Document Number: D-NOTE Rev: S2

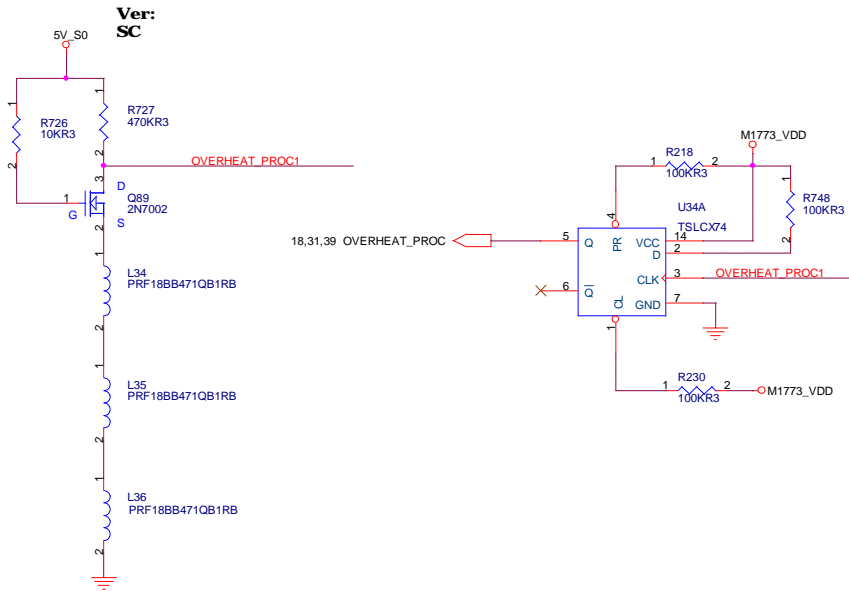
Date: Monday, June 03, 2002 Sheet: 41 of 45

# THERMAL SENSOR & FAN CONTROLLER

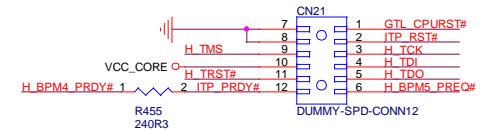
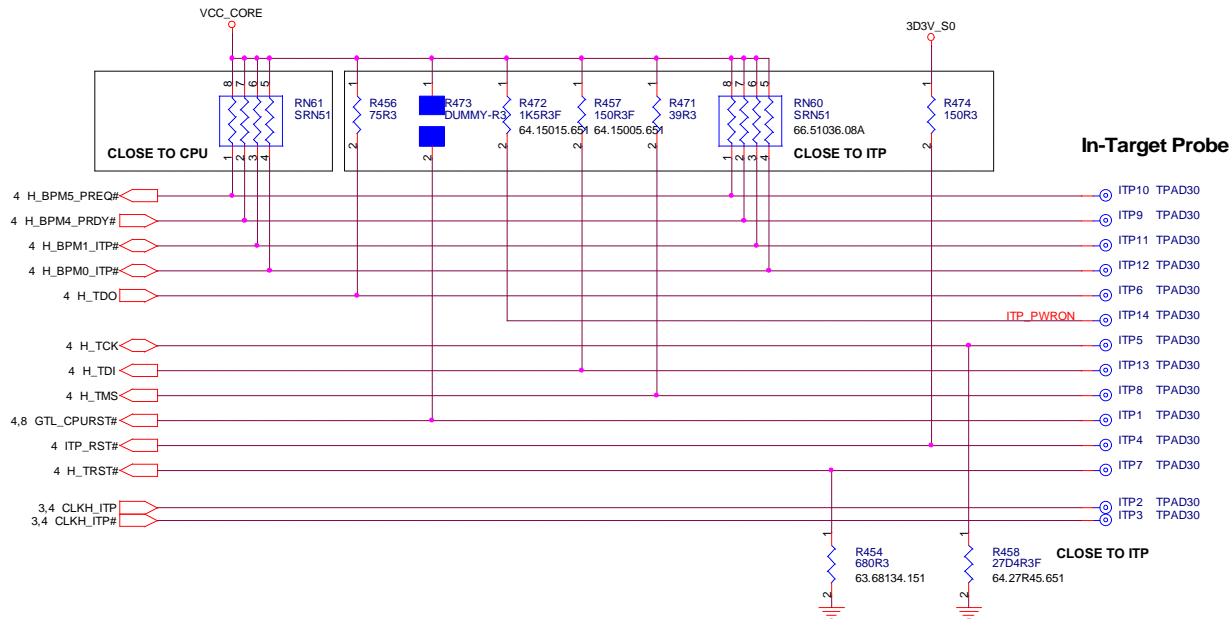
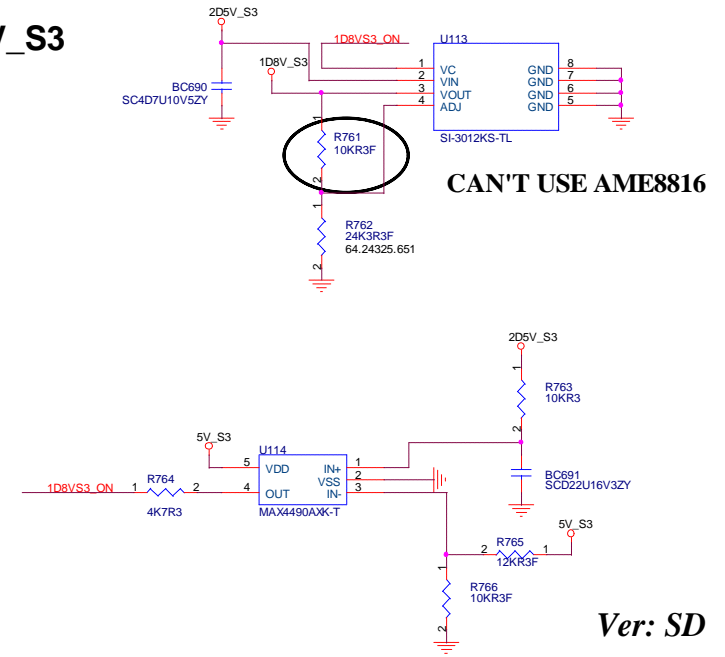


# Crypto Card CONN

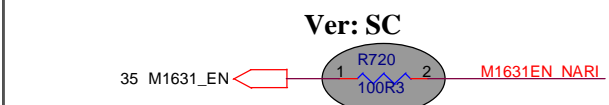
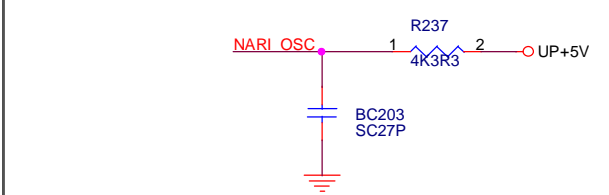
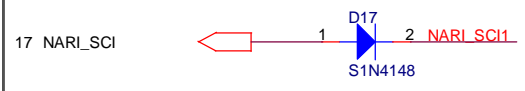
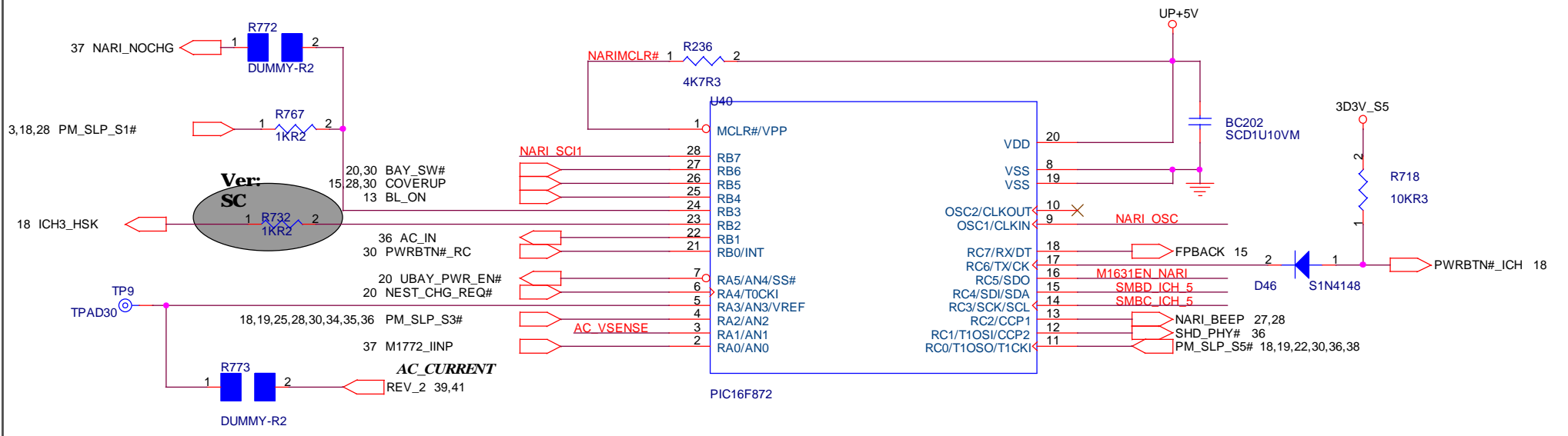




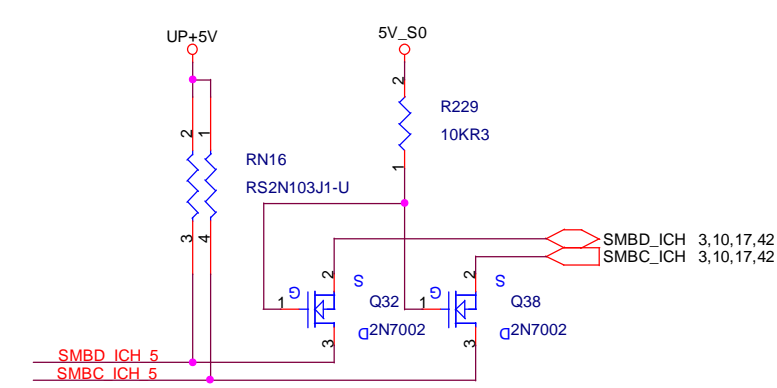
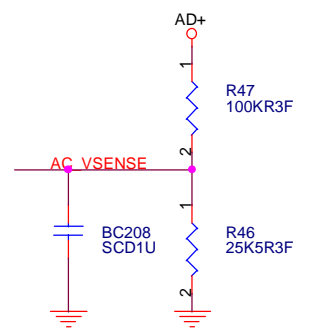
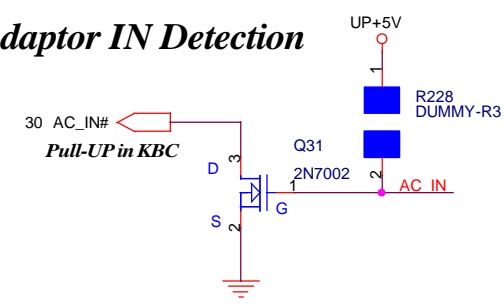
# 1D8V\_S3



A



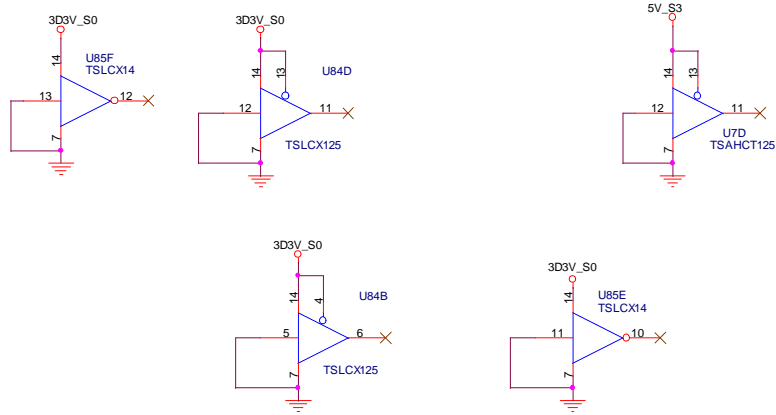
### Adaptor IN Detection



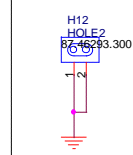
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**PIC16F872 : 71.46872.001**  
**PIC16F73 : 71.16F73.001**

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Nari			
Size: A4	Document Number: D-Note	Rev: S2	
Date: Monday, June 03, 2002	Sheet: 44	of:	45

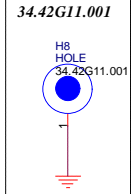
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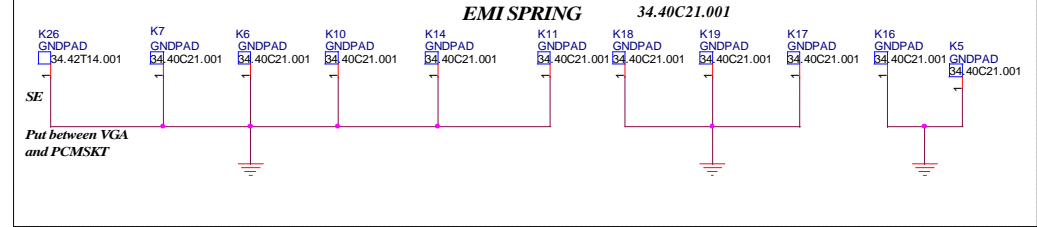
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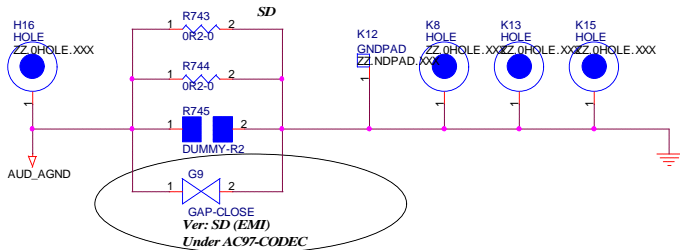
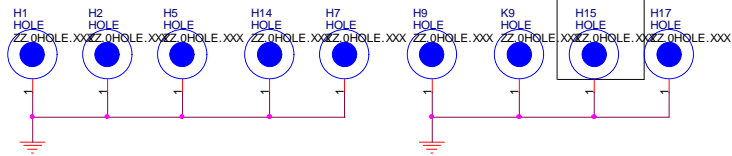
**CDC BOSS**



**EMI SPRING**



Change shape like H5

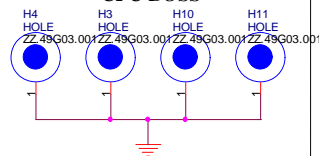


D-NOTE1 PCB 8L OSP

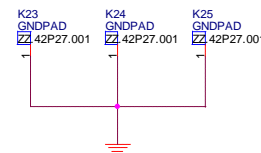
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PCB Part #: 48.42T01.0SA

DNOTE-SA  
48.42T01.0SC

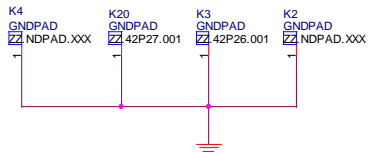
**CPU BOSS**



**VGA Shield GND**



**DCDC RIGHT-END**



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