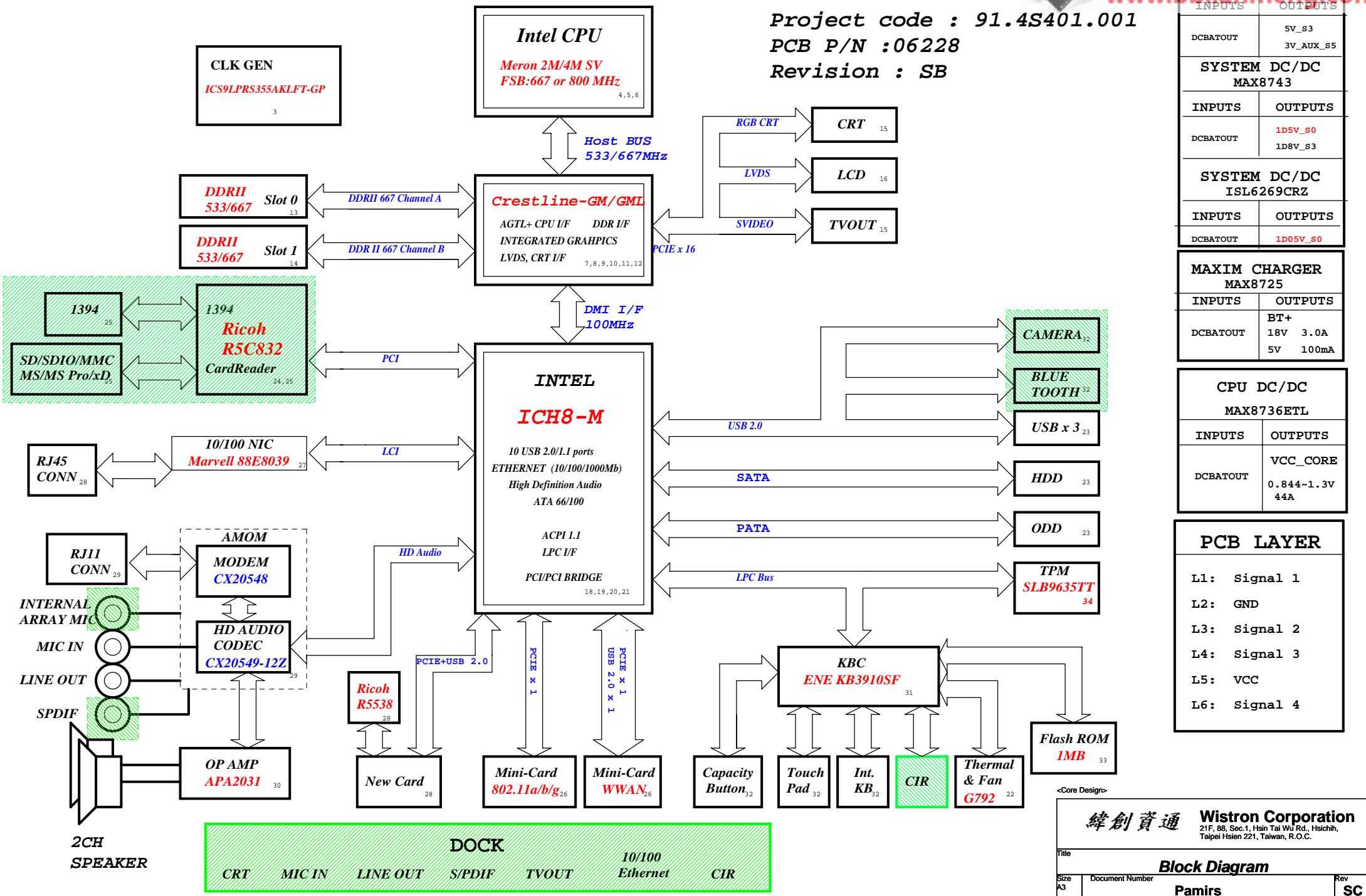


# Pamirs UMA Block Diagram



Project code : 91.4S401.001  
PCB P/N : 06228  
Revision : SB



SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	5V_s3
	3V_AUX_S5

SYSTEM DC/DC ISL6269CRZ	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S0
	1D8V_S3

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+
	18V 3.0A
	5V 100mA

CPU DC/DC MAX8736ETL	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
	0.844~1.3V
	44A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size: A3 Document Number: **Pamirs** Rev: **SC**

Date: Wednesday, November 08, 2006 Sheet 1 of 41

# INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIe Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIe LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
ICH_RSVP3	AZ_DOUT_ICH	Description	RSVD
0	0	Enter XOR Chain	
1	1	Normal Operation(default)	
1	1	Set PCIe port config bit1	

A16 swap override strap	
PCI_GNT#3	low = A16 swap override enable high = default

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	DCT
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5	
SM_INTVRMEN	High=Enable Low=Disable
Integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

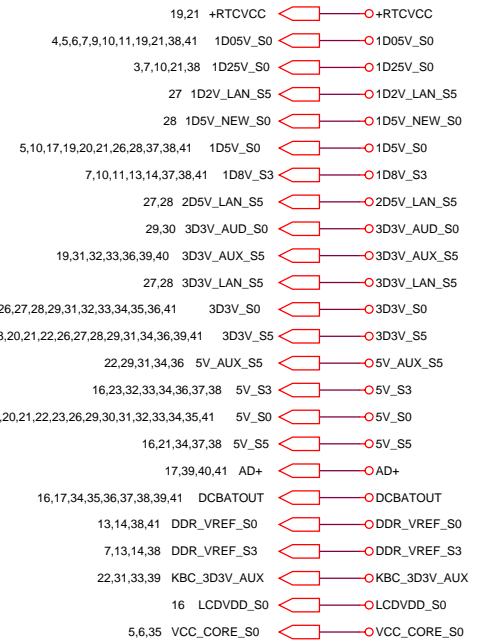
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule High=No Reboot

8.2K PULL HIGH

# INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

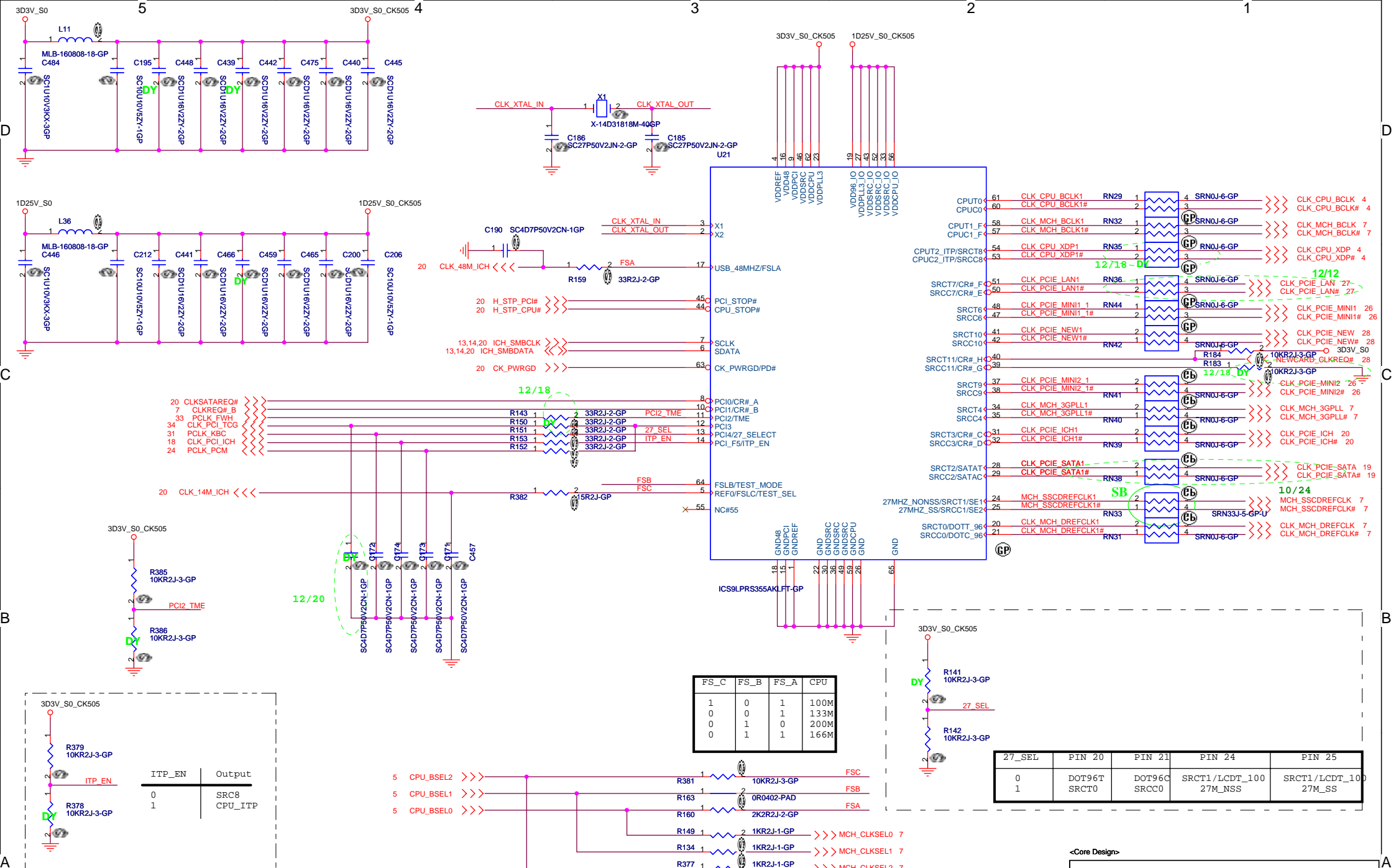


# INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4
CFG 8 Low Power PCI Express	Normal	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled
CFG 19 DMI Lane Reserved	Normal Operation	Reserved Lane
CFG 20 Concurrent SDVO/PCIe	Only PCIe or SDVO is operation	PCIe and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present	SDVO Card Present
CFG 12	XOR/ALL-Z	
CFG 13	Reserved	
LL(00)	Reserved	
LH(01)	XOR Mode Enabled	
HL(10)	All Z Mode Enabled	
HH(11)	Normal Operation	

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<b>Table of Content</b>			
Title			
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**Design Note:**

- All of Input pin didn't have internal pull up resistor.
- Clock Request (CR) function are enable by registers.
- CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	200M
0	1	1	166M

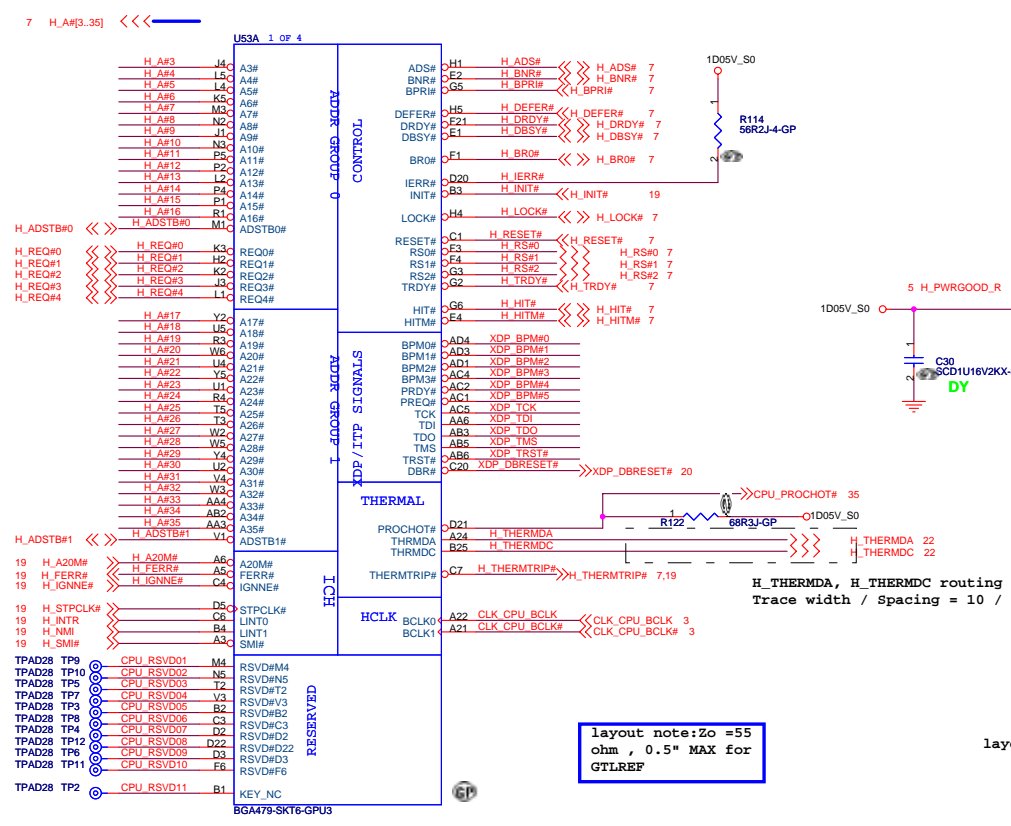
27_SEL	PIN 20	PIN 21	PIN 24	PIN 25
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1	SRCT0	SRCC0	27M_NSS	27M_SS

**<Core Design>**

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**Clock generator CY28548**

Title	Clock generator CY28548		
Size	Document Number	Rev	
A3	<b>Pamirs</b>	<b>SC</b>	
Date:	Wednesday, December 20, 2006	Sheet 3	of 41

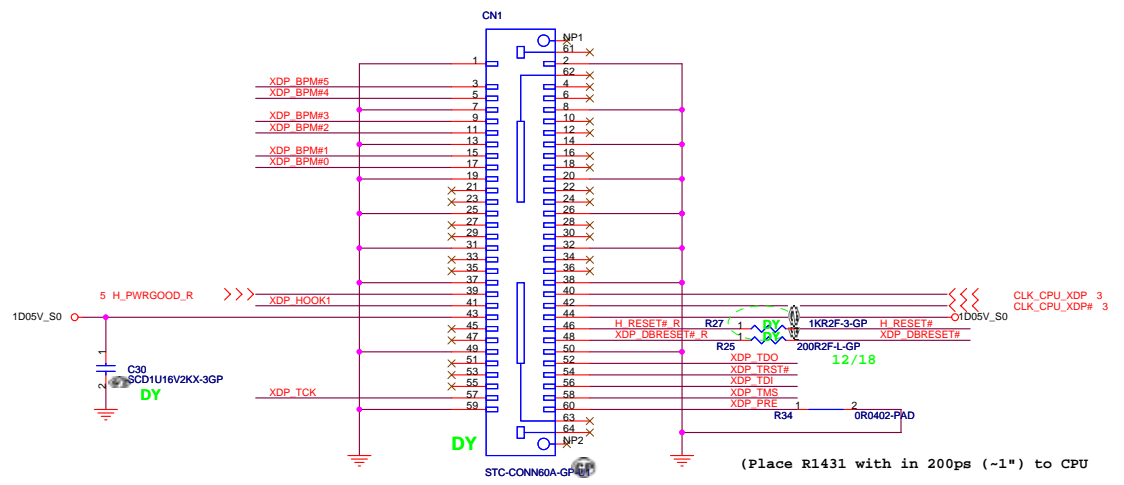


original value: BGA479-SKT6-GPU1

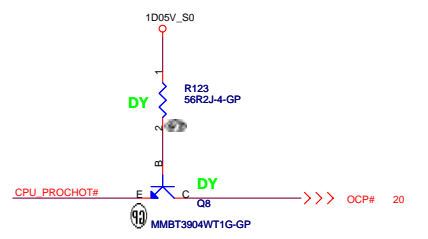
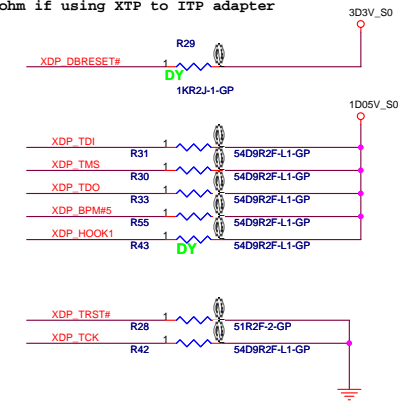
layout note: Zo = 55 ohm, 0.5" MAX for GTLREF

layout note : Change R237 to 649 ohm if using XTP to ITP adapter

### XDP Connector

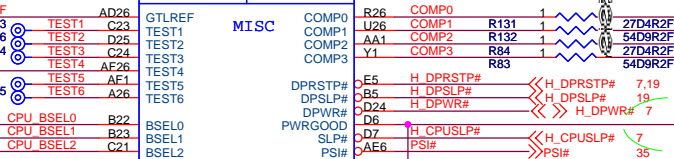
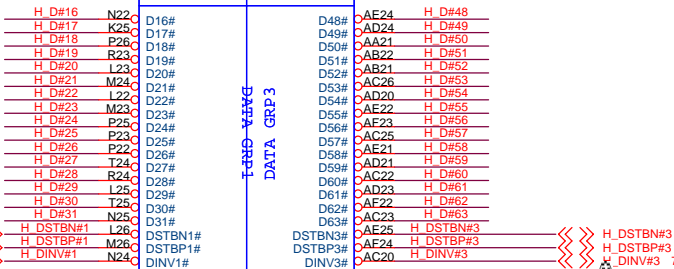
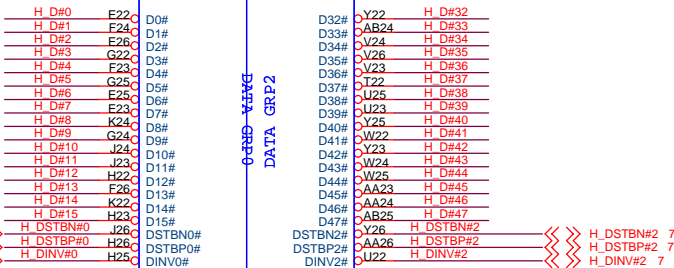


Note:  
If install XDP, need to put R25&R27&C30

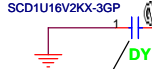


7 H\_D#(0..63) <<>>

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BGA479-SKT6-GPU3



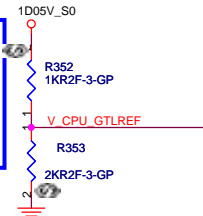
3 CPU\_BSEL0  
3 CPU\_BSEL1  
3 CPU\_BSEL2

PLACE C173 close to the TEST4 PIN, make sure TEST3,TEST4,TEST5 trace routing is reference to GND and away other noisy signals

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

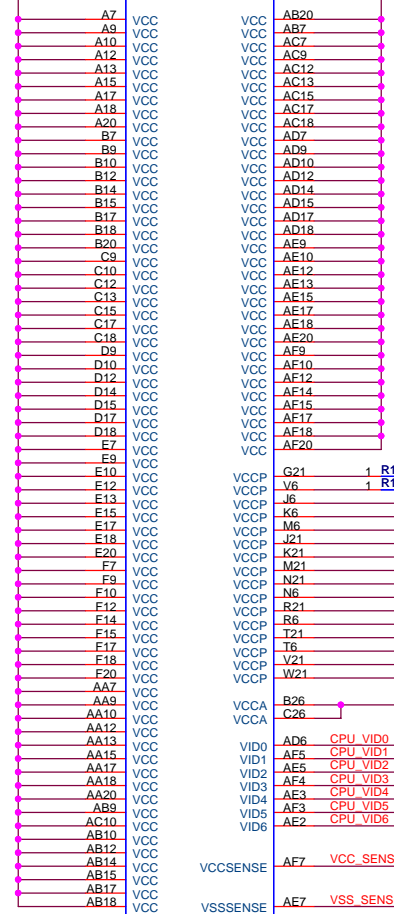
Resistor Placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils .

Close to CPU pin AD26  
Z0=55 ohm  
with in 500mils .



VCC\_CORE\_S0

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BGA479-SKT6-GPU3

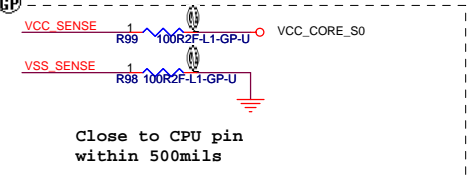
VCC\_CORE\_S0

1D05V\_S0

1D5V\_S0

layout note:  
place C3 near  
PIN B26

Length match within 25 mils . The trace width/space/other is 20/7/25 .



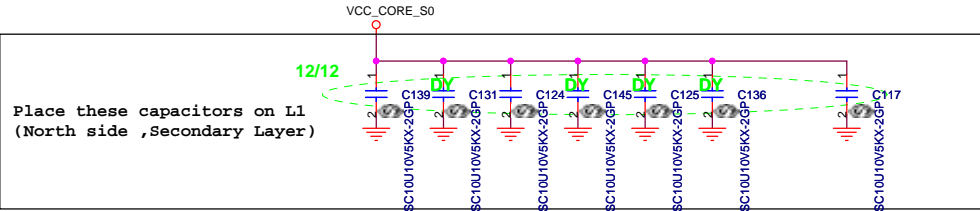
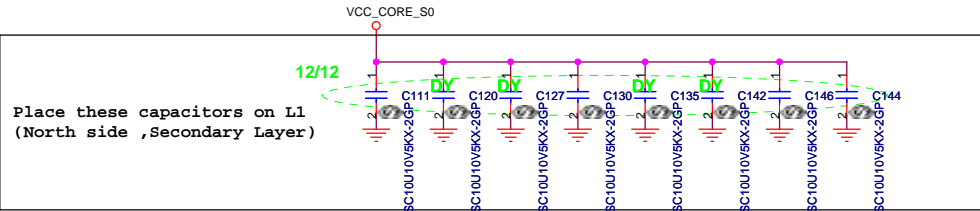
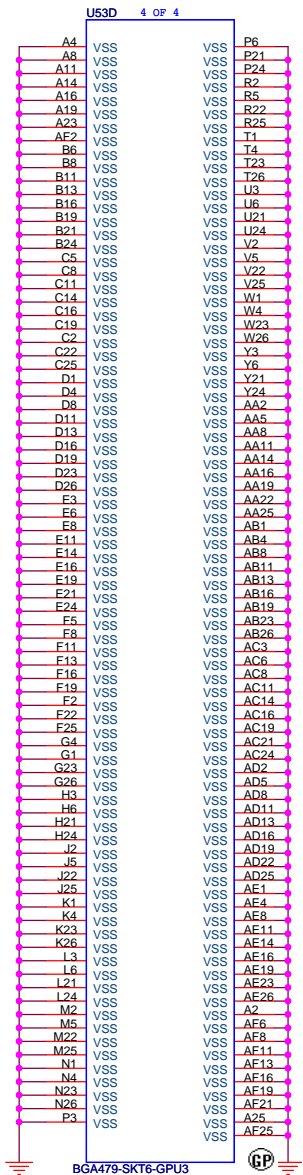
<Core Design>

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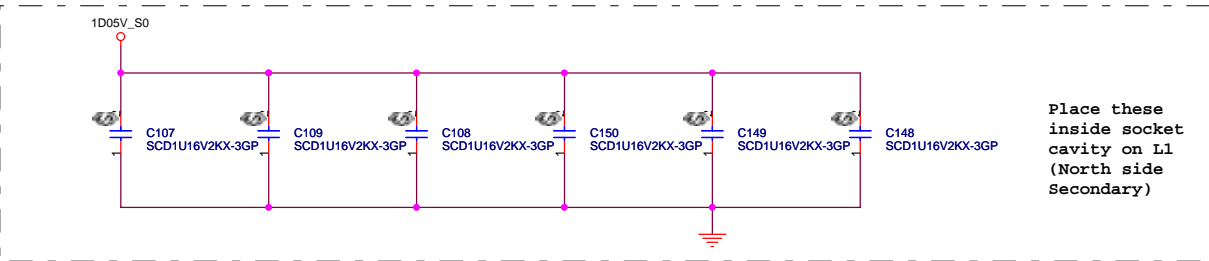
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Size A3 Document Number Rev SC

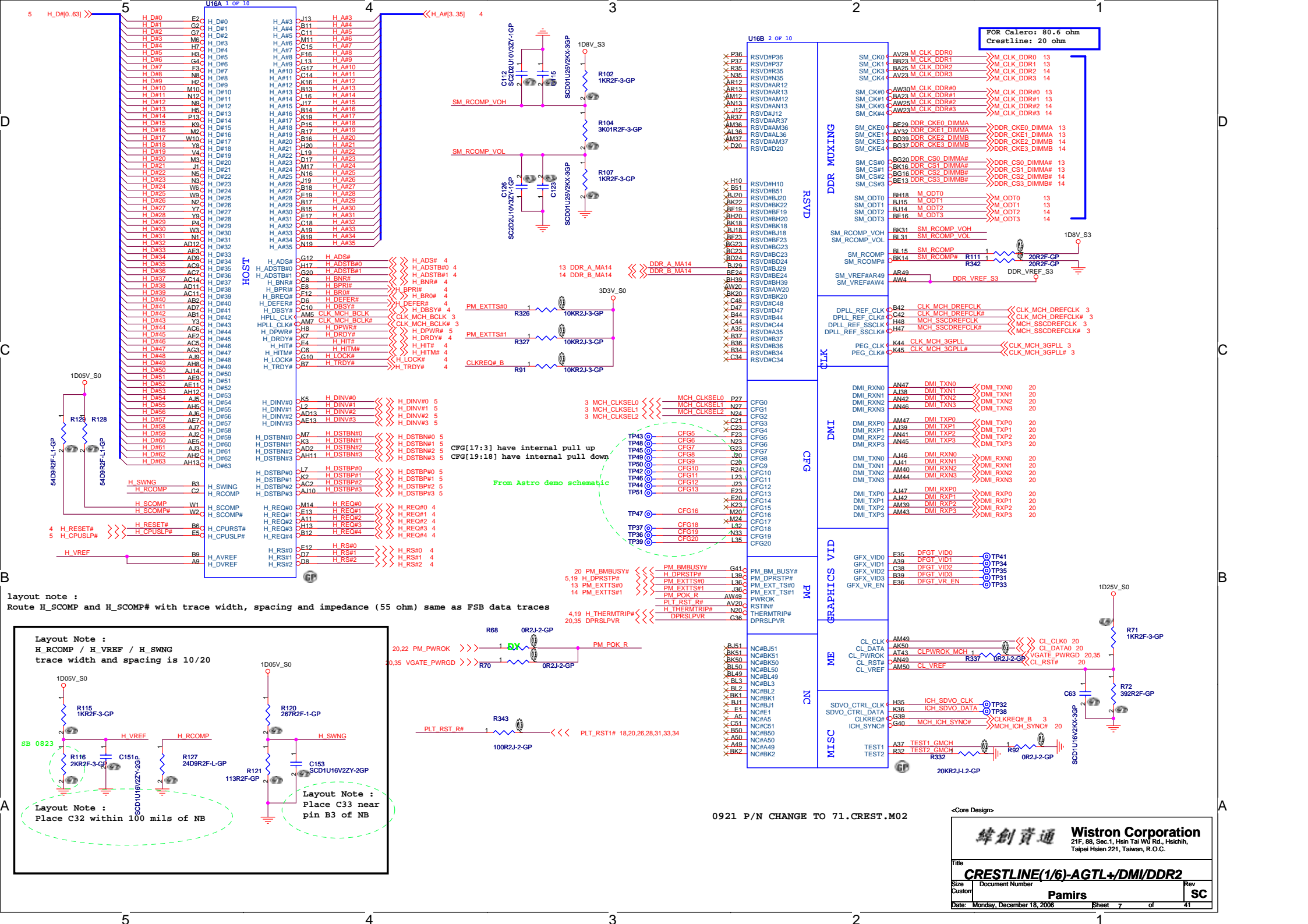
Date: Friday, December 15, 2006 Sheet 5 of 41



Mid Frequncd Decoupling







<< >> DDR\_A\_D[0..63] 13  
 << >> DDR\_A\_BS[0..2] 13  
 << >> DDR\_A\_DM[0..7] 13  
 << >> DDR\_A\_DQS[0..7] 13  
 << >> DDR\_A\_DQS#[0..7] 13  
 << >> DDR\_A\_MA[0..13] 13

<< >> DDR\_B\_D[0..63] 14  
 << >> DDR\_B\_BS[0..2] 14  
 << >> DDR\_B\_DM[0..7] 14  
 << >> DDR\_B\_DQS[0..7] 14  
 << >> DDR\_B\_DQS#[0..7] 14  
 << >> DDR\_B\_MA[0..13] 14

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DDR A D0	AR43	SA_DQ0	SA_BS0	BB19	DDR A BS0
DDR A D1	AW44	SA_DQ1	SA_BS1	BK19	DDR A BS1
DDR A D2	BA45	SA_DQ2	SA_BS2	BF29	DDR A BS2
DDR A D3	AY46	SA_DQ3			
DDR A D4	AR41	SA_DQ4	SA_CAS#	BL17	DDR A CAS# >>> DDR_A_CAS# 13
DDR A D5	AR45	SA_DQ5			
DDR A D6	AT42	SA_DM0	AT45	DDR A DM0	
DDR A D7	AW47	SA_DM1	BD44	DDR A DM1	
DDR A D8	BB45	SA_DM2	BD42	DDR A DM2	
DDR A D9	BF48	SA_DM3	AW38	DDR A DM3	
DDR A D10	BC47	SA_DM4	AW13	DDR A DM4	
DDR A D11	B145	SA_DM5	BC8	DDR A DM5	
DDR A D12	BB47	SA_DM6	AY5	DDR A DM6	
DDR A D13	BG50	SA_DM7	AN6	DDR A DM7	
DDR A D14	BH49	SA_DQ14			
DDR A D15	BE45	SA_DQ15	AT46	DDR A DQS0	
DDR A D16	AW43	SA_DQ16	BE48	DDR A DQS1	
DDR A D17	BF44	SA_DQ17	BE43	DDR A DQS2	
DDR A D18	BG42	SA_DQ18	BC37	DDR A DQS3	
DDR A D19	BE40	SA_DQ19	BB16	DDR A DQS4	
DDR A D20	BF44	SA_DQ20	BH6	DDR A DQS5	
DDR A D21	BH45	SA_DQ21	BB2	DDR A DQS6	
DDR A D22	BG40	SA_DQ22	AP3	DDR A DQS7	
DDR A D23	BF40	SA_DQ23	CA147	DDR A DQS#0	
DDR A D24	AR40	SA_DQ24	BD47	DDR A DQS#1	
DDR A D25	AW40	SA_DQ25	BC41	DDR A DQS#2	
DDR A D26	AT39	SA_DQ26	CA37	DDR A DQS#3	
DDR A D27	AW36	SA_DQ27	CA16	DDR A DQS#4	
DDR A D28	AW41	SA_DQ28	BH7	DDR A DQS#5	
DDR A D29	AY41	SA_DQ29	BC1	DDR A DQS#6	
DDR A D30	AY38	SA_DQ30	AP2	DDR A DQS#7	
DDR A D31	AT38	SA_DQ31			
DDR A D32	AV13	SA_DQ32	B119	DDR A MA0	
DDR A D33	AT13	SA_DQ33	BD20	DDR A MA1	
DDR A D34	AW11	SA_DQ34	BK27	DDR A MA2	
DDR A D35	AV11	SA_DQ35	BH28	DDR A MA3	
DDR A D36	AU15	SA_DQ36	BL24	DDR A MA4	
DDR A D37	AT11	SA_DQ37	BK28	DDR A MA5	
DDR A D38	BA13	SA_DQ38	B127	DDR A MA6	
DDR A D39	BA11	SA_DQ39	B125	DDR A MA7	
DDR A D40	BE10	SA_DQ40	BL28	DDR A MA8	
DDR A D41	BD10	SA_DQ41	BA28	DDR A MA9	
DDR A D42	BD8	SA_DQ42	BC19	DDR A MA10	
DDR A D43	AY9	SA_DQ43	BE28	DDR A MA11	
DDR A D44	BG10	SA_DQ44	BG30	DDR A MA12	
DDR A D45	AW9	SA_DQ45	B116	DDR A MA13	
DDR A D46	BD7	SA_DQ46			
DDR A D47	BB9	SA_DQ47			
DDR A D48	BB5	SA_DQ48	BE18	DDR A RAS# >>> DDR_A_RAS# 13	
DDR A D49	AY7	SA_DQ49	AY20	SA RCVEN# @TP52	
DDR A D50	AT5	SA_DQ50			
DDR A D51	AT7	SA_DQ51	BA19	DDR A WE# >>> DDR_A_WE# 13	
DDR A D52	AY6	SA_DQ52			
DDR A D53	BB7	SA_DQ53			
DDR A D54	AR5	SA_DQ54			
DDR A D55	AR8	SA_DQ55			
DDR A D56	AR9	SA_DQ56			
DDR A D57	AN3	SA_DQ57			
DDR A D58	AM8	SA_DQ58			
DDR A D59	AN10	SA_DQ59			
DDR A D60	AT9	SA_DQ60			
DDR A D61	AN9	SA_DQ61			
DDR A D62	AM9	SA_DQ62			
DDR A D63	AN11	SA_DQ63			

DDR SYSTEM MEMORY A

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DDR B D0	AP49	SB_DQ0	SB_BS0	AY17	DDR B BS0
DDR B D1	AR51	SB_DQ1	SB_BS1	BG18	DDR B BS1
DDR B D2	AW50	SB_DQ2	SB_BS2	BG36	DDR B BS2
DDR B D3	AW51	SB_DQ3			
DDR B D4	AN51	SB_DQ4	SB_CAS#	BE17	DDR B CAS# >>> DDR_B_CAS# 14
DDR B D5	AN50	SB_DQ5			
DDR B D6	AV50	SB_DM0	AR50	DDR B DM0	
DDR B D7	AV49	SB_DM1	BD49	DDR B DM1	
DDR B D8	BA50	SB_DM2	BK45	DDR B DM2	
DDR B D9	BB50	SB_DM3	BL39	DDR B DM3	
DDR B D10	BA49	SB_DM4	BH12	DDR B DM4	
DDR B D11	BE50	SB_DM5	B17	DDR B DM5	
DDR B D12	BA51	SB_DM6	BF3	DDR B DM6	
DDR B D13	AY49	SB_DM7	AW2	DDR B DM7	
DDR B D14	BF50	SB_DQ14			
DDR B D15	BF49	SB_DQ15	AT50	DDR B DQS0	
DDR B D16	B150	SB_DQ16	BD50	DDR B DQS1	
DDR B D17	B144	SB_DQ17	BK46	DDR B DQS2	
DDR B D18	B143	SB_DQ18	BK39	DDR B DQS3	
DDR B D19	BL43	SB_DQ19	B112	DDR B DQS4	
DDR B D20	BK47	SB_DQ20	BL7	DDR B DQS5	
DDR B D21	BK49	SB_DQ21	BE2	DDR B DQS6	
DDR B D22	BK43	SB_DQ22	AV2	DDR B DQS7	
DDR B D23	BK42	SB_DQ23	AJ50	DDR B DQS#0	
DDR B D24	B141	SB_DQ24	BC50	DDR B DQS#1	
DDR B D25	BL41	SB_DQ25	BL45	DDR B DQS#2	
DDR B D26	B137	SB_DQ26	BK38	DDR B DQS#3	
DDR B D27	B136	SB_DQ27	BK12	DDR B DQS#4	
DDR B D28	BK41	SB_DQ28	BK7	DDR B DQS#5	
DDR B D29	BL40	SB_DQ29	BE2	DDR B DQS#6	
DDR B D30	BL35	SB_DQ30	AV3	DDR B DQS#7	
DDR B D31	BK37	SB_DQ31			
DDR B D32	BK13	SB_DQ32	BC18	DDR B MA0	
DDR B D33	BE11	SB_DQ33	BG28	DDR B MA1	
DDR B D34	BK11	SB_DQ34	BG25	DDR B MA2	
DDR B D35	BC11	SB_DQ35	AW17	DDR B MA3	
DDR B D36	BC13	SB_DQ36	BE25	DDR B MA4	
DDR B D37	BE12	SB_DQ37	BE25	DDR B MA5	
DDR B D38	BC12	SB_DQ38	BA29	DDR B MA6	
DDR B D39	BG12	SB_DQ39	BC28	DDR B MA7	
DDR B D40	B110	SB_DQ40	AY28	DDR B MA8	
DDR B D41	BL9	SB_DQ41	BD37	DDR B MA9	
DDR B D42	BK5	SB_DQ42	BG17	DDR B MA10	
DDR B D43	BL5	SB_DQ43	BE37	DDR B MA11	
DDR B D44	BK9	SB_DQ44	BA39	DDR B MA12	
DDR B D45	BK10	SB_DQ45	BG13	DDR B MA13	
DDR B D46	B18	SB_DQ46			
DDR B D47	B16	SB_DQ47	AV16	DDR B RAS# >>> DDR_B_RAS# 14	
DDR B D48	BF4	SB_DQ48	AY18	SA RCVEN# @TP53	
DDR B D49	BH5	SB_DQ49			
DDR B D50	BG1	SB_DQ50	BC17	DDR B WE# >>> DDR_B_WE# 14	
DDR B D51	BC2	SB_DQ51			
DDR B D52	BK3	SB_DQ52			
DDR B D53	BE4	SB_DQ53			
DDR B D54	BD3	SB_DQ54			
DDR B D55	B12	SB_DQ55			
DDR B D56	BA3	SB_DQ56			
DDR B D57	BB3	SB_DQ57			
DDR B D58	AR1	SB_DQ58			
DDR B D59	AT3	SB_DQ59			
DDR B D60	AY2	SB_DQ60			
DDR B D61	AY3	SB_DQ61			
DDR B D62	AU2	SB_DQ62			
DDR B D63	AT2	SB_DQ63			

DDR SYSTEM MEMORY B

<Core Design>

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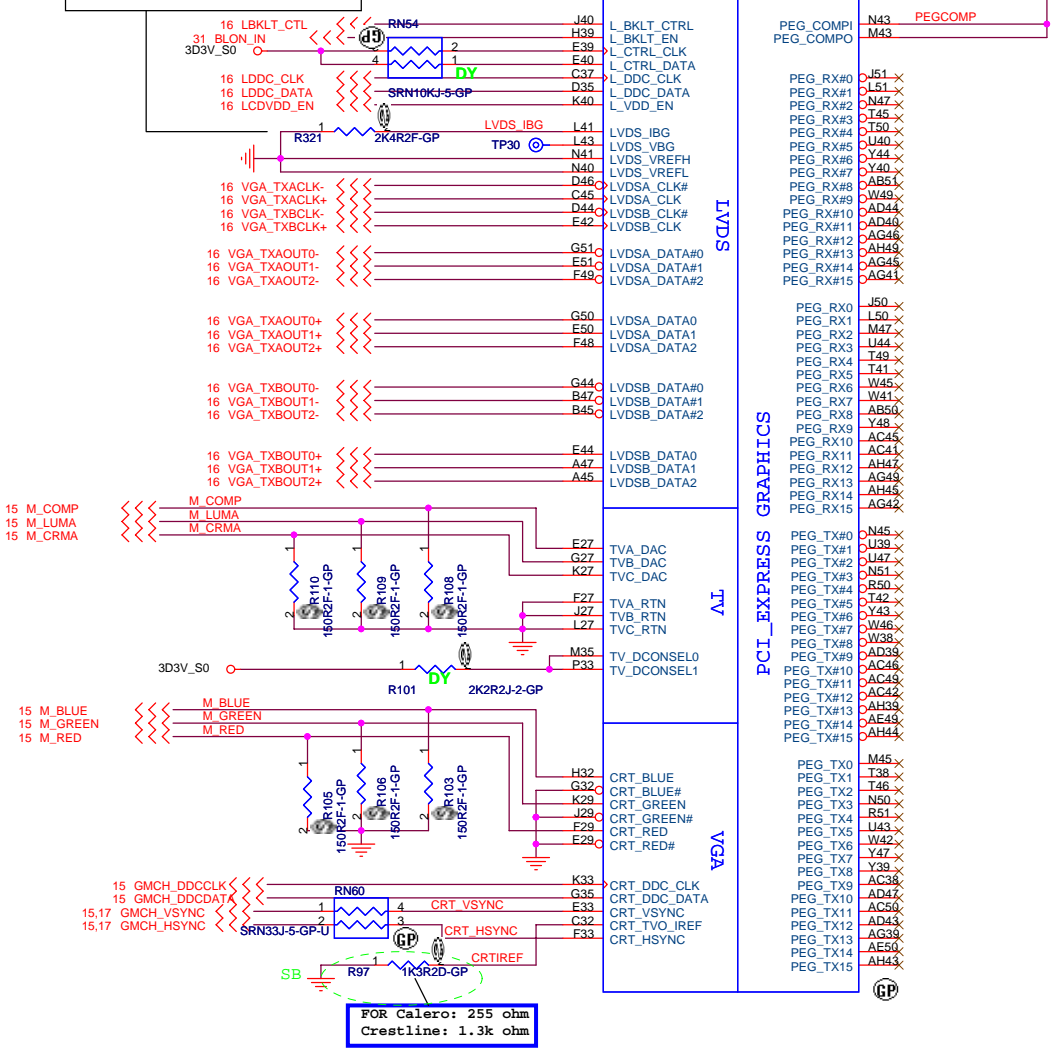
Title: **CRESTLINE(2/6)-DDR2 A/B CH**

Size A3 Document Number **Pamirs** Rev **SC**

Date: Monday, December 18, 2006 Sheet 8 of 41



For Crestline : 2.4 Kohm  
For Calero : 1.5Kohm



FOR Calero: 255 ohm  
Crestline: 1.3k ohm

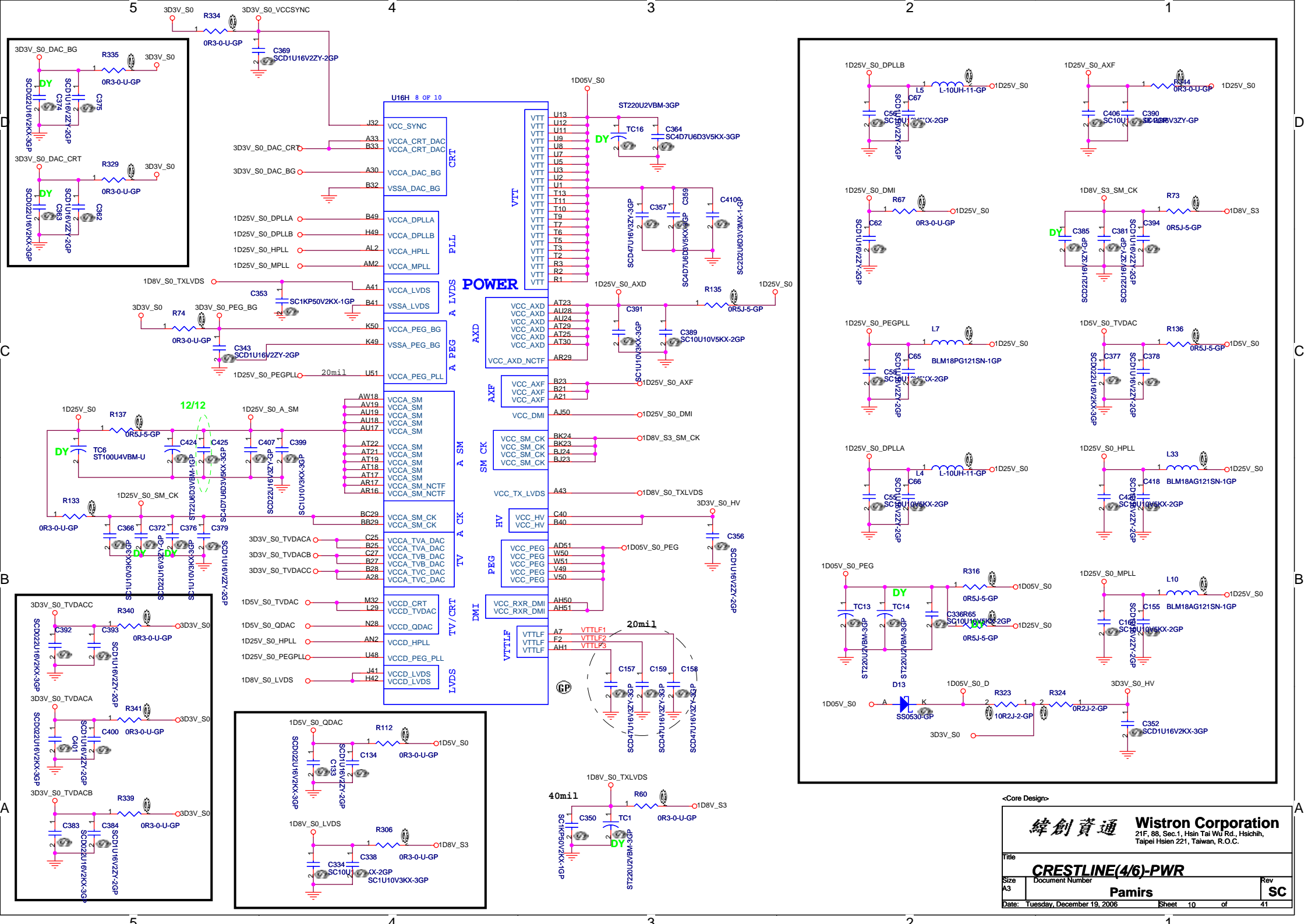
PEGCOMP trace width and spacing is 20/25 mils.

### Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

<Core Design>

<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>CRESTLINE(3/6)-VGA/LVDS/TV</b>	
Title	Rev
Size A3	SC
Document Number	Sheet 9 of 41
Date: Monday, December 18, 2006	



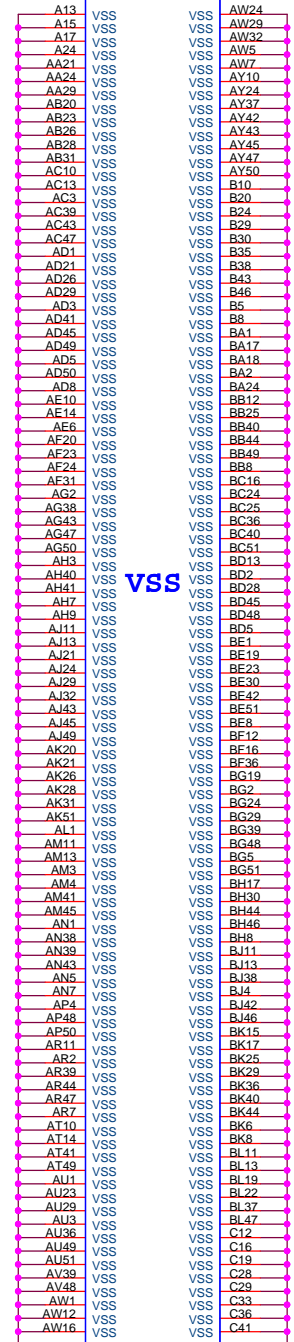
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**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

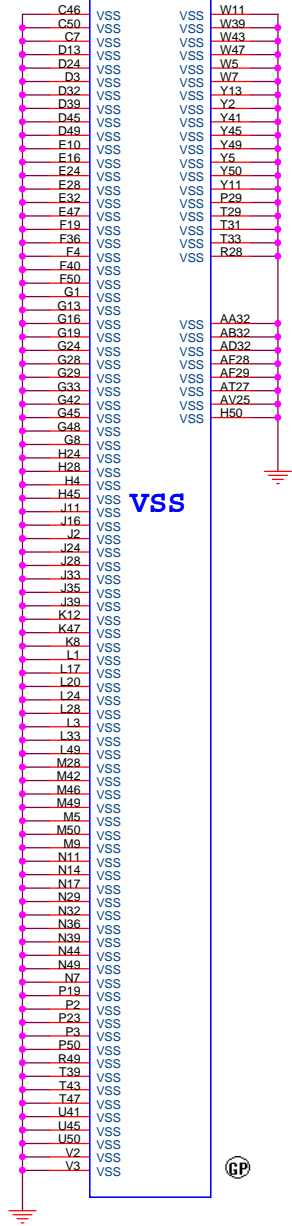
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Size A3	Document Number	Rev <b>SC</b>
<b>Pamirs</b>		
Date: Tuesday, December 19, 2006		Sheet 10 of 41



U16I 9 OF 10



U16J 10 OF 10

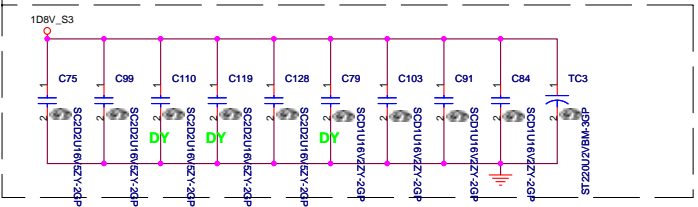


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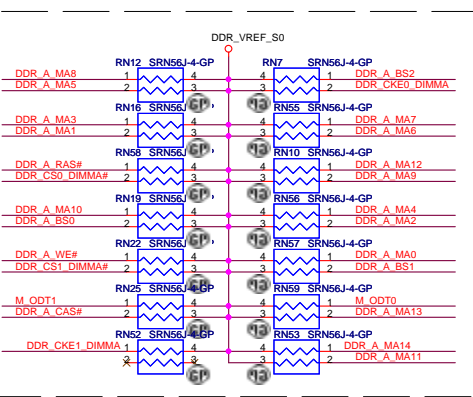
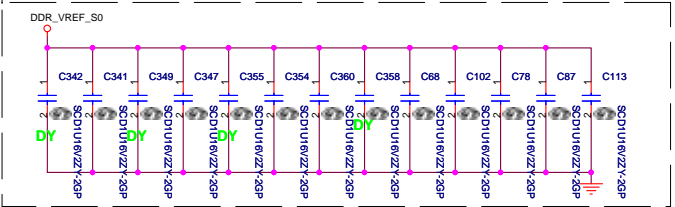
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		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>CRESTLINE(6/6)-PWR/GND</b>			
Title		Document Number	
Size	A3	Rev	SC
Date:	Monday, December 18, 2006	Sheet	12 of 41

8 DDR\_A\_DQS#[0..7] <<>>  
 8 DDR\_A\_DQ[0..63] <<>>  
 8 DDR\_A\_DM[0..7] <<>>  
 8 DDR\_A\_DQS#[0..7] <<>>  
 8 DDR\_A\_MA[0..13] <<>>  
 8 DDR\_A\_BS[0..2] <<>>

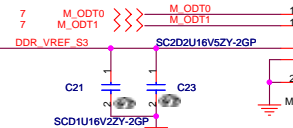
Layout Note:  
Place near DM1



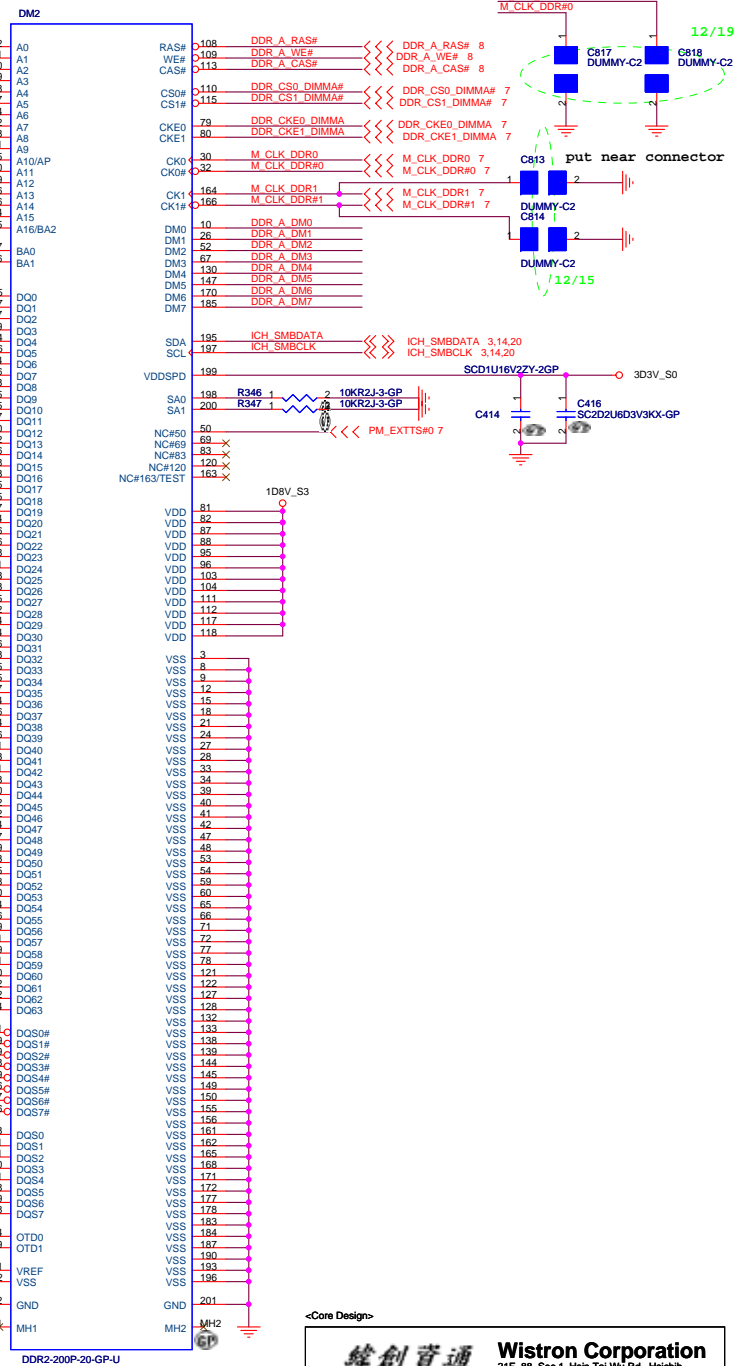
Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9V5



Layout Note:  
Place these resistors closely DM1, all trace length Max=1.5"



Signal	Pin	Signal	Pin
DDR_A_MA0	102	A0	
DDR_A_MA1	101	A1	
DDR_A_MA2	100	A2	
DDR_A_MA3	99	A3	
DDR_A_MA4	98	A4	
DDR_A_MA5	97	A5	
DDR_A_MA6	94	A6	
DDR_A_MA7	92	A7	
DDR_A_MA8	93	A8	
DDR_A_MA9	91	A8	
DDR_A_MA10	105	A9	
DDR_A_MA11	90	A10/AP	
DDR_A_MA12	89	A11	
DDR_A_MA13	116	A12	
DDR_A_MA14	86	A13	
DDR_A_MA15	84	A14	
DDR_A_MA16	85	A15	
DDR_A_MA17	85	A16/BA2	
DDR_A_BS0	107	BA0	
DDR_A_BS1	106	BA1	
DDR_A_D0	5	D00	
DDR_A_D1	7	D01	
DDR_A_D2	17	D02	
DDR_A_D3	19	D03	
DDR_A_D4	4	D04	
DDR_A_D5	6	D05	
DDR_A_D6	14	D06	
DDR_A_D7	16	D07	
DDR_A_D8	23	D08	
DDR_A_D9	25	D09	
DDR_A_D10	35	DQ10	
DDR_A_D11	37	DQ11	
DDR_A_D12	20	DQ12	
DDR_A_D13	22	DQ13	
DDR_A_D14	36	DQ14	
DDR_A_D15	38	DQ15	
DDR_A_D16	43	DQ16	
DDR_A_D17	45	DQ17	
DDR_A_D18	57	DQ18	
DDR_A_D19	57	DQ19	
DDR_A_D20	44	DQ20	
DDR_A_D21	46	DQ21	
DDR_A_D22	56	DQ22	
DDR_A_D23	58	DQ23	
DDR_A_D24	61	DQ24	
DDR_A_D25	63	DQ25	
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DDR_A_D34	135	DQ34	
DDR_A_D35	137	DQ35	
DDR_A_D36	124	DQ36	
DDR_A_D37	126	DQ37	
DDR_A_D38	134	DQ38	
DDR_A_D39	136	DQ39	
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DDR_A_D41	143	DQ41	
DDR_A_D42	151	DQ42	
DDR_A_D43	153	DQ43	
DDR_A_D44	140	DQ44	
DDR_A_D45	142	DQ45	
DDR_A_D46	152	DQ46	
DDR_A_D47	154	DQ47	
DDR_A_D48	157	DQ48	
DDR_A_D49	159	DQ49	
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DDR_A_D51	175	DQ51	
DDR_A_D52	158	DQ52	
DDR_A_D53	174	DQ53	
DDR_A_D54	180	DQ54	
DDR_A_D55	176	DQ55	
DDR_A_D56	179	DQ56	
DDR_A_D57	181	DQ57	
DDR_A_D58	188	DQ58	
DDR_A_D59	181	DQ59	
DDR_A_D60	180	DQ60	
DDR_A_D61	182	DQ61	
DDR_A_D62	192	DQ62	
DDR_A_D63	194	DQ63	
DDR_A_DQS#0	11	DQS0#	
DDR_A_DQS#1	29	DQS1#	
DDR_A_DQS#2	49	DQS2#	
DDR_A_DQS#3	69	DQS3#	
DDR_A_DQS#4	129	DQS4#	
DDR_A_DQS#5	146	DQS5#	
DDR_A_DQS#6	167	DQS6#	
DDR_A_DQS#7	186	DQS7#	
DDR_A_DQS#8	11	DQS8#	
DDR_A_DQS#9	31	DQS9	
DDR_A_DQS#10	51	DQS10	
DDR_A_DQS#11	70	DQS11	
DDR_A_DQS#12	131	DQS12	
DDR_A_DQS#13	148	DQS13	
DDR_A_DQS#14	169	DQS14	
DDR_A_DQS#15	188	DQS15	
DDR_A_DQS#16	114	ODT0	
DDR_A_DQS#17	119	ODT1	
DDR_A_DQS#18	114	ODT0	
DDR_A_DQS#19	119	ODT1	



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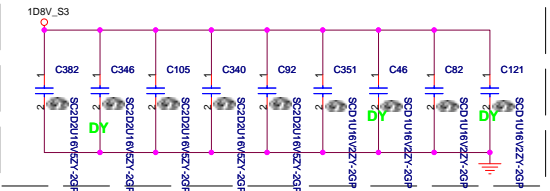
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Size: Custom Document Number: Pamirs Rev: SC

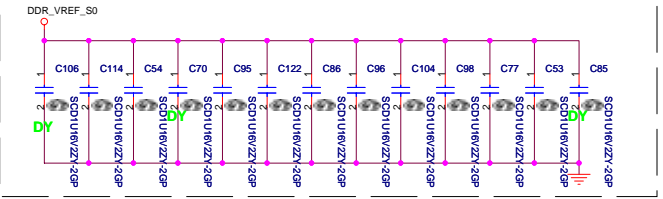
Date: Tuesday, December 19, 2006 Sheet 13 of 41

- 8 DDR\_B\_DQS#0..7 <<<>
- 8 DDR\_B\_DQ0..63 <<>
- 8 DDR\_B\_DM0..7 <<>
- 8 DDR\_B\_DQS#0..7 <<>
- 8 DDR\_B\_MA0..13 <<>
- 8 DDR\_B\_BS0..2 <<>

Layout Note:  
Place near DM2



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9VS

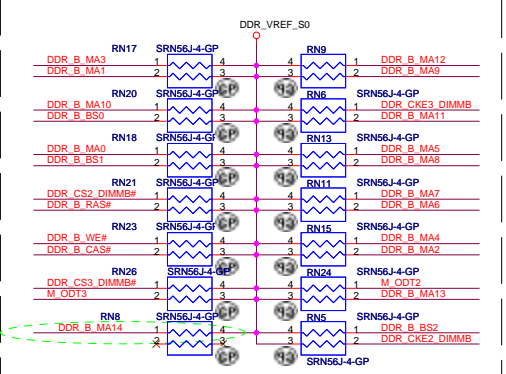
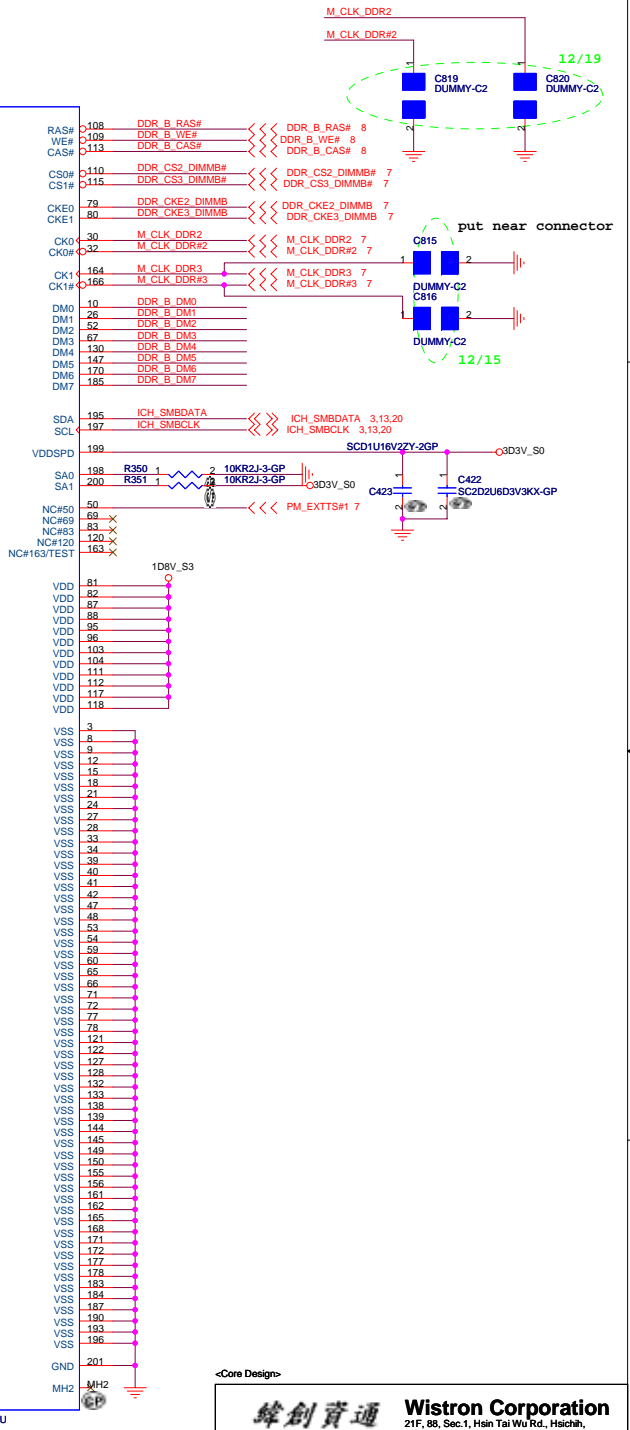
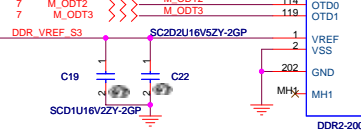


DDR_B_MA0	102	A0
DDR_B_MA1	101	A1
DDR_B_MA2	100	A2
DDR_B_MA3	99	A3
DDR_B_MA4	98	A4
DDR_B_MA5	97	A5
DDR_B_MA6	96	A6
DDR_B_MA7	95	A7
DDR_B_MA8	94	A8
DDR_B_MA9	93	A9
DDR_B_MA10	92	A10/AP
DDR_B_MA11	91	A11
DDR_B_MA12	90	A12
DDR_B_MA13	89	A13
DDR_B_MA14	88	A14
DDR_B_MA14	84	A15
DDR_B_BS2	85	A16/BA2
DDR_B_BS0	107	BA0
DDR_B_BS1	106	BA1

DDR_B_D0	5	DQ0
DDR_B_D1	7	DQ1
DDR_B_D2	17	DQ2
DDR_B_D3	19	DQ3
DDR_B_D4	4	DQ4
DDR_B_D5	6	DQ5
DDR_B_D6	14	DQ6
DDR_B_D7	16	DQ7
DDR_B_D8	23	DQ8
DDR_B_D9	25	DQ9
DDR_B_D10	45	DQ10
DDR_B_D11	37	DQ11
DDR_B_D12	20	DQ12
DDR_B_D13	22	DQ13
DDR_B_D14	36	DQ14
DDR_B_D15	38	DQ15
DDR_B_D16	14	DQ16
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DDR_B_D20	44	DQ20
DDR_B_D21	46	DQ21
DDR_B_D22	58	DQ22
DDR_B_D23	58	DQ23
DDR_B_D24	61	DQ24
DDR_B_D25	63	DQ25
DDR_B_D26	73	DQ26
DDR_B_D27	75	DQ27
DDR_B_D28	62	DQ28
DDR_B_D29	62	DQ29
DDR_B_D30	74	DQ30
DDR_B_D31	76	DQ31
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DDR_B_D34	135	DQ34
DDR_B_D35	137	DQ35
DDR_B_D36	124	DQ36
DDR_B_D37	126	DQ37
DDR_B_D38	134	DQ38
DDR_B_D39	136	DQ39
DDR_B_D40	141	DQ40
DDR_B_D41	143	DQ41
DDR_B_D42	151	DQ42
DDR_B_D43	153	DQ43
DDR_B_D44	140	DQ44
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DDR_B_D48	157	DQ48
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DDR_B_D50	173	DQ50
DDR_B_D51	175	DQ51
DDR_B_D52	158	DQ52
DDR_B_D53	160	DQ53
DDR_B_D54	174	DQ54
DDR_B_D55	176	DQ55
DDR_B_D56	179	DQ56
DDR_B_D57	181	DQ57
DDR_B_D58	189	DQ58
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DDR_B_D61	182	DQ61
DDR_B_D62	192	DQ62
DDR_B_D63	194	DQ63

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DDR_B_D1	7	DQ1
DDR_B_D2	17	DQ2
DDR_B_D3	19	DQ3
DDR_B_D4	4	DQ4
DDR_B_D5	6	DQ5
DDR_B_D6	14	DQ6
DDR_B_D7	16	DQ7
DDR_B_D8	23	DQ8
DDR_B_D9	25	DQ9
DDR_B_D10	45	DQ10
DDR_B_D11	37	DQ11
DDR_B_D12	20	DQ12
DDR_B_D13	22	DQ13
DDR_B_D14	36	DQ14
DDR_B_D15	38	DQ15
DDR_B_D16	14	DQ16
DDR_B_D17	45	DQ17
DDR_B_D18	55	DQ18
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DDR_B_D20	44	DQ20
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DDR_B_D26	73	DQ26
DDR_B_D27	75	DQ27
DDR_B_D28	62	DQ28
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DDR_B_D34	135	DQ34
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DDR_B_D59	190	DQ59
DDR_B_D60	180	DQ60
DDR_B_D61	182	DQ61
DDR_B_D62	192	DQ62
DDR_B_D63	194	DQ63

DDR_B_DQS0	114	DQS0#
DDR_B_DQS#1	29	DQS1#
DDR_B_DQS#2	49	DQS2#
DDR_B_DQS#3	68	DQS3#
DDR_B_DQS#4	129	DQS4#
DDR_B_DQS#5	146	DQS5#
DDR_B_DQS#6	167	DQS6#
DDR_B_DQS#7	186	DQS7#
DDR_B_DQS0	13	DQS0
DDR_B_DQS1	31	DQS1
DDR_B_DQS2	51	DQS2
DDR_B_DQS3	70	DQS3
DDR_B_DQS4	131	DQS4
DDR_B_DQS5	148	DQS5
DDR_B_DQS6	169	DQS6
DDR_B_DQS7	188	DQS7



Layout Note:  
Place these resistors closely DM2, all trace length Max=1.5"

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

Title: **DDR2-200P-21-GP-U**

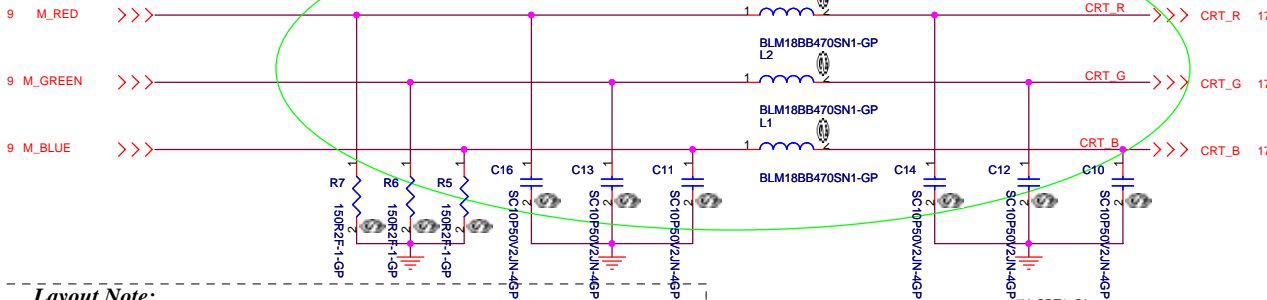
Size: Document Number  
Custom: Pamirs  
Date: Tuesday, December 19, 2006 Sheet 14 of 41

Rev: SC



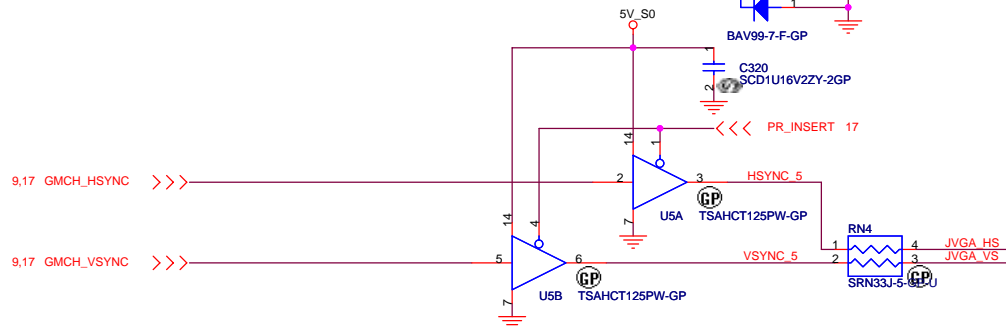
# CRT I/F & CONNECTOR

Layout Note:  
Place these resistors  
close to the CRT-out  
connector



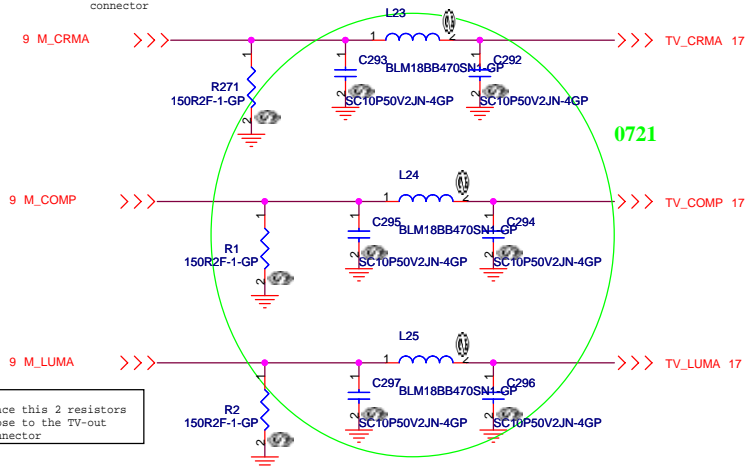
**Layout Note:**  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift



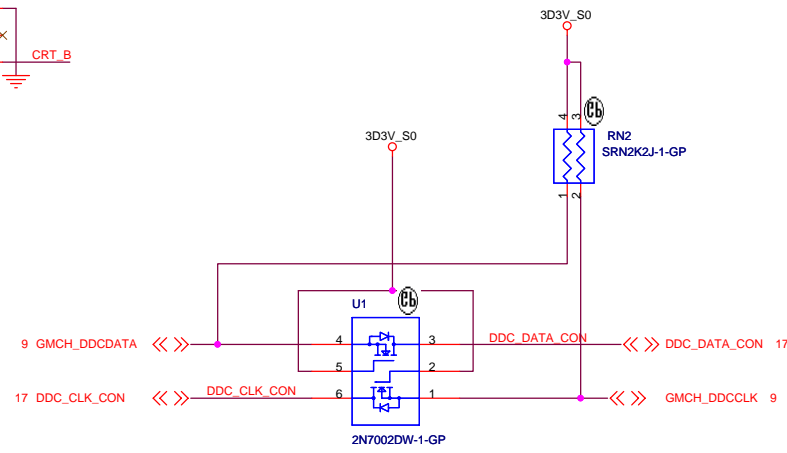
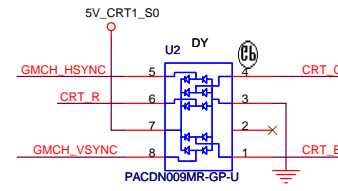
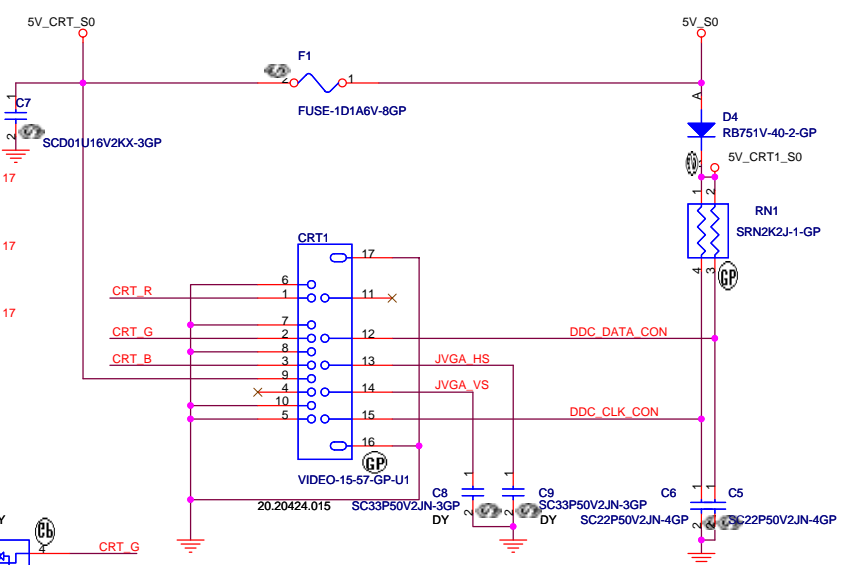
## TV OUT CONN

connector

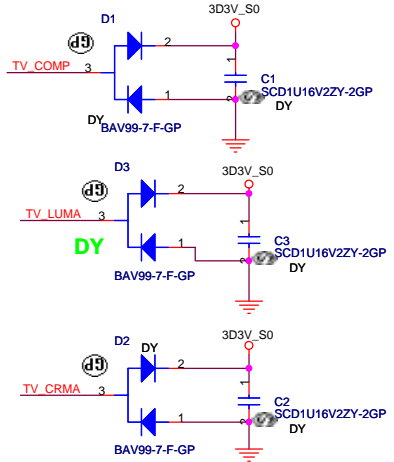
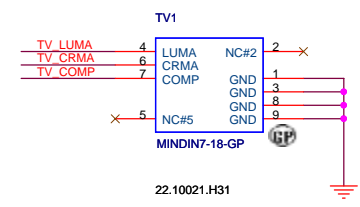


Place this 2 resistors  
close to the TV-out  
connector

0721



5V @ ext. CRT side



<Core Design>

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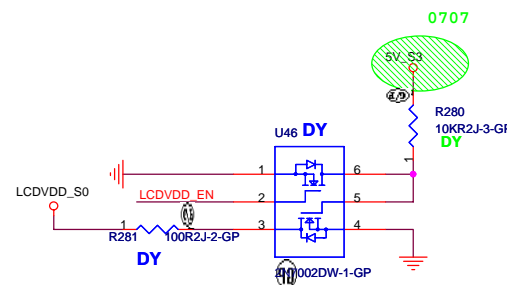
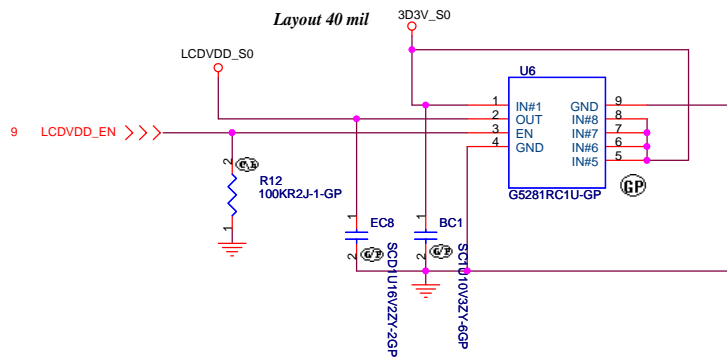
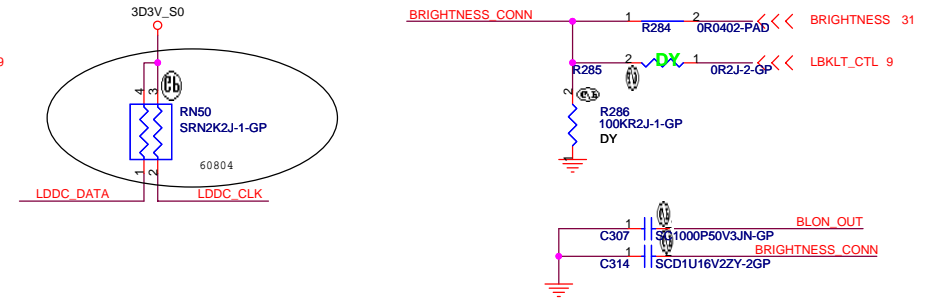
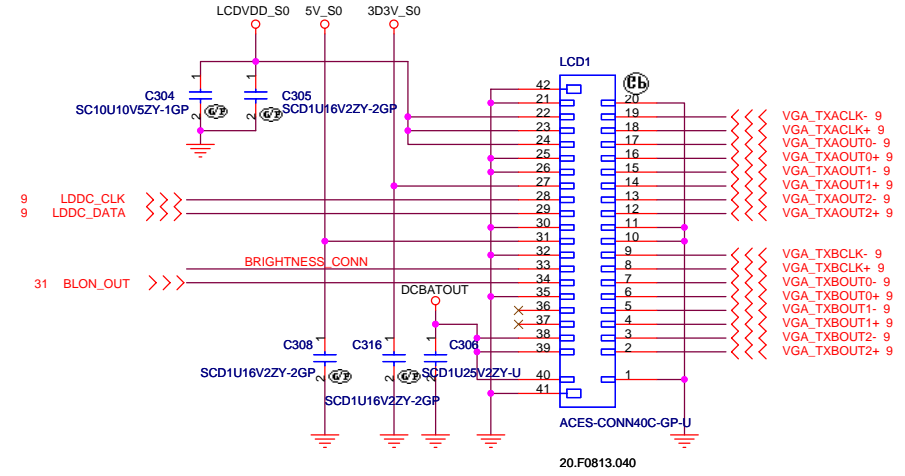
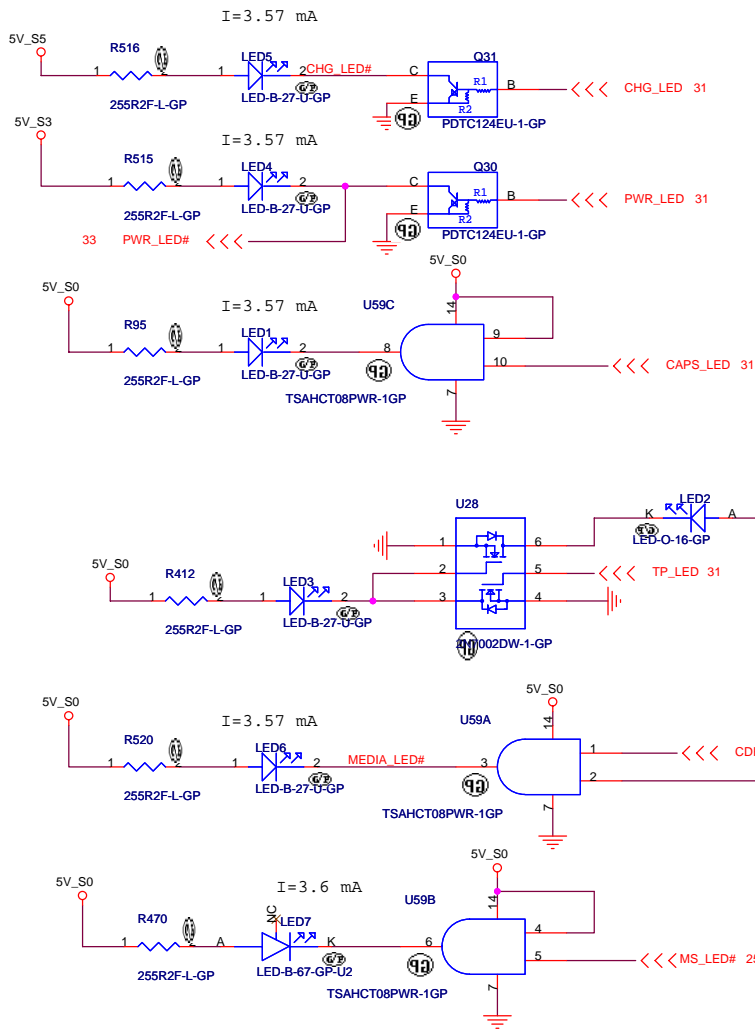
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Size A3 Document Number: **Pamirs** Rev: **SC**

Date: Friday, December 15, 2006 Sheet 15 of 41

# LED / INVERTER INTERFACE

## LCD/INV CONN

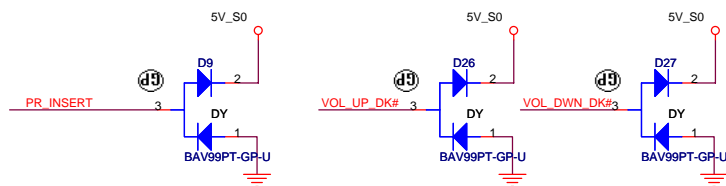


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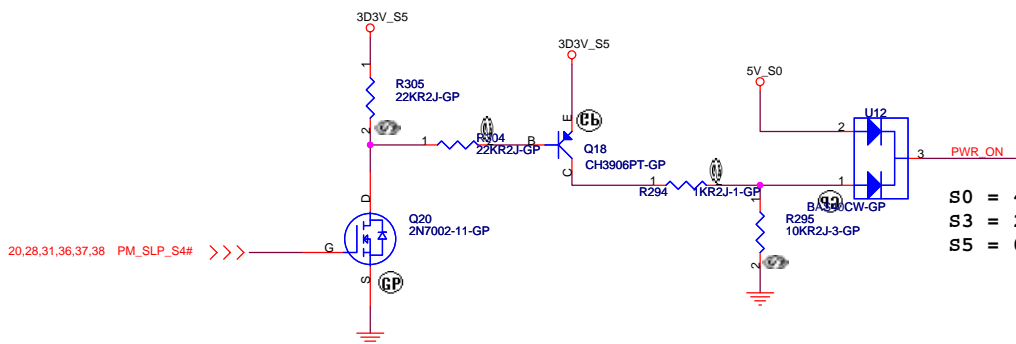
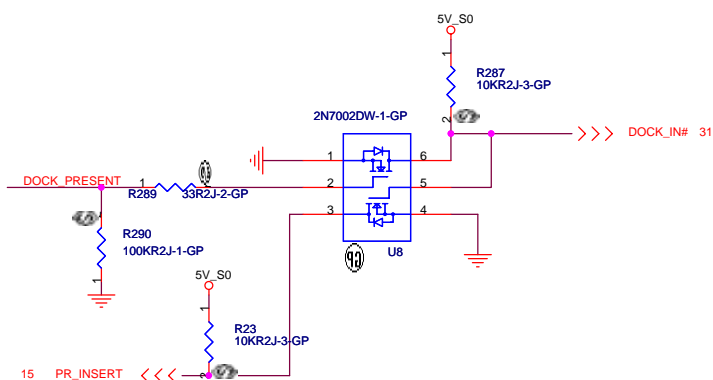
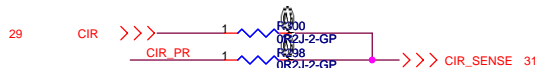
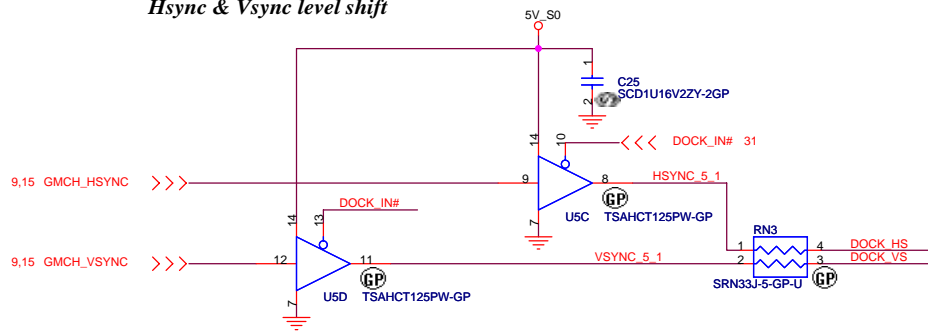
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>LCD/Inverter Connector</b>			
Size	Document Number	Rev	
Custom		SC	
Date:	Tuesday, December 19, 2006	Sheet	16 of 41

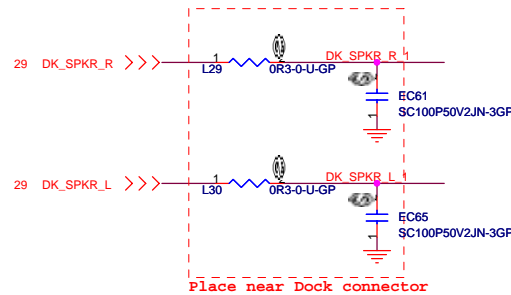
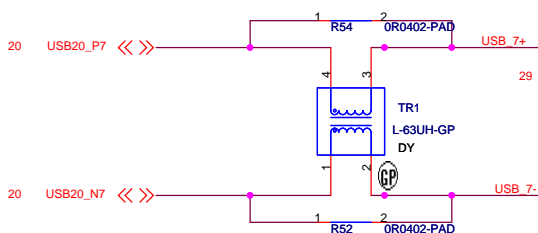
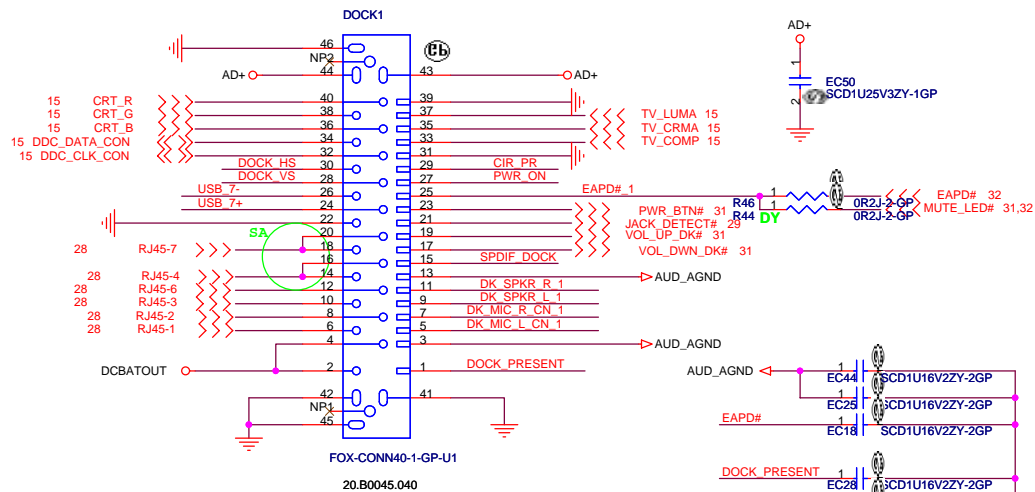
# Docking Connector



## Hsync & Vsync level shift



S0 = 4V  
S3 = 2.5V  
S5 = 0V

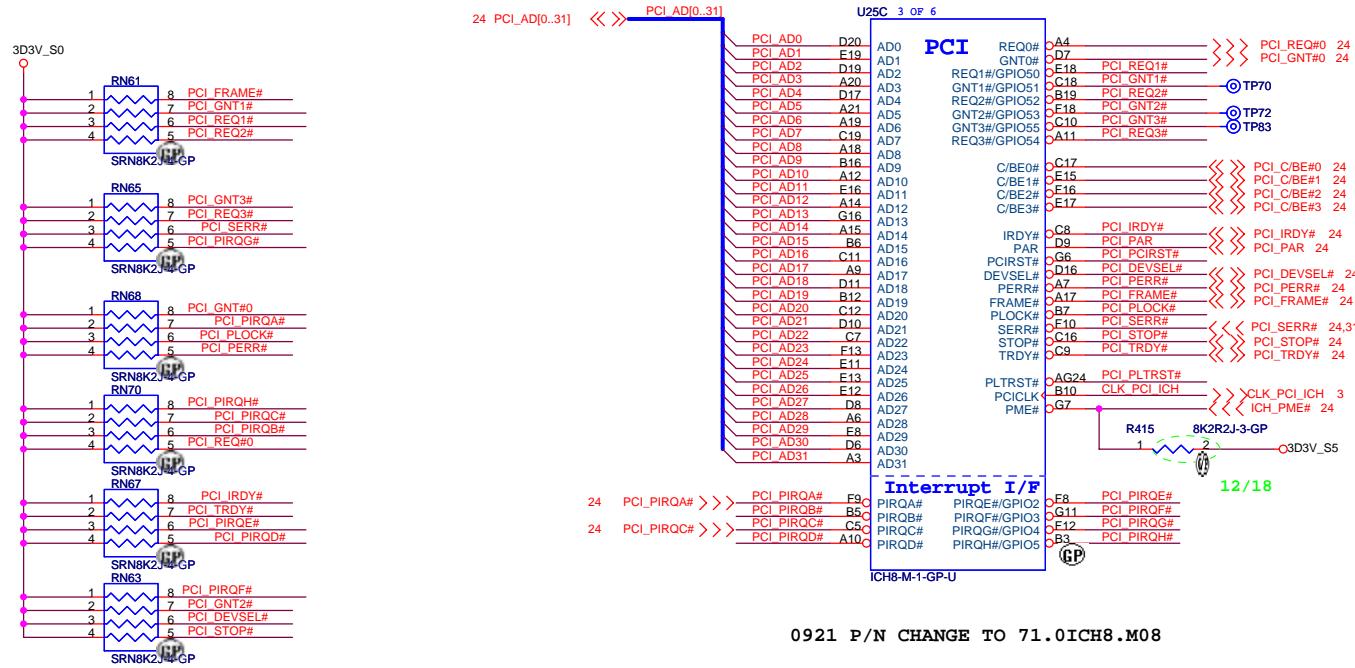


Place near Dock connector

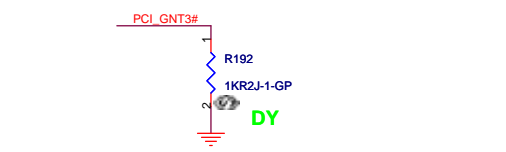
Place near Codec

<Core Design>

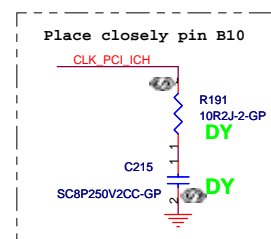
<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Board to board conn/ Docking</b>	
Title	Rev
Size	SC
A3	Document Number
<b>Pamirs</b>	
Date: Friday, December 15, 2006	Sheet 17 of 41



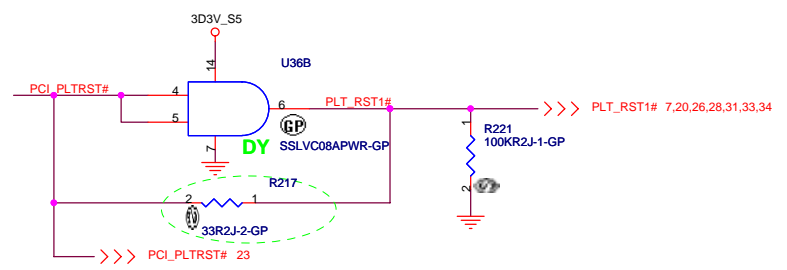
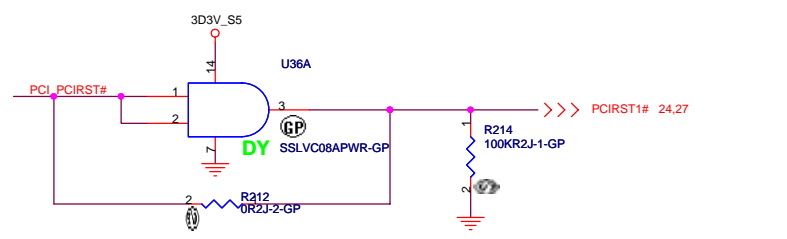
0921 P/N CHANGE TO 71.0ICH8.M08



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



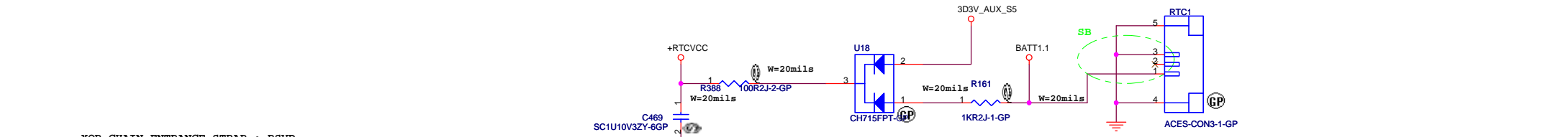
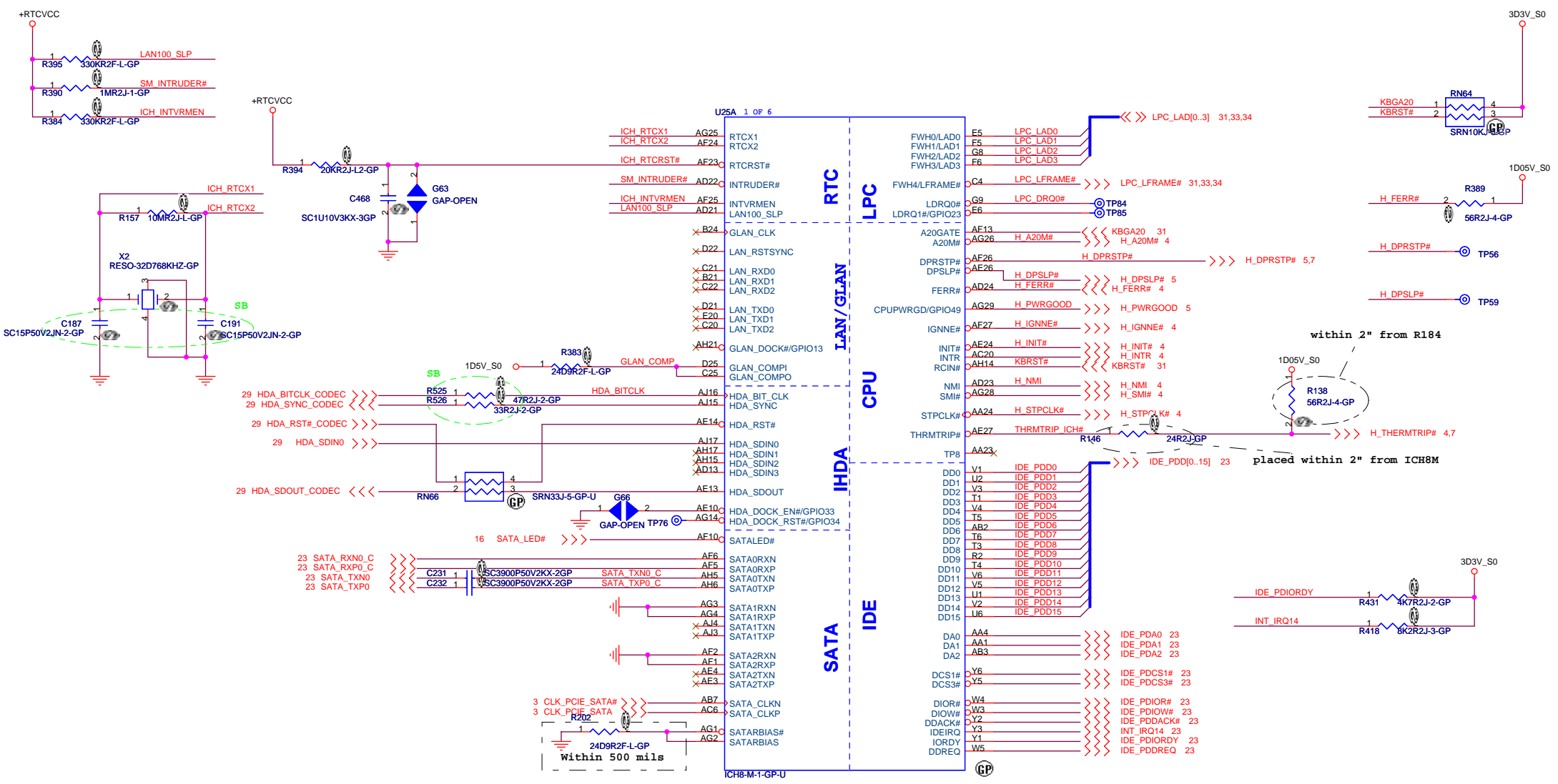
<Core Design>

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Title: ICH8(1/4)-PCI/INT

Size: A3 Document Number: Pamris Rev: SC

Date: Monday, December 18, 2006 Sheet: 18 of 41



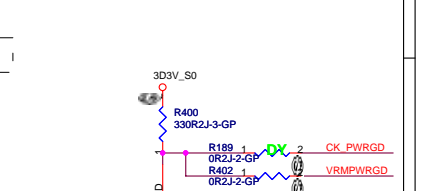
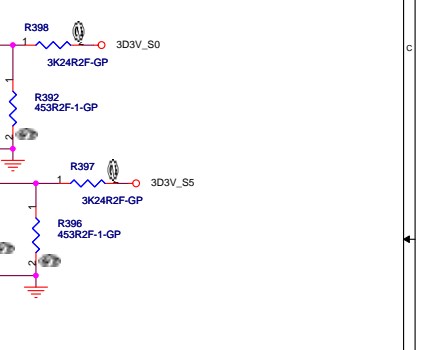
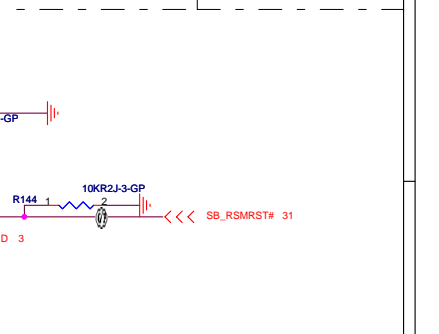
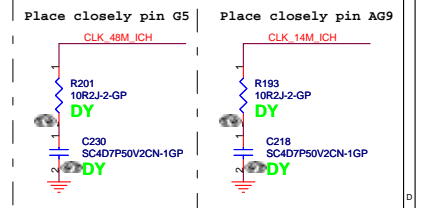
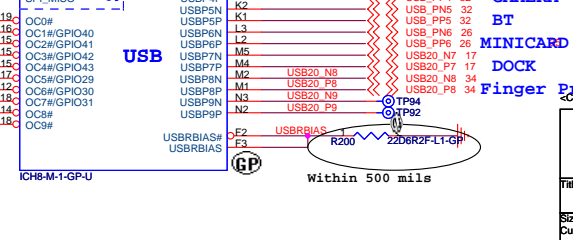
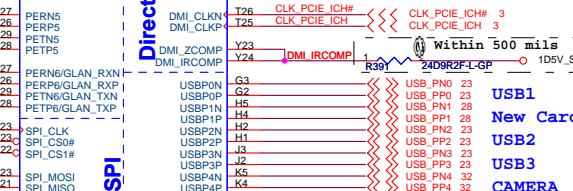
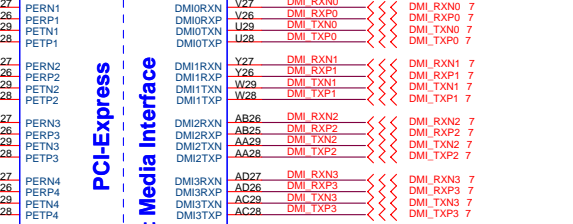
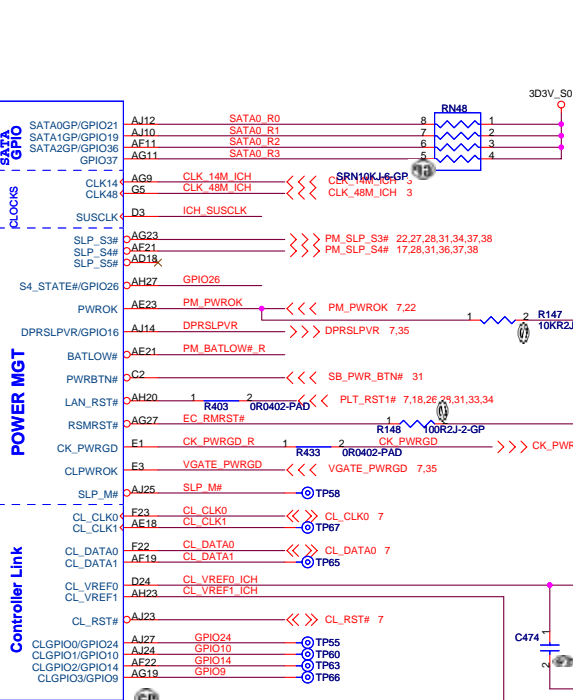
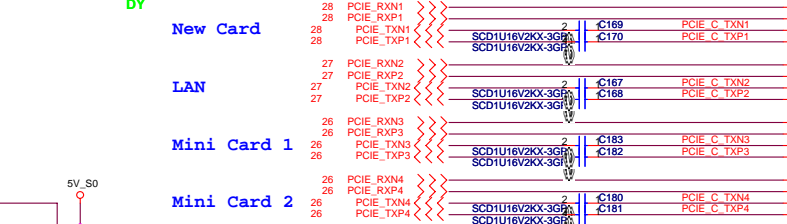
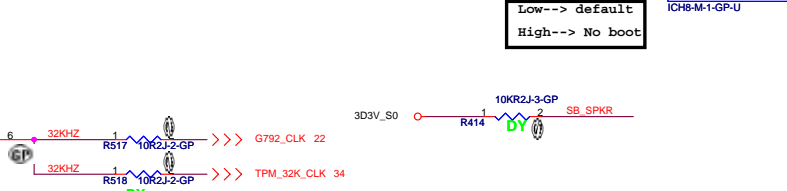
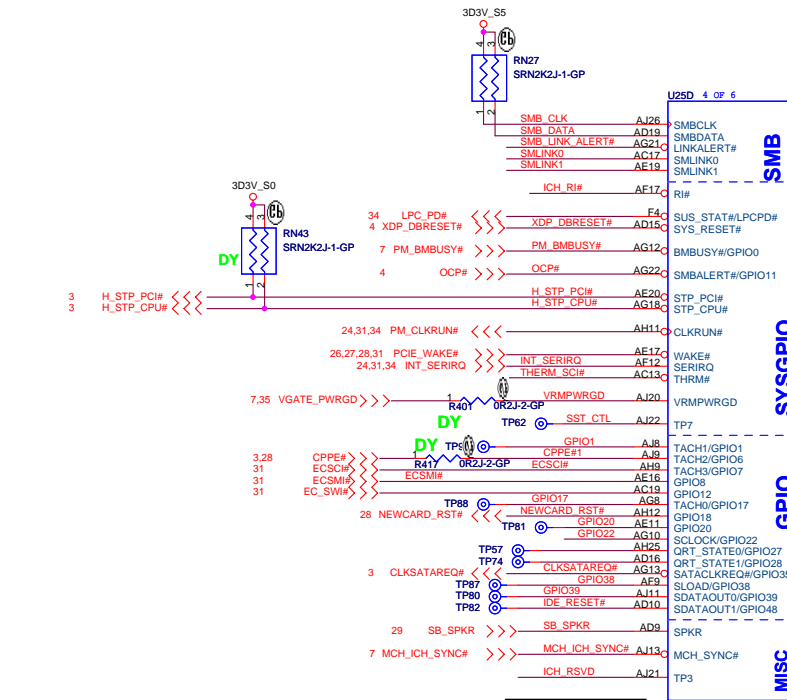
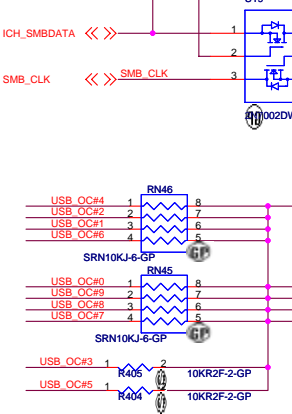
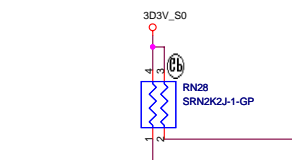
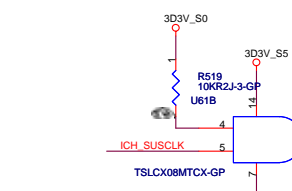
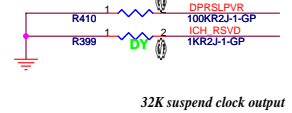
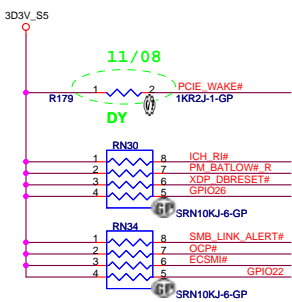
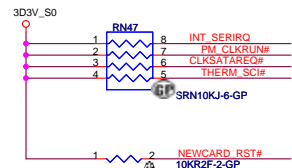
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Title: **ICH8(2/4) LAN,HD,IDE,LPC**

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Wistron Corporation logo and contact information, including address and phone number.

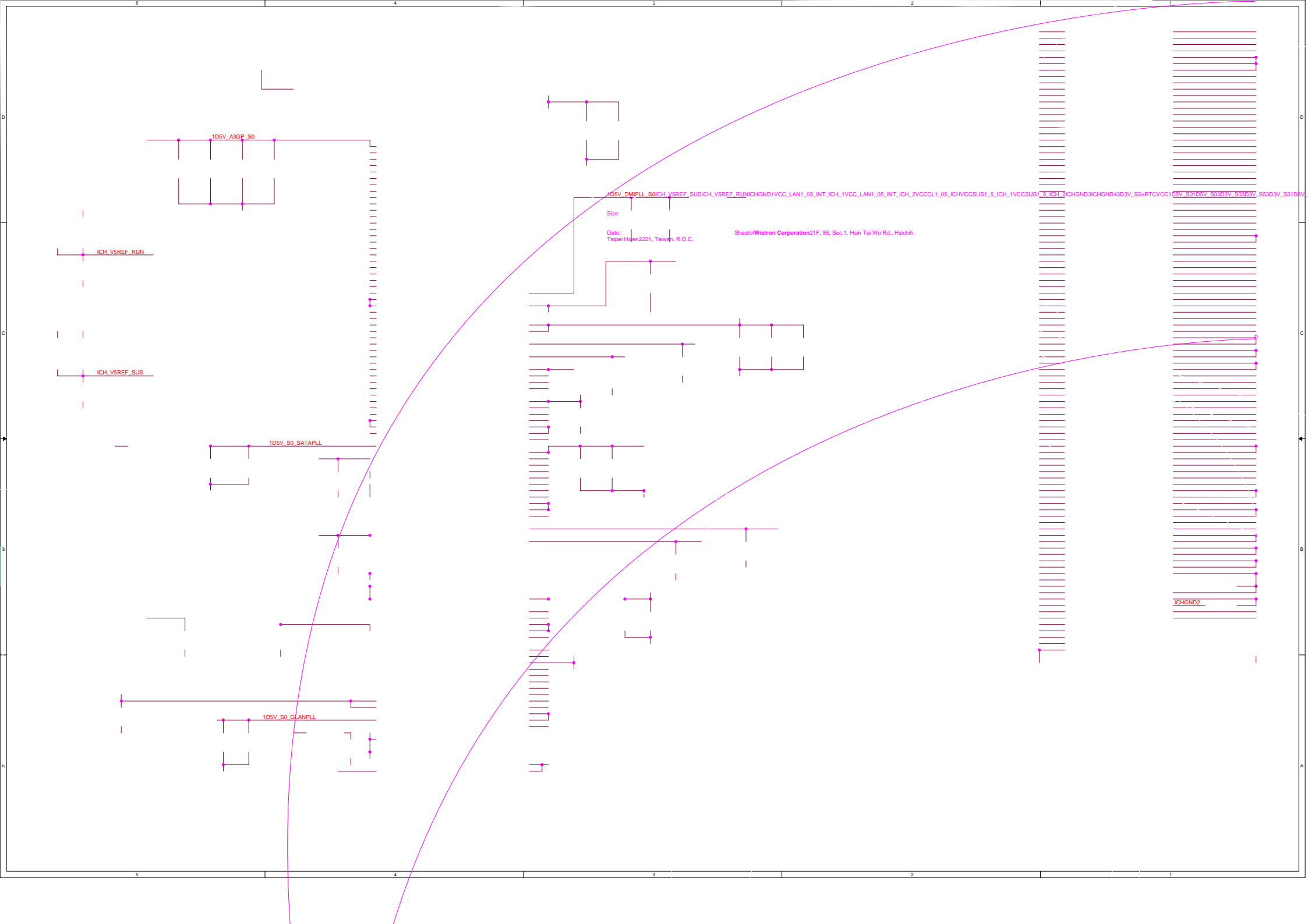
Low--> default  
High--> No boot

Within 500 mils

Within 500 mils

Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.





1D5V\_A3GP\_S0

1D5V\_DMIPLL\_S0ICH\_V5REF\_SUSICH\_V5REF\_RUNICHGND1VCC\_LAN1\_05\_INT\_ICH\_1VCC\_LAN1\_05\_INT\_ICH\_2VCCCL1\_05\_ICHVCCSUS1\_5\_ICH\_1VCCSUS1\_5\_ICH\_2ICHGND3ICHGND43D3V\_S5+RTCVC10D5V\_S01D5V\_S03D3V\_S03D3V\_S53D3V\_S51D5V

Size

Date:  
Taipei Hsien2221, Taiwan, R.O.C.

Sheet of Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

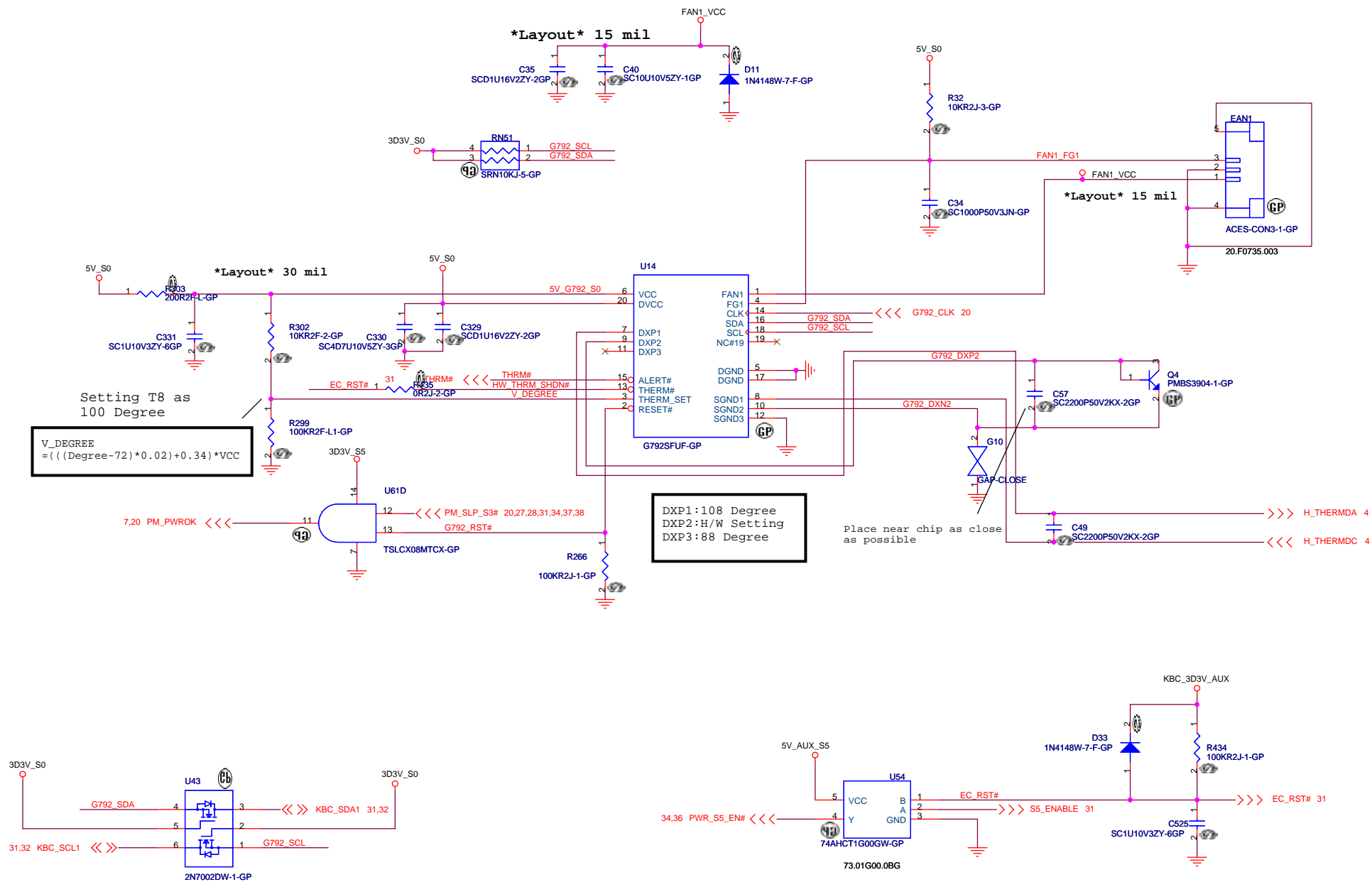
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ICH\_V5REF\_SUS

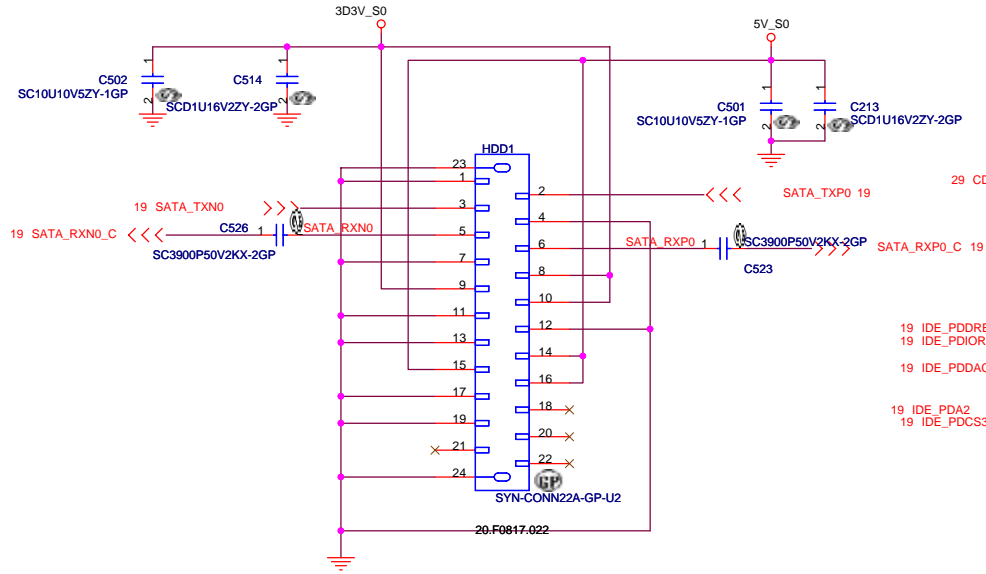
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1D5V\_S0\_GLANPLL

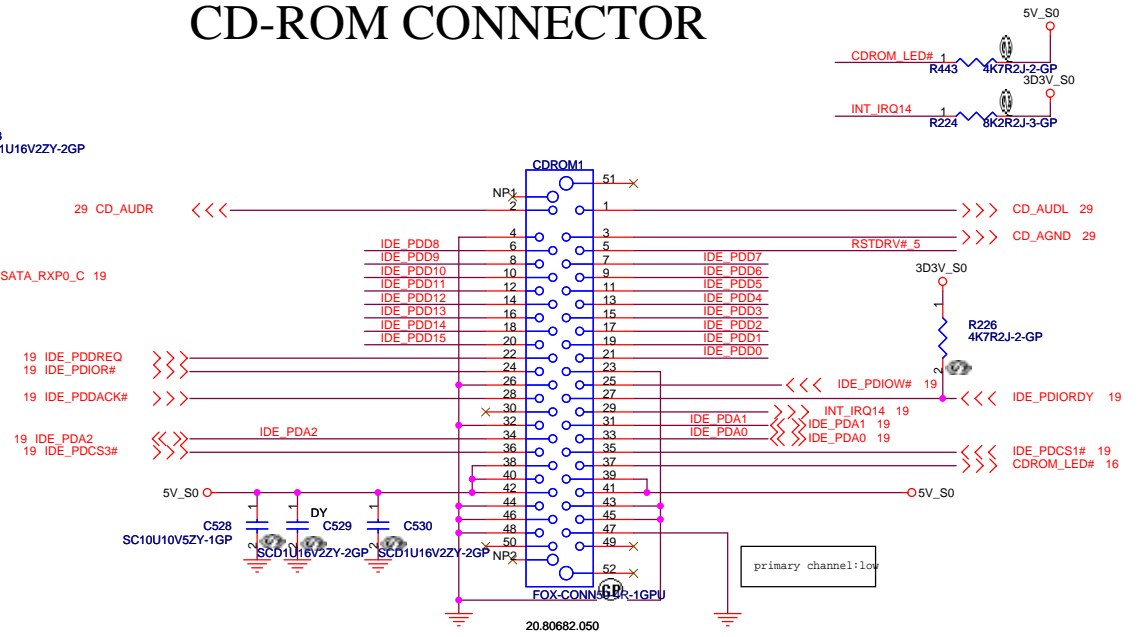
ICHGND2



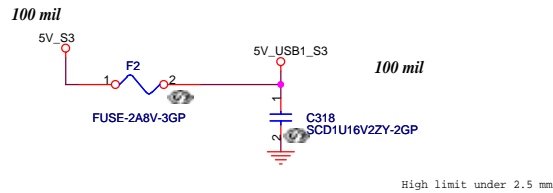
# SATA HD Connector



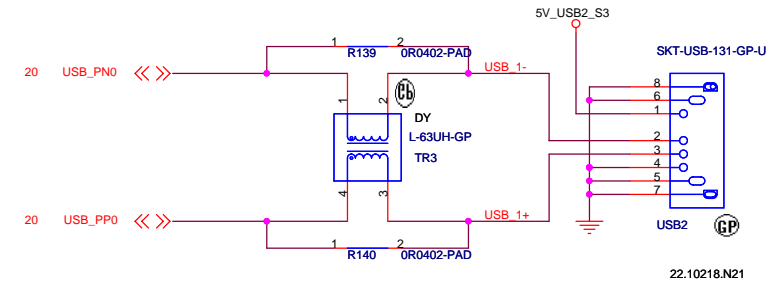
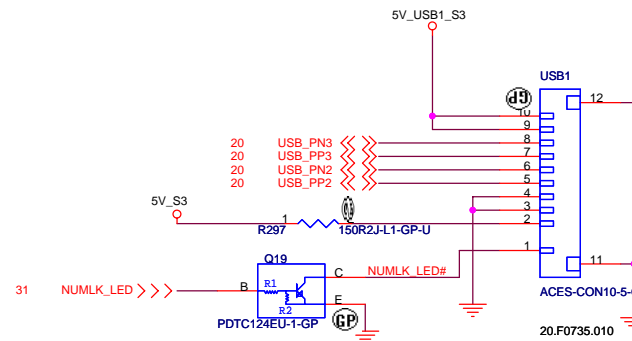
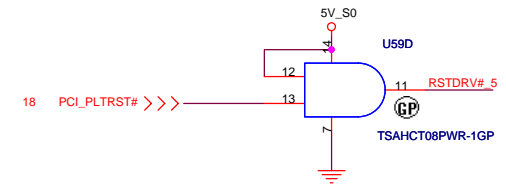
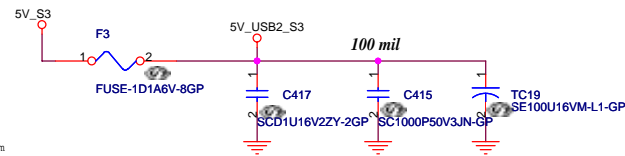
# CD-ROM CONNECTOR



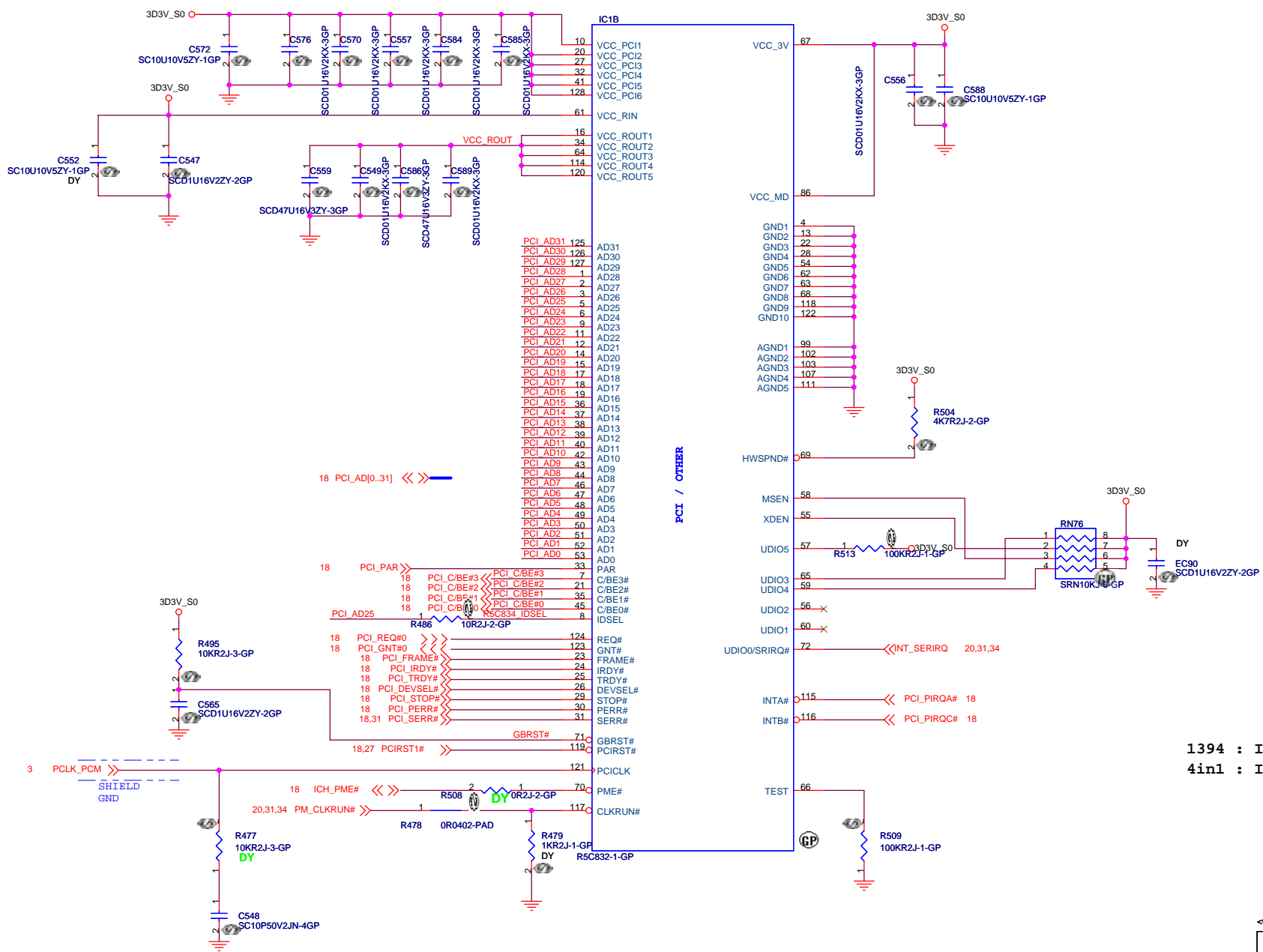
# USB PORT



High limit under 2.5 mm



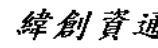
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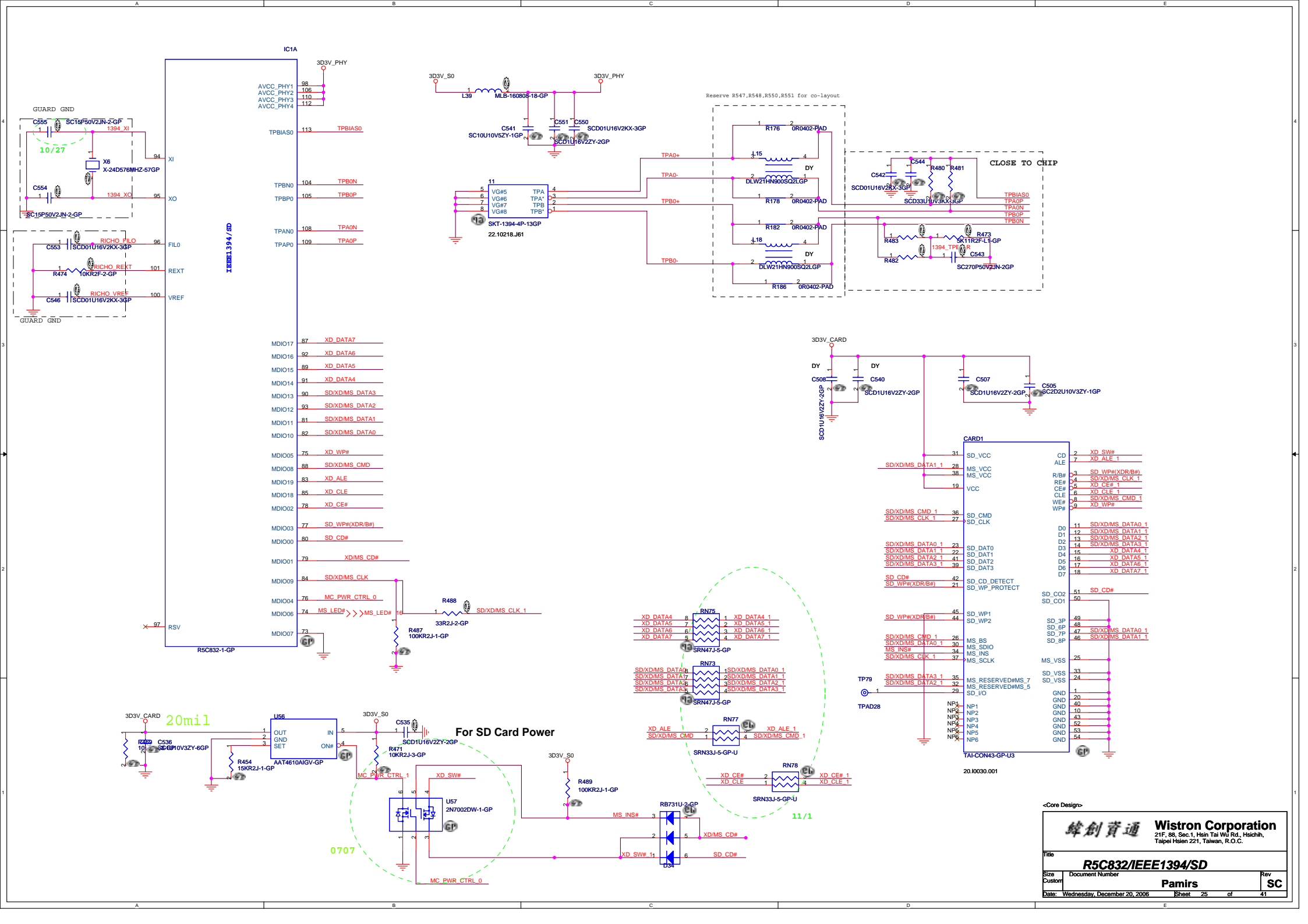


PCI / OTHER

1394 : INTA#  
4in1 : INTB#

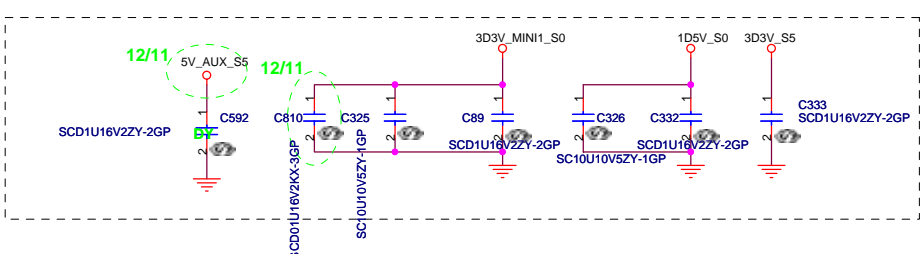
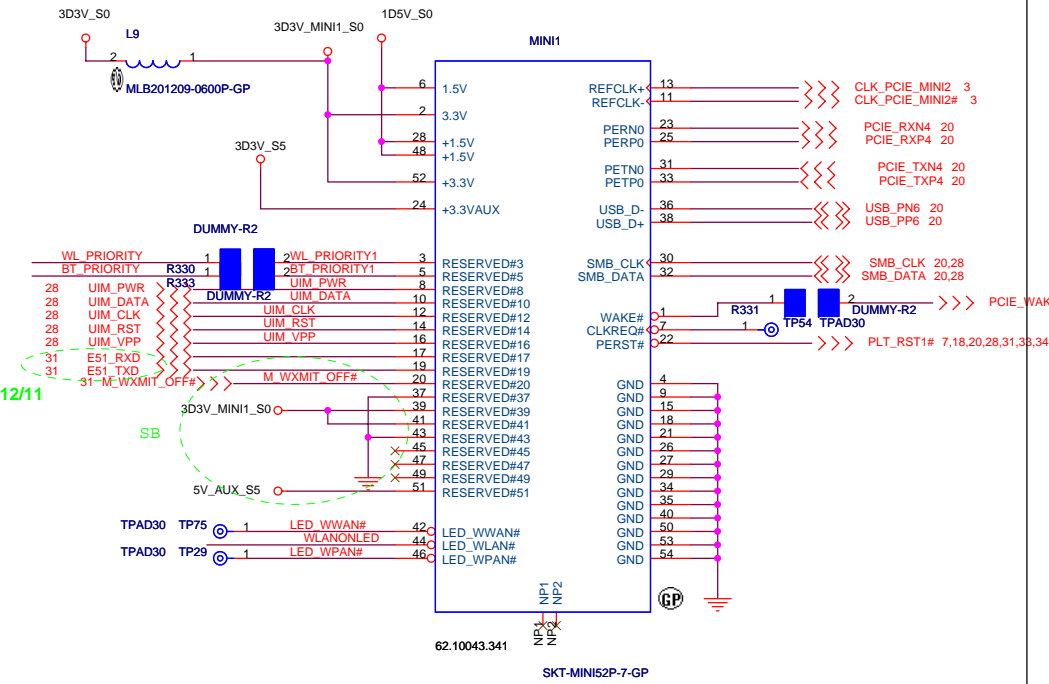
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<b>R5C832/PCI</b>	
Title <b>R5C832/PCI</b>	Rev <b>SC</b>
Size A3	Document Number <b>Pamirs</b>
Date: Monday, December 18, 2006	Sheet 24 of 41

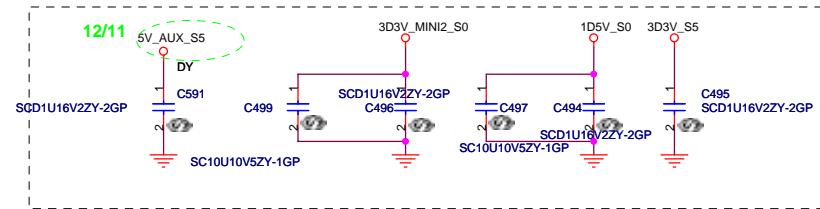
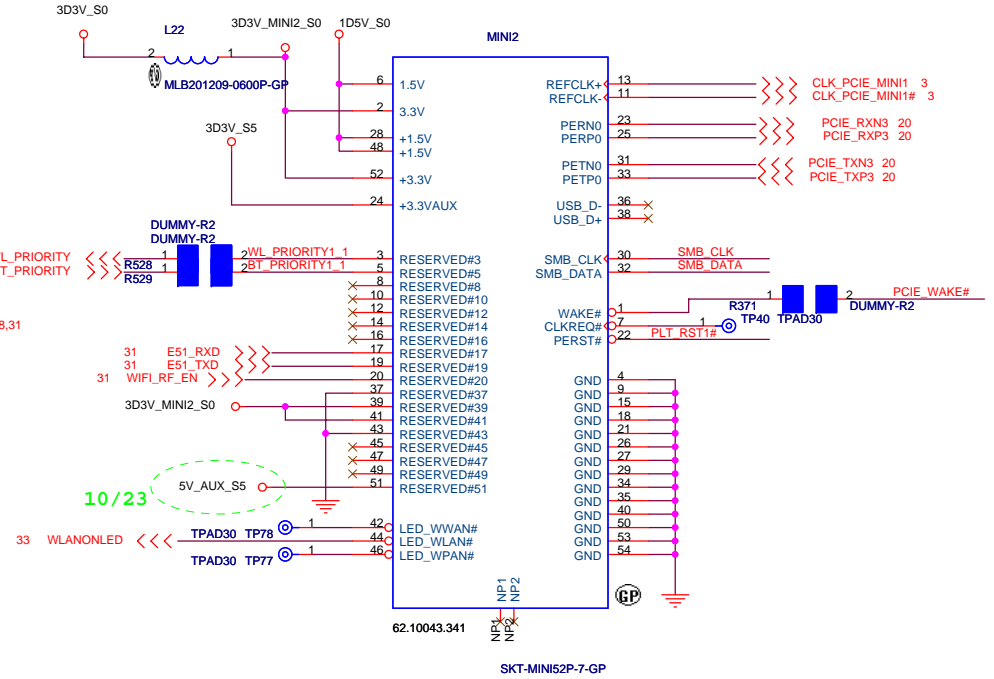


# Mini Card Connector

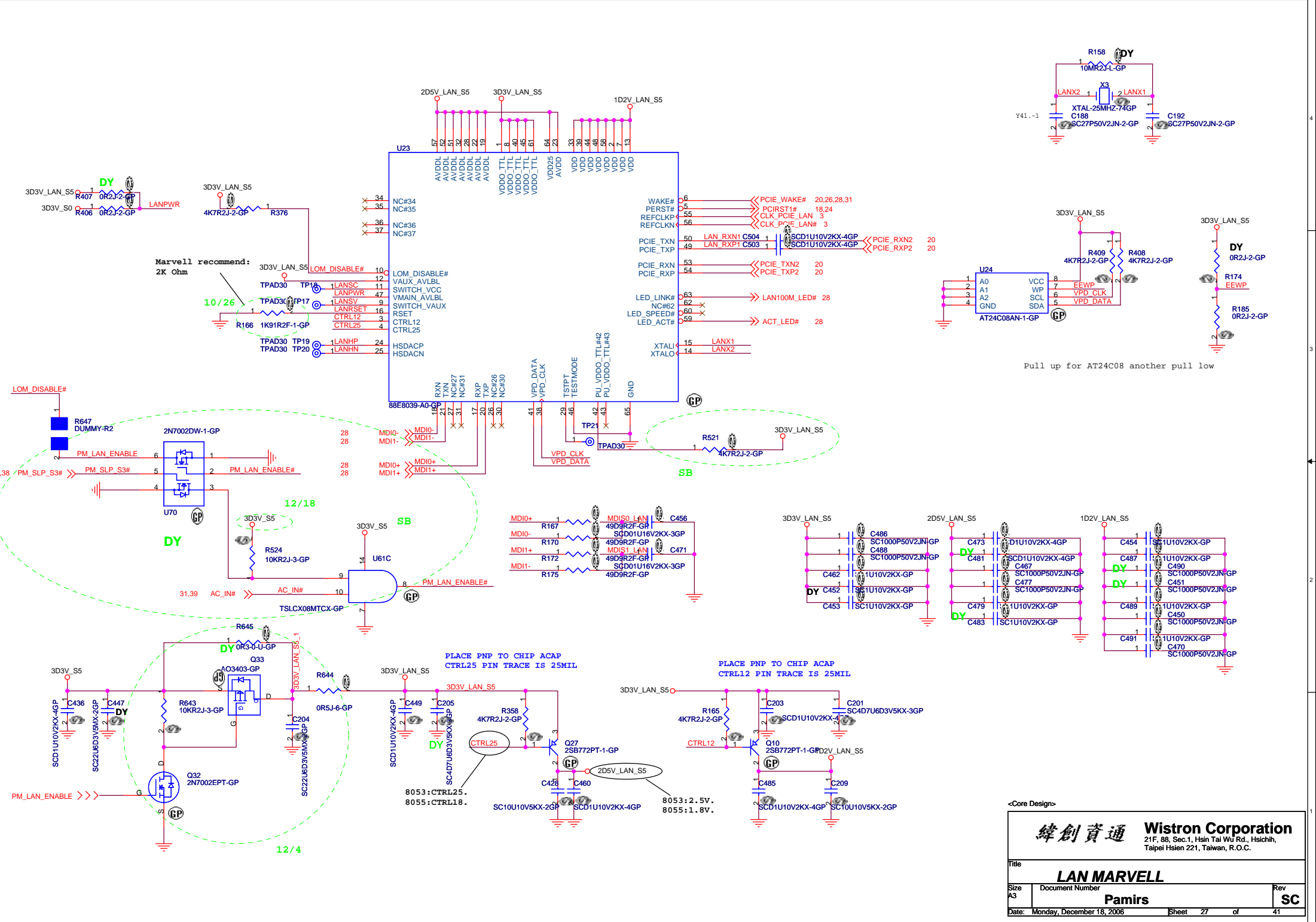
## Mini Card Connector 1(WWAN)



# Mini Card Connector 2(802.11a/b/g)







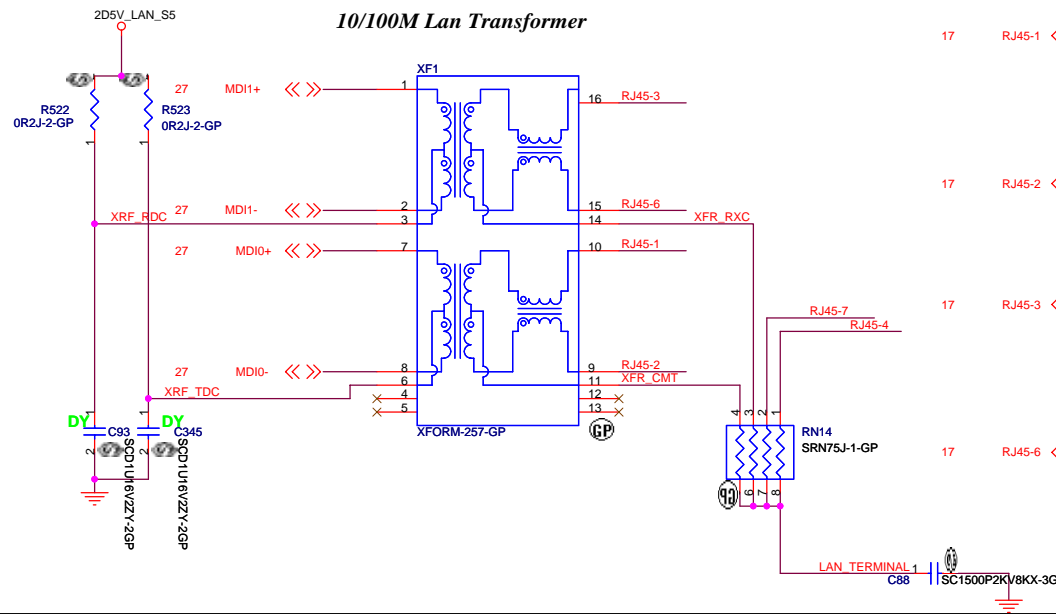
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN MARVELL**

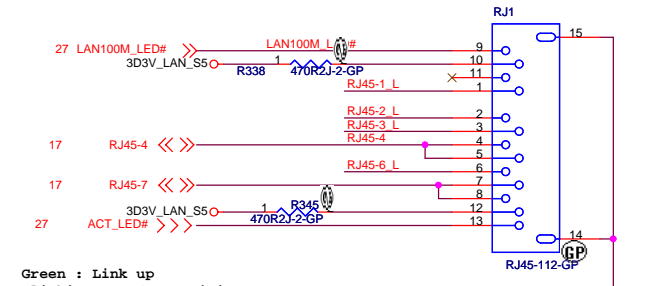
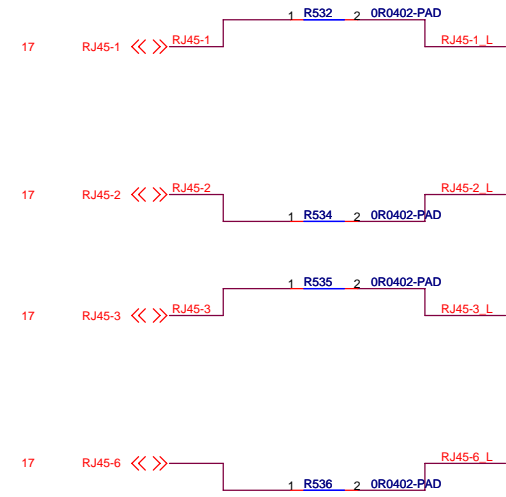
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1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

PIN09 : GREEN  
PIN11 : ORANGE  
PIN13 : YELLOW

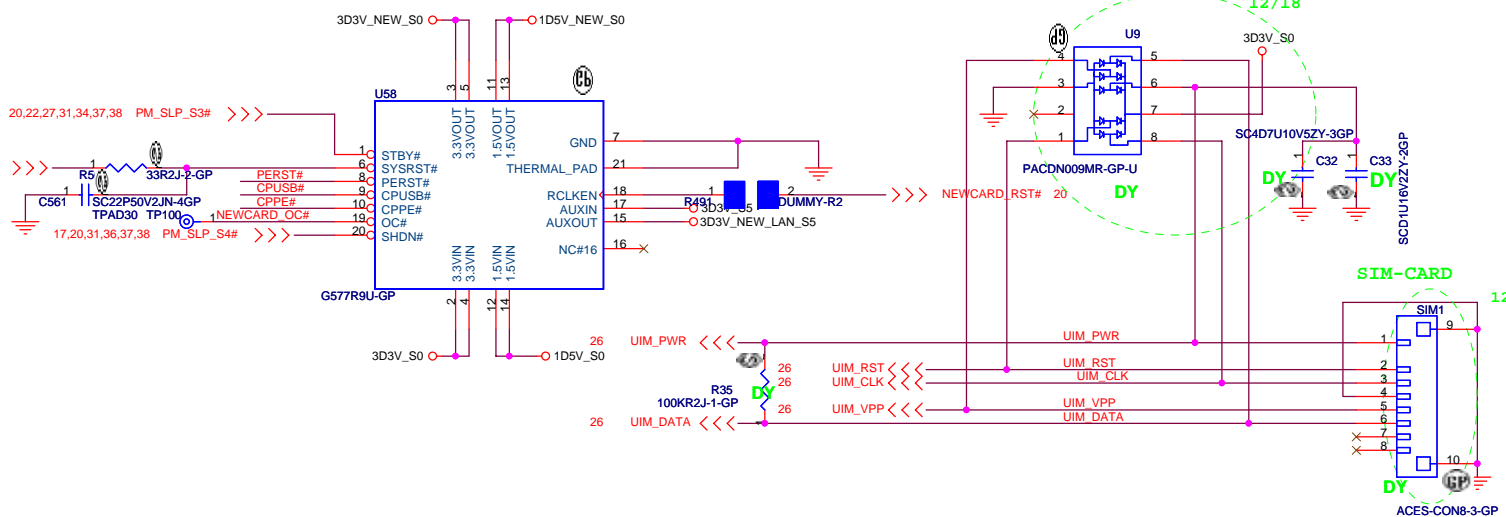
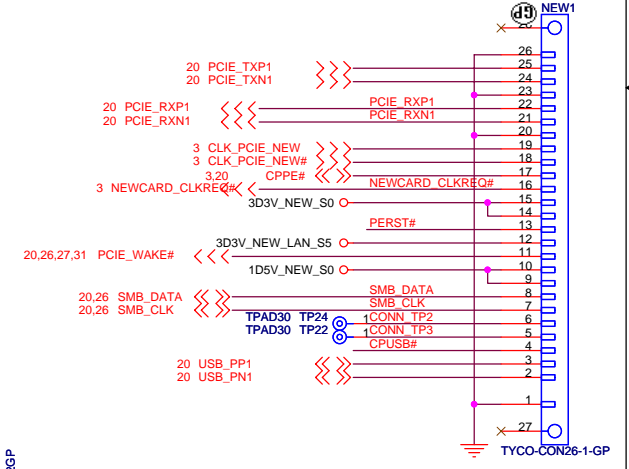
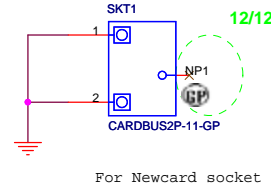
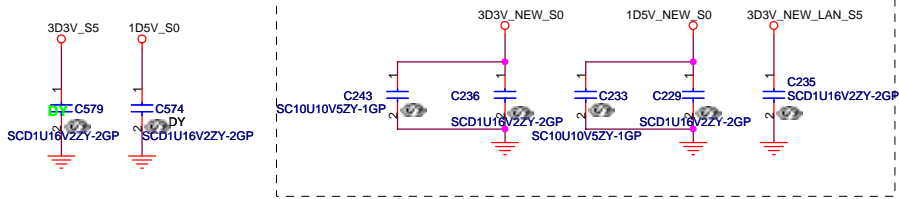


Green : Link up  
Blinking : TX/RX activity

### NEWCARD Connector

Place them Near to Connector

Place them Near to Chip

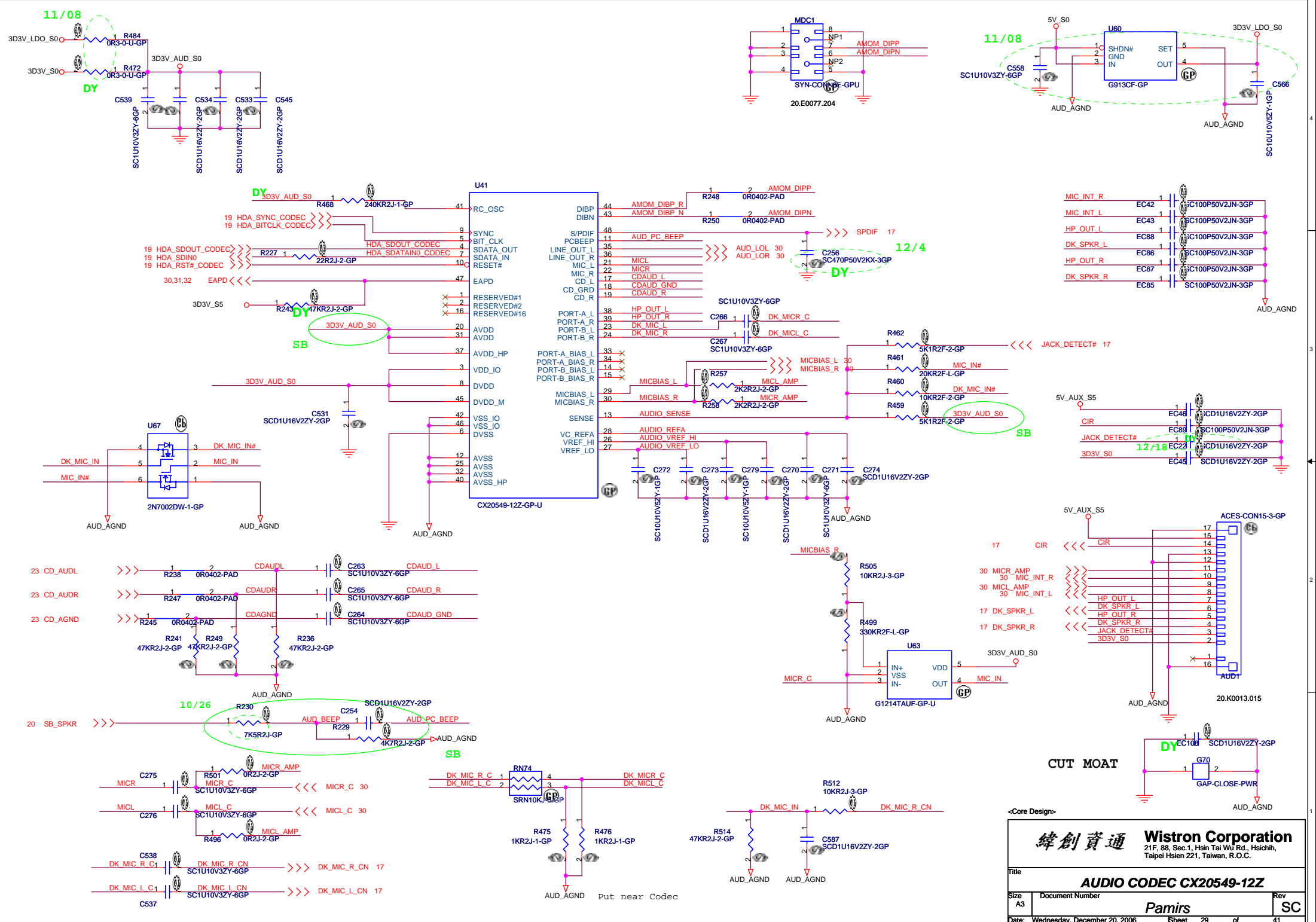


<Core Design>

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Title: **LAN connector/NEW CARD/SIM**

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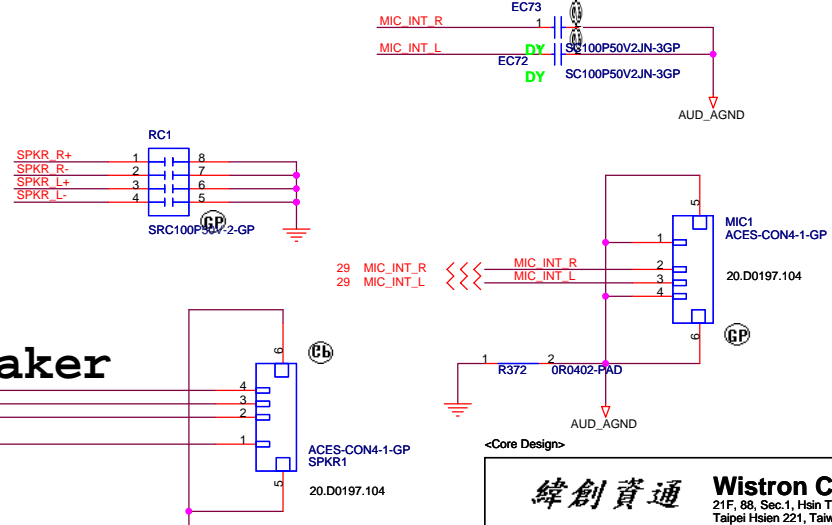
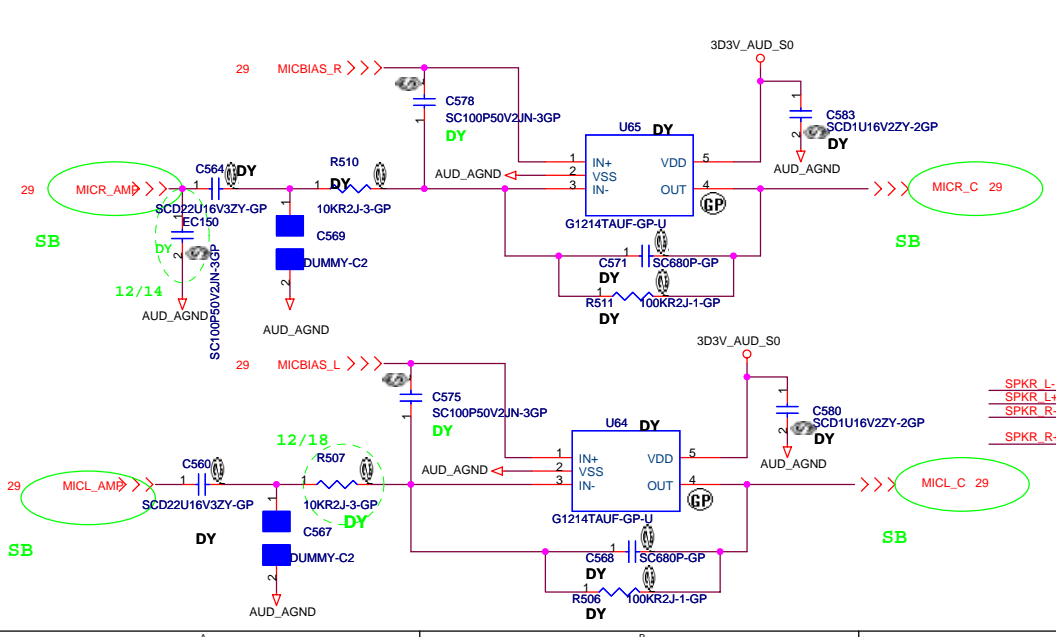
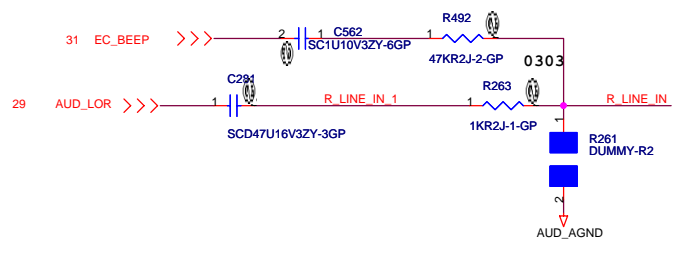
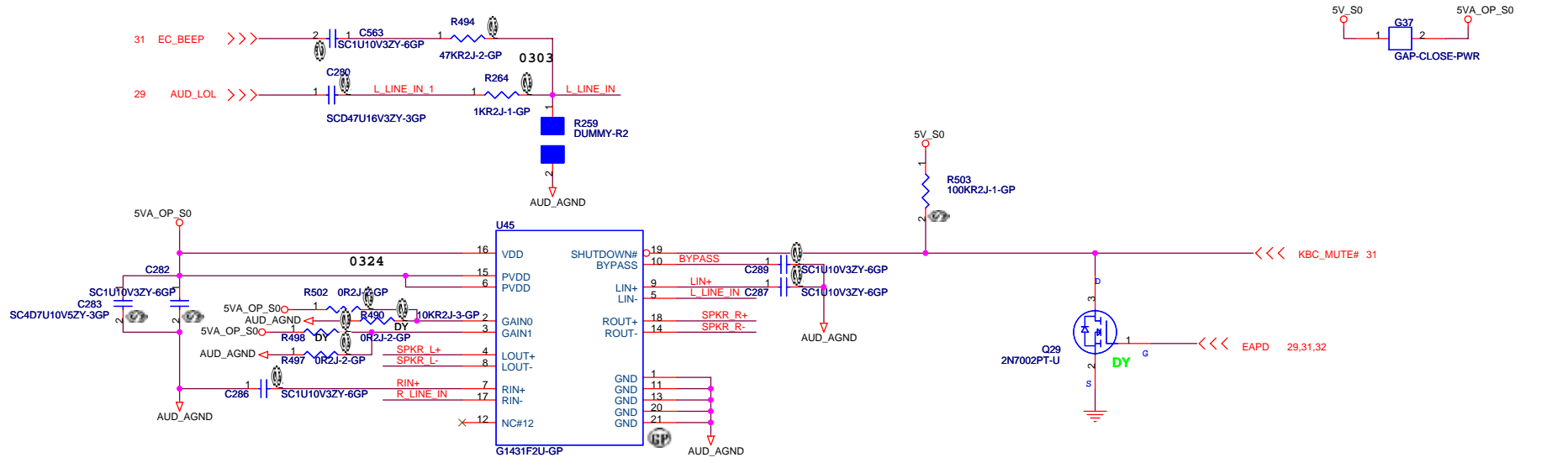
<Core Design>

**緯創資通**     **Wistron Corporation**  
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 Taipei Hsein 221, Taiwan, R.O.C.

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Title: **AUDIO CODEC CX20549-12Z**

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**Speaker**

**MICROPHONE**

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<b>AUDIO AMP/SPEAKER</b>	
Title	Rev
Size A3	SC
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# CAMERA

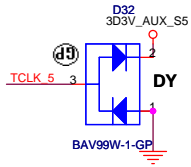
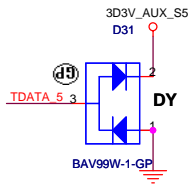
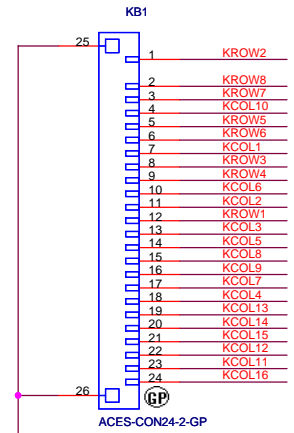
# Blue thumb

## Internal Keyboard Connector

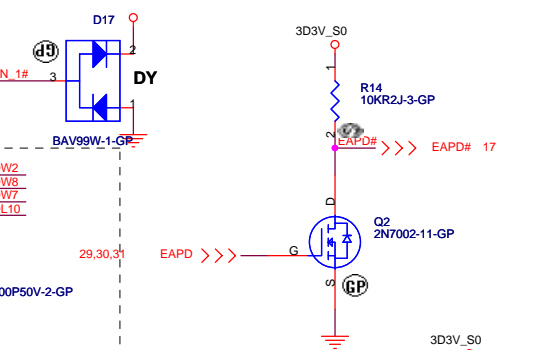
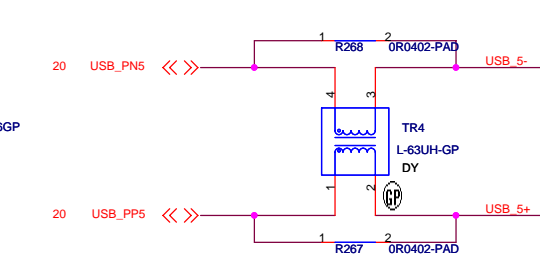
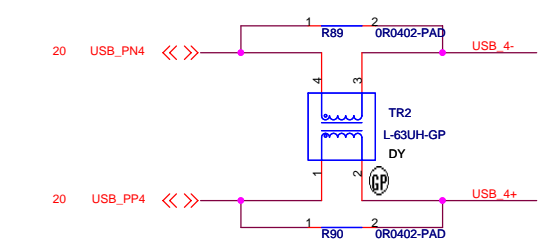
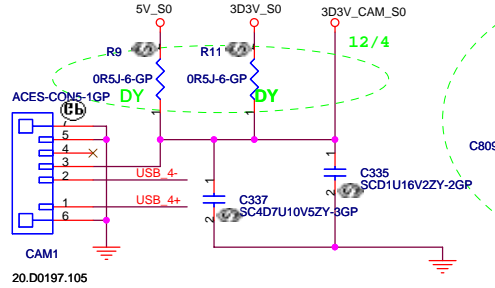
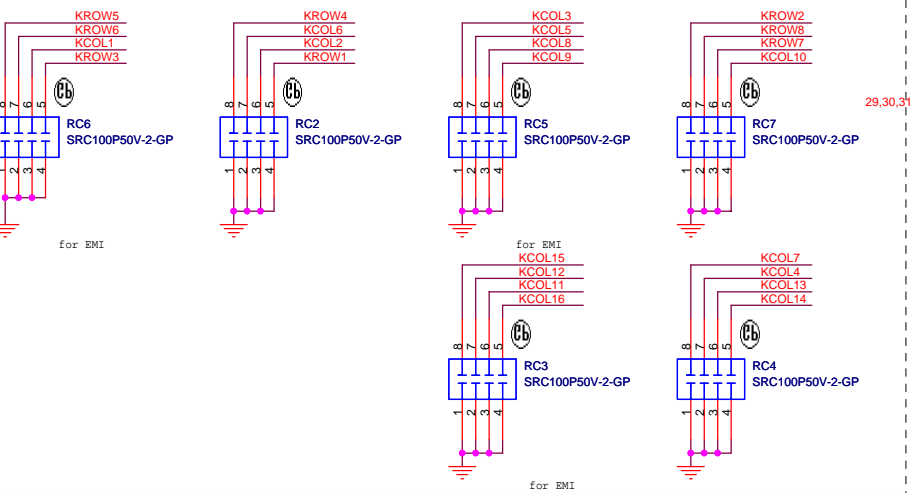
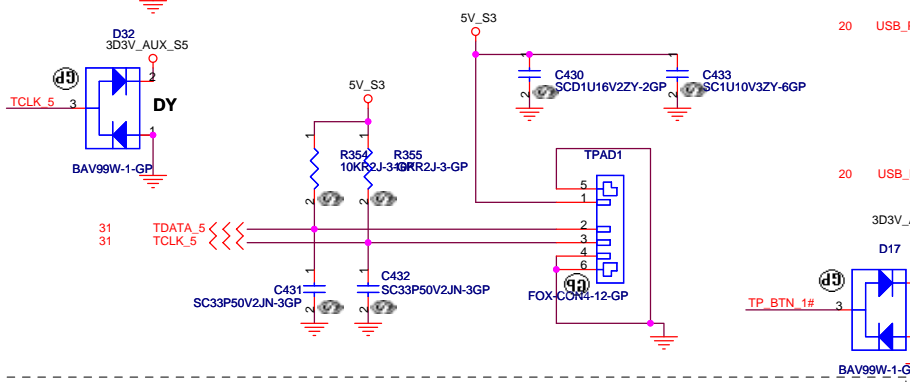
31 KROW[1..8] <<<<   
 31 KCOL[1..16] <<<< 

Keyboard matrix ( from vendor )

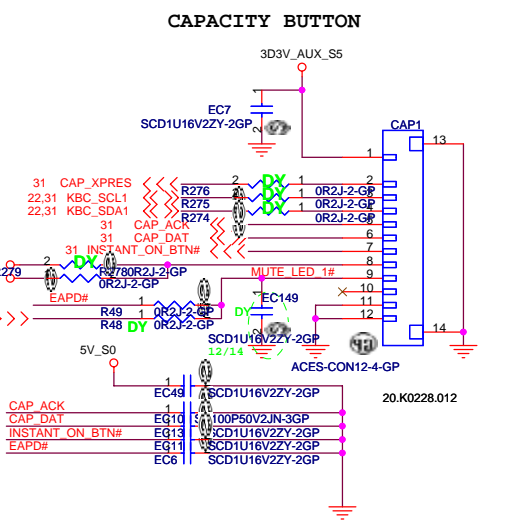
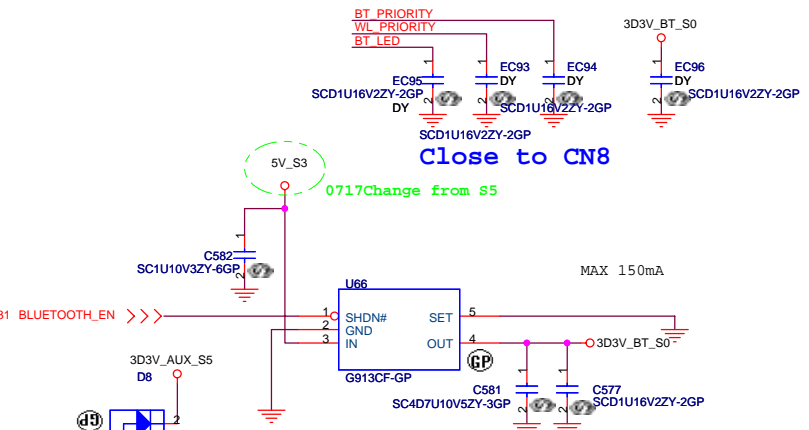
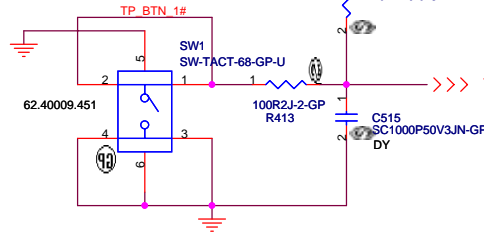
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



## TouchPad Connector



## TOUCH-PAD SWITCH



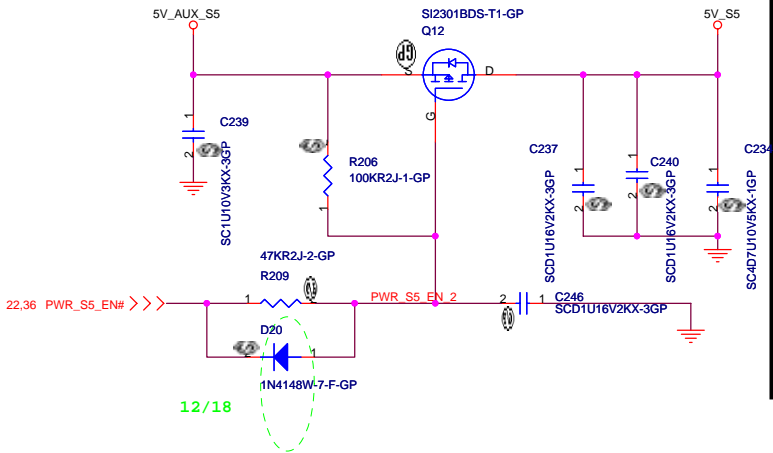
<Core Design>

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>KeyBoard-CONN</b>	
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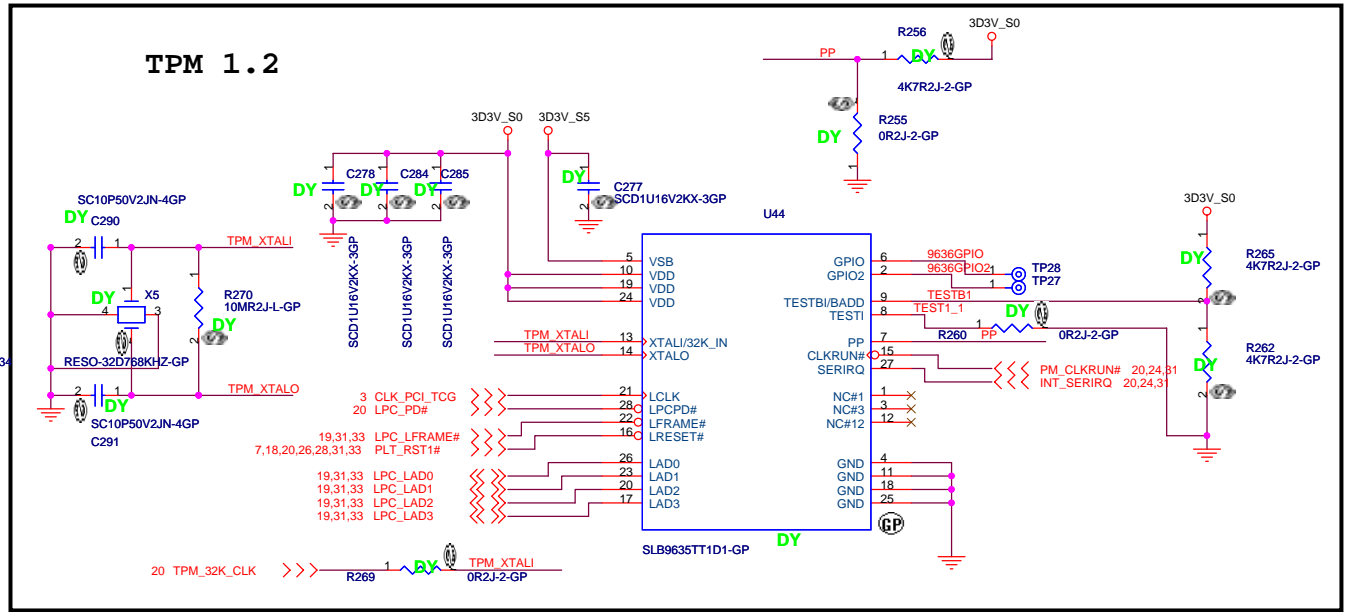




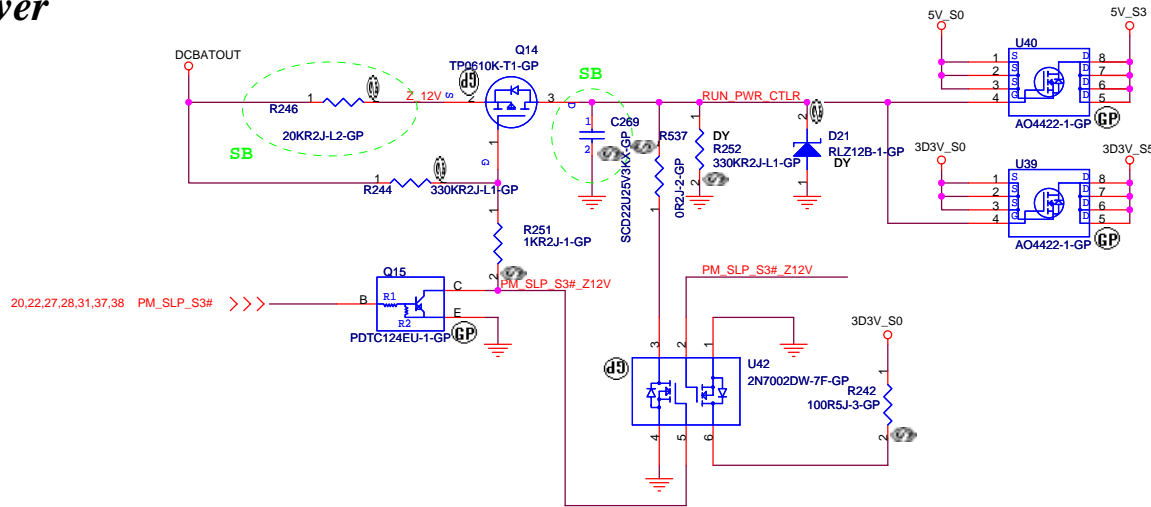
### 5V\_AUX\_S5 TO 5V\_S5



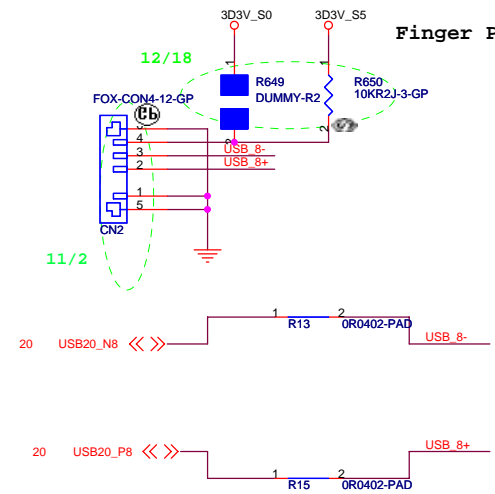
### TPM 1.2



### Run Power

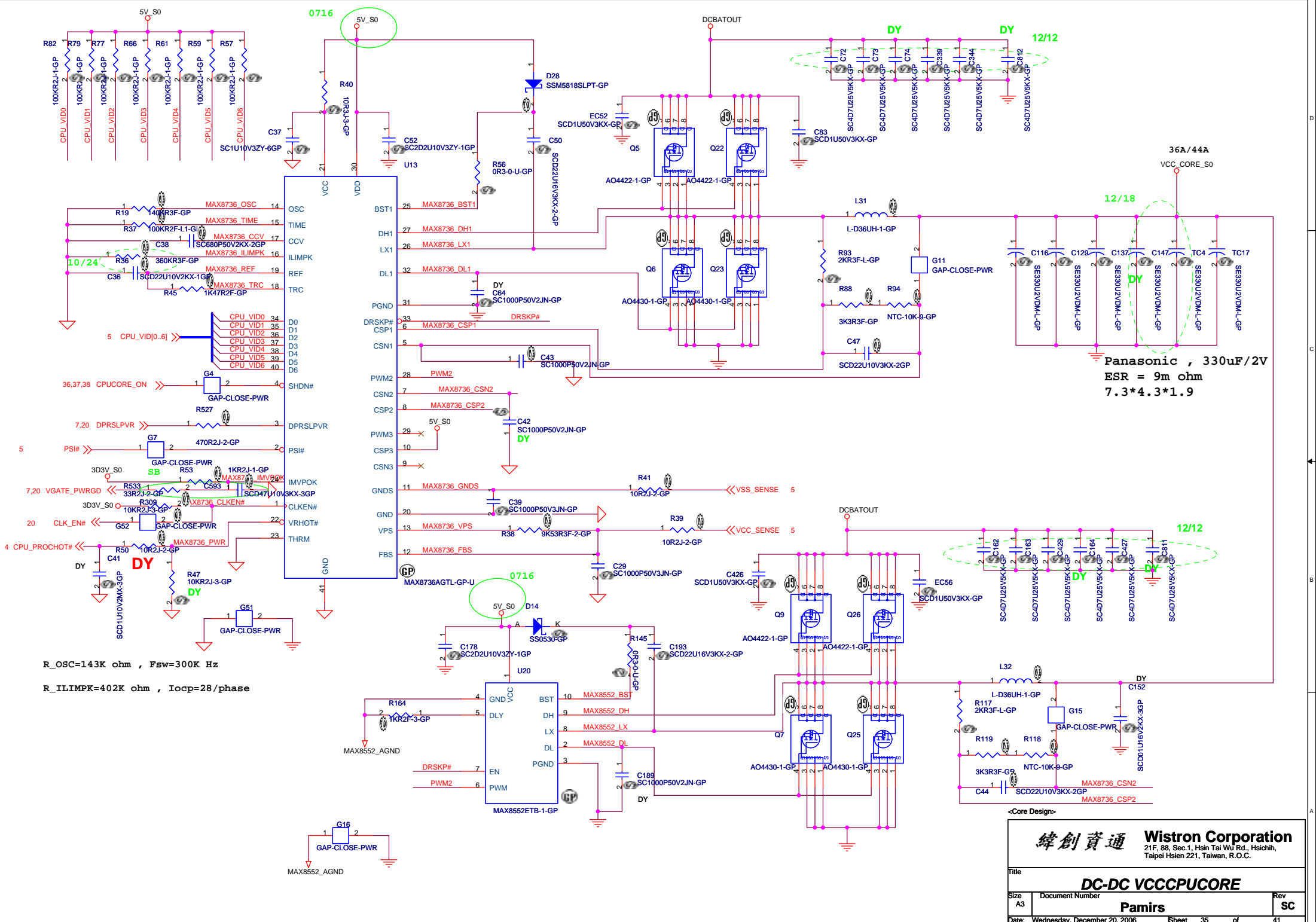


### Finger Printer



<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
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<b>Title</b>			
<b>PWRPLANE&amp;RESETLOGIC</b>			
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Date:	Monday, December 18, 2006	Sheet	34 of 41



R\_OSC=143K ohm , Fsw=300K Hz  
 R\_ILIMPK=402K ohm , Iocp=28/phase

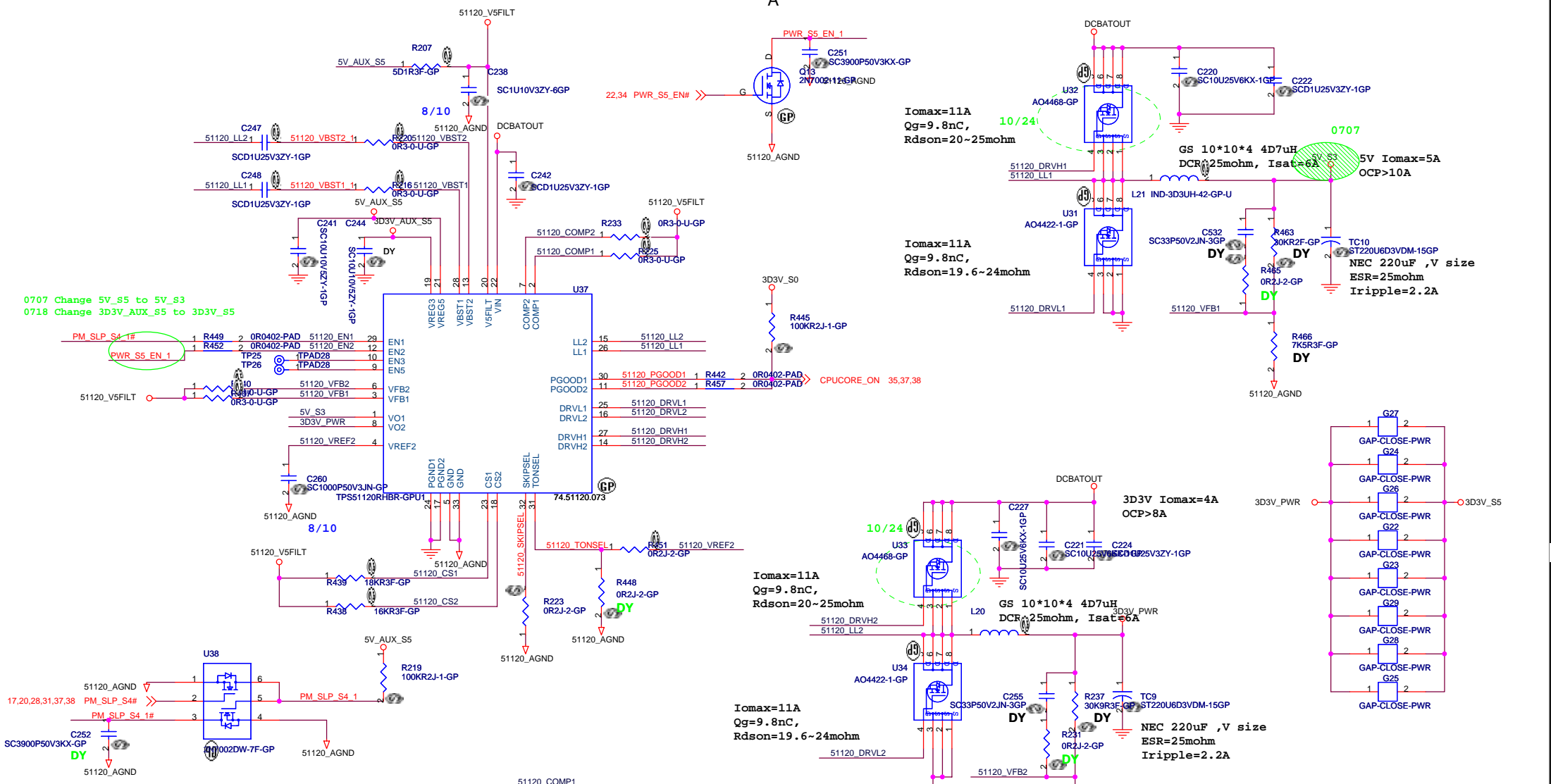
Panasonic , 330uF/2V  
 ESR = 9m ohm  
 7.3\*4.3\*1.9

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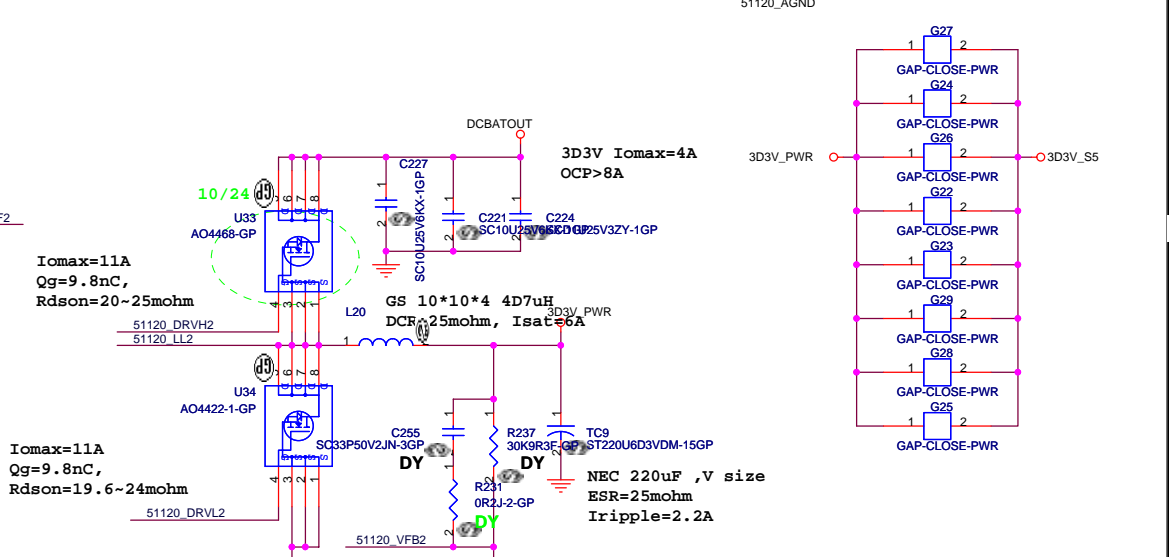
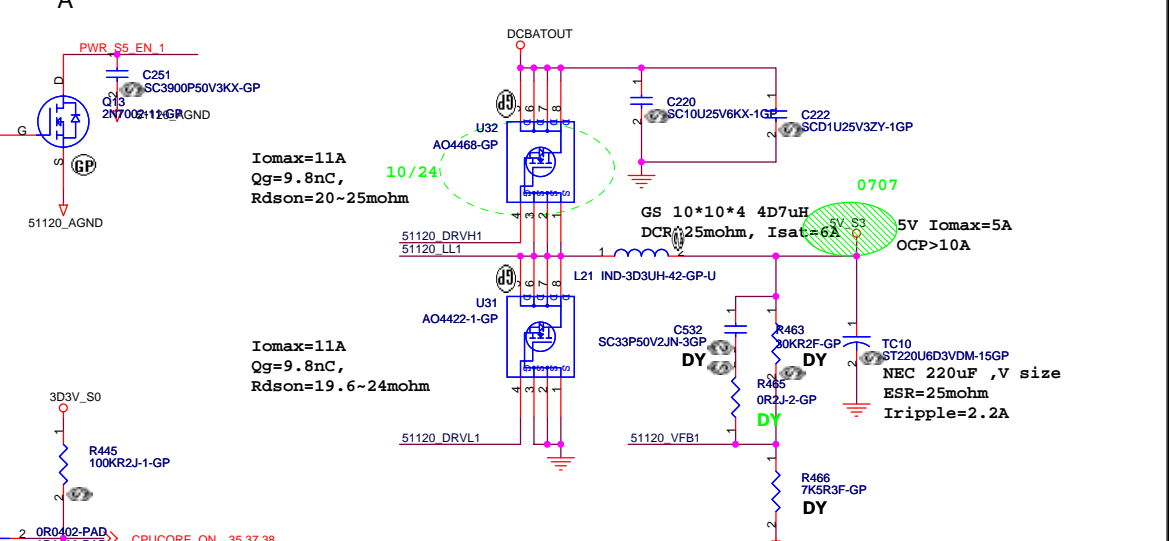
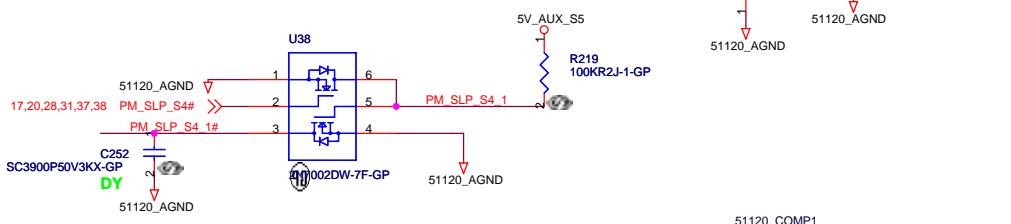
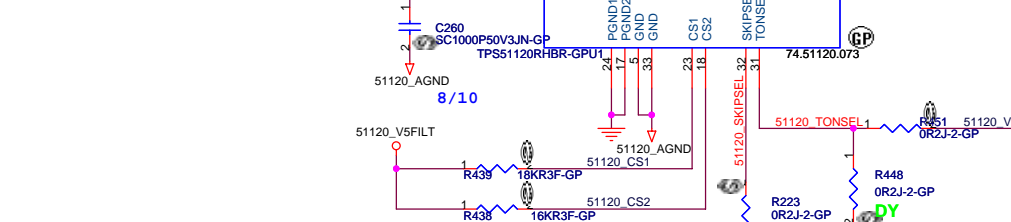
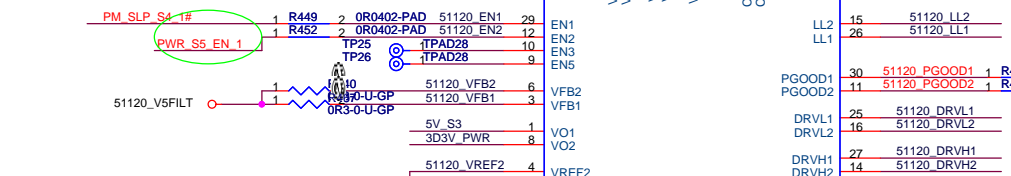
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Title: **DC-DC VCCPUCORE**

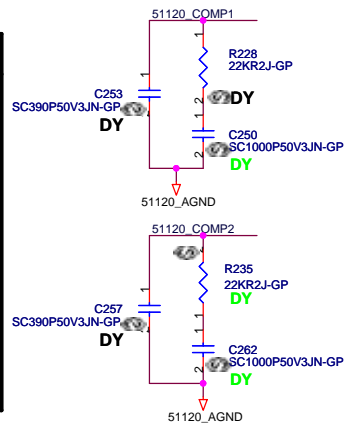
Size: A3	Document Number: <b>Pamirs</b>	Rev: <b>SC</b>
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0707 Change 5V\_S5 to 5V\_S3  
0718 Change 3D3V\_AUX\_S5 to 3D3V\_S5



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	switcher OFF	not use	Switchchr ON	switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on



**Vout=1V\*(R1+R2)/R2**

For TPS51120,  
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

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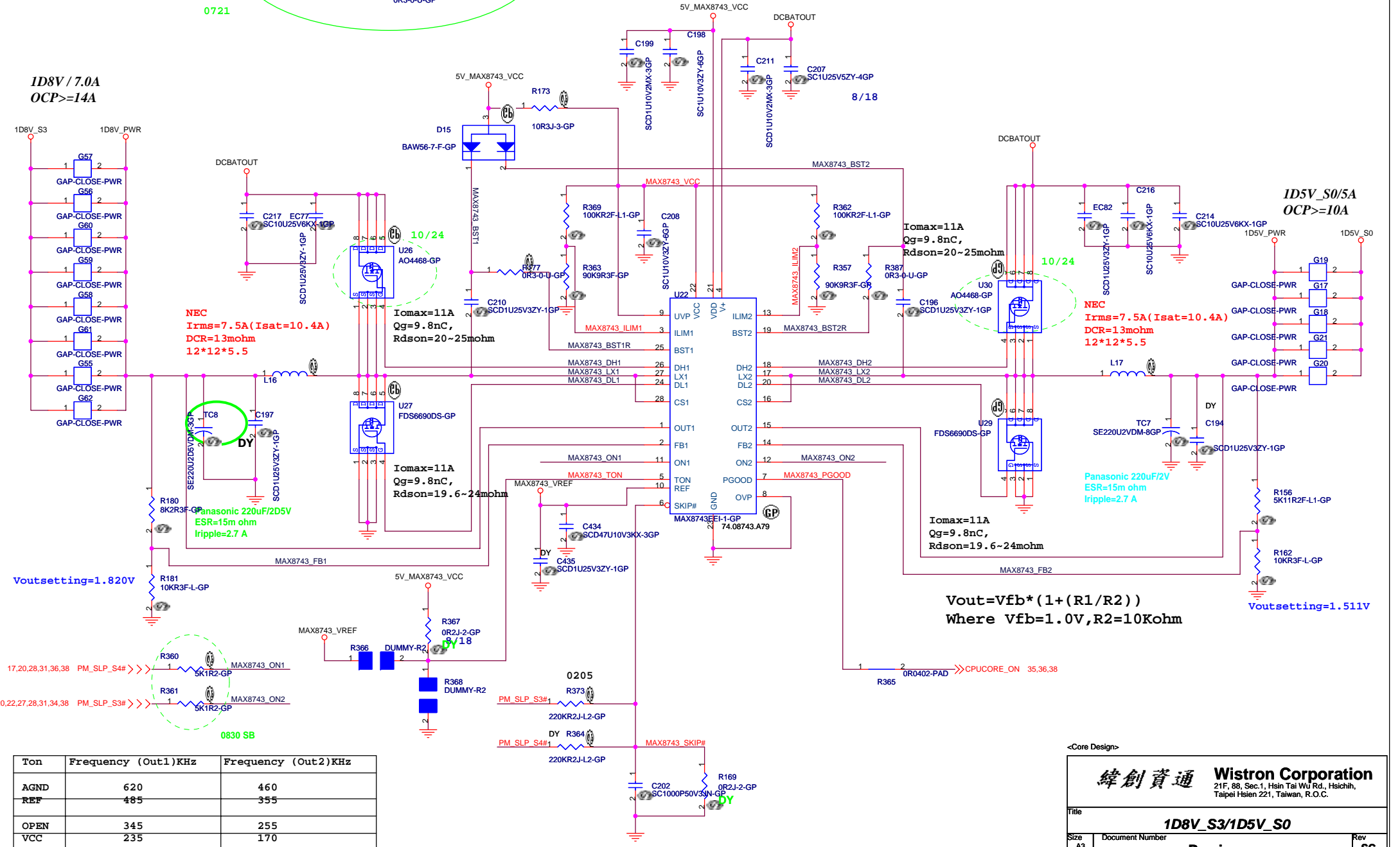
Title: **5V\_S3/3D3V\_S5**

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$I_{ocp}=7.0*2=14A$   
 $R_{ds,on}=17m\ \Omega$   
 $V_{cs1}=I_{ocp}*R_{ds,on}=238mV$   
 $VILIM=V_{cs1}/0.1=2.38V$

$I_{ocp}=7.0*2=14A$   
 $R_{ds,on}=17m\ \Omega$   
 $V_{cs2}=I_{ocp}*R_{ds,on}=28mV$   
 $VILIM2=V_{cs2}/0.1=2.38V$



**1D8V / 7.0A**  
**OCP >= 14A**

**1D5V\_S0/5A**  
**OCP >= 10A**

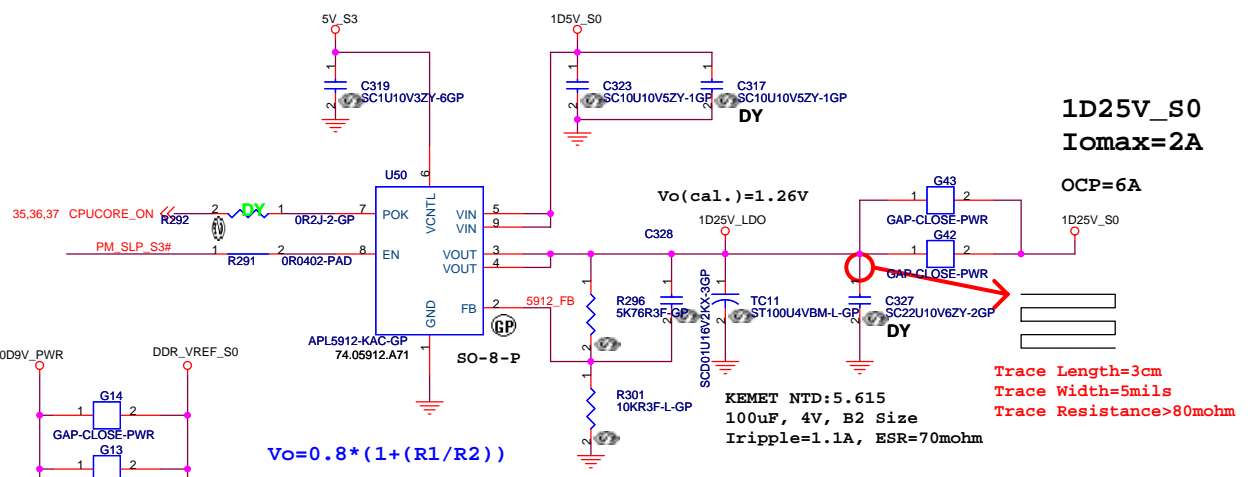
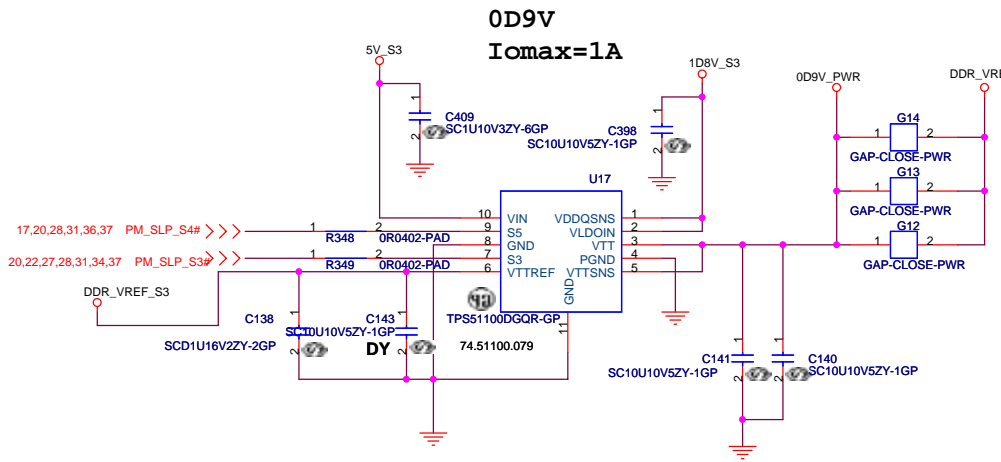
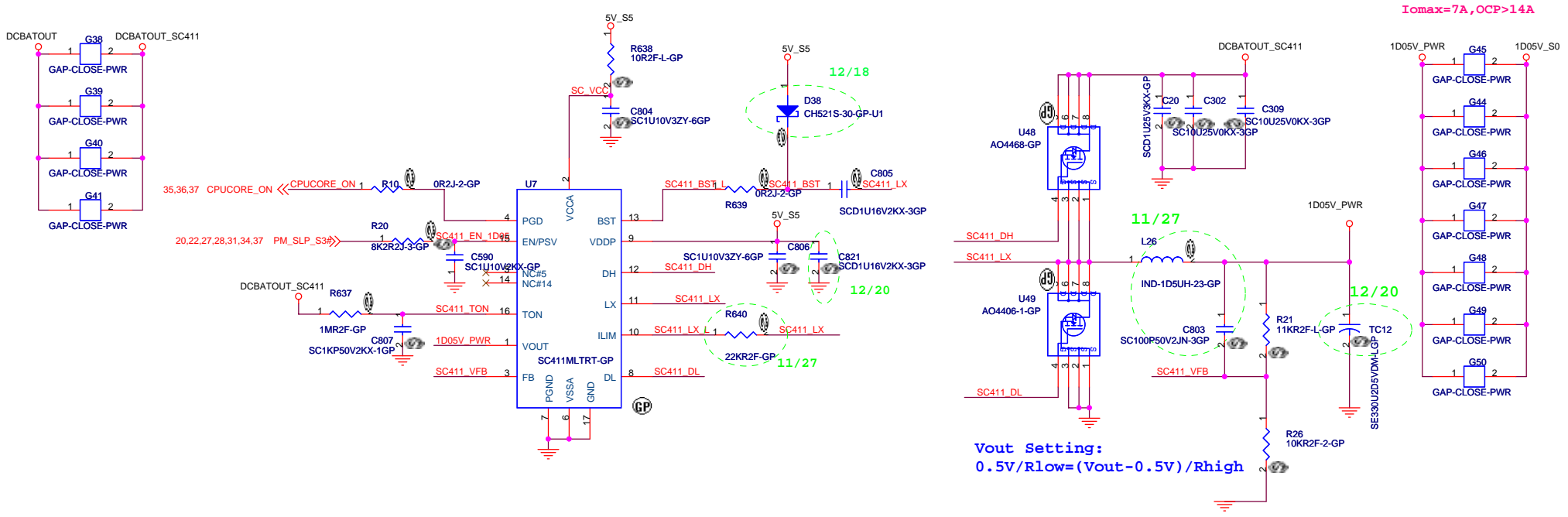
**NEC**  
 $I_{rms}=7.5A (I_{sat}=10.4A)$   
 $DCR=1.3m\ \Omega$   
 $12*12*5.5$

**NEC**  
 $I_{rms}=7.5A (I_{sat}=10.4A)$   
 $DCR=1.3m\ \Omega$   
 $12*12*5.5$

$V_{out} = V_{fb} * (1 + (R1/R2))$   
 Where  $V_{fb}=1.0V, R2=10Kohm$

Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

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 Title: **1D8V\_S3/1D5V\_S0**  
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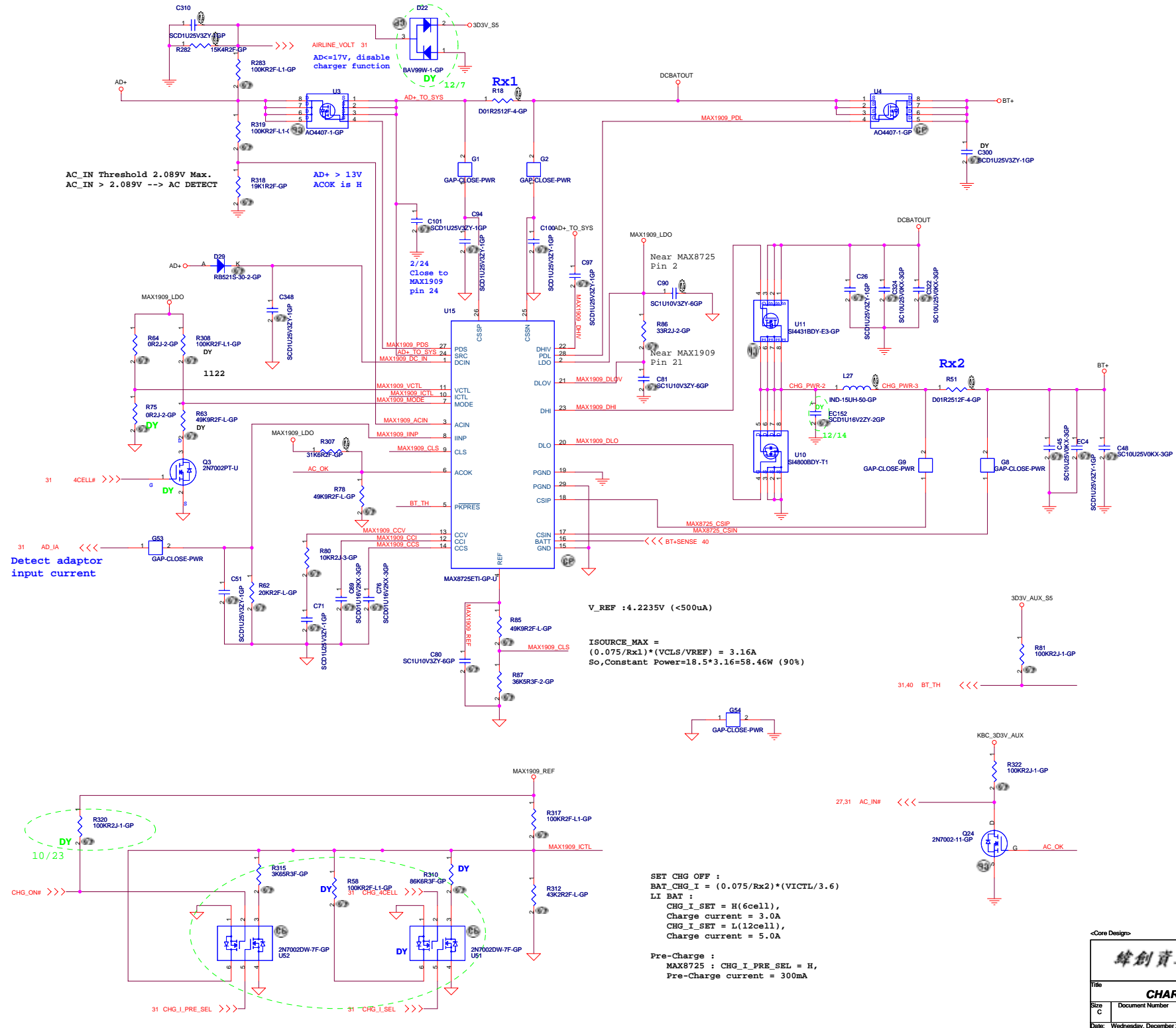
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Title: **0D9V\_LDO/1D25V\_LDO/1D05V**

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AC\_IN Threshold 2.089V Max.  
AC\_IN > 2.089V --> AC DETECT

Detect adaptor  
input current

V\_REF : 4.2235V (<500uA)

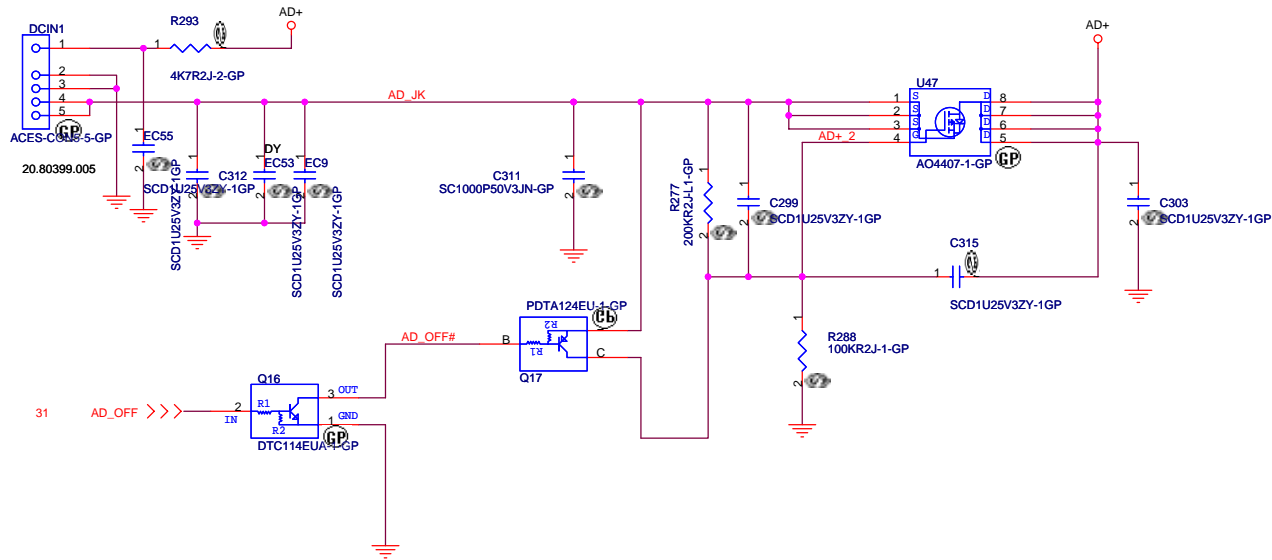
ISOURCE\_MAX =  
(0.075/Rx1)\*(VCLs/VREF) = 3.16A  
So, Constant Power=18.5\*3.16=58.46W (90%)

SET CHG OFF :  
BAT\_CHG\_I = (0.075/Rx2)\*(VICTL/3.6)  
LI BAT :  
CHG\_I\_SET = H(6cell),  
Charge current = 3.0A  
CHG\_I\_SET = L(12cell),  
Charge current = 5.0A

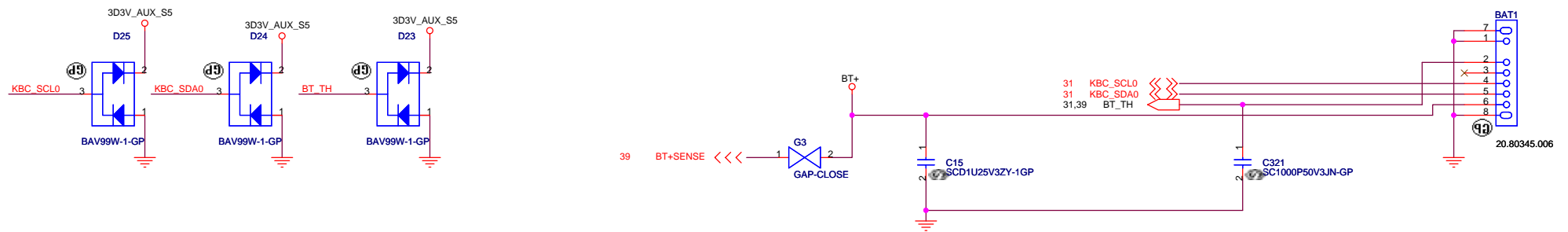
Pre-Charge :  
MAX8725 : CHG\_I\_PRE\_SEL = H,  
Pre-Charge current = 300mA



# Adaptor in to generate DCBATOUT



# BATTERY CONNECTOR

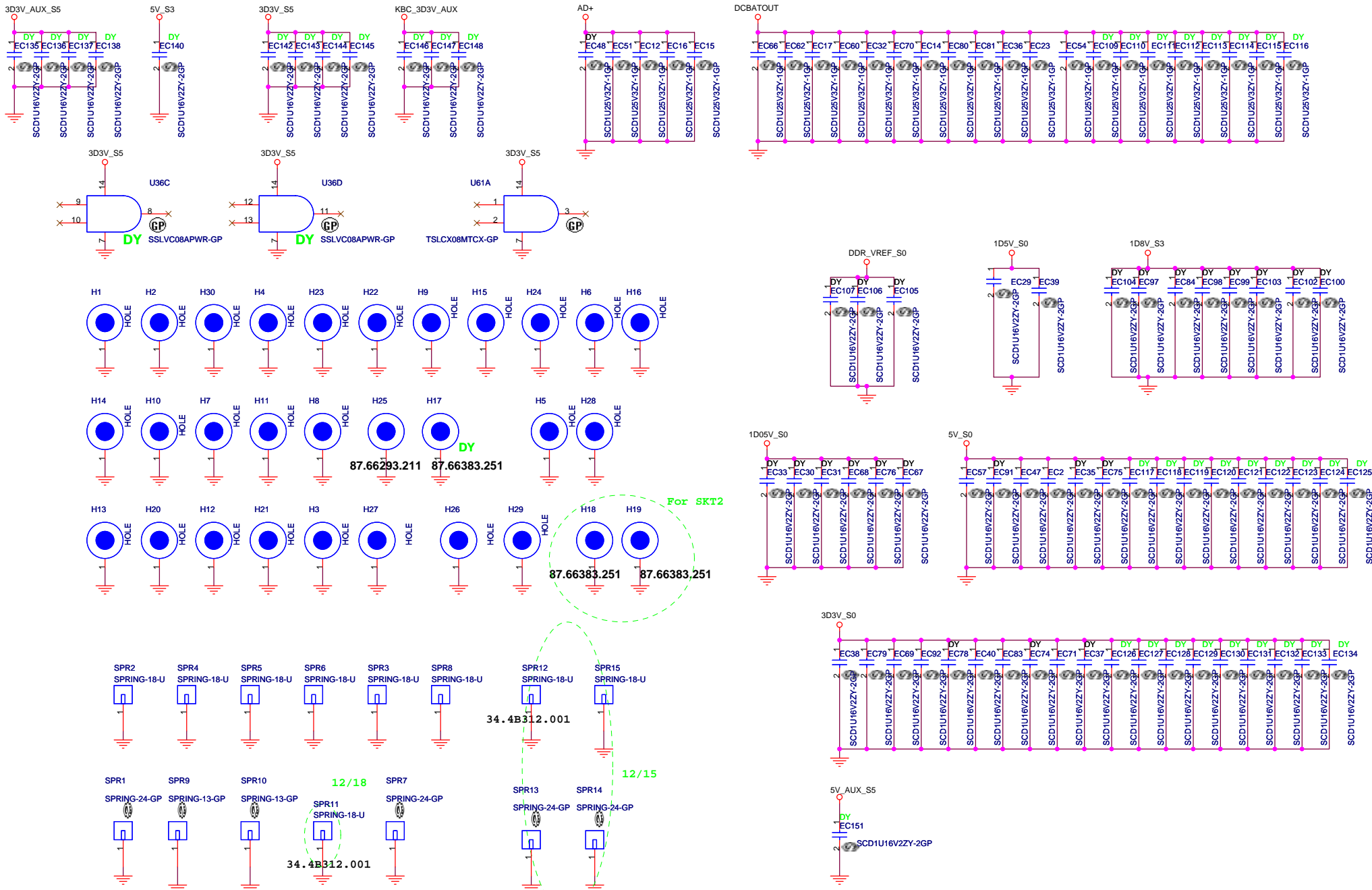


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Title: **AD/BATT CONN**

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Title: **MISC**

Size: A3 Document Number: **Pamirs** Rev: **SC**

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