

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT

Cable Docking

- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

PAGE 38

SYSTEM CHARGER ISL6251AHAZ-T
PAGE 39

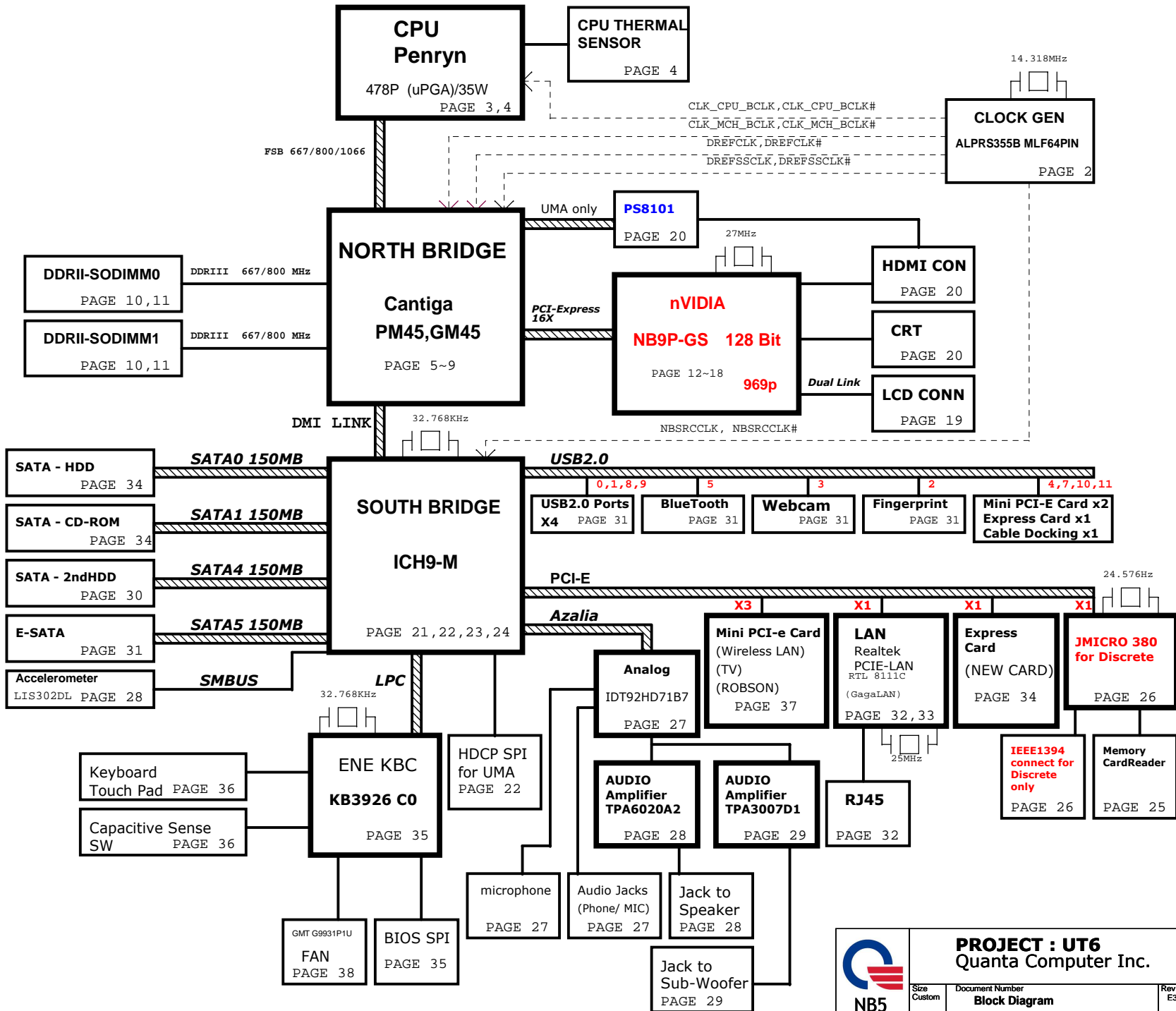
SYSTEM POWER ISL6237IRZ-T
PAGE 40

DDR II SMD DR_VTERM
1.8V/1.8VSUS(TPS51116REGR)
PAGE 44

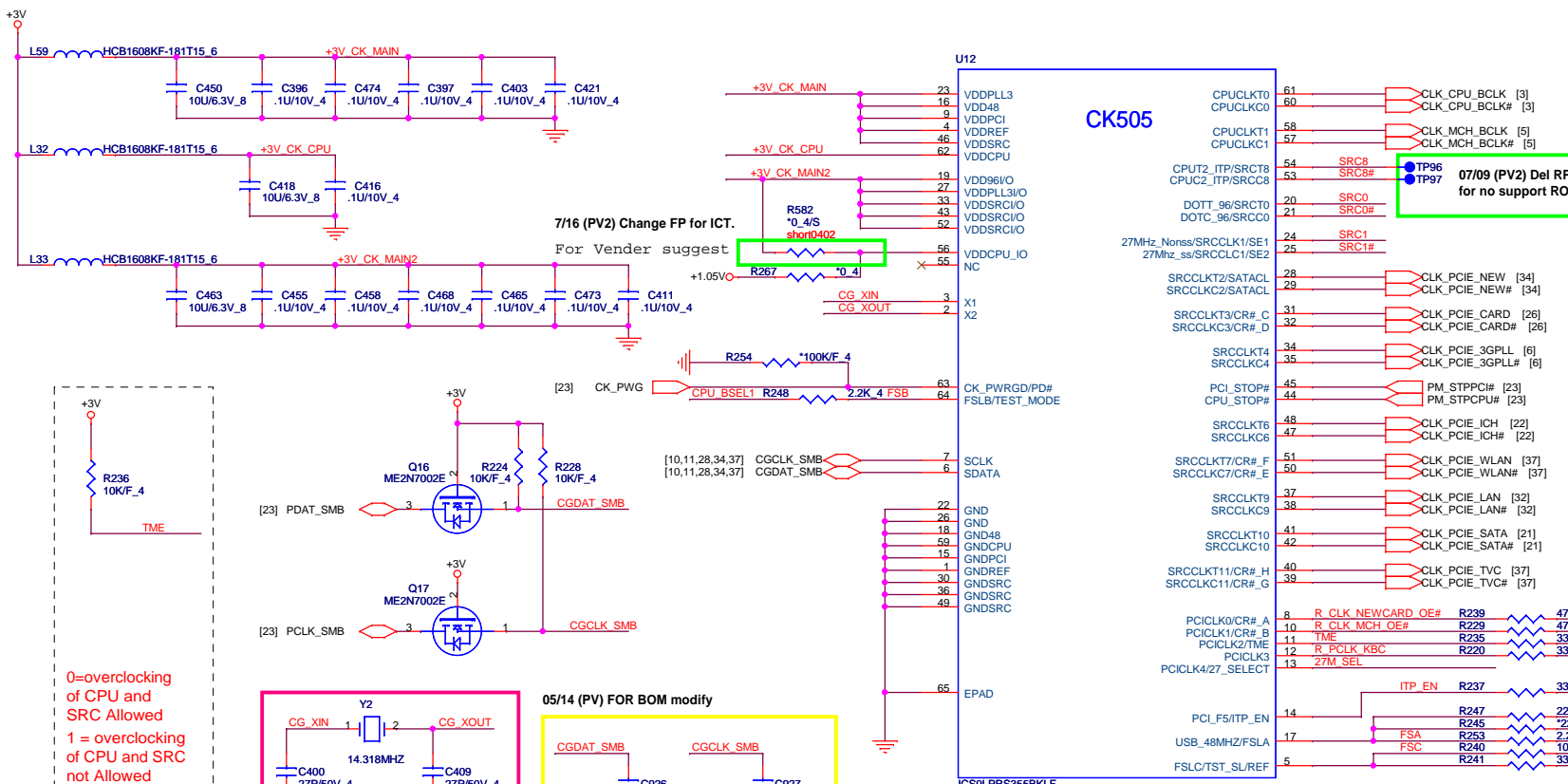
VCCP +1.5V AND GMCH
1.05V(RT8204)
PAGE 44

VGACORE(1.025V)Oz8118
PAGE 43

CPU CORE ISL6266A
PAGE 42



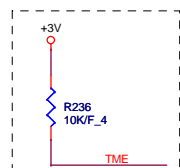
PROJECT : UT6
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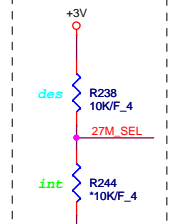
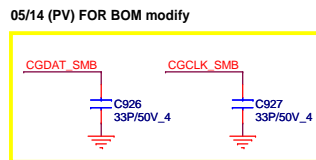
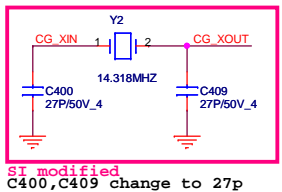
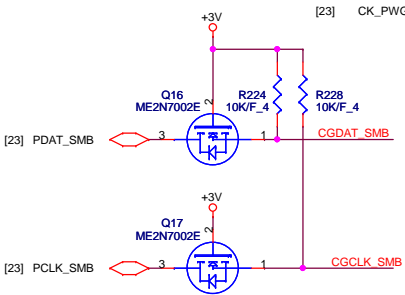
Delete RP49 for delete ITP conn.

07/09 (PV2) Del RP53, add TP96, TP97 for no support ROBSON card.

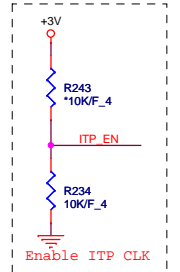
07/14 (PV2) Change footprint for PE require.



0=overclocking of CPU and SRC Allowed
1 = overclocking of CPU and SRC not Allowed



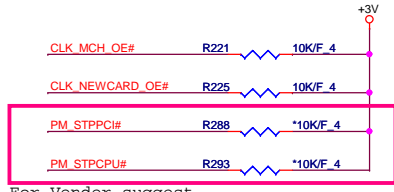
0=UMA
1 = External VGA



27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

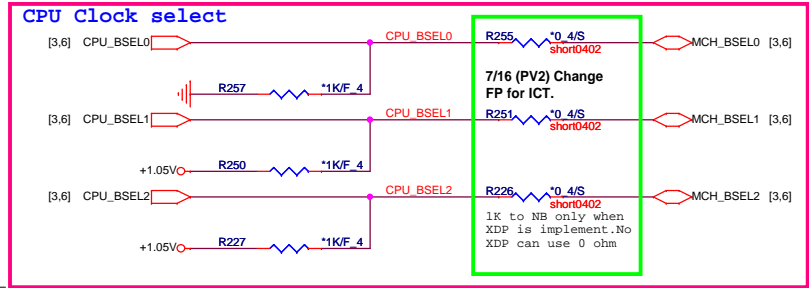
CK505 QFN64

- ICS ICS9LPRS355BKLF ALPRS355000
- Silego SLG8SP513VTR AL8SP513000
- Realtek RTM875N-606-VD-GR AL000875000

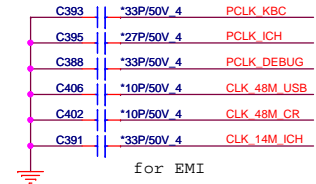


For Vender suggest

QT6 modified-0117



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	1	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

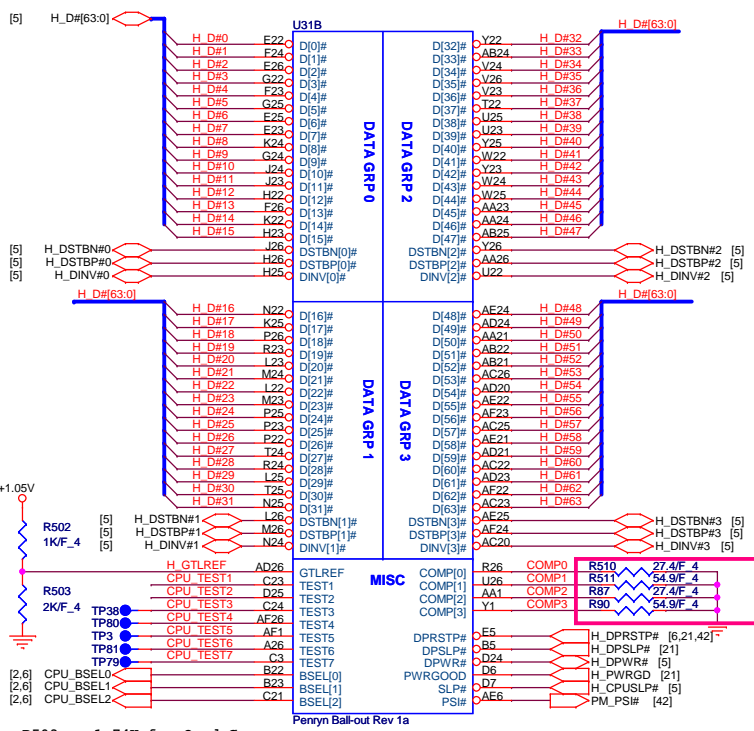
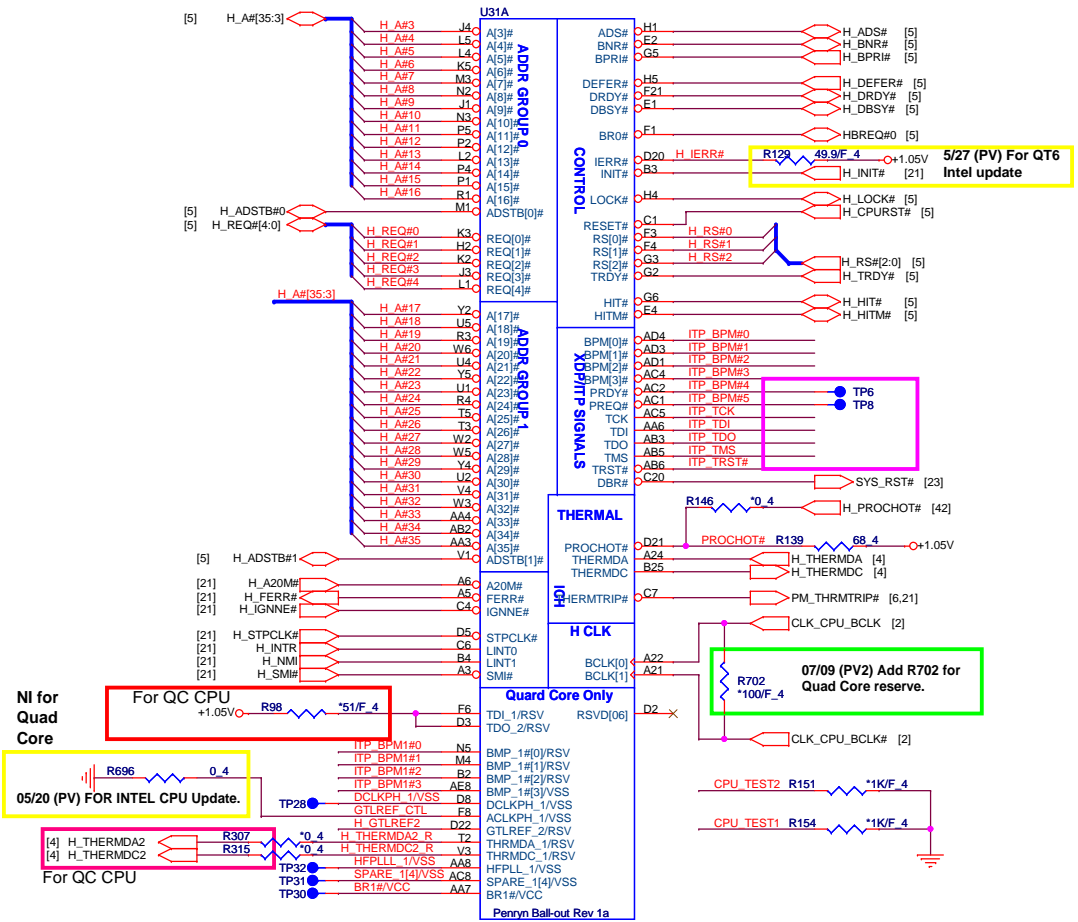


for EMI

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NB5

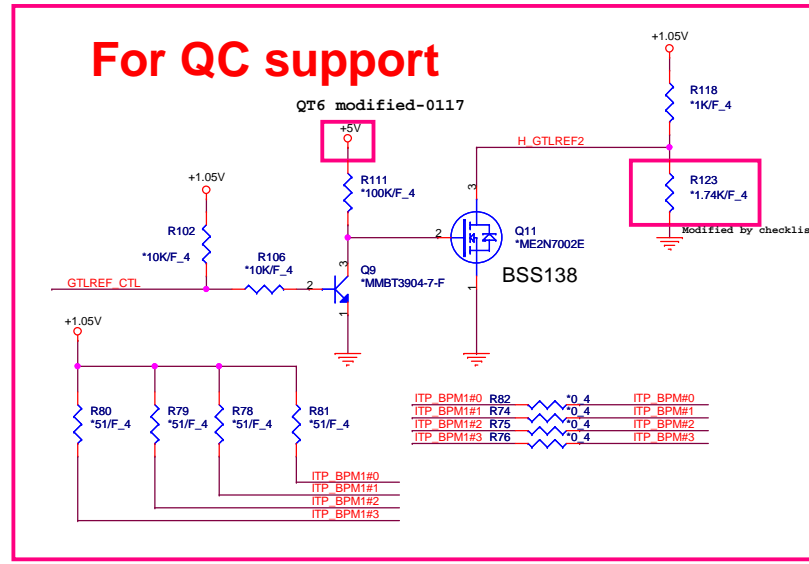
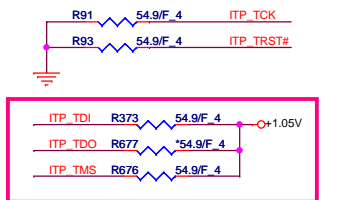
Size Custom	Document Number Clock Generator	Rev E3A
Date: Wednesday, August 06, 2008		Sheet 2 of 46



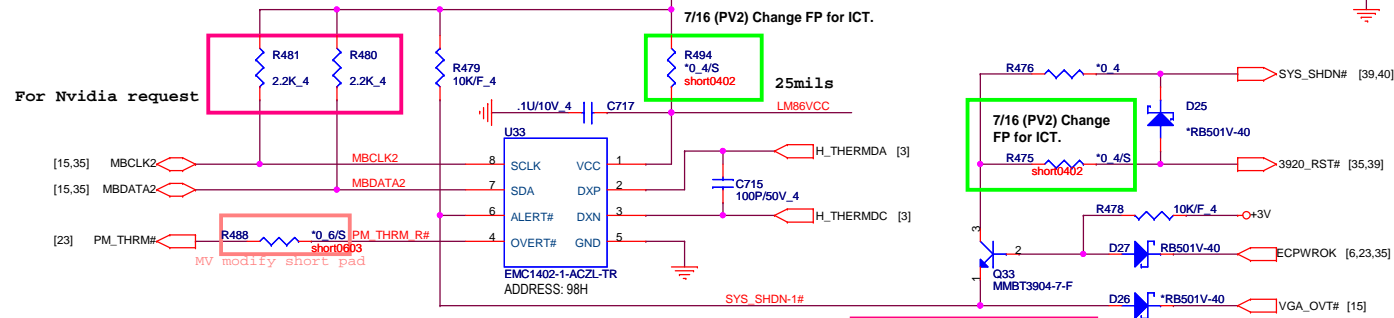
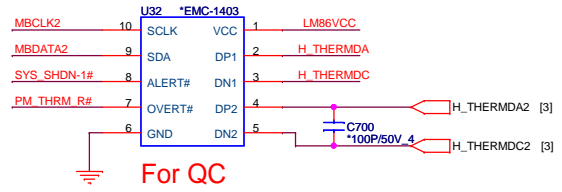
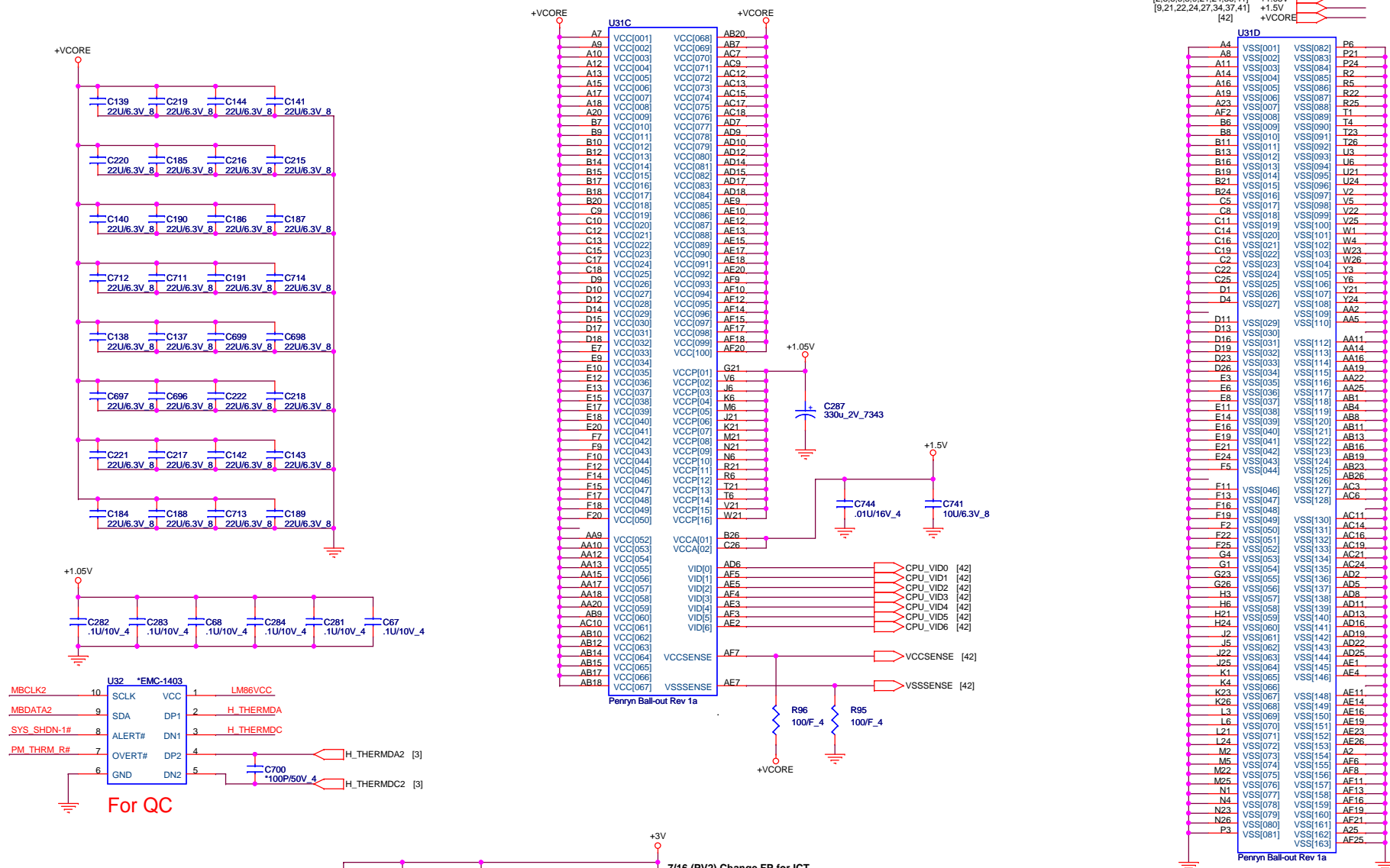
	COMP0/2	COMP1/3
Dual Core	27.4 Ohm (CS02742FB19)	54.9 Ohm (CS05492FB19)
Quad Core	24.9 Ohm (CS02492FB29)	49.9 Ohm (CS04992FB31)

MODEL	UT7 Quad Core	UT6 Dual Core
R696	*0_4	0_4

Populate ITP700Flex for bringup

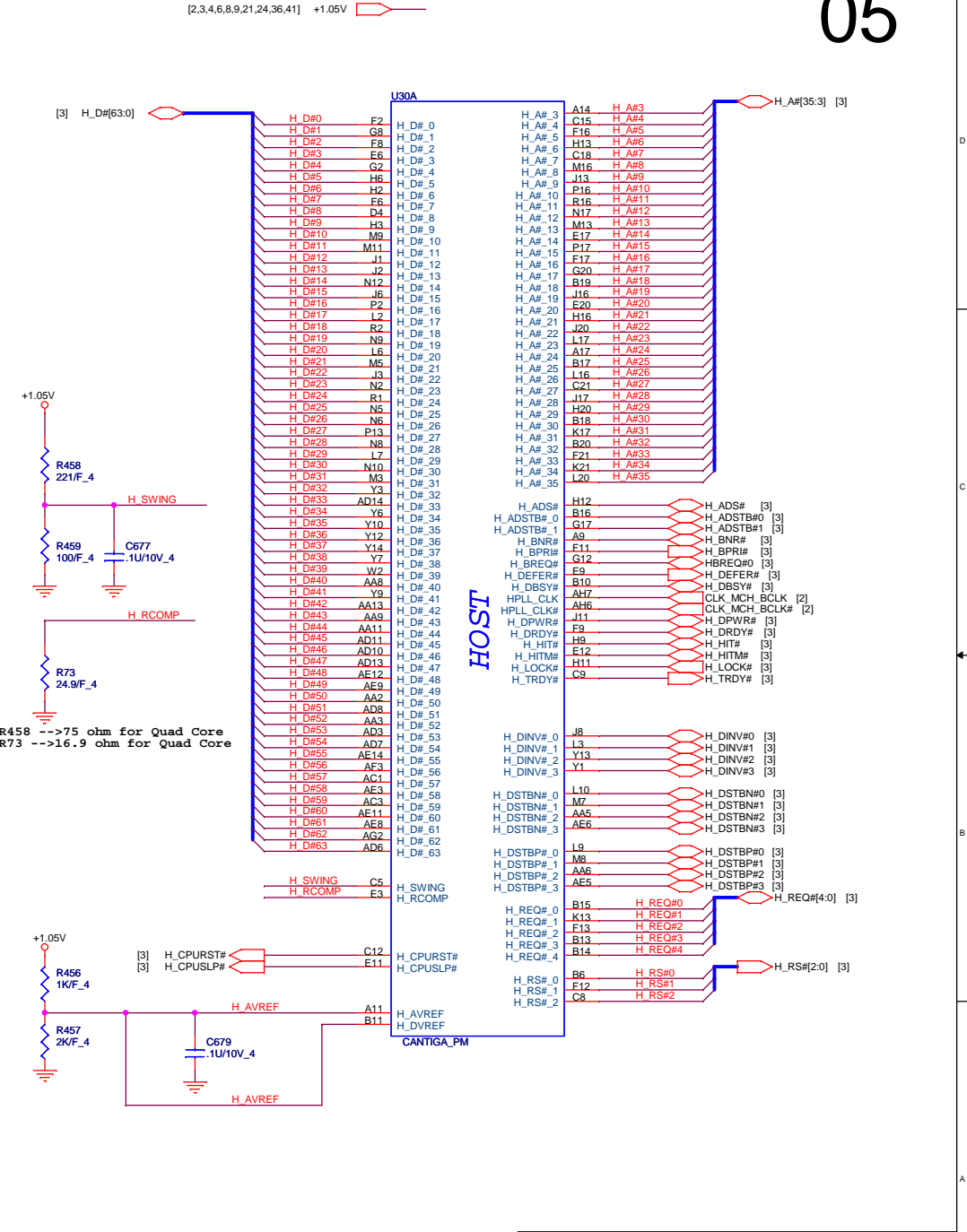
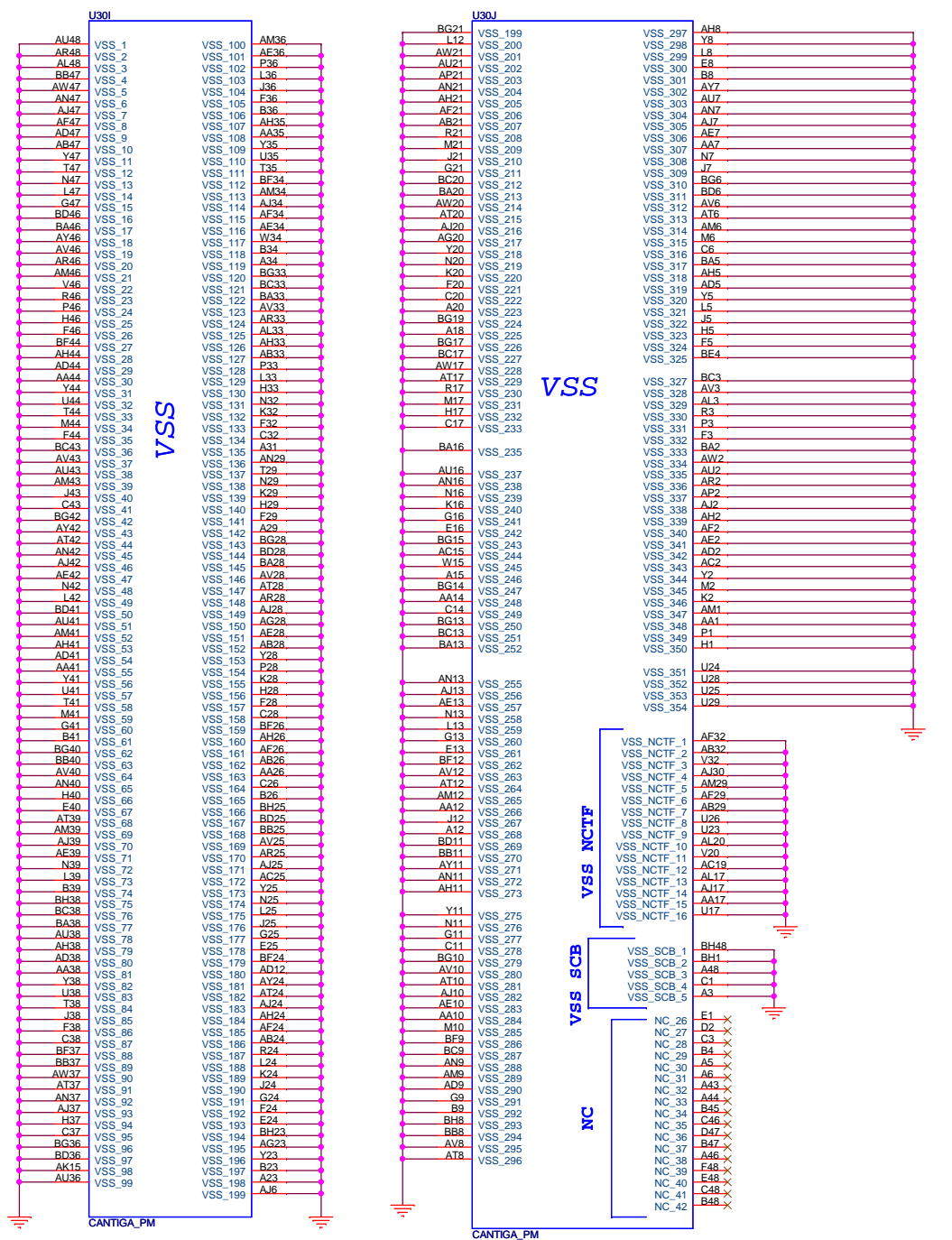


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[2,3,4,6,8,9,21,24,36,41] +1.05V



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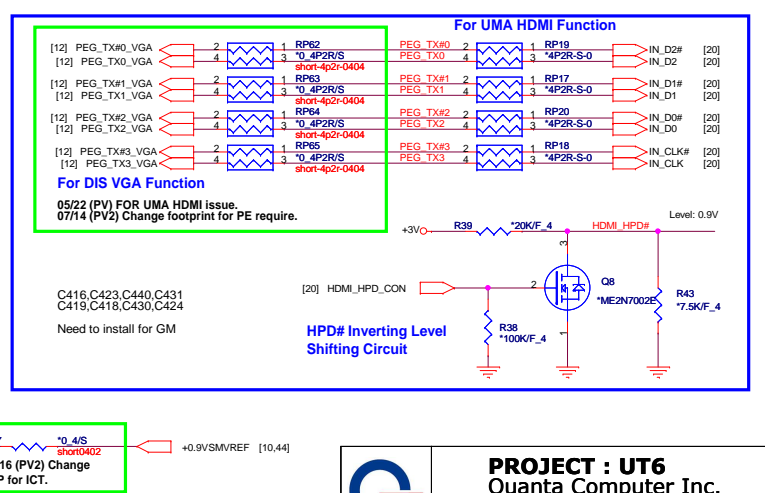
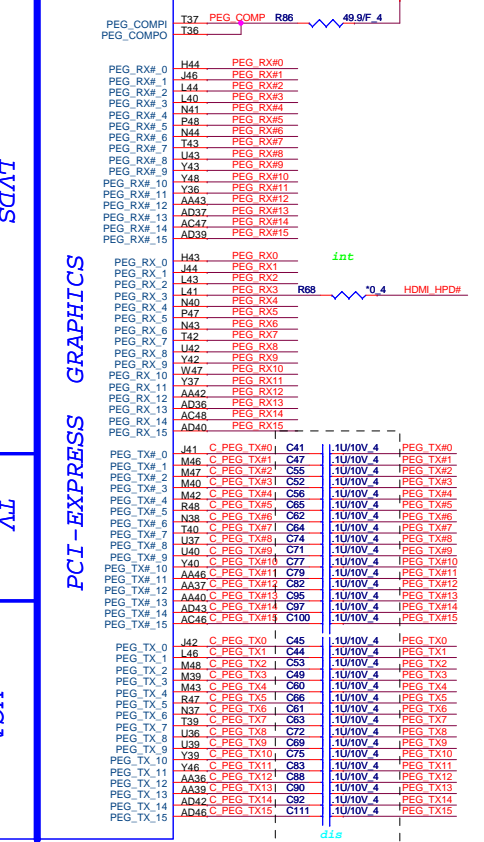
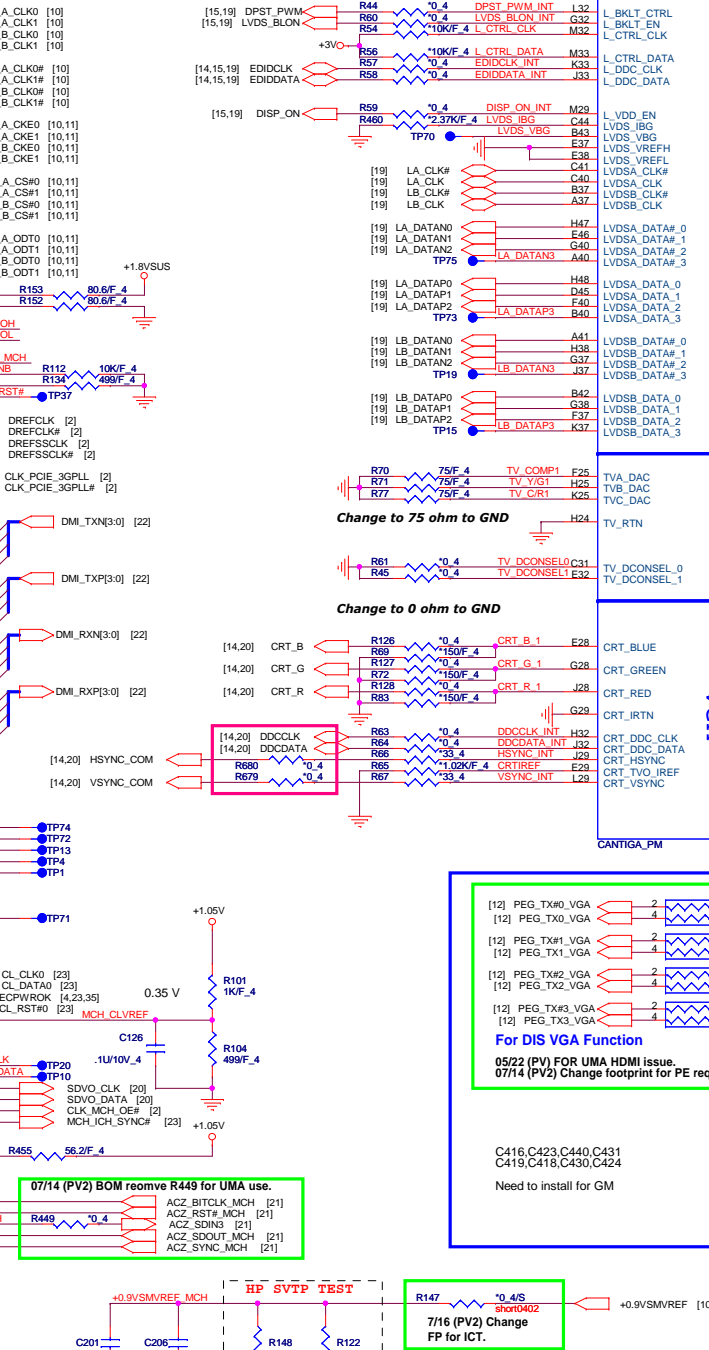
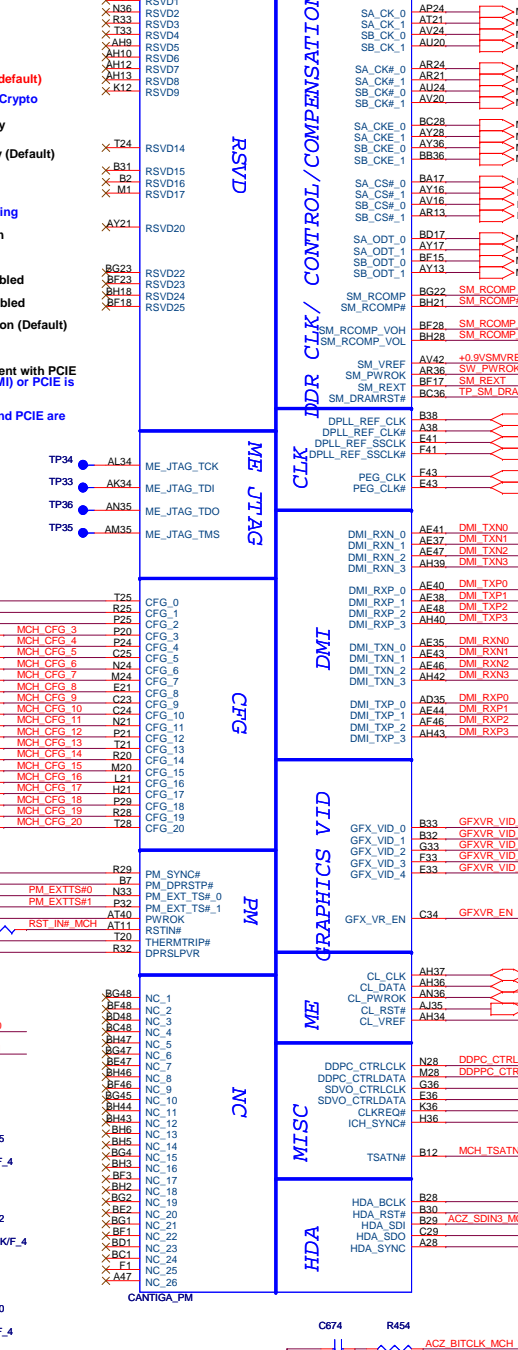
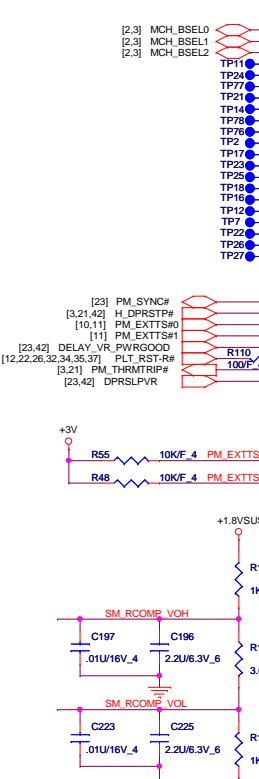
- MCH_CFG_5 DMiX2 selection
 Low = DMi X2
 High = DMi X4 (Default)
- MCH_CFG_16 FSB Dynamic ODT
 Low = Dynamic ODT disabled
 High = Dynamic ODT enabled (default)
- MCH_CFG_9 PCI Express Graphic Lane
 Low = Reverse Lane
 High = Normal operation(Default)
- MCH_CFG_19 DMi Lane Reversal
 Low = Normal operation (Default)
 High = Reverse Lanes
- MCH_CFG_6 ITPM Host Interface
 Low = The ITPM Host Interface is enabled
 High = The ITPM Host Interface is disabled (default)
- MCH_CFG_7 Intel (R) Management Engine Crypto
 Low = Intel (R) Management Engine Crypto
 TLS cipher suite with no confidentiality
 High = Intel (R) Management Engine Crypto
 TLS cipher suite with no confidentiality (Default)
- MCH_CFG_10 PCIe Lookback Enable
 Low = Enabled
 High = Disabled (Default)
- MCH_CFG_12/13 XOR/ALL/CLOCK Un-gating
- MCH_CFG_13 MCH_CFG_12 Configuration

0	0	Reserved
0	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

- MCH_CFG_20

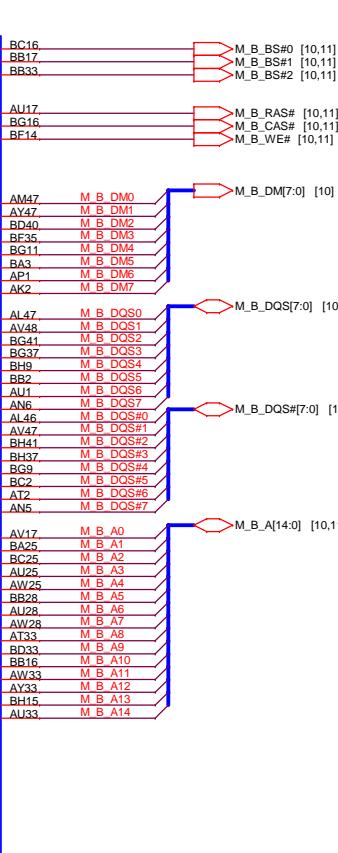
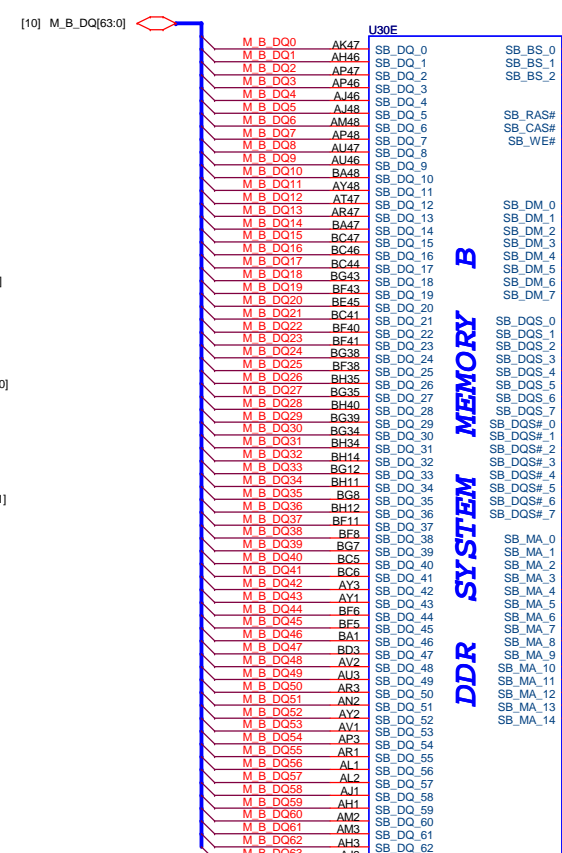
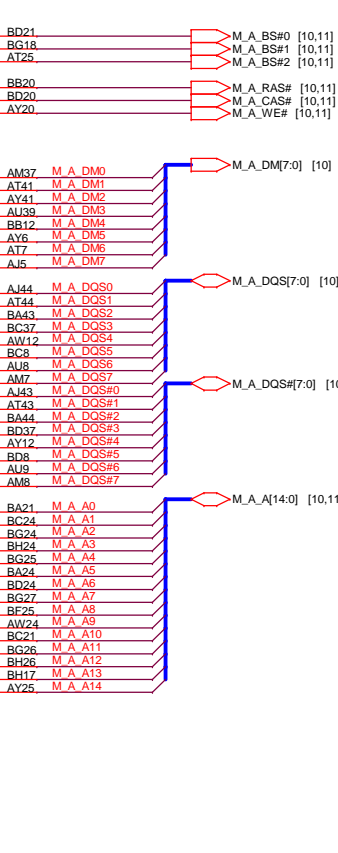
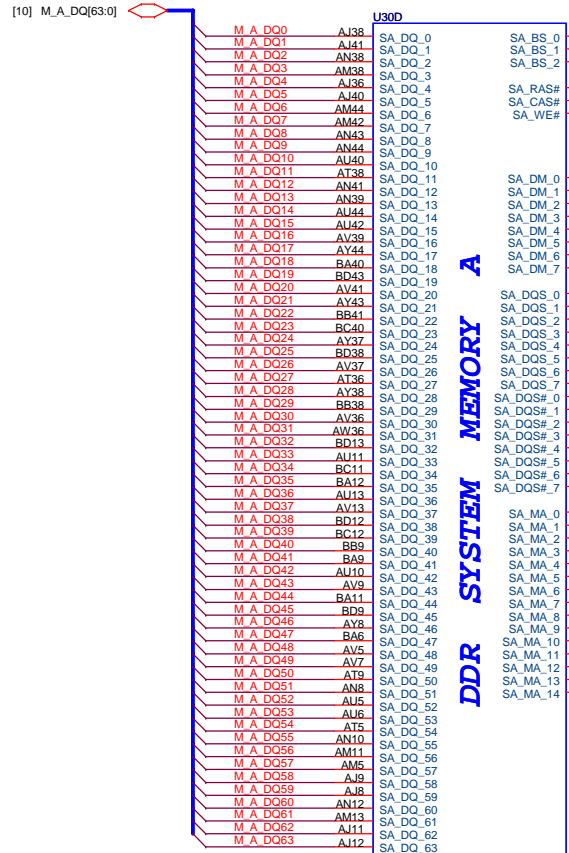
0	0	Reserved
0	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)
- Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIE
 Low = Only digital display port (SDVO/DP/HDMI) or PCIE is operational (default)
 High = Digital display port (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port
- MCH_CFG2:0

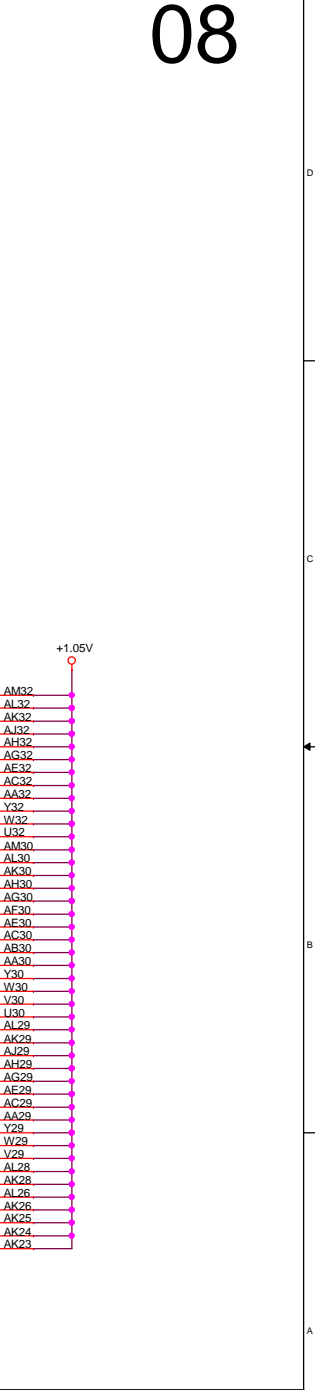
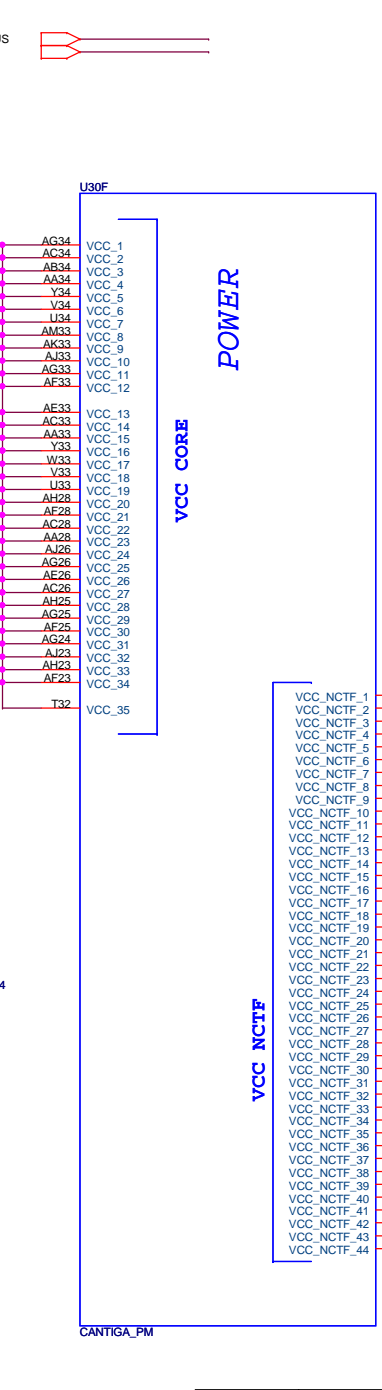
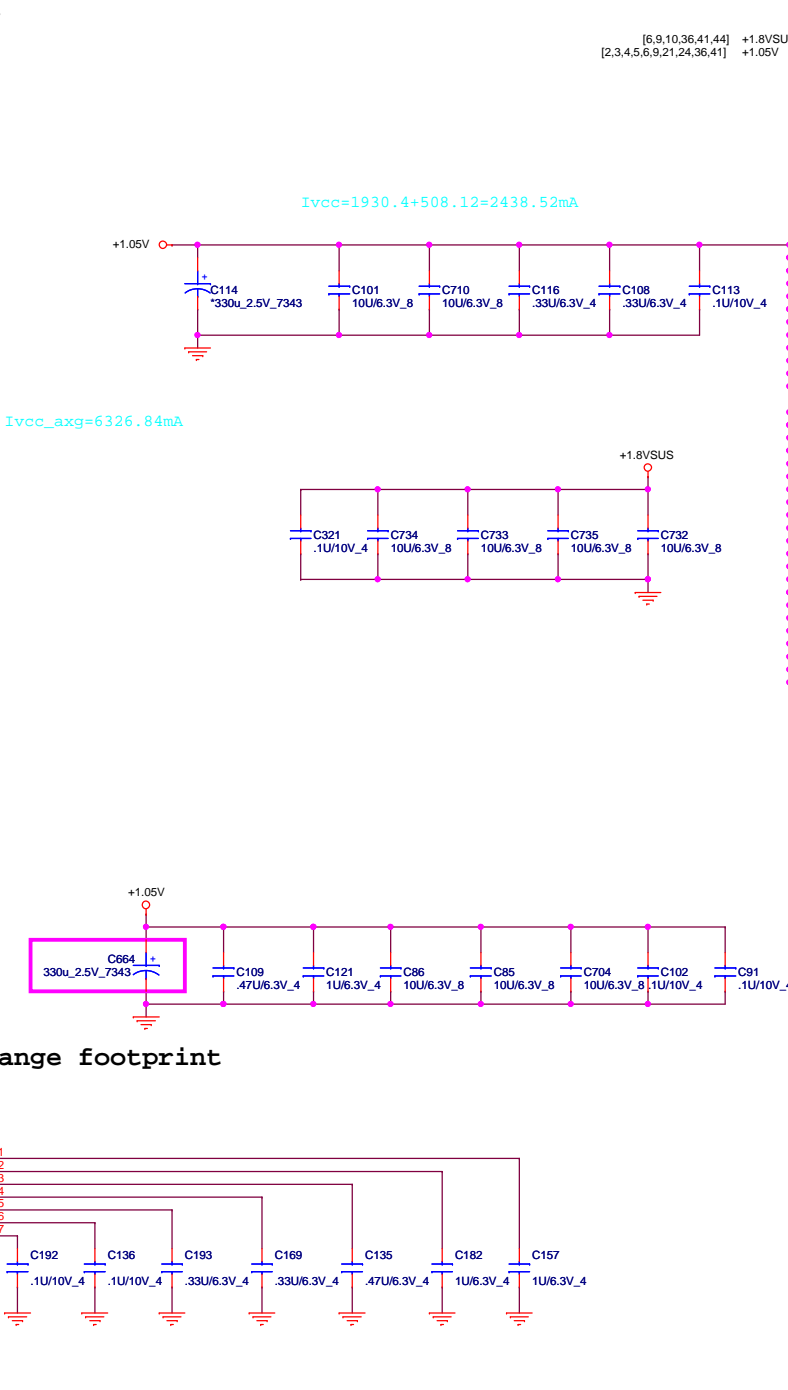
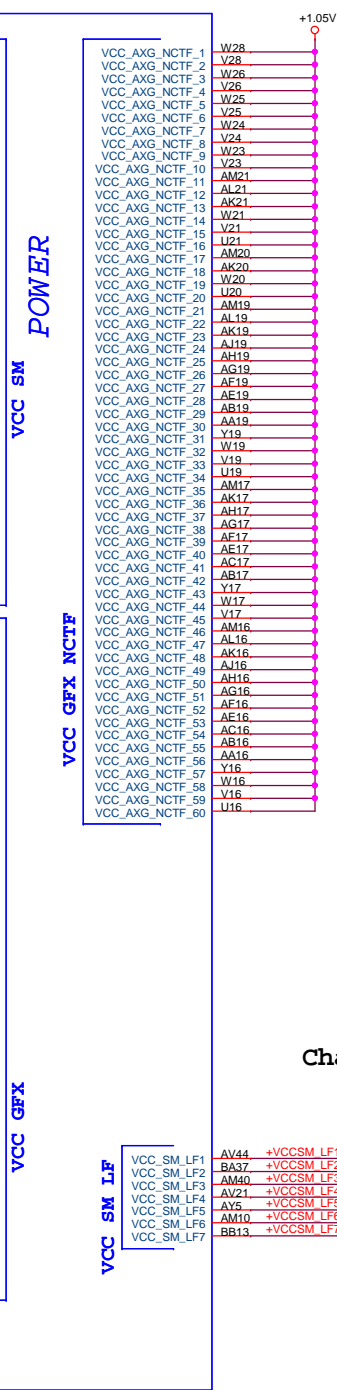
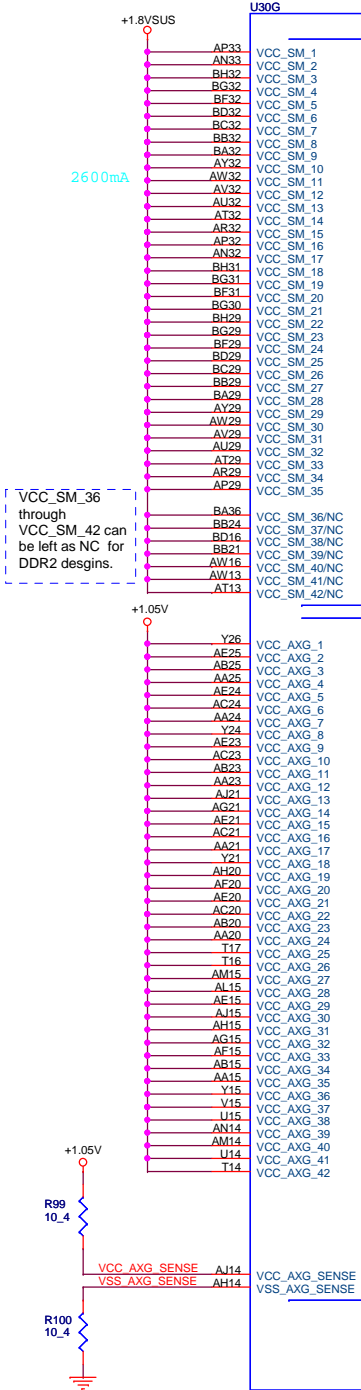
000 = FSB1066
010 = FSB800
011 = FSB667
- Others = Reserved



PROJECT : UT6
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Size Custom	Document Number Cantiga DMi/DISP 2/5	Rev E3A
Date: Wednesday, August 06, 2008		Sheet 6 of 46

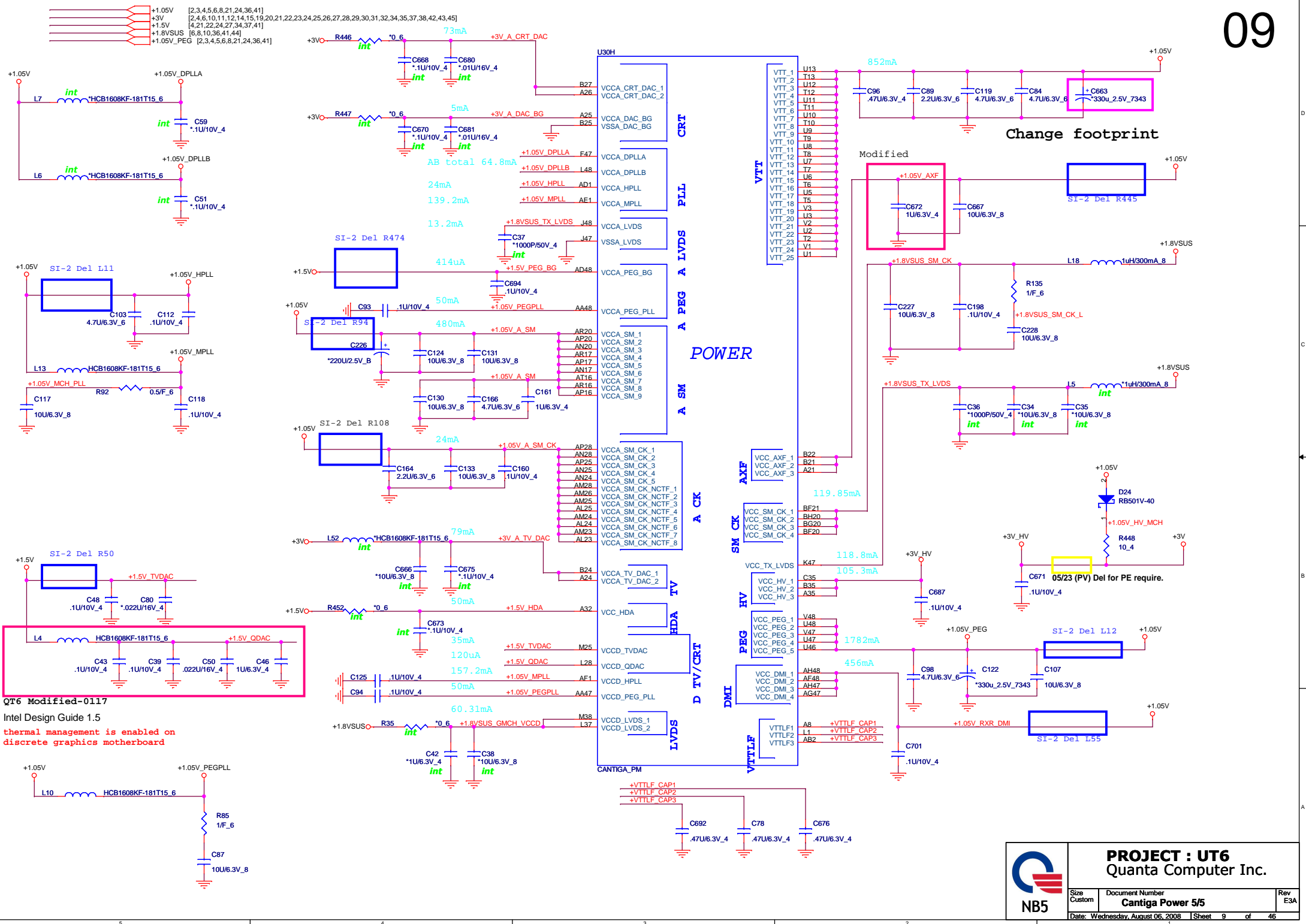




PROJECT : UT6
Quanta Computer Inc.

Size Custom Document Number **Cantiga Vcc 4/5** Rev E3A

Date: Wednesday, August 06, 2008 Sheet 8 of 46



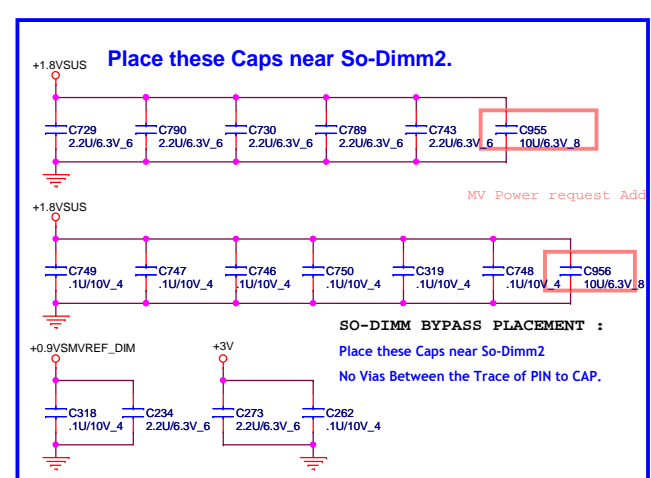
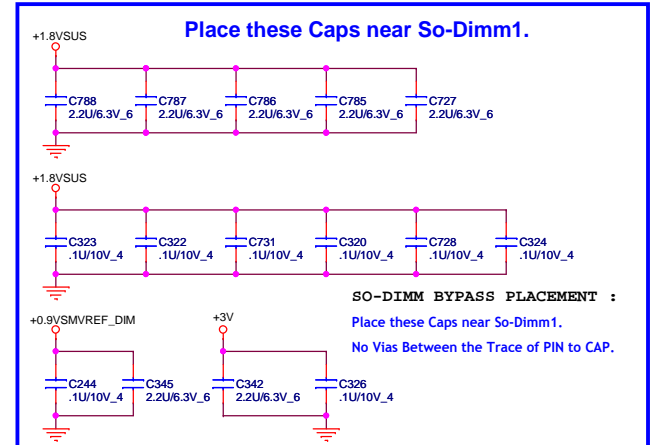
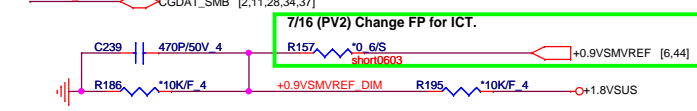
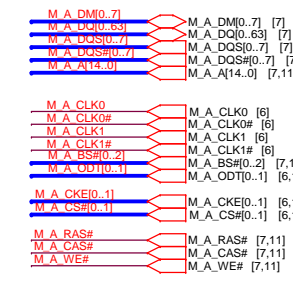
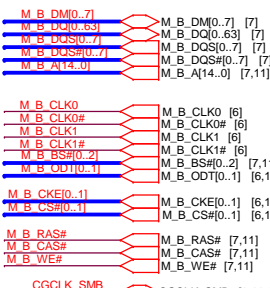
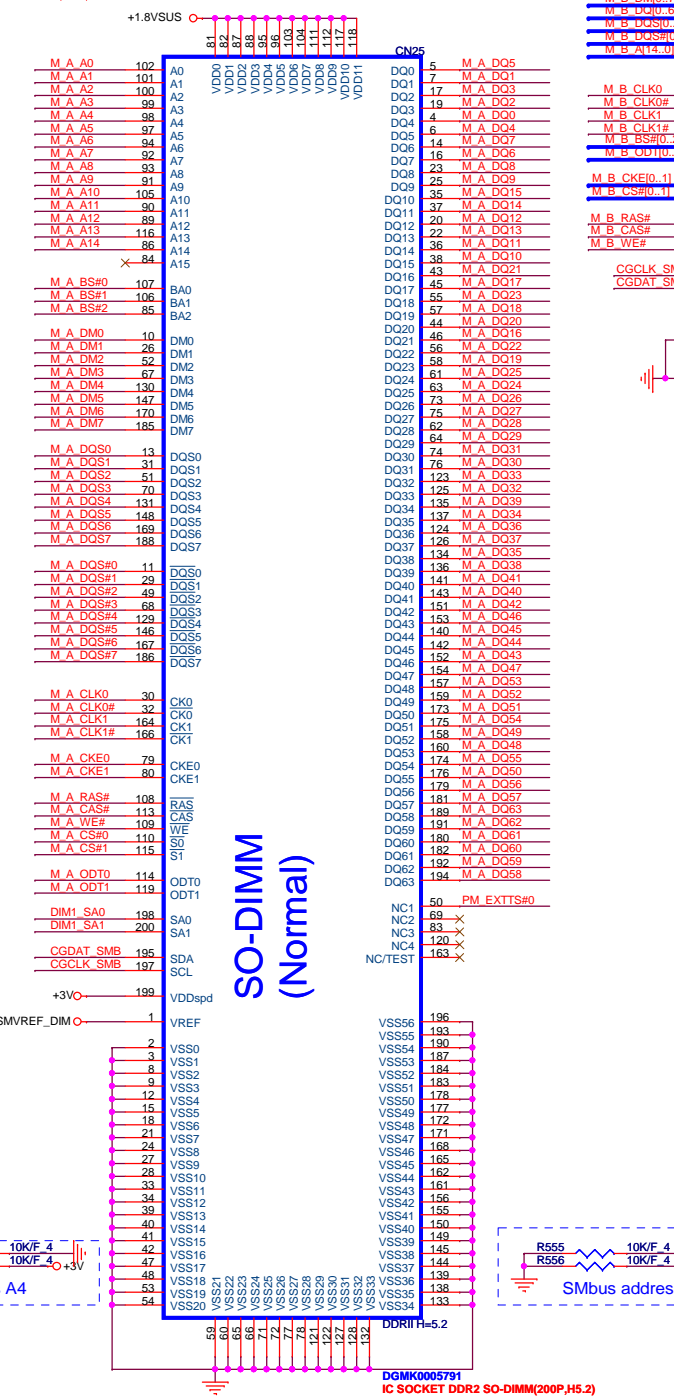
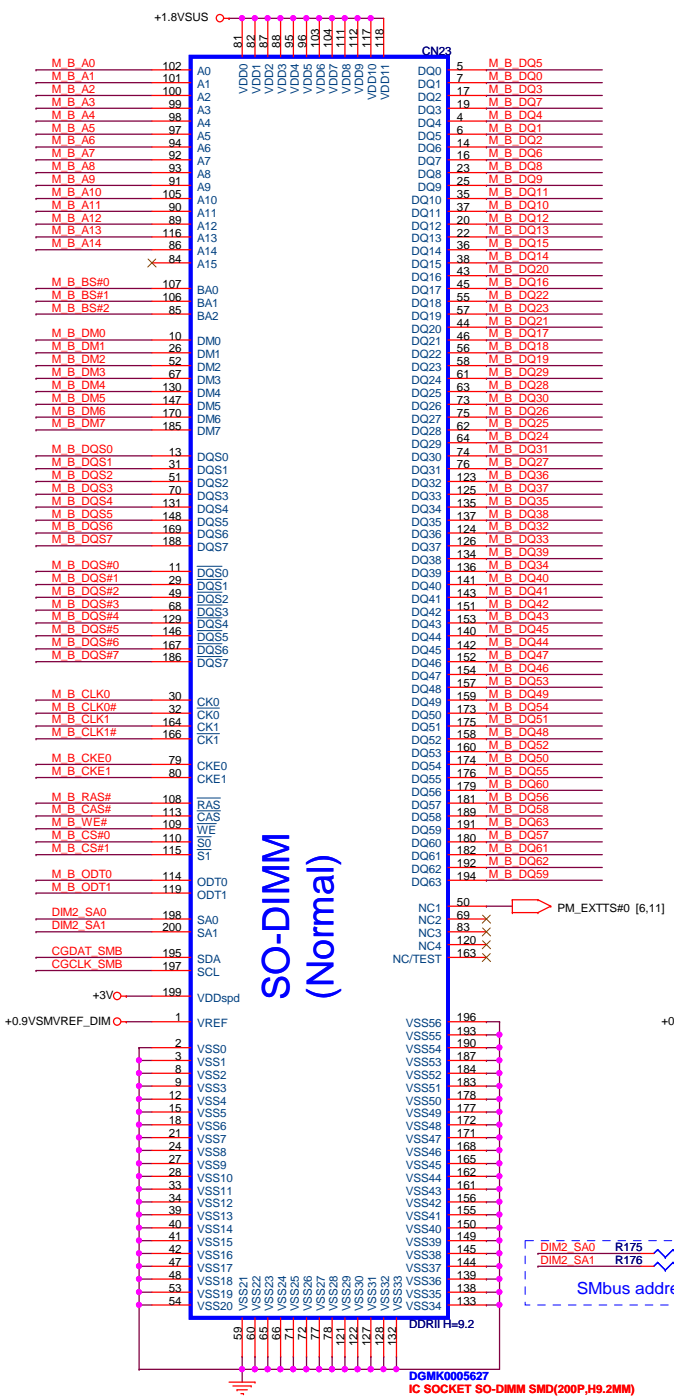
QT6 Modified-0117
 Intel Design Guide 1.5
 thermal management is enabled on discrete graphics motherboard

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[2,4,6,9,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45]

[6,8,9,36,41,44] +1.8VSUS

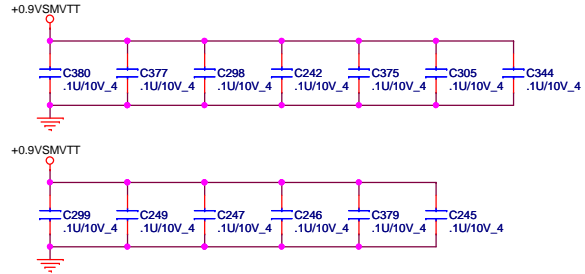


PROJECT : UT6
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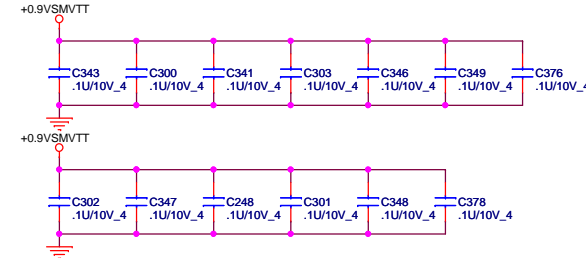
Size Custom	Document Number	Rev E3A
	DDR2 DIMM	
Date: Thursday, August 07, 2008	Sheet 10 of 46	

DDRII DUAL CHANNEL A,B.

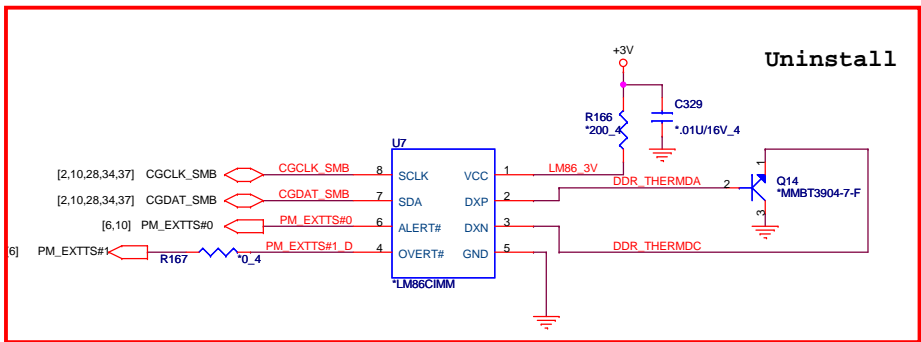
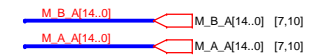
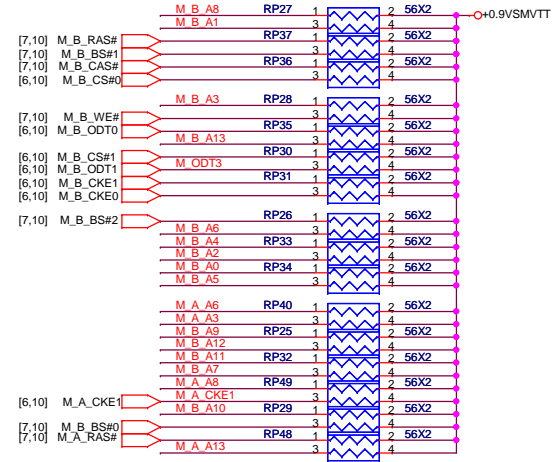
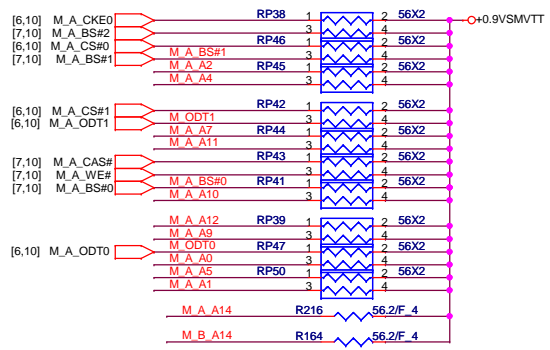
DDRII A CHANNEL



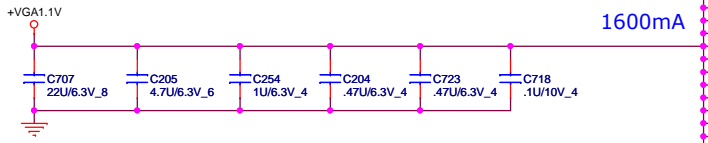
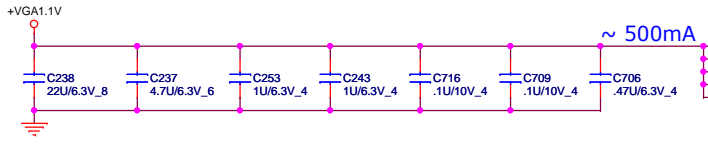
DDRII B CHANNEL



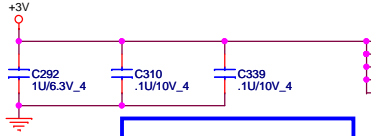
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



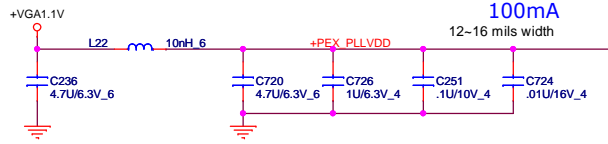
[2,4,6,9,10,11,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V [13,14,44] +VGA1.1V



Near BGA



[43] VGA_SENSE SI-2 4/10 For Nvidia recommend.

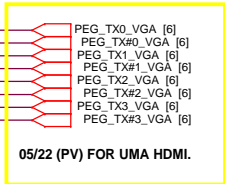


U35A BG4699-NVIDIA-NB8P-GS COMMON

- AK16 PEX_IOVDD_1
- AK17 PEX_IOVDD_2
- AK21 PEX_IOVDD_3
- AK24 PEX_IOVDD_4
- AK27 PEX_IOVDD_5
- AG11 PEX_IOVDDQ_1
- AG12 PEX_IOVDDQ_2
- AG13 PEX_IOVDDQ_3
- AG15 PEX_IOVDDQ_4
- AG16 PEX_IOVDDQ_5
- AG17 PEX_IOVDDQ_6
- AG18 PEX_IOVDDQ_7
- AG22 PEX_IOVDDQ_8
- AG23 PEX_IOVDDQ_9
- AG24 PEX_IOVDDQ_10
- AG25 PEX_IOVDDQ_11
- AG26 PEX_IOVDDQ_12
- AJ14 PEX_IOVDDQ_13
- AJ15 PEX_IOVDDQ_14
- AJ19 PEX_IOVDDQ_15
- AJ21 PEX_IOVDDQ_16
- AJ22 PEX_IOVDDQ_17
- AJ24 PEX_IOVDDQ_18
- AJ25 PEX_IOVDDQ_19
- AJ27 PEX_IOVDDQ_20
- AK18 PEX_IOVDDQ_21
- AK20 PEX_IOVDDQ_22
- AK23 PEX_IOVDDQ_23
- AK26 PEX_IOVDDQ_24
- AL16 PEX_IOVDDQ_25

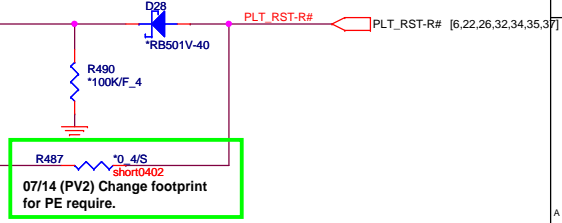
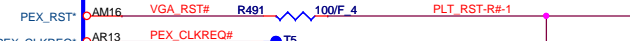
PCI EXPRESS

- PEX_RX0 AP17 PEG TX0 VGA
- PEX_RX0* AN17 PEG TX#0 VGA
- PEX_RX1 AN19 PEG TX1 VGA
- PEX_RX1* AP19 PEG TX#1 VGA
- PEX_RX2 AR20 PEG TX2 VGA
- PEX_RX2* AR20 PEG TX#2 VGA
- PEX_RX3 AN20 PEG TX#3 VGA
- PEX_RX3* AN22 PEG TX4
- PEX_RX4 AP22 PEG TX#4
- PEX_RX5 AR22 PEG TX5
- PEX_RX5* AR23 PEG TX#5
- PEX_RX6 AP23 PEG TX6
- PEX_RX6* AN23 PEG TX#6
- PEX_RX7 AN25 PEG TX7
- PEX_RX7* AP25 PEG TX#7
- PEX_RX8 AR25 PEG TX8
- PEX_RX8* AR26 PEG TX#8
- PEX_RX9 AP26 PEG TX9
- PEX_RX9* AN26 PEG TX#9
- PEX_RX10 AN28 PEG TX10
- PEX_RX10* AP28 PEG TX#10
- PEX_RX11 AR28 PEG TX11
- PEX_RX11* AR29 PEG TX#11
- PEX_RX12 AN29 PEG TX12
- PEX_RX12* AN29 PEG TX#12
- PEX_RX13 AN31 PEG TX13
- PEX_RX13* AR31 PEG TX#13
- PEX_RX14 AR32 PEG TX14
- PEX_RX14* AR34 PEG TX15
- PEX_RX15 AP34 PEG TX#15



- PEX_TX0 AL17 C PEG RX0 C171 .1U/10V_4
- PEX_TX0* AM17 C PEG RX#0 C170 .1U/10V_4
- PEX_TX1 AM18 C PEG RX1 C209 .1U/10V_4
- PEX_TX1* AM19 C PEG RX#1 C210 .1U/10V_4
- PEX_TX2 AL19 C PEG RX2 C172 .1U/10V_4
- PEX_TX2* AK19 C PEG RX#2 C173 .1U/10V_4
- PEX_TX3 AL20 C PEG RX3 C145 .1U/10V_4
- PEX_TX3* AM20 C PEG RX#3 C146 .1U/10V_4
- PEX_TX4 AM21 C PEG RX4 C211 .1U/10V_4
- PEX_TX4* AM22 C PEG RX#4 C212 .1U/10V_4
- PEX_TX5 AL22 C PEG RX5 C213 .1U/10V_4
- PEX_TX5* AK22 C PEG RX#5 C214 .1U/10V_4
- PEX_TX6 AL23 C PEG RX6 C147 .1U/10V_4
- PEX_TX6* AM23 C PEG RX#6 C148 .1U/10V_4
- PEX_TX7 AM24 C PEG RX7 C174 .1U/10V_4
- PEX_TX7* AK25 C PEG RX#7 C175 .1U/10V_4
- PEX_TX8 AL25 C PEG RX8 C149 .1U/10V_4
- PEX_TX8* AK26 C PEG RX#8 C150 .1U/10V_4
- PEX_TX9 AL26 C PEG RX9 C176 .1U/10V_4
- PEX_TX9* AM26 C PEG RX#9 C177 .1U/10V_4
- PEX_TX10 AM27 C PEG RX10 C151 .1U/10V_4
- PEX_TX10* AM28 C PEG RX#10 C152 .1U/10V_4
- PEX_TX11 AL28 C PEG RX11 C199 .1U/10V_4
- PEX_TX11* AK28 C PEG RX#11 C200 .1U/10V_4
- PEX_TX12 AM29 C PEG RX12 C178 .1U/10V_4
- PEX_TX12* AL29 C PEG RX#12 C179 .1U/10V_4
- PEX_TX13 AM29 C PEG RX13 C162 .1U/10V_4
- PEX_TX13* AM30 C PEG RX#13 C163 .1U/10V_4
- PEX_TX14 AM31 C PEG RX14 C156 .1U/10V_4
- PEX_TX14* AM32 C PEG RX#14 C157 .1U/10V_4
- PEX_TX15 AN32 C PEG RX15 C180 .1U/10V_4
- PEX_TX15* AP32 C PEG RX#15 C181 .1U/10V_4

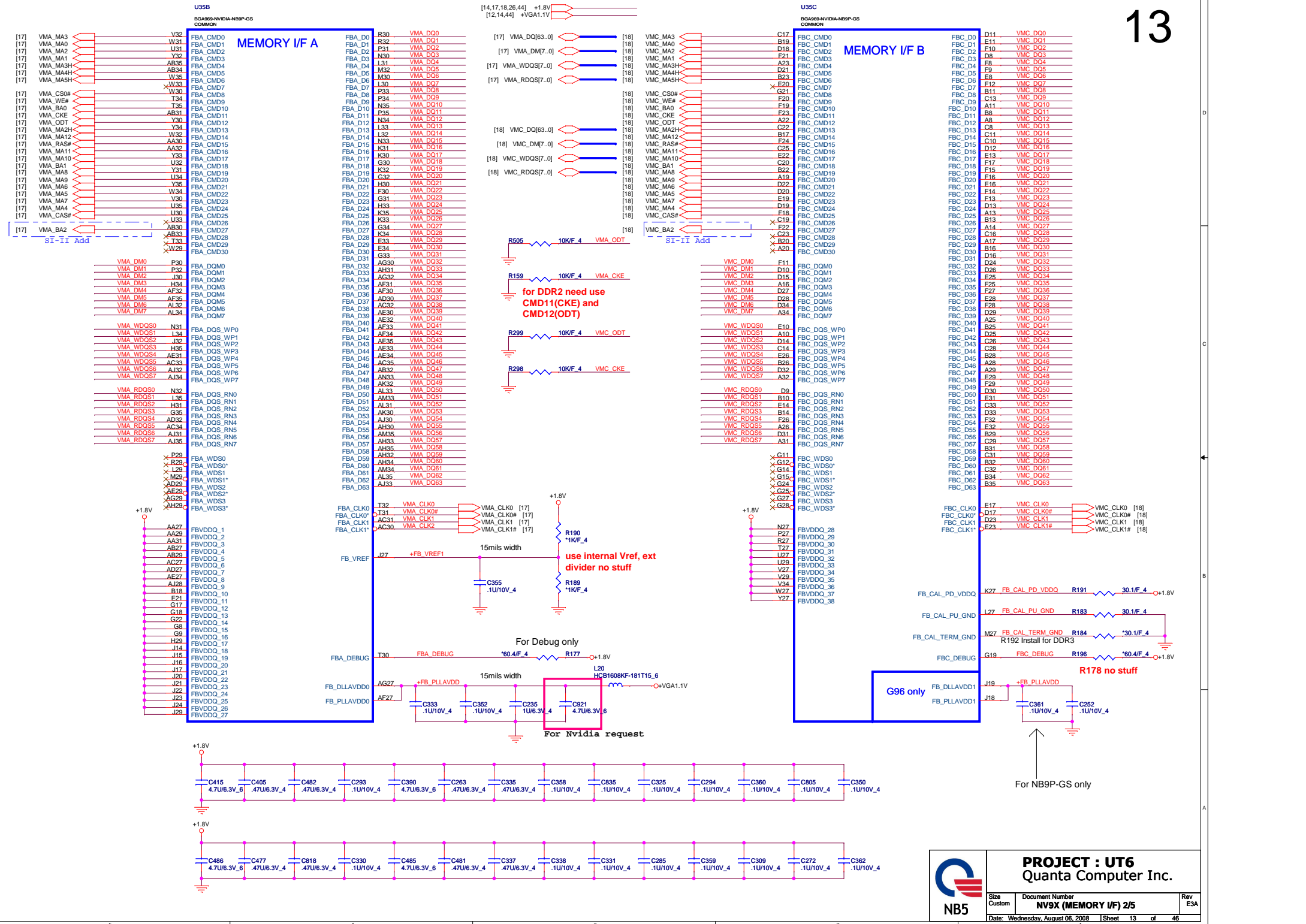
- PEX_REFCLK AR16 CLK_PCIE_VGA
- PEX_REFCLK* AR17 CLK_PCIE_VGA#



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NB5

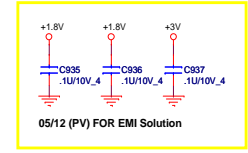
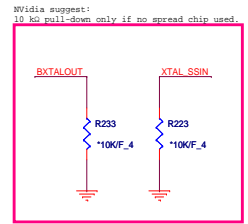
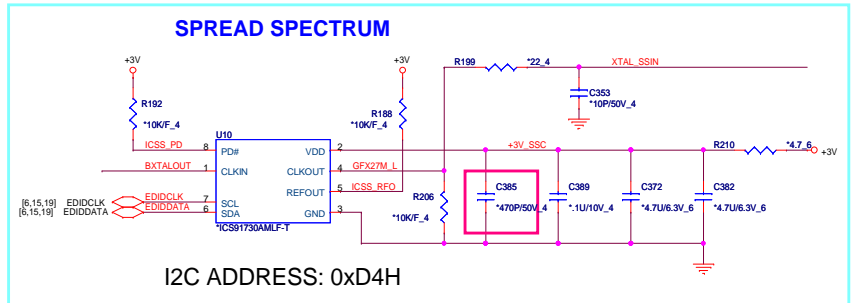
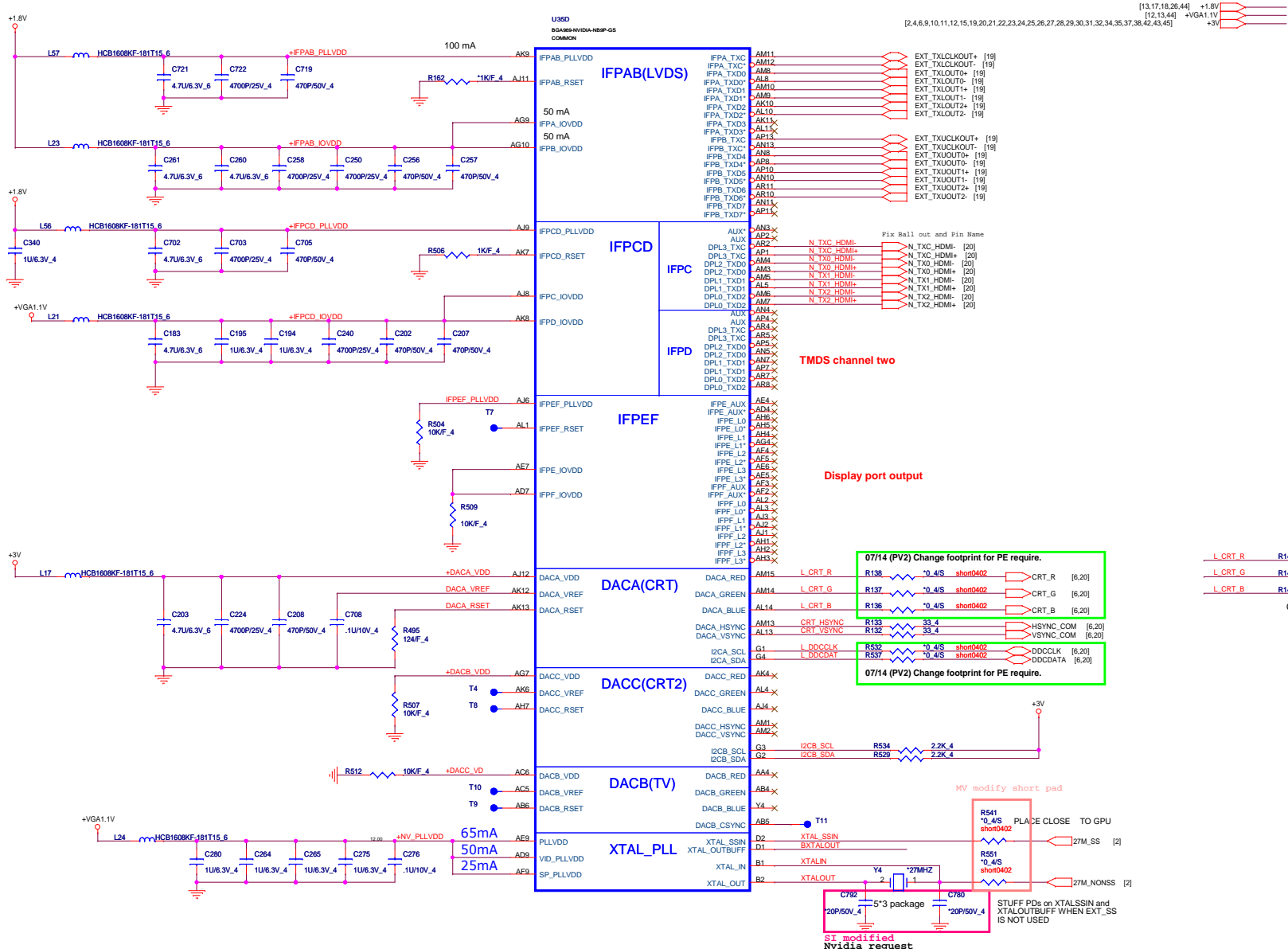
Size Custom	Document Number NV9X (PCIE I/F) 1/5	Rev E3A
Date: Wednesday, August 06, 2008		Sheet 12 of 46

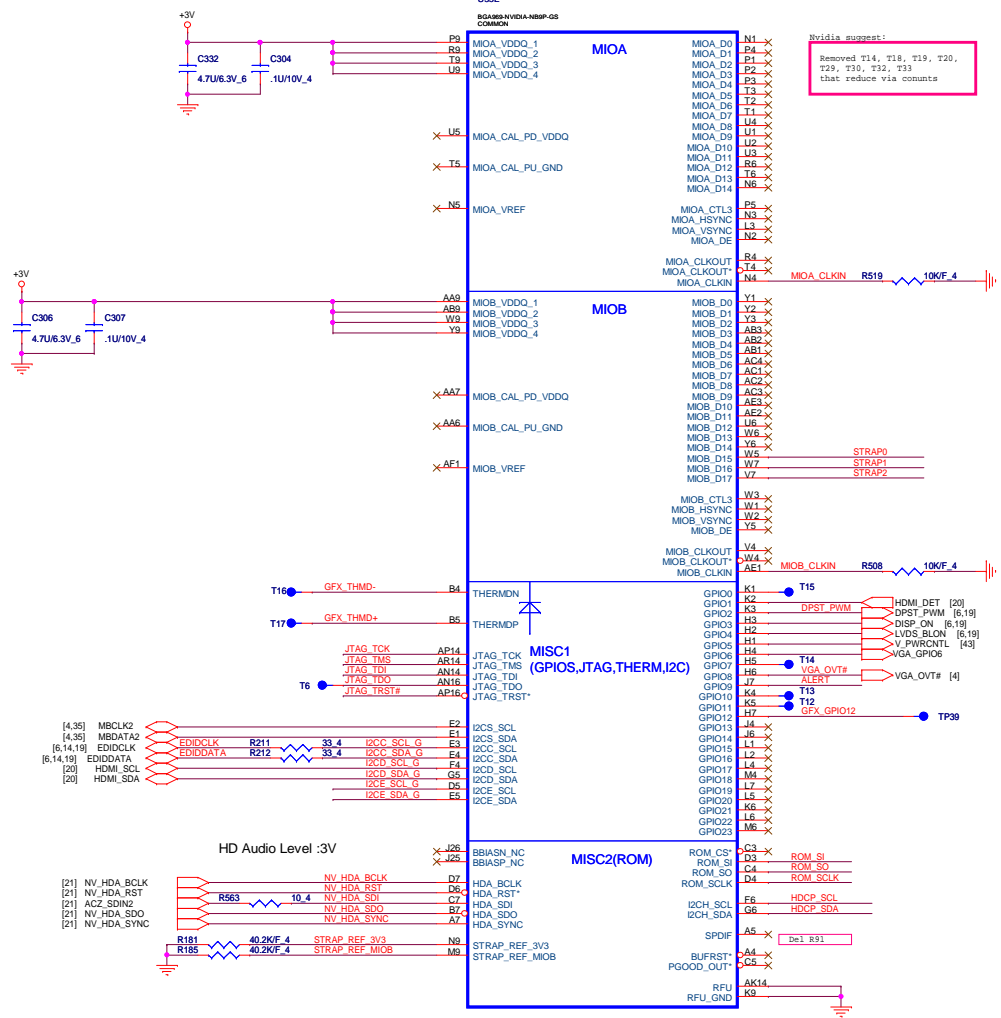


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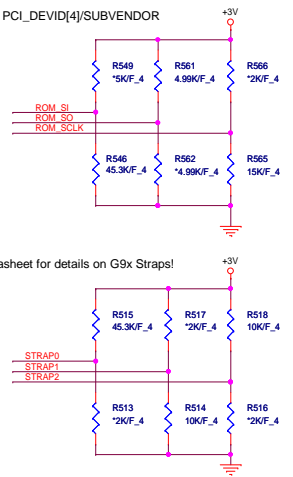
Size Custom	Document Number NV9X (MEMORY I/F) 2/5	Rev E3A
Date: Wednesday, August 06, 2008 Sheet 13 of 46		





NB9P-GS (G96) Straps NB9M-GE (G98) Straps GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

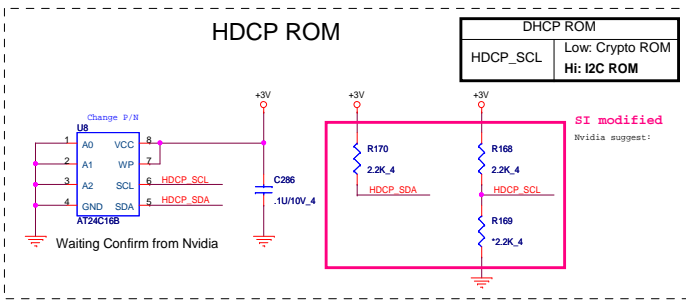


Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

Delete VGA thermal circuit



NB9X VRAM Configuration Table

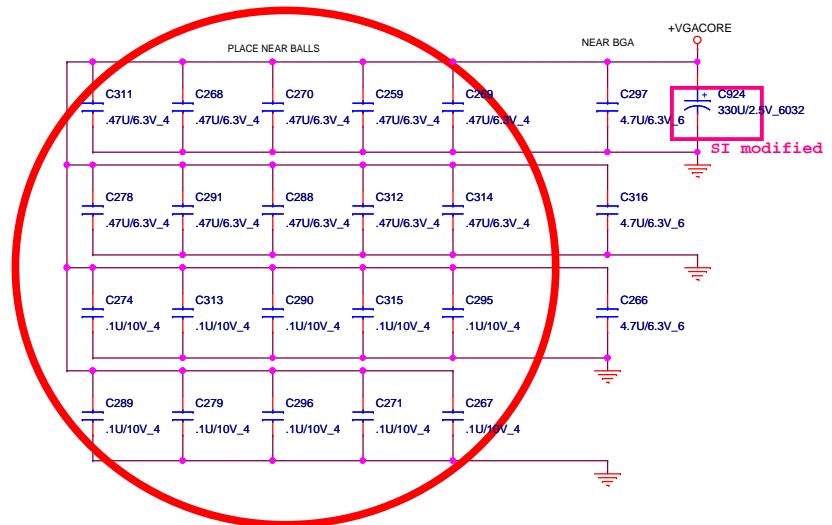
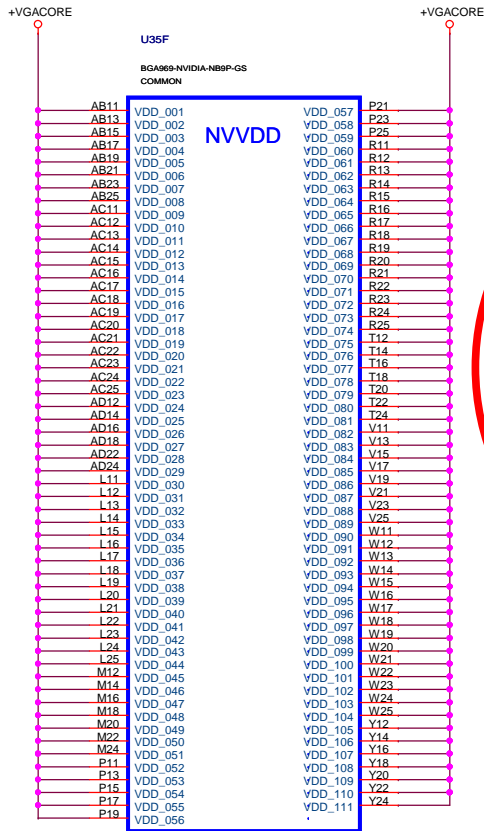
RAM_CFG[3:0]	DESCRIPTION	Vendor
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix HY5PS12162TGF-25
0110	DDR2 32Mx16x8, 128bit, 512MB	Olmonda HYB18T1216182P-25
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung K4N51163QE-ZC25
0100	DDR2 32Mx16x8, 128bit, 512MB	Nanya/Elipida
0000	DDR2 64Mx16x8, 128bit, 1GB	Hynix
0001	DDR2 64Mx16x8, 128bit, 1GB	Samsung
0010	DDR2 64Mx16x8, 128bit, 1GB	Olmonda

PCI_DEVID: STRAP2

- NB9M-GE 0x06E 8 1000 default
- NB9M-GS 0x06E 9 1001
- NB9P-GE2 0x064 8 1000
- NB9P-GS 0x064 9 1001 default

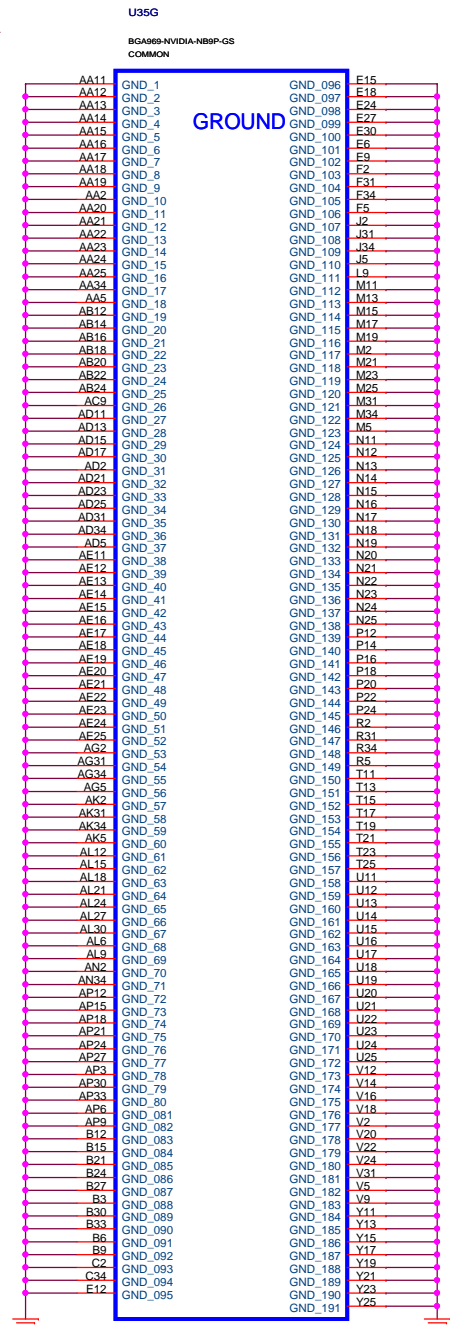
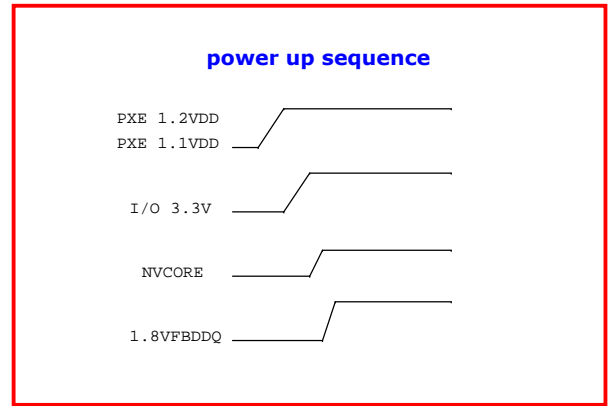
CS33572FB13 RES CHIP 35.7K 1/16W +-1%(0402)

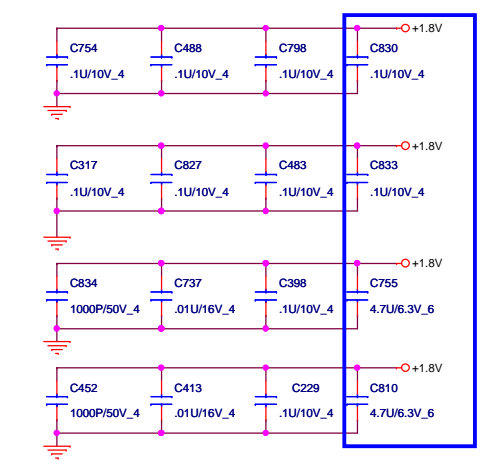
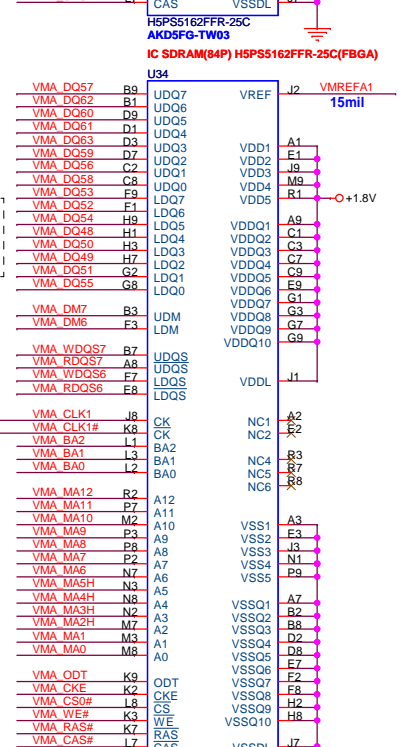
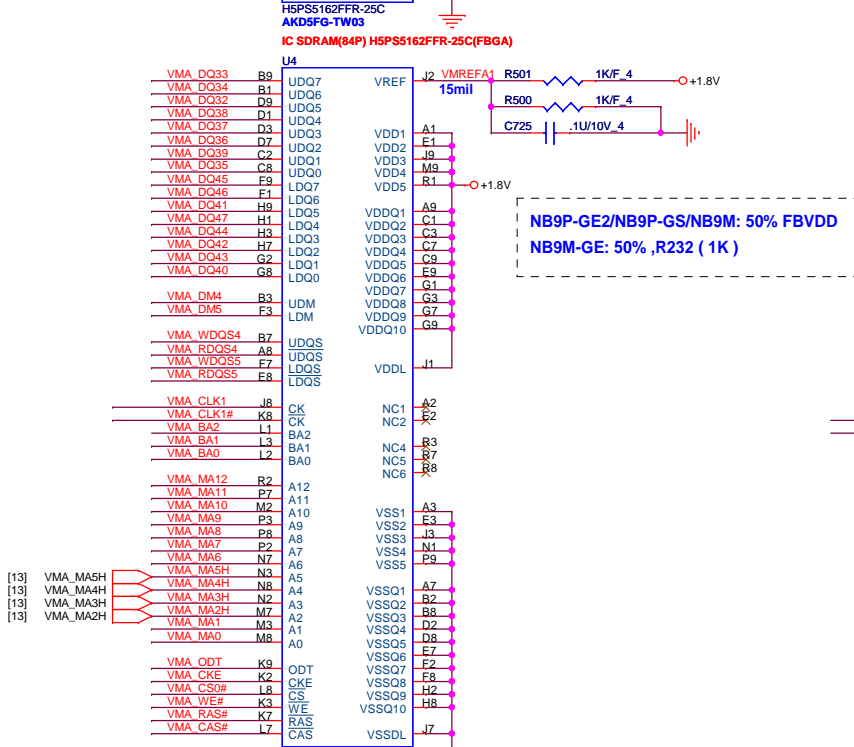
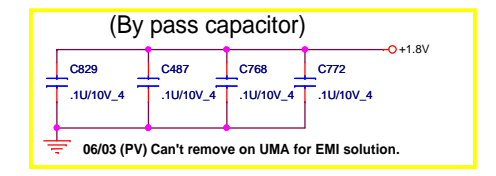
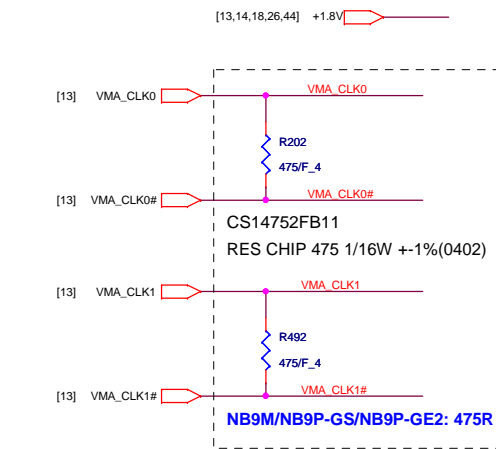
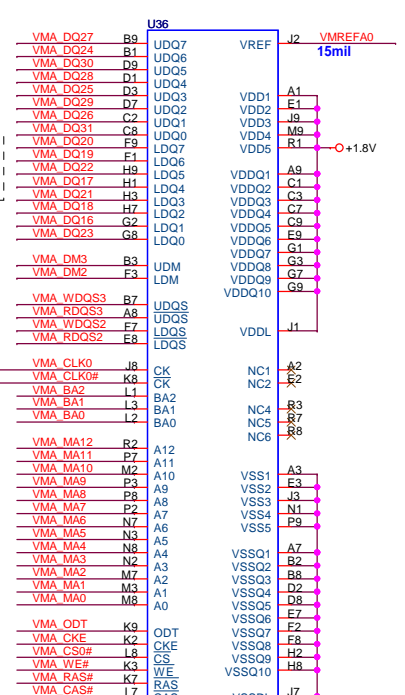
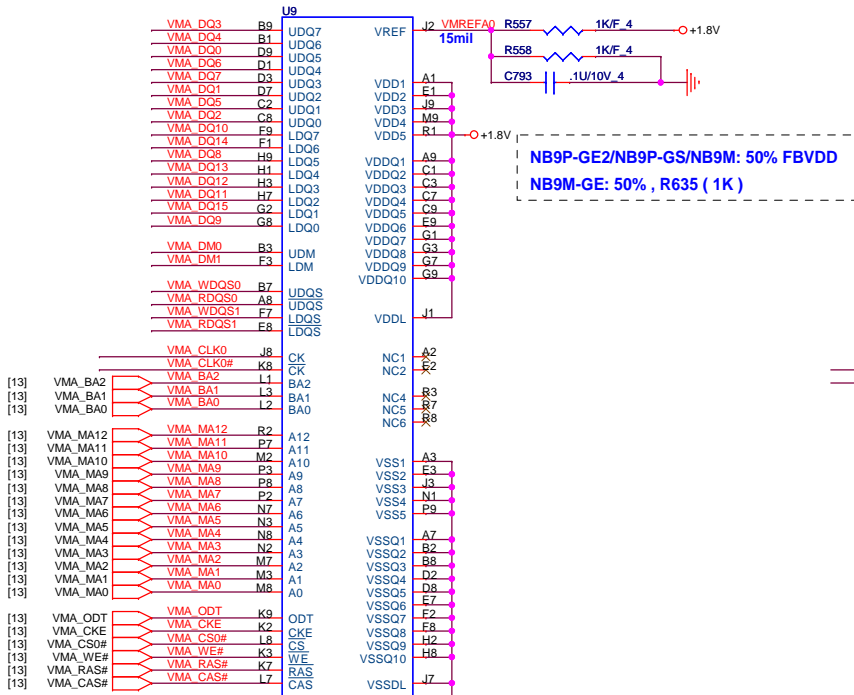
NVVDD Decoupling



Follow Design Guide DG-03276-001 4.7uF x3 and 0.47x10 uF instead of 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V





For DB:
 NB9P : AKD59G-T502(Samsung,32M*16)
 NB9M : AKD5FG-TW31(Hynix,32M*16)
 AKD5FG-T*03(Qimonda 32M*16)

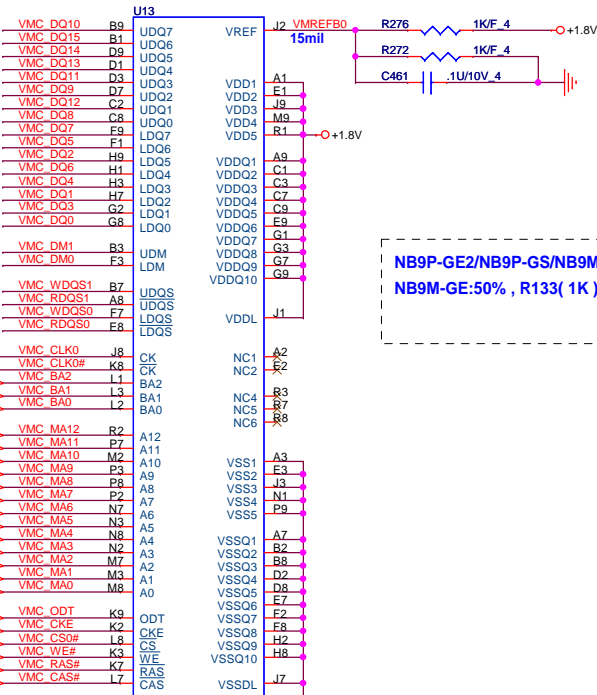
[13] VMA_DQ[63..0]
 [13] VMA_DM[7..0]
 [13] VMA_WDQS[7..0]
 [13] VMA_RDQS[7..0]

256Mb : AKD5JGAT*05
 512Mb : AKD59G-T*01

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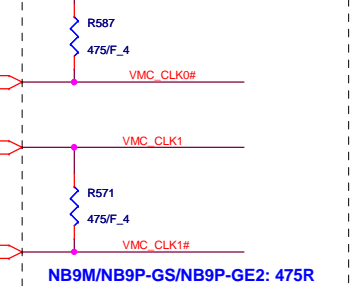
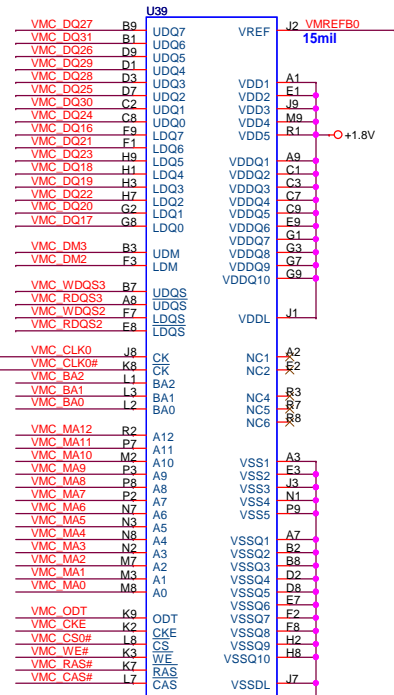
Size Custom Document Number NV9X VRAM-1(GDDR2 BGA84) Rev E3A
 Date: Wednesday, August 06, 2008 Sheet 17 of 46

[13,14,17,26,44] +1.8V

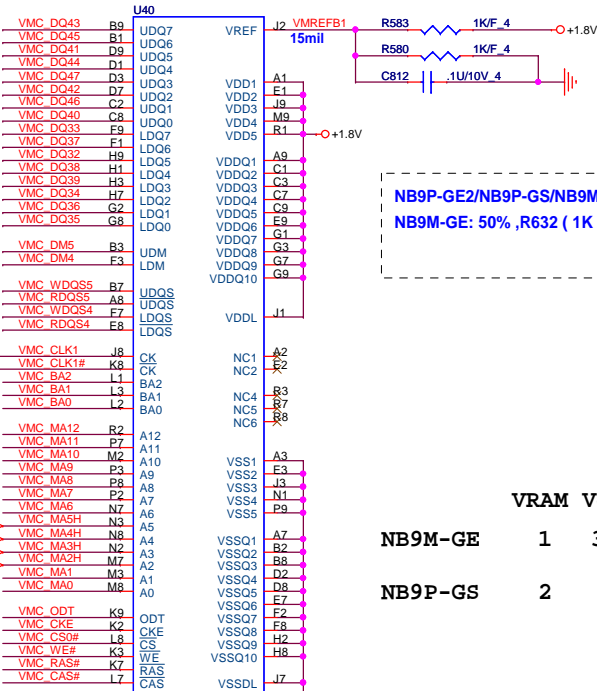


NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE:50%, R133(1K)

H5PS5162FFR-25C
AKD5FG-TW03
IC SDRAM(84P) H5PS5162FFR-25C(FBGA)

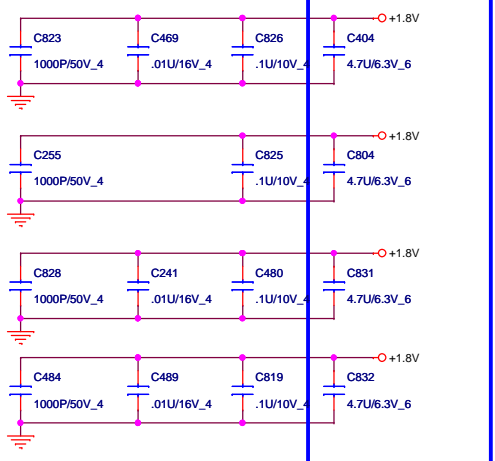
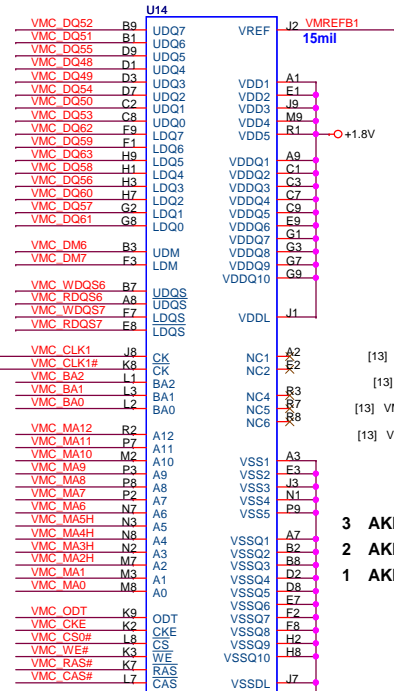


CS14752FB11 RES CHIP 475 1/16W +-1%(0402)



NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50%, R632 (1K)

H5PS5162FFR-25C
AKD5FG-TW03
IC SDRAM(84P) H5PS5162FFR-25C(FBGA)



VRAM Vendor

NB9M-GE	1	3
NB9P-GS	2	

- [13] VMC_DQ[63..0]
- [13] VMC_DM[7..0]
- [13] VMC_WDQS[7..0]
- [13] VMC_RDQS[7..0]

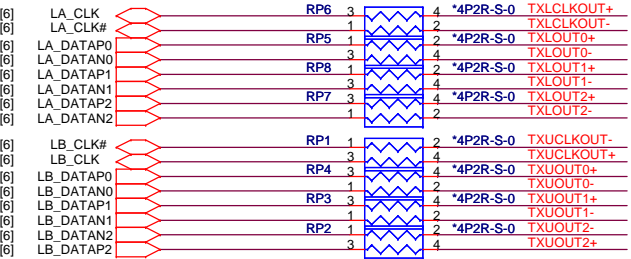
- 3 AKD5FG-T501 IC SDRAM(84P) K4N51163QG-HC25(FBGA) Samsung
- 2 AKD5FG-T*03 IC SDRAM(84P)HYB18T512161B2F-25(TFBGA) Qimonda
- 1 AKD5FG-TW31 IC SDRAM(84P) HY5PS121621CFP-25(FBGA) Hynix



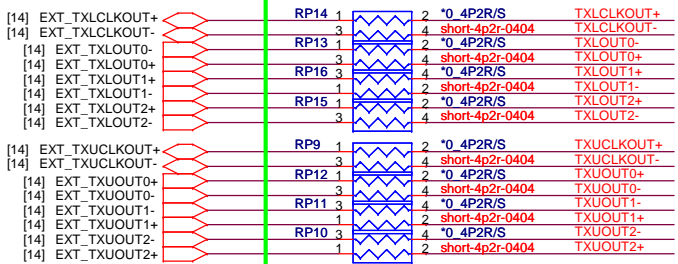
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1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

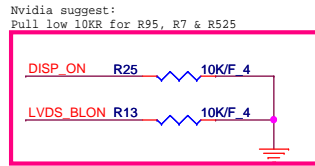
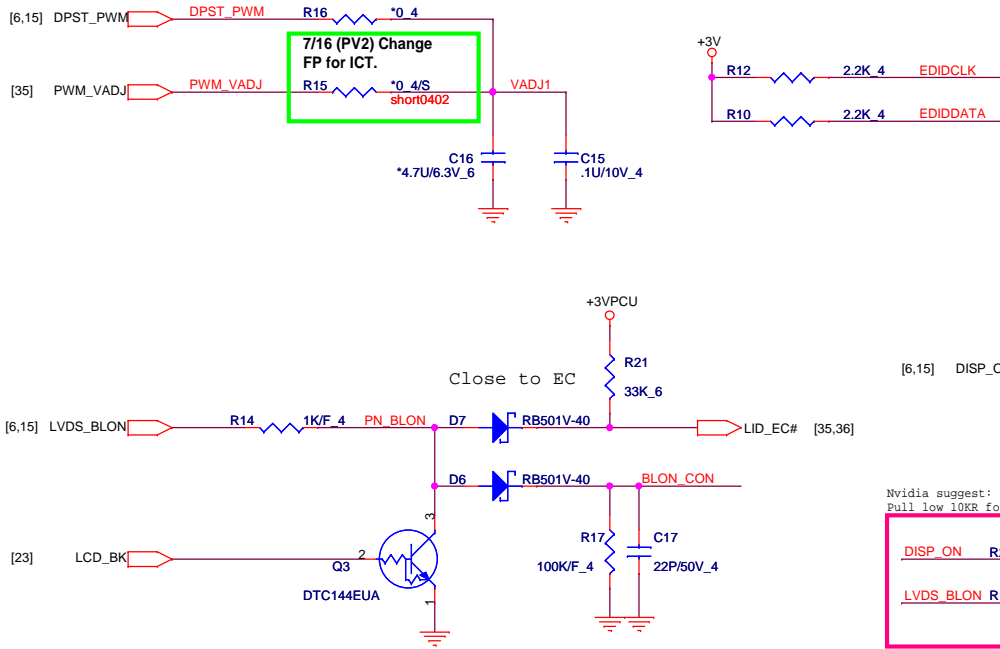
OPTION SIGNAL FROM NB FOR UMA VGA



OPTION SIGNAL FROM Nvidia to VGA

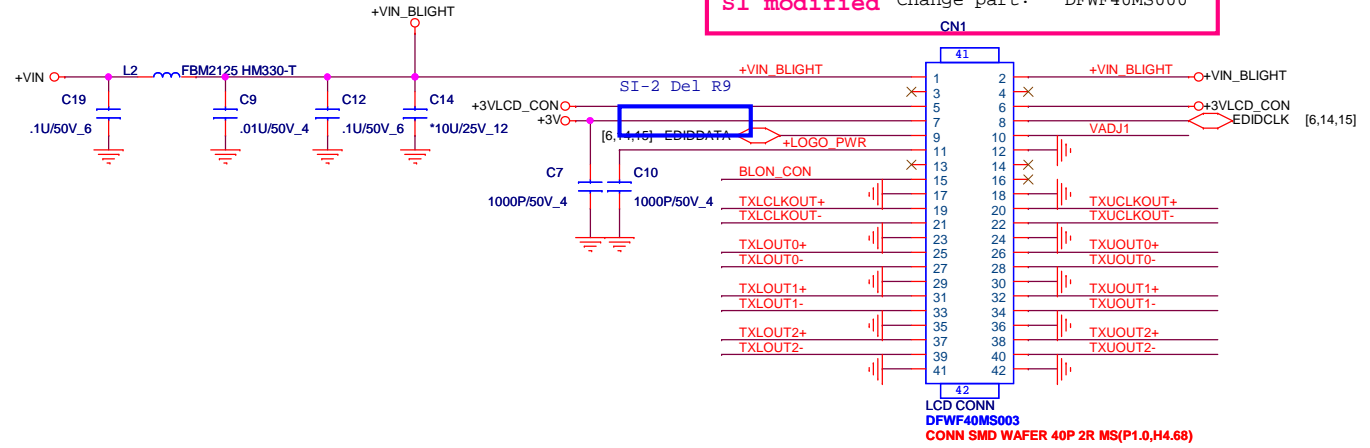


07/14 (PV2) Change footprint for PE require.



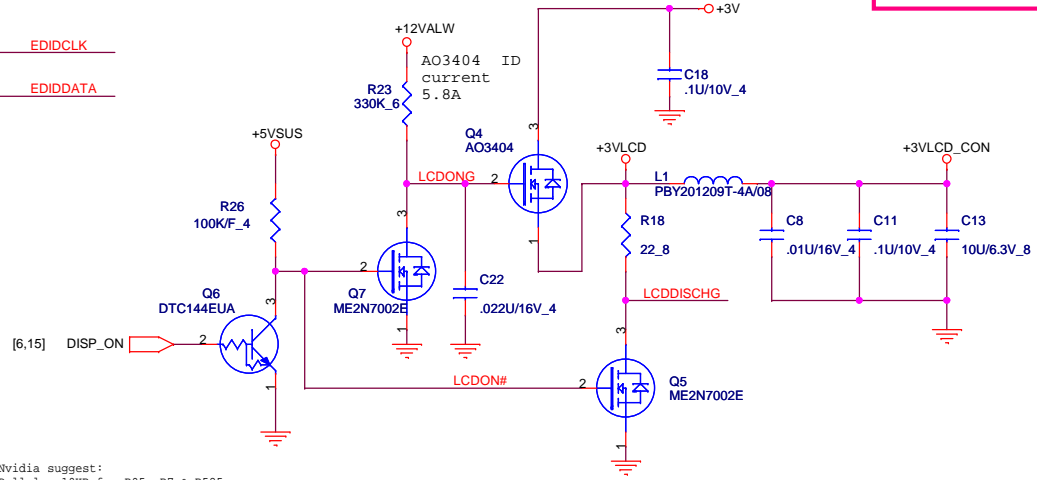
[2,4,6,9,10,11,12,14,15,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V
 [3,20,24,25,27,28,30,31,34,36,38,45] +5V
 [29,38,39,40,41,42,43,44,45] +VIN
 [21,30,31,35,36,38,39,40,45] +3VPCU
 [27,30,36,40,45] +12VALW

19



+5V R11 75R/F 6 +LOGO_PWR
 0090 use 100 ohm and must change back to 75ohm

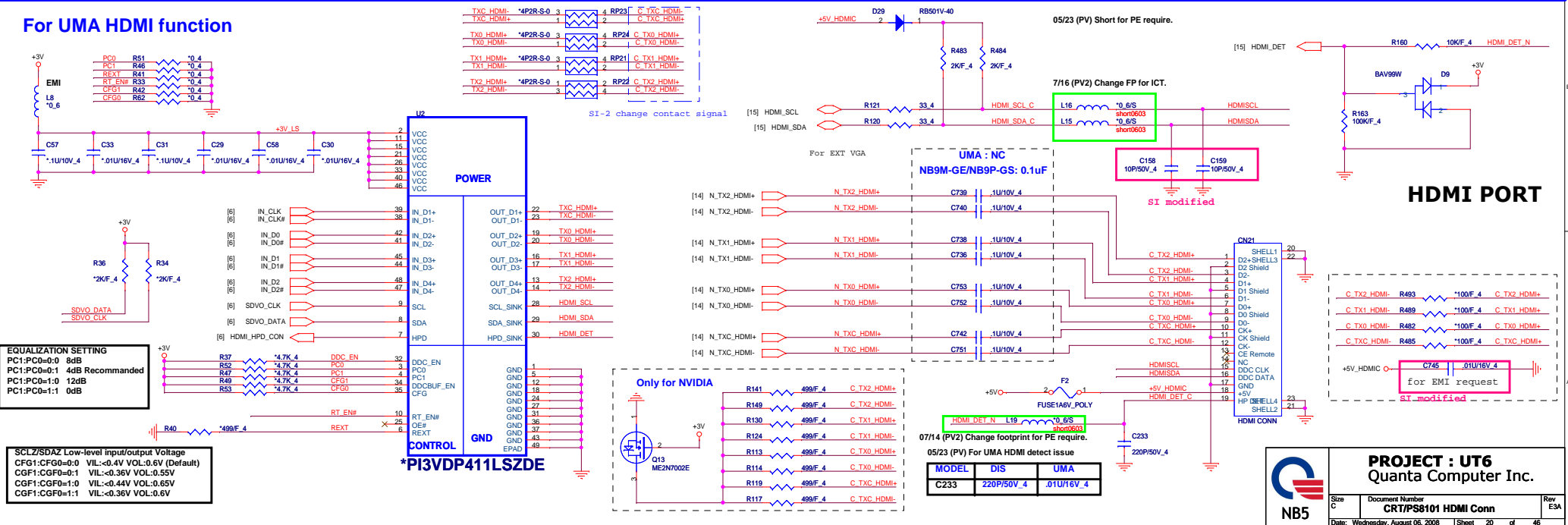
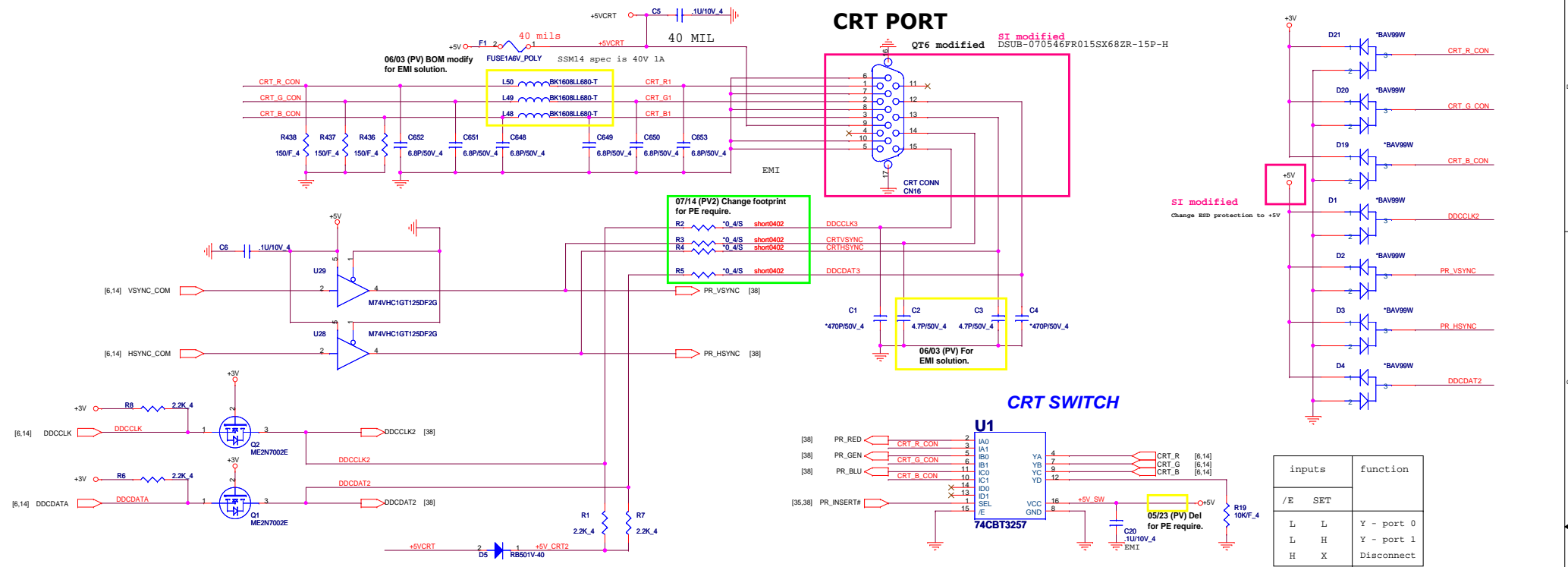
SI modified
 Del CN7,R88,C115
 Remove Logo light2

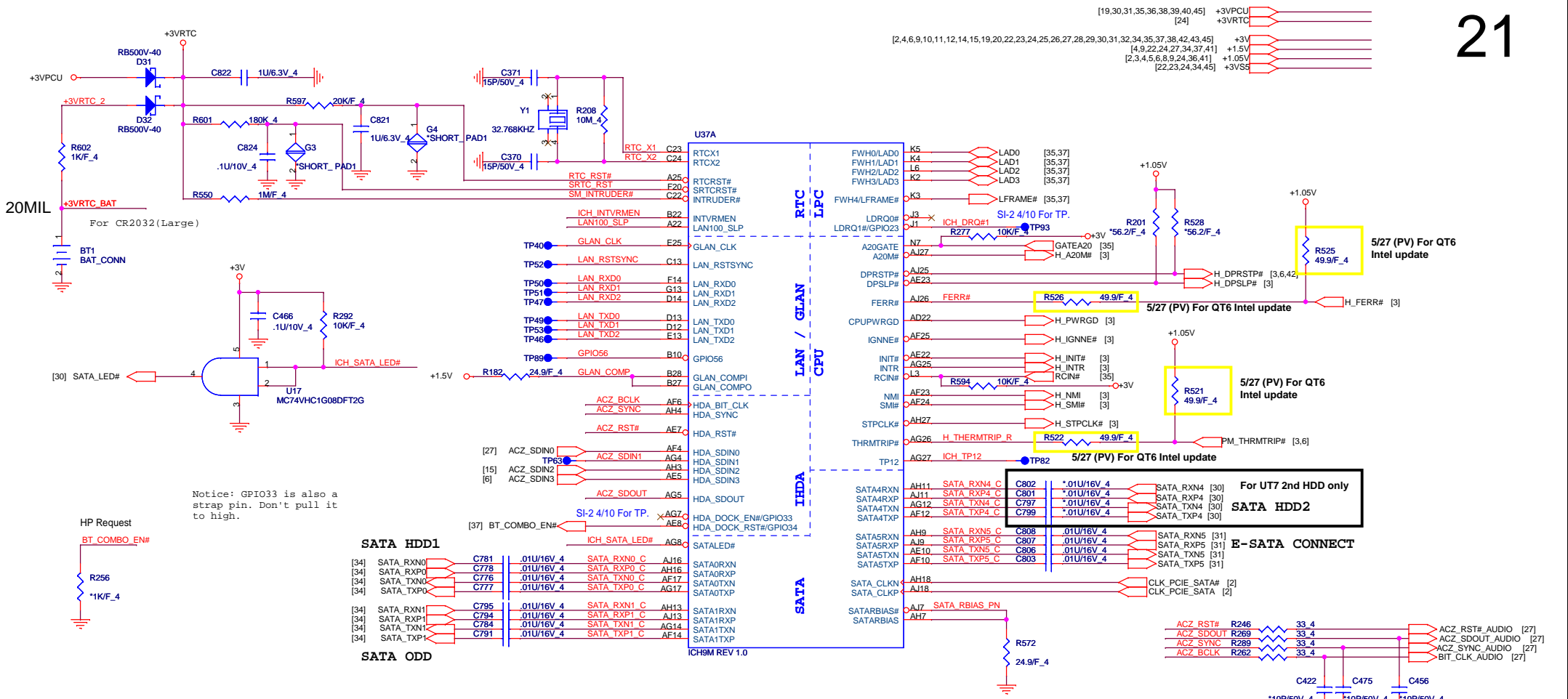


NB5

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Size B	Document Number LCD CONN/Lid function	Rev E3A
Date: Wednesday, August 06, 2008	Sheet 19	of 46





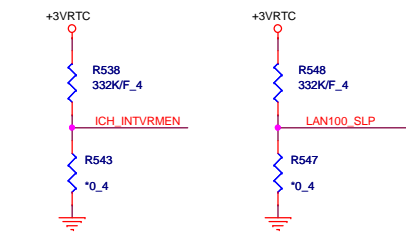
SB Strap

ICH9-M Internal VR Enable strap
(Internal VR for VccSus1_05, VccSus1_5 and VccCL1_5)

ICH9-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

INTVRMEN Low = Internal VR disable
High = Internal VR enable(Default)

LAN100_SLP Low = Internal VR disable
High = Internal VR enable(Default)



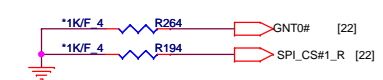
XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPL_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)



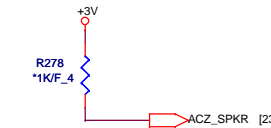
A16 swap override strap

PCI_GNT#3	Low = A16 swap override enabled Hi = Default
-----------	---



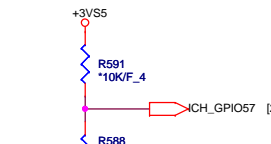
No Reboot Strap

ACZ_SPKR	Low: Default Hi: No reboot
----------	-------------------------------



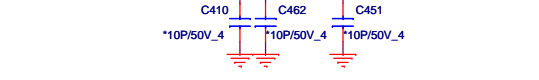
TPM physical presence

ICH_GPIO57	Low: Default
------------	--------------



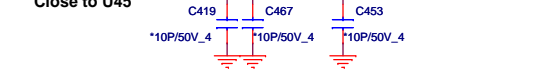
For GM UMA only

ACZ_RST#	R242	*33 4	ACZ_RST#_MCH	[6]
ACZ_SDOUT	R266	*33 4	ACZ_SDOUT_MCH	[6]
ACZ_SYNC	R274	*33 4	ACZ_SYNC_MCH	[6]
ACZ_BCLK	R258	*33 4	ACZ_BITCLK_MCH	[6]



Close to U45

ACZ_RST#	R252	22 4	NV_HDA_RST	[15]
ACZ_SDOUT	R268	22 4	NV_HDA_SDO	[15]
ACZ_SYNC	R283	22 4	NV_HDA_SYNC	[15]
ACZ_BCLK	R261	22 4	NV_HDA_BCLK	[15]



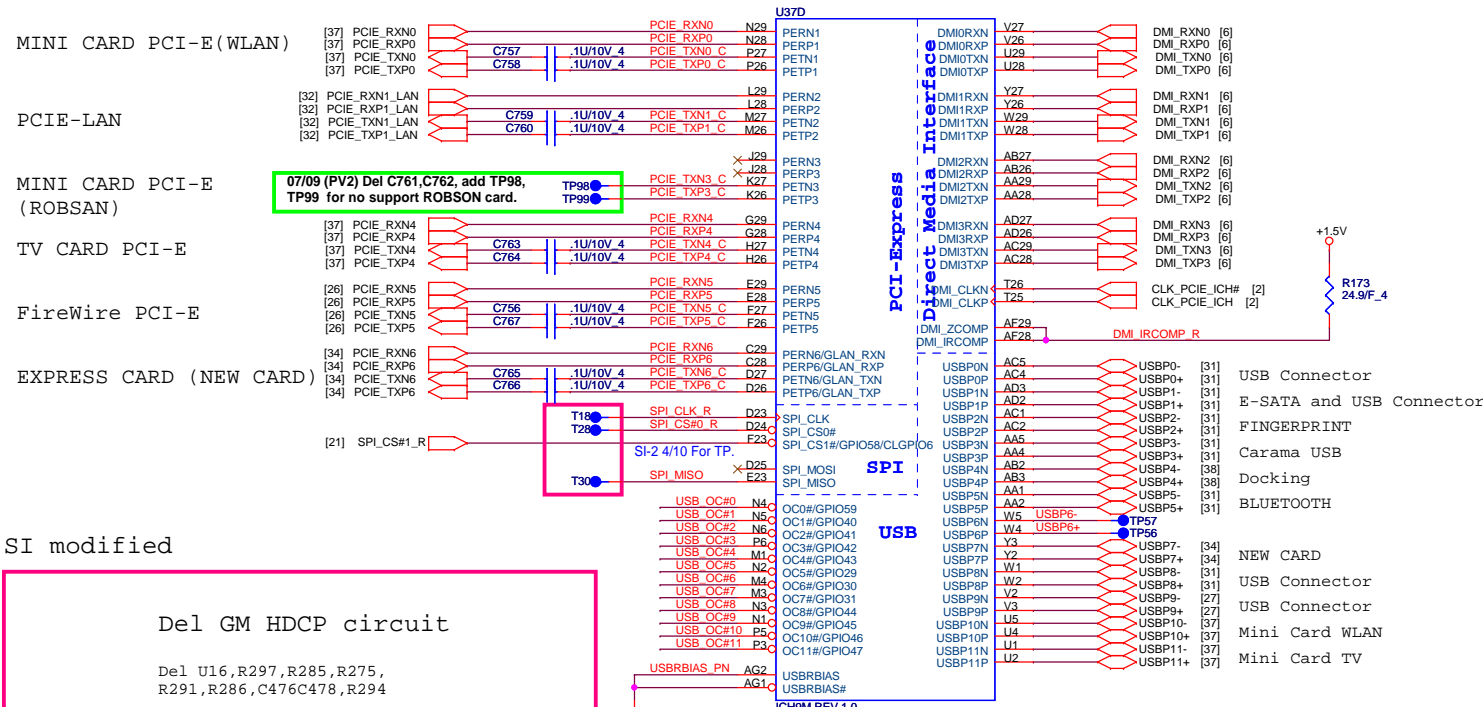
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NB5 Size Custom Document Number **ICH9-M Host 1/4** Rev E3A

Date: Wednesday, August 06, 2008 | Sheet 21 of 46

SWAP PCIE PORT6 to PORT2 (Lan and New card swap) -->Rename the port name by function and port

[2,4,6,9,10,11,12,14,15,19,20,21,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V
 [4,9,21,24,27,34,37,41] +1.5V
 [23,31,37,41,42,43,45] +3VSUS
 [21,23,24,34,45] +3VSS

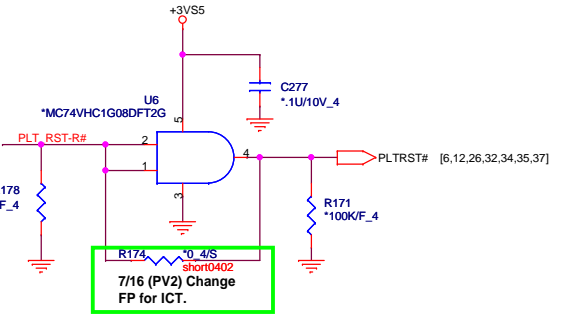
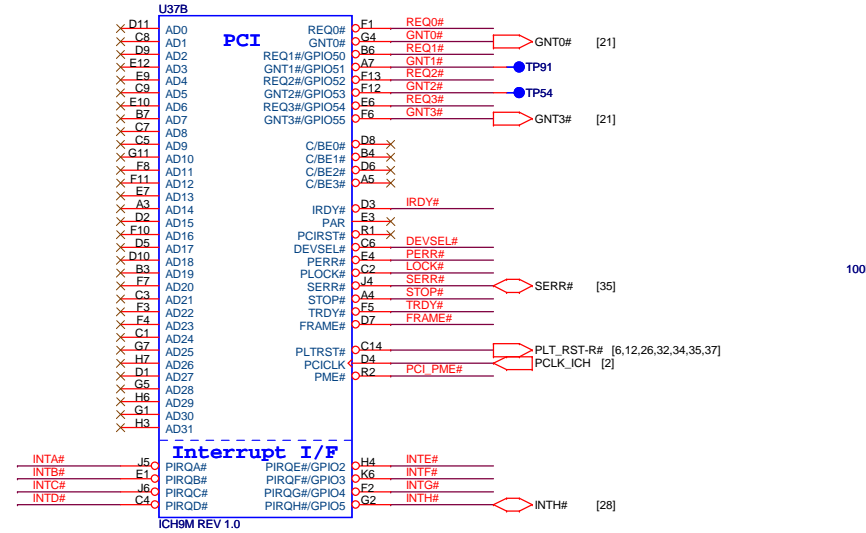
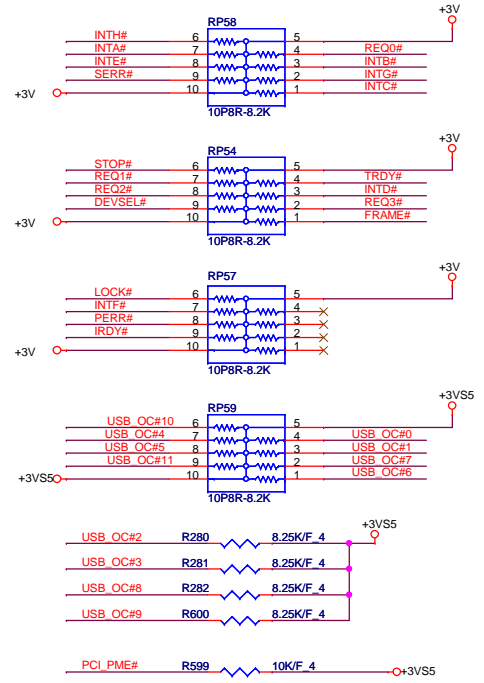


SI modified

Del GM HDCP circuit

Del U16, R297, R285, R275, R291, R286, C476C478, R294

512K byte SPI ROM
For HDCP only
For GM HDCP

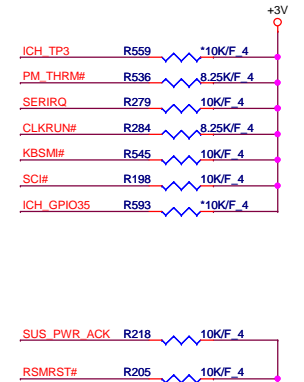
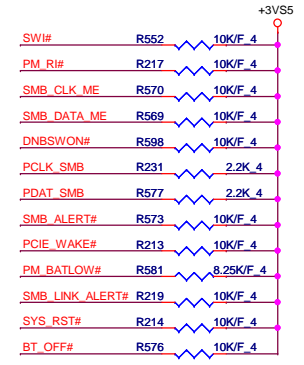
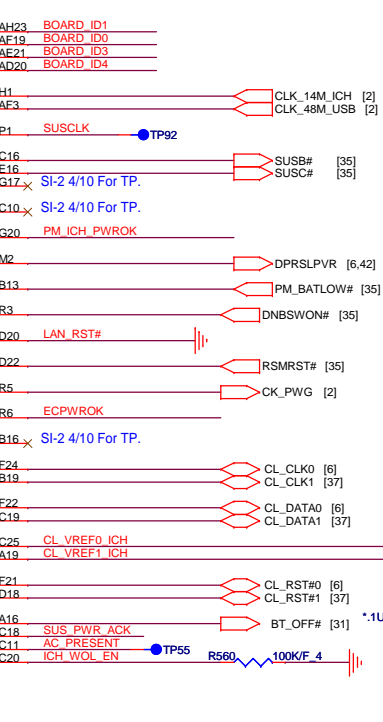
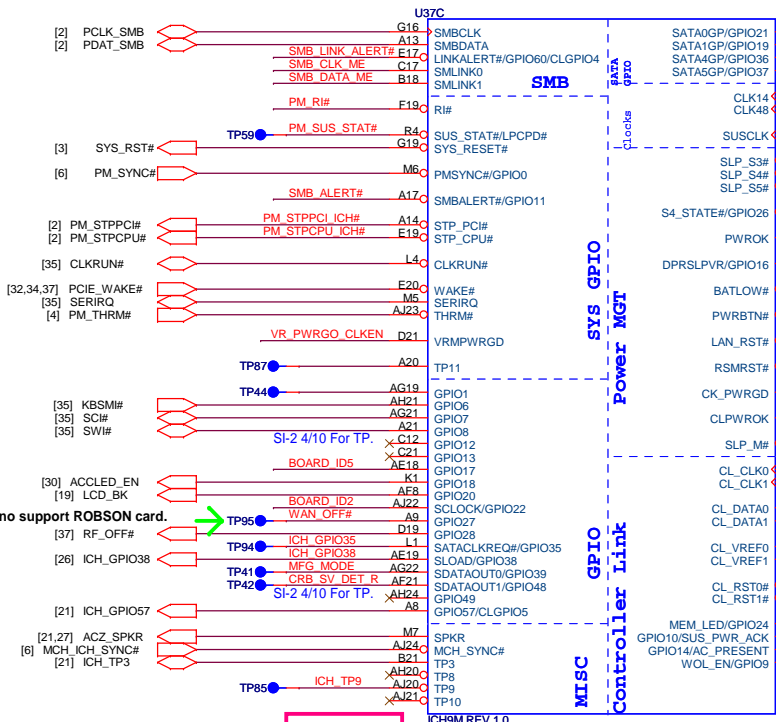


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NB5

Size Custom	Document Number ICH9-M PCIE 2/4	Rev E3A
Date: Wednesday, August 06, 2008		Sheet 22 of 46

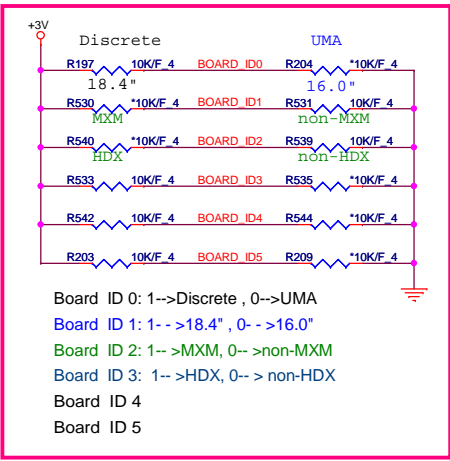
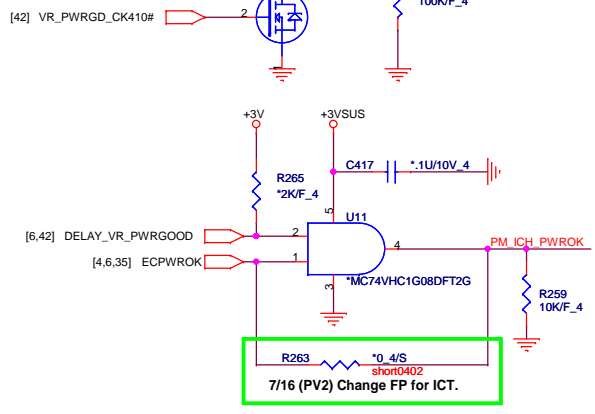
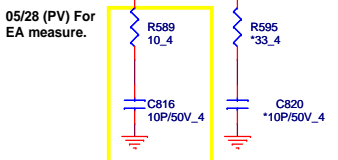
[2,4,6,9,10,11,12,14,15,19,20,21,22,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V
 [21,22,24,34,45] +3VS5
 [31,37,41,42,43,45] +3VSUS



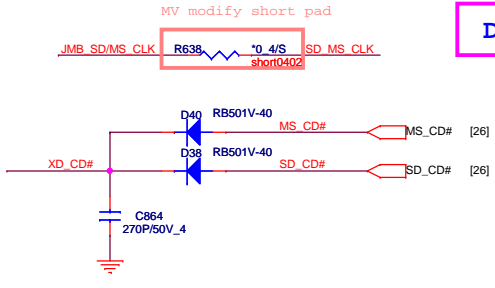
07/09 (PV2) Add TP95 for no support ROBSON card.

SI modified per T18, TP84, TP86

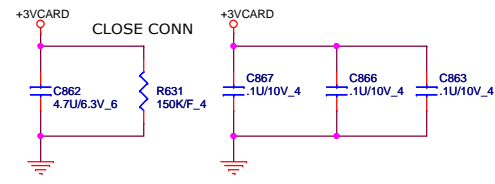
SI-2 Build
 Delete R574, G2 as Bios_Rec can be cover by Bios



Delete JMB 385

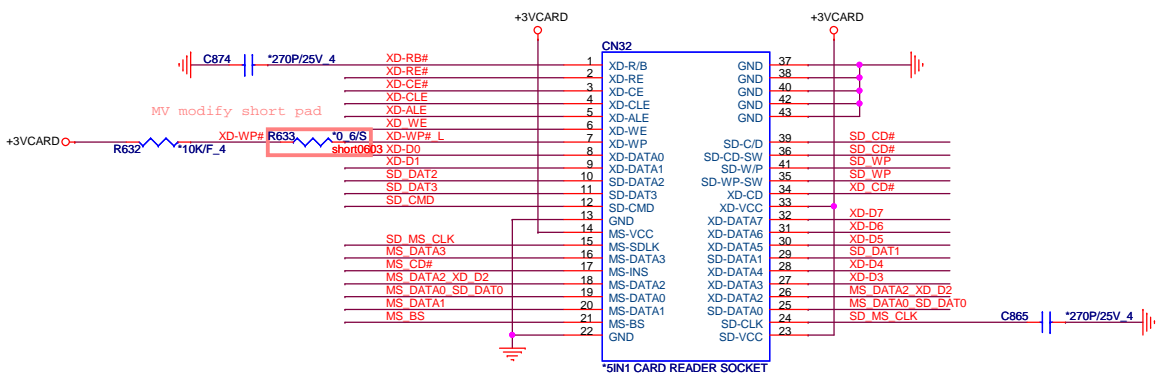


Close to CN34



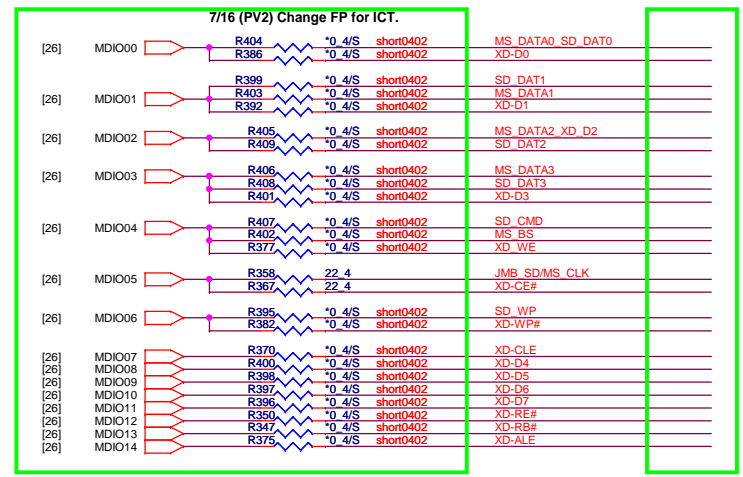
	SD/MMC	MS	XD
MDID0	SD DAT0	MS D0	XD D0
MDID1	SD DAT1	MS D1	XD D1
MDID2	SD DAT2	MS D2	XD D2
MDID3	SD DAT3	MS D3	XD D3
MDID4	SD CMD	MS BS	XD WE#
MDID5	SD CLK	MS SCLK	XD CE#
MDID6	SD WP		XD WP#
MDID7			XD CLE
MDID8	SD DAT4		XD D4
MDID9	SD DAT5		XD D5
MDID10	SD DAT6		XD D6
MDID11	SD DAT7		XD D7
MDID12			XD RE#
MDID13			XD R#B#
MDID14			XD ALE
CR1 LEDN	SD1 LED#	MS1 LED#	XD LED#
CR1 PCTLN	SD1 PCTL#	MS1 PCTL#	XD1 PCTL#
CR1 CD0	SD1 CD#		XD CV#
CR1 CD1		MS1 CD#	XD CD#

**5 IN1 CARD READER
XD, MMC/SD, MS/MSP**

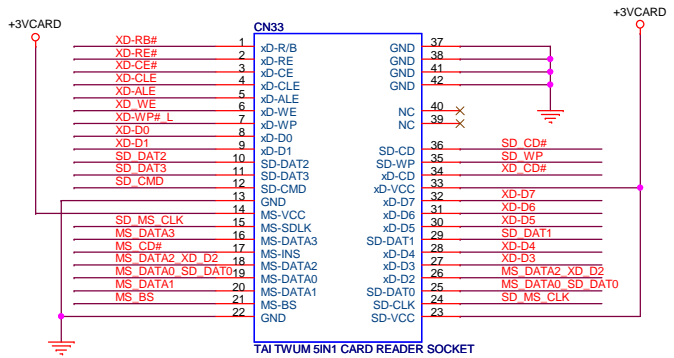


SI modified Footprint: "4in1-72700327123-43p-1"

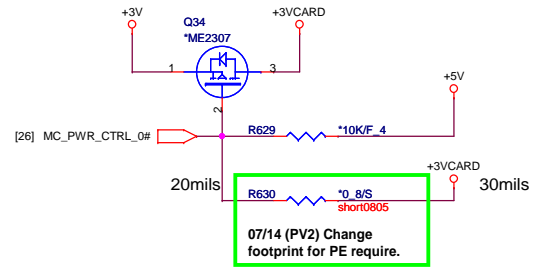
7/16 (PV2) Delete net for ICT.



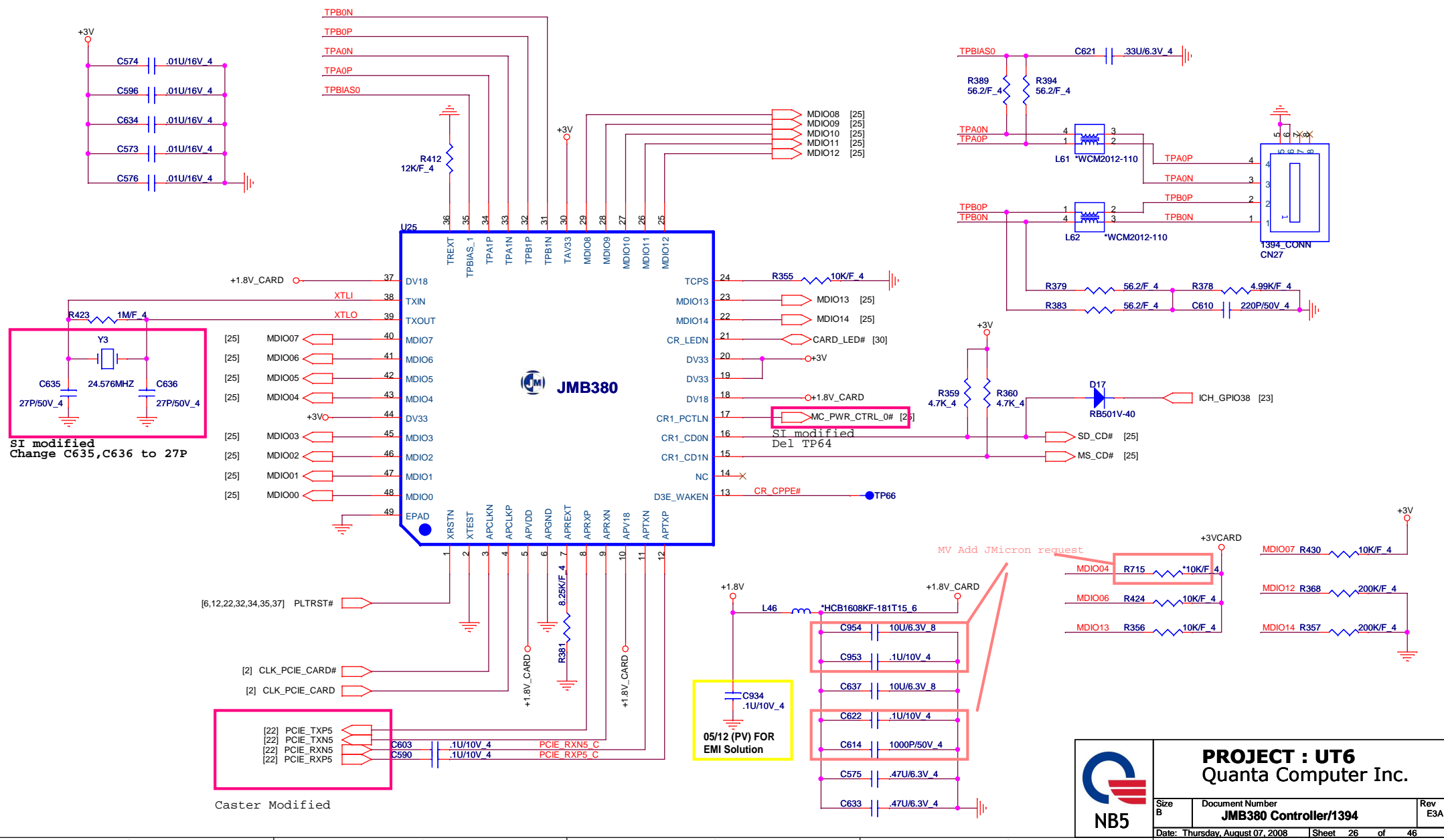
2ND SOURCE



SI modified Footprint: "7IN1-R015-B11-LM-42P-L"

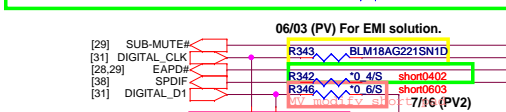


PROJECT : UT6
Quanta Computer Inc.



PROJECT : UT6 Quanta Computer Inc.		
Size B	Document Number JMB380 Controller/1394	Rev E3A
Date: Thursday, August 07, 2008 Sheet 26 of 46		

05/23 (PV) For IDT Dolby functionality.
07/14 (PV2) R697 change footprint for PE require.



06/03 (PV) For EMI solution.



07/16 (PV2) Change FP for ICT.



07/14 (PV2) Change footprint for PE require.



Close to Pin1



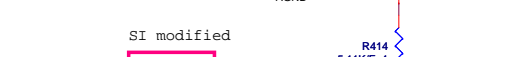
Close to Pin9



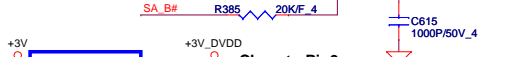
Close to Pin9



Close to Pin9



Close to Pin9



Close to Pin9



Close to Pin9



Close to Pin9



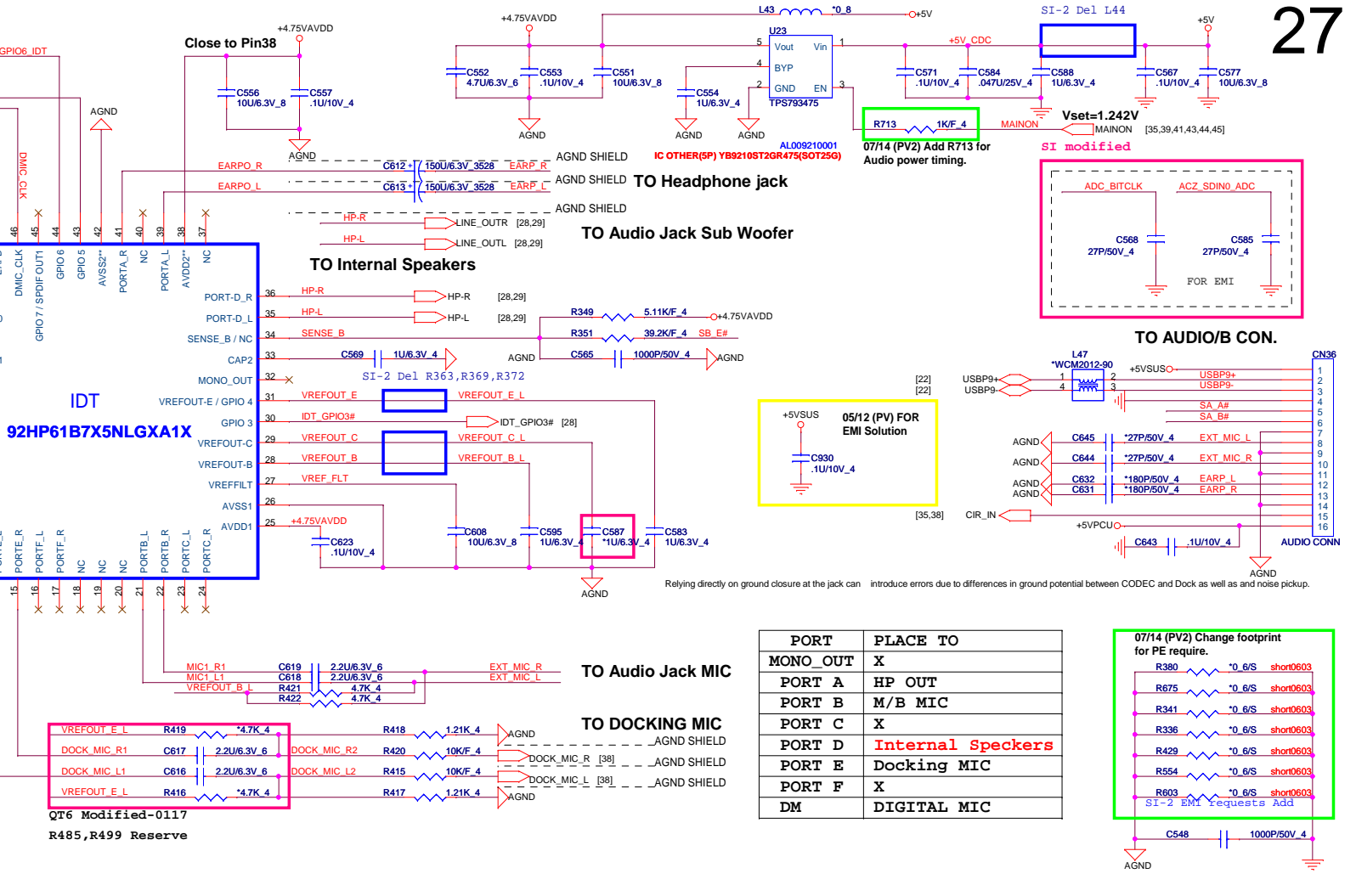
Close to Pin9



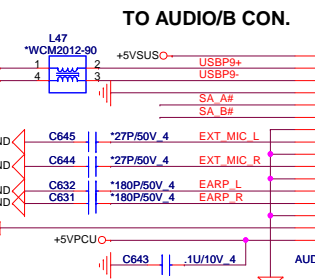
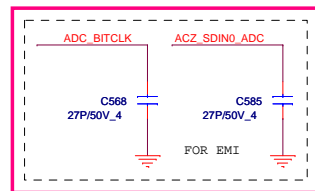
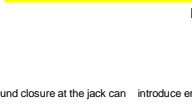
Close to Pin9



Close to Pin9

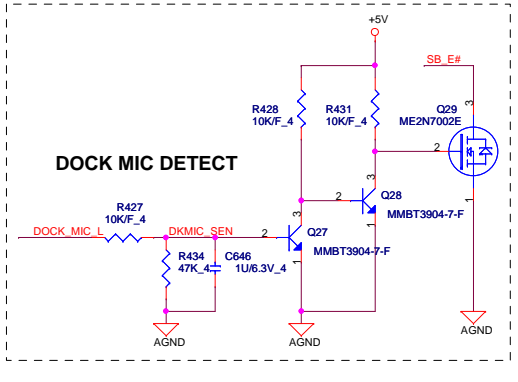
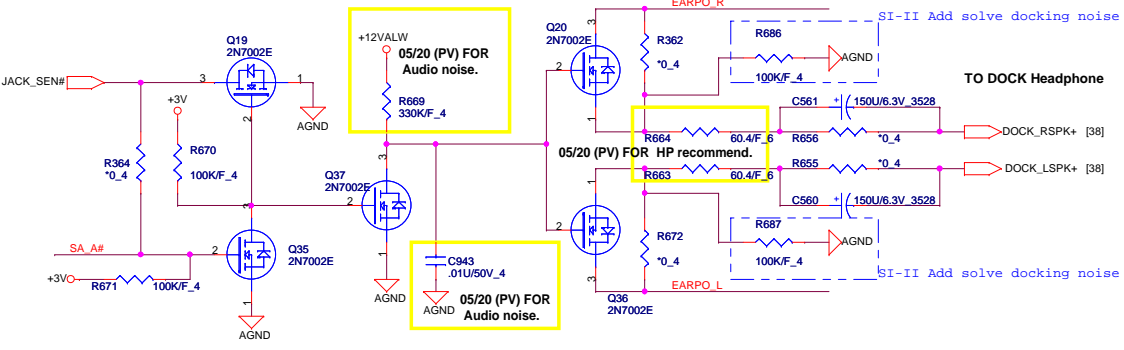
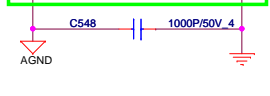


05/12 (PV) FOR EMI Solution



PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	X
DM	DIGITAL MIC

07/14 (PV2) Change footprint for PE require.

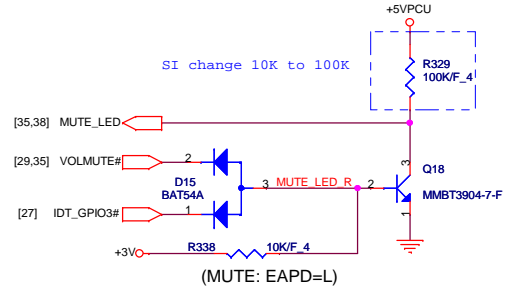
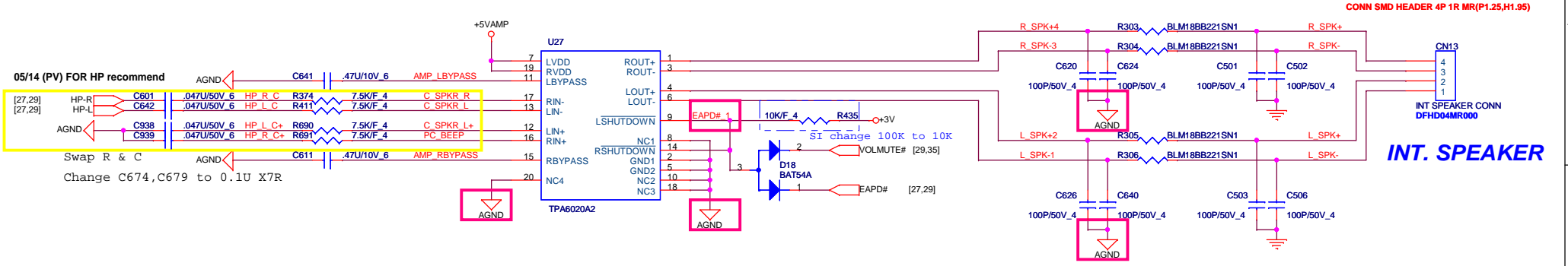
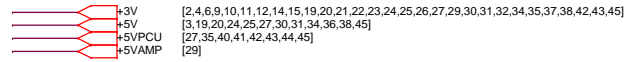


SA_A# -->EXT HP
 SA_B# -->EXT MIC
 SB_E#--> DOCK MIC
 Audio JACK: Normal Open

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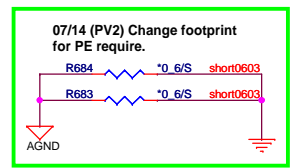
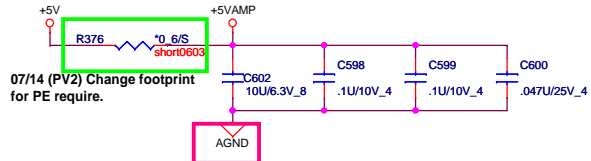
Size Custom	Document Number	Rev E3A
Azalia IDT92HD71B7		
Date: Wednesday, August 06, 2008	Sheet 27	of 46

AUDIO AMPLIFIER



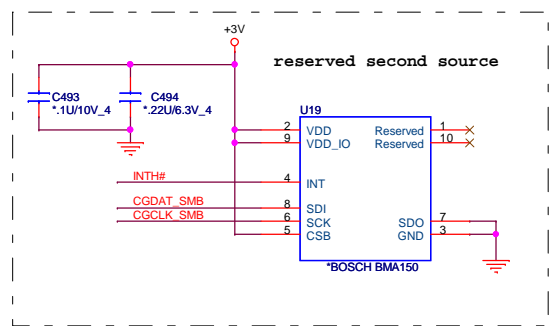
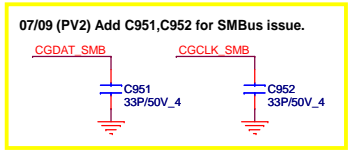
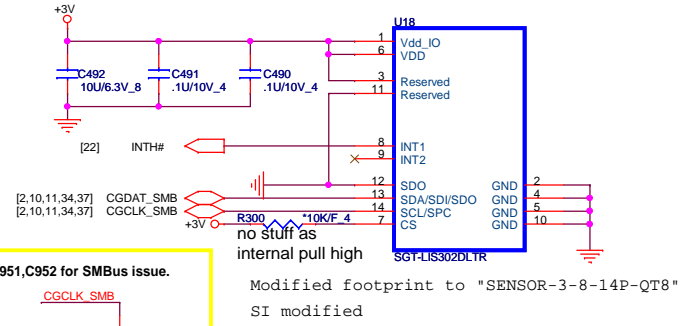
07/09 (PV2) Delete for 2ND FAN function.

Delete Gain set



Del R373, R677, R676
 Del AMP_GND to AGND

Accelerometer Sensor

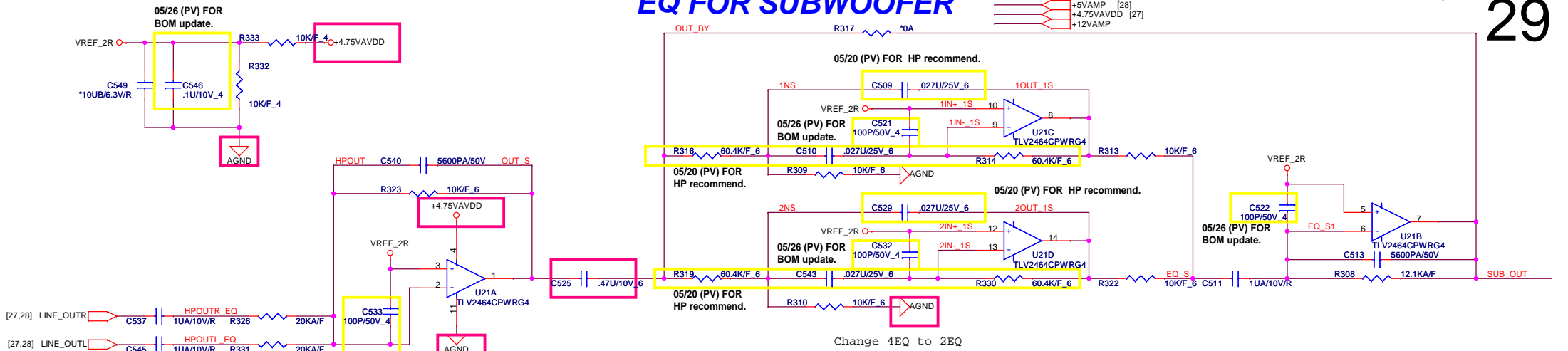


PROJECT : UT6
 Quanta Computer Inc.

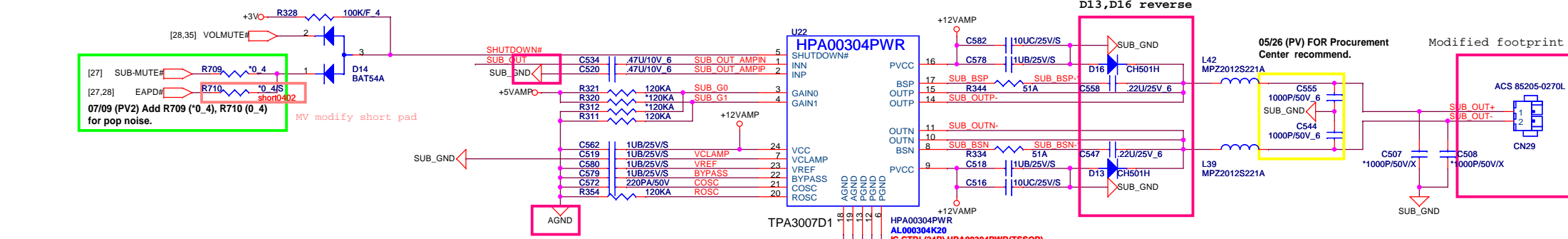
Size Custom	Document Number AMP_TPA6017/Accelerometer	Rev E3A
Date: Wednesday, August 06, 2008		Sheet 28 of 46

EQ FOR SUBWOOFER

+3V [2,4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,30,31,32,34,35,37,38,42,43,45]
 +5VAMP [28]
 +4.75VAVDD [27]
 +12VAMP

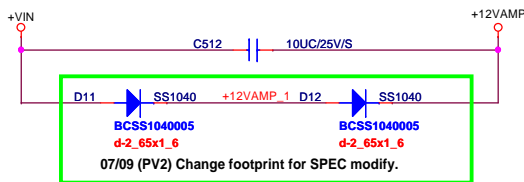


MODEL	UT6	UT7
R316	60.4K/F_6	40.2K/F_6
R319	60.4K/F_6	40.2K/F_6
R330	60.4K/F_6	80.6K/F_6
R314	60.4K/F_6	80.6K/F_6
C509	0.027U/25V_6	0.022U/50V_6
C510	0.027U/25V_6	0.022U/50V_6
C529	0.027U/25V_6	0.039U/16V_6
C543	0.027U/25V_6	0.039U/16V_6



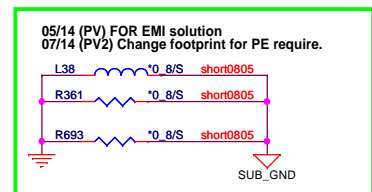
C534	.47U/10V_6	SUB_OUT AMPIN
C520	.47U/10V_6	SUB_OUT AMPHP
R321	120KA	SUB_G0
R320	*120KA	SUB_G1
R312	*120KA	
R311	120KA	
C562	1U/25V/S	VCLAMP
C519	1U/25V/S	VREF
C580	1U/25V/S	BYPASS
C579	1U/25V/S	COSC
C572	220PA/50V	ROSC
R354	120KA	

Sub-Woofer power



Del HP_GND to GND
 Del R307,R315

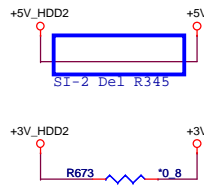
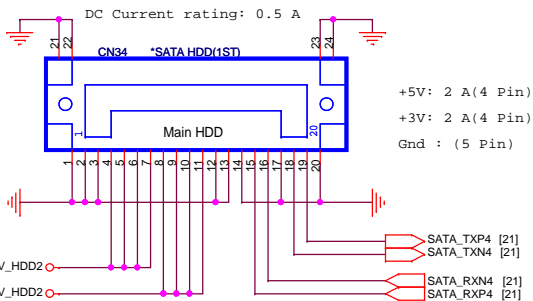
Delete L1003



PROJECT : UT6
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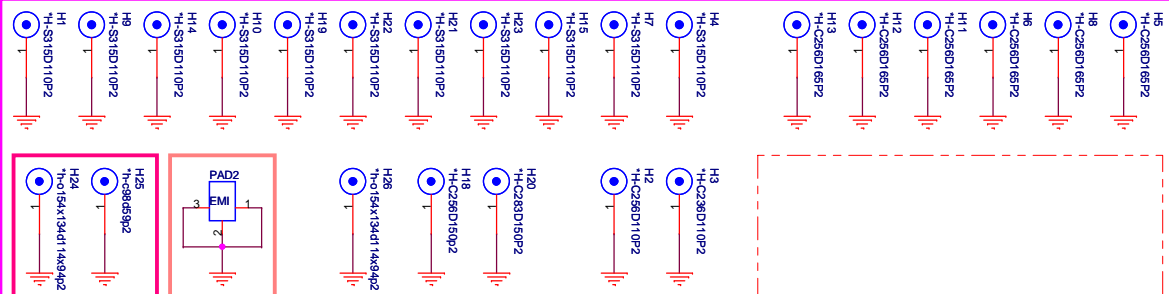
Size Custom	Document Number SUBWOOFER(EQ & AMP.)	Rev E3A
Date: Wednesday, August 06, 2008 Sheet 29 of 46		

SATA_2 CONNECTOR



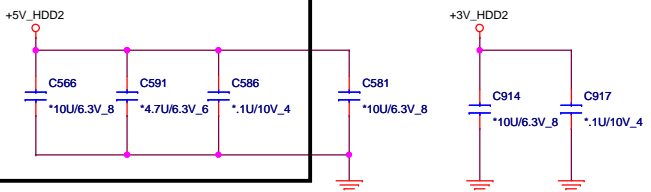
- +3VPCU_LED [36]
- +3V_LED [35]
- +5V [3, 19, 20, 24, 25, 27, 28, 31, 34, 36, 38, 45]
- +3V [2, 4, 6, 9, 10, 11, 12, 14, 15, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 31, 32, 34, 35, 37, 38, 42, 43, 45]
- +12VALW [19, 27, 36, 40, 45]

M/B Screw Hole



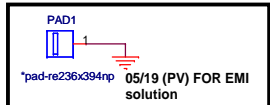
30

FOR UT7 2ND HDD ONLY.



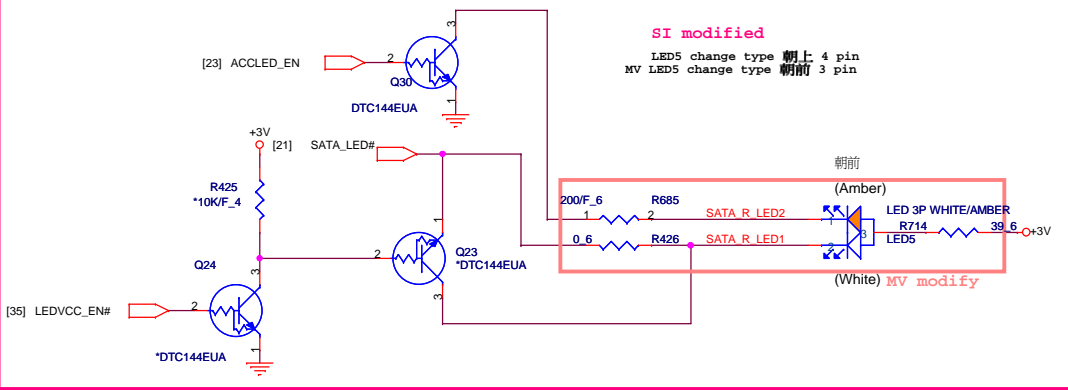
delete all PAD & change screw footprint

07/14 (PV2) Delete H16,H17 for no support ROBSON card.

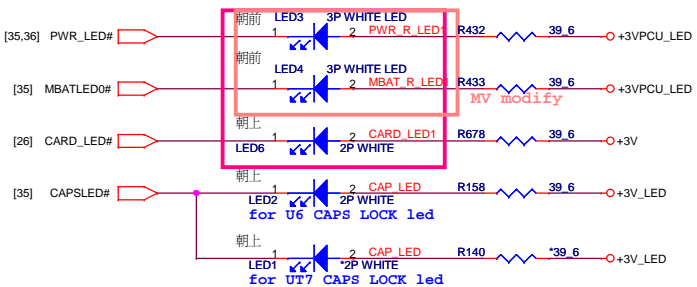


05/19 (PV) FOR M/E recommend for UT7 BAT NUT

SI modified
LED5 change type 朝上 4 pin
MV LED5 change type 朝前 3 pin

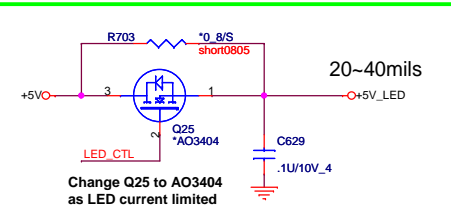
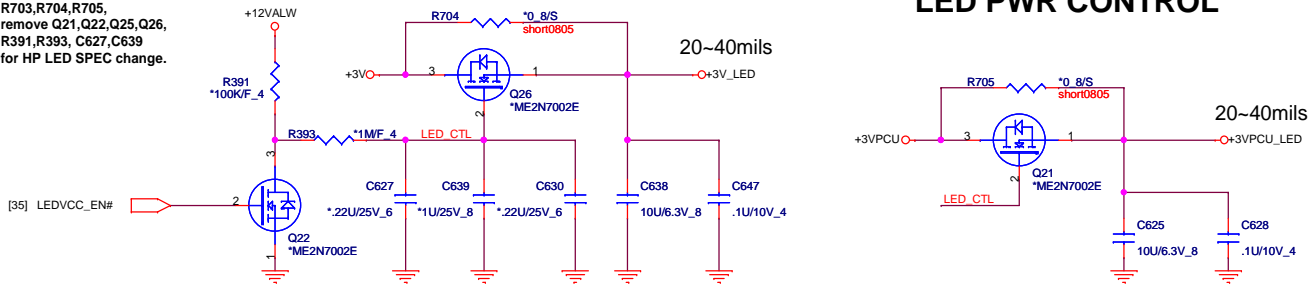


SI modified LED3,4,6 change type 朝上 2 pin



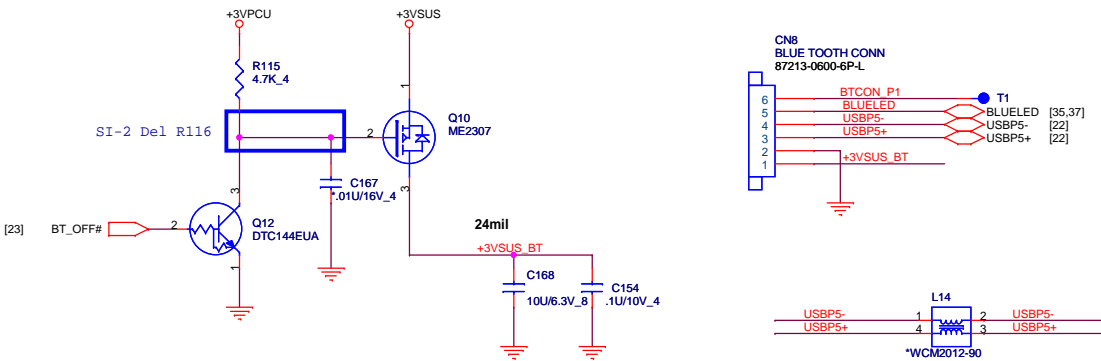
07/09 (PV2) Add R703,R704,R705, remove Q21,Q22,Q25,Q26, R391,R393, C627,C639 for HP LED SPEC change.

LED PWR CONTROL

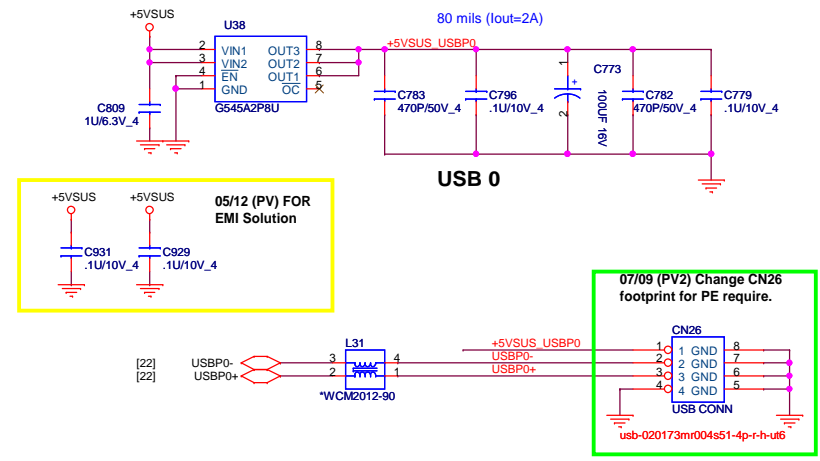


PROJECT : UT6
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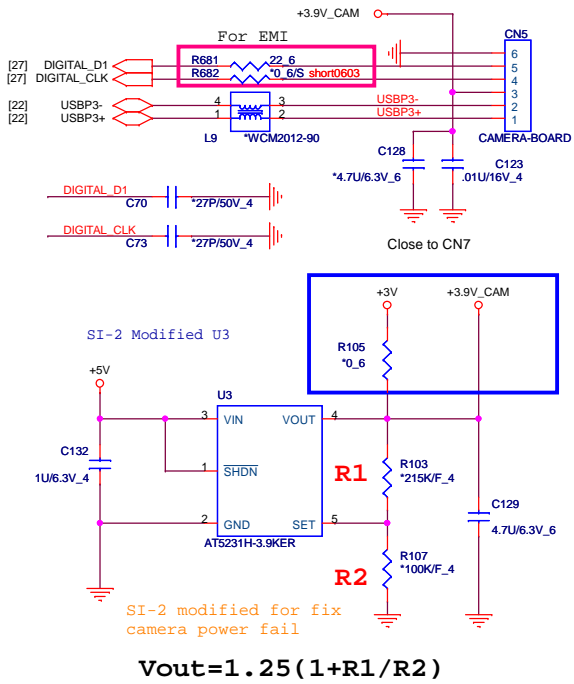
BLUETOOTH



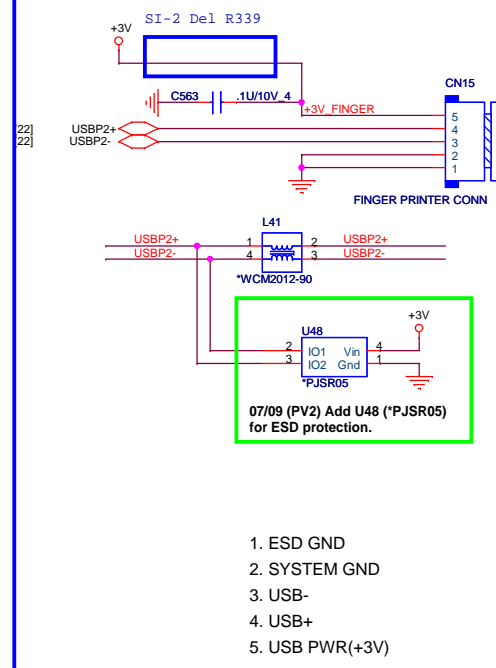
USBX1 and E-SATA



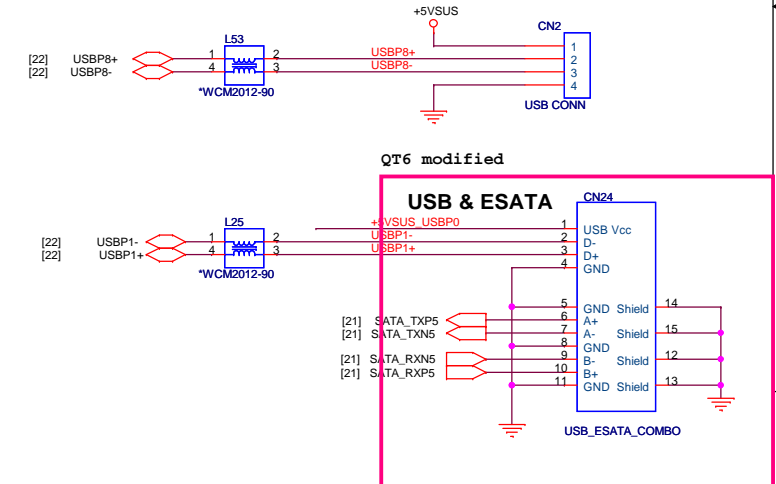
USB CAMERA /DIGITAL MIC CONNECT



USB fingerprint CON



1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)



PROJECT : UT6
Quanta Computer Inc.

Size Custom	Document Number BT/WC/FT/TS/ESATA/USB	Rev E3A
Date: Wednesday, August 06, 2008 Sheet 31 of 46		

T : Stuffed for RTL8111C(10/100/1000)

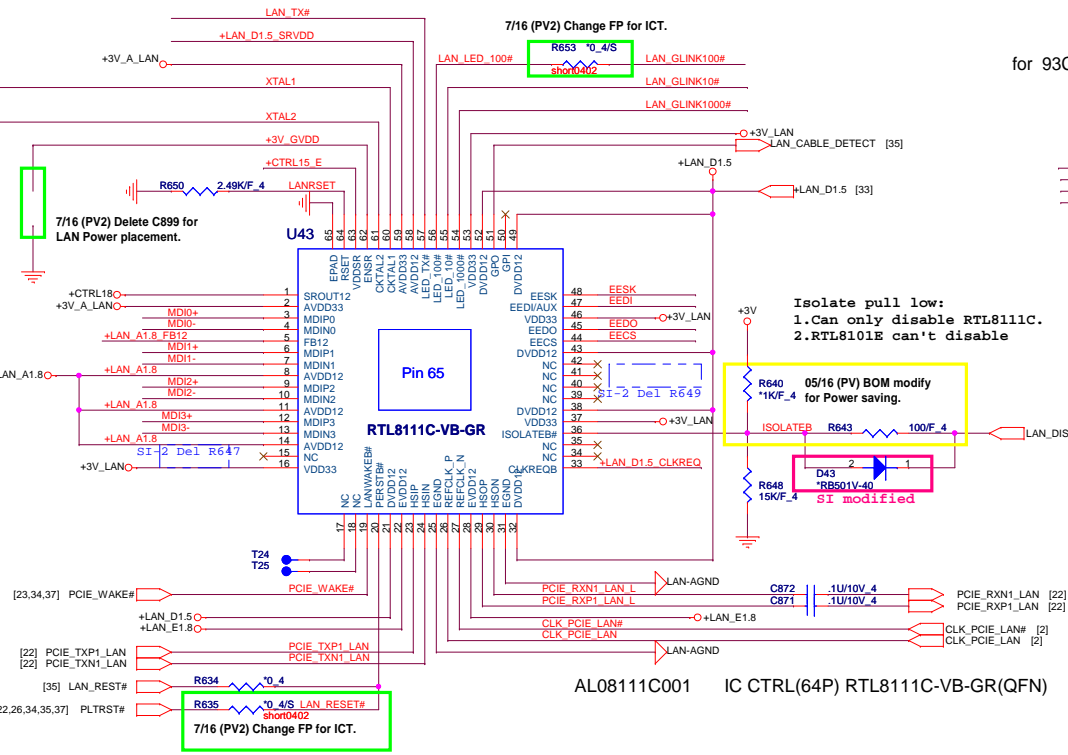
[2,4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,34,35,37,38,42,43,45]

+LAN_D1.5 +LAN_D1.5_SRVDV 05/23 (PV) Del for PE require. +LAN_D1.5_CLKREQ Stuffed for 8102E/RTL8111C

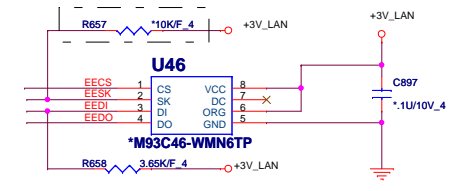
+3VLANVCC +3V_GVDD +3VLANVCC +CTRL15_E 05/23 (PV) Del for PE require. Power trace Layout 宽度 > 40mil Stuffed for RTL8111C(10/100/1000)

SI modified change C913,C912 to 33P

U18#63 wider than 40 mils U18#1 wider than 60 mils

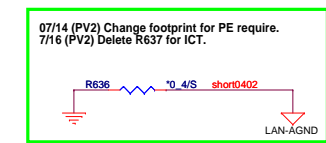
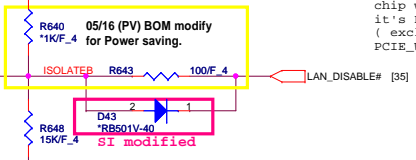


for 93C56 used. NC if 93C46 is used.



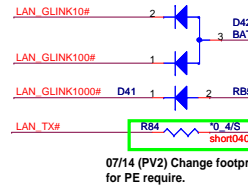
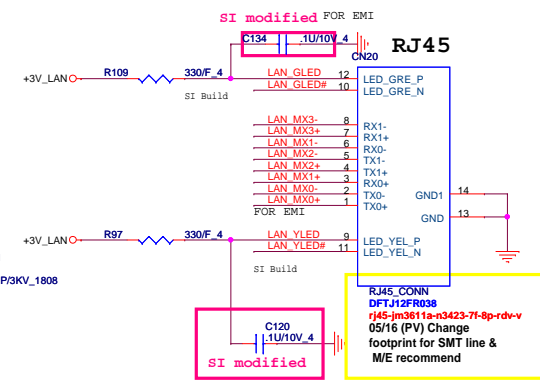
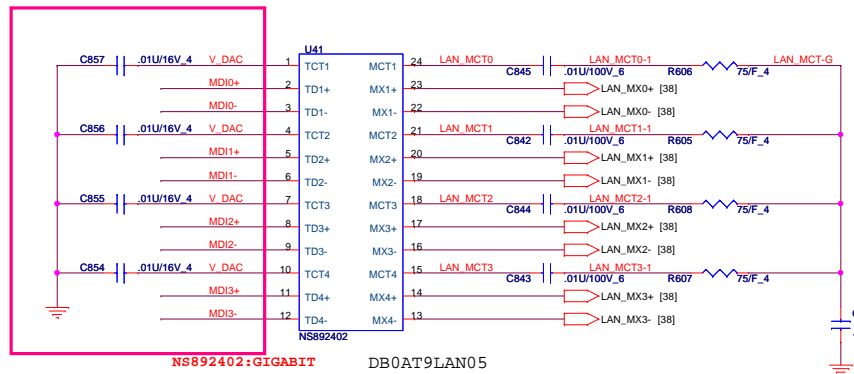
Isolate pull low: 1.Can only disable RTL8111C. 2.RTL8101E can't disable

if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

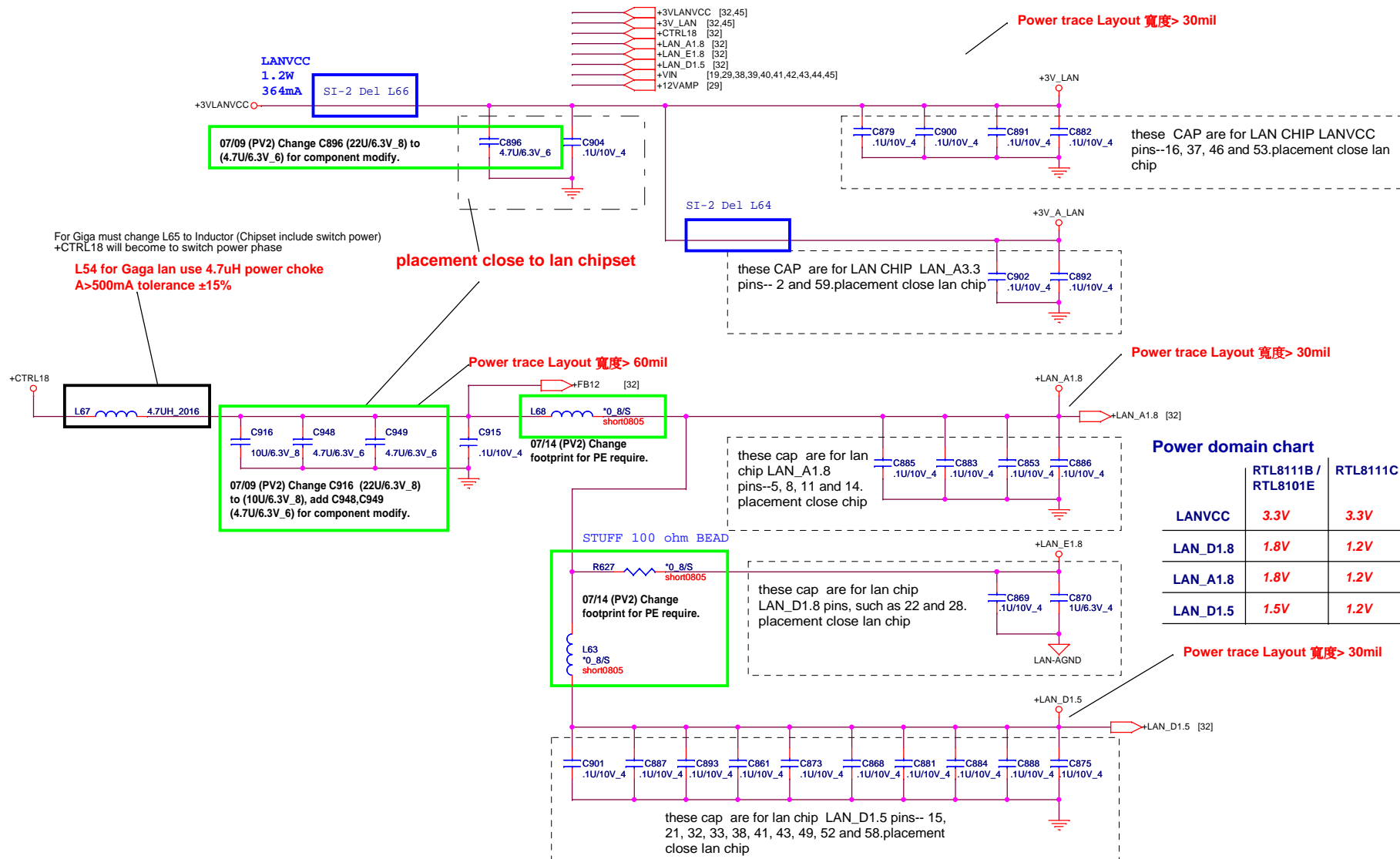


AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)

Caster Modified



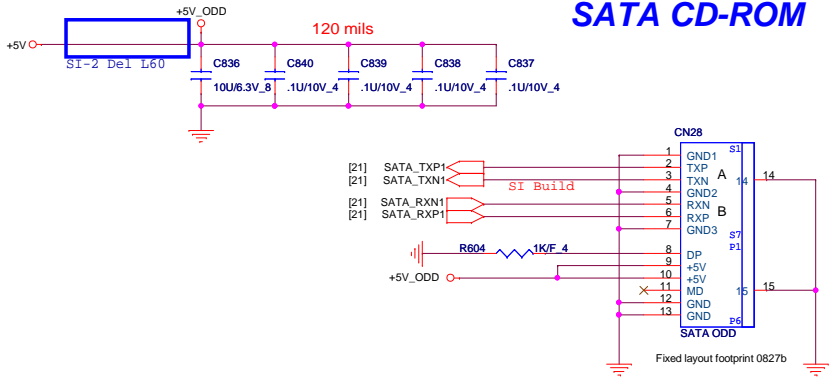
PROJECT : UT6 Quanta Computer Inc. NB5 Size Custom Document Number RTL8111C & RJ45 Rev E3A Date: Wednesday, August 06, 2008 1 Sheet 32 of 46



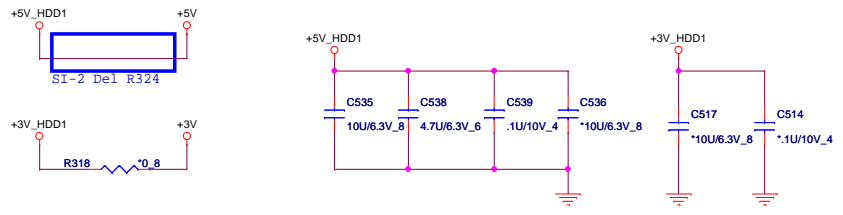
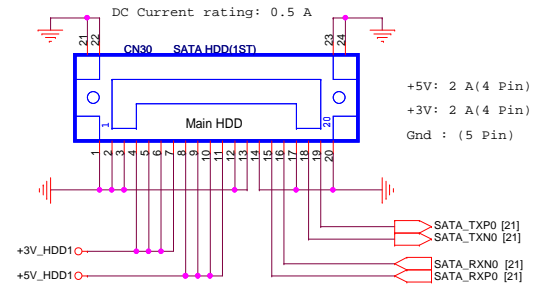
Power domain chart

	RTL8111B / RTL8101E	RTL8111C
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V

SATA CD-ROM

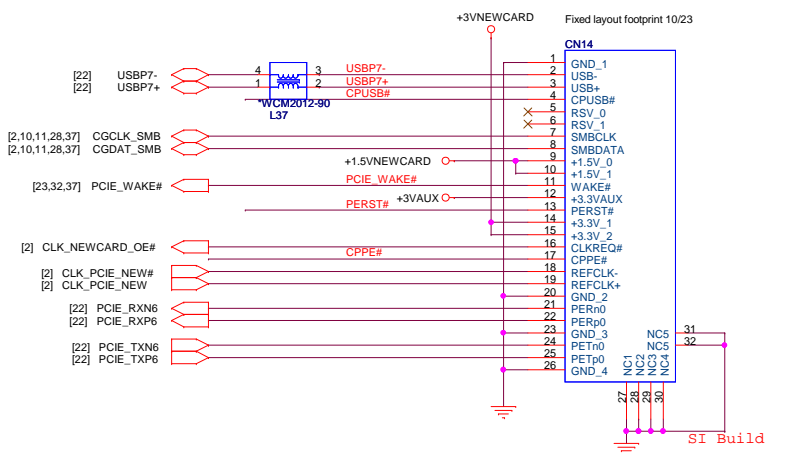


SATA_1 CONNECTOR

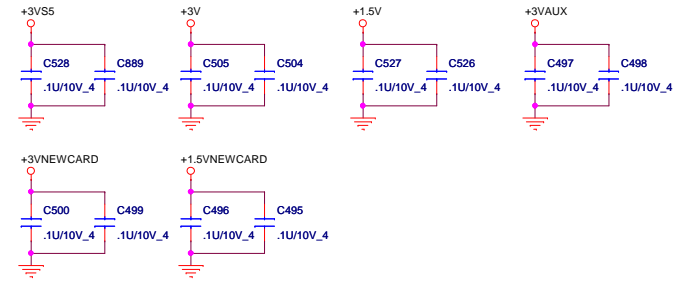
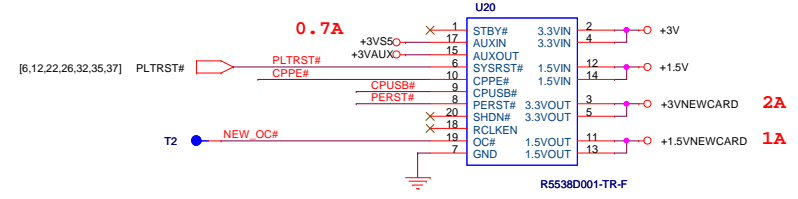


NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)



EXPCARD-48303-0042-26P-L-QT6
DFHD26MS017
CONN SMD HEADER 26P 1R MS(P1.0,H6.45)



	<p>PROJECT : UT6 Quanta Computer Inc.</p>	
	<p>Size Custom</p>	<p>Document Number ODD/HDD/NEW CARD</p>
<p>Date: Wednesday, August 06, 2008 Sheet 34 of 46</p>		

[2,4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,37,38,42,43,45]
+3V [19,21,30,31,36,38,39,40,45]
+3VPCU [19,27,31,38,45]
+5VSUS [27,28,40,41,42,43,44,45]

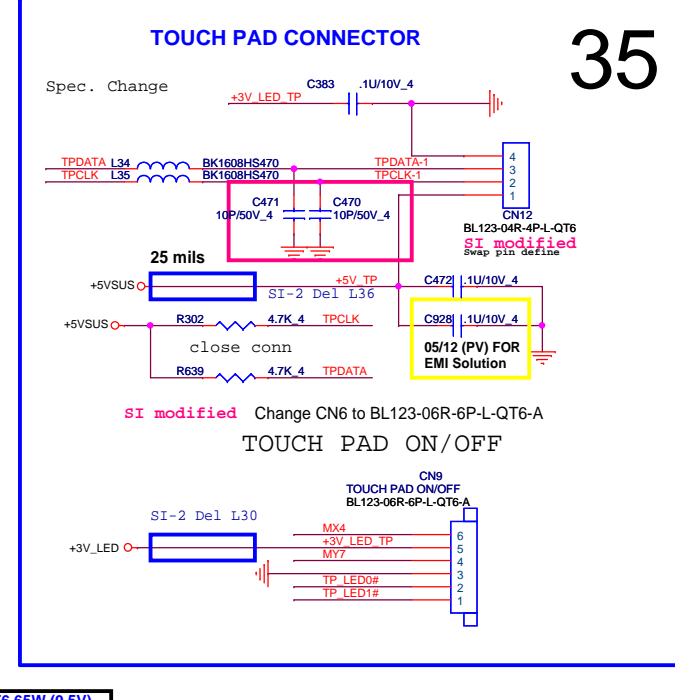
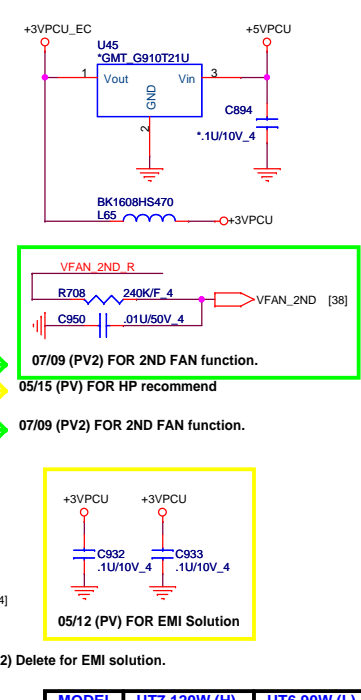
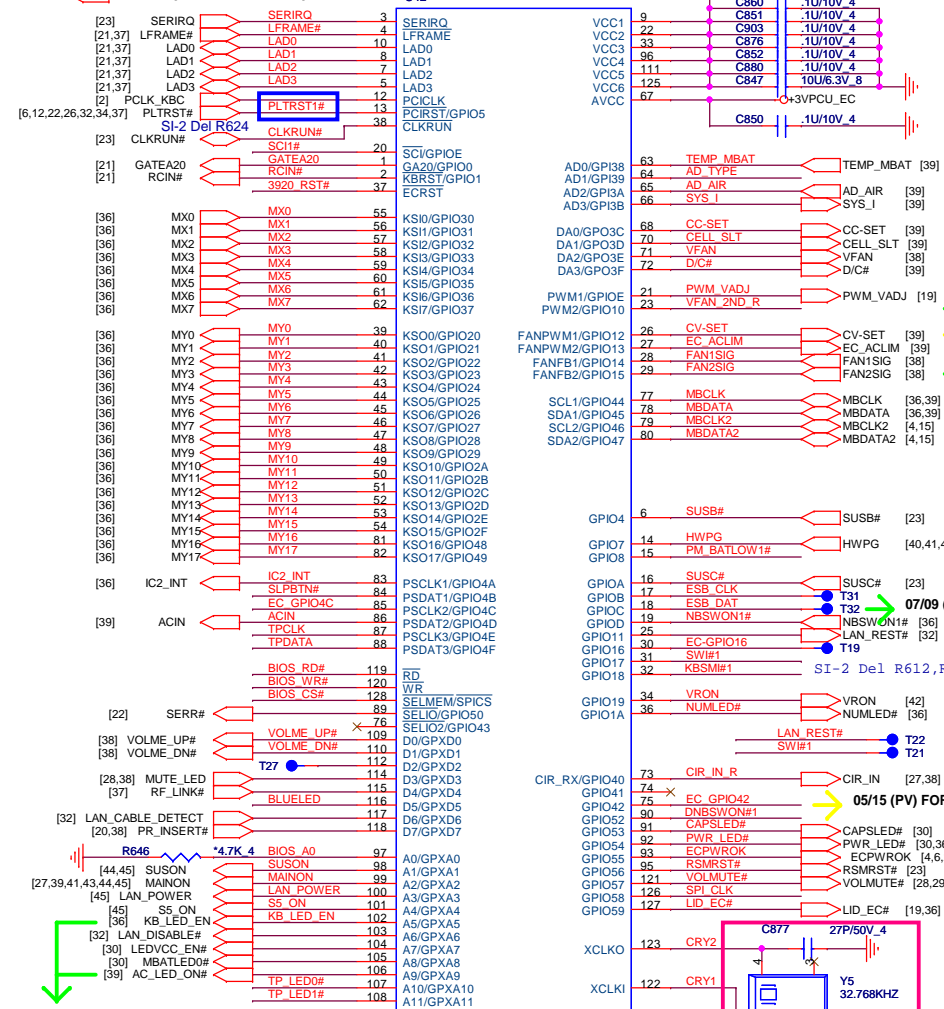
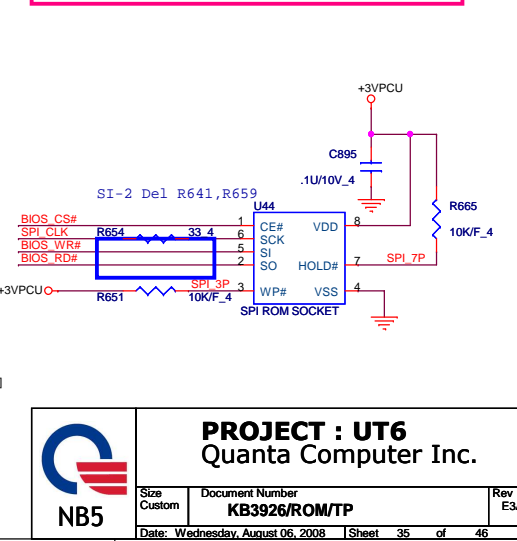
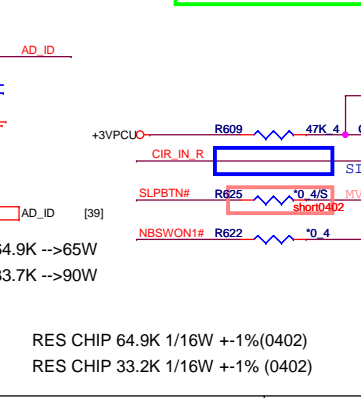
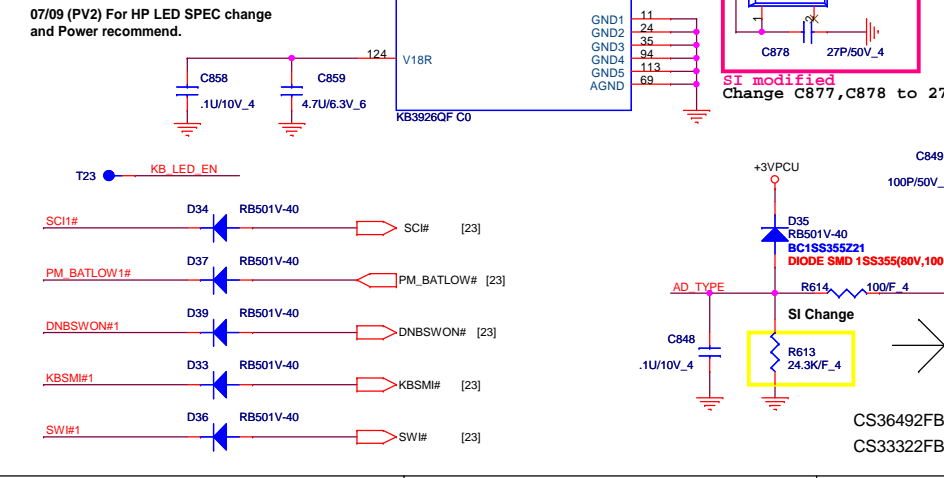
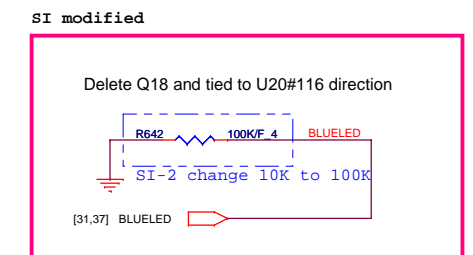
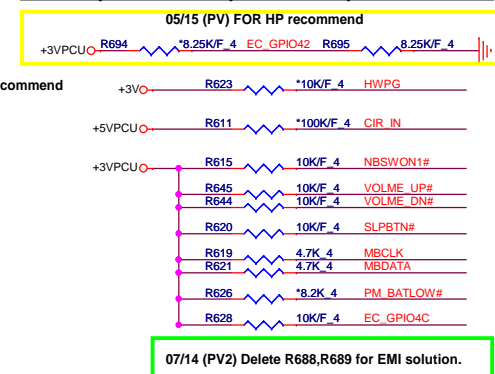


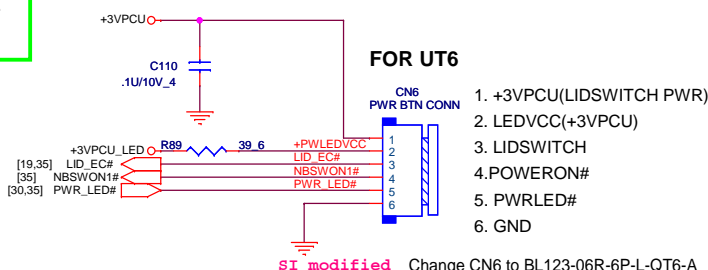
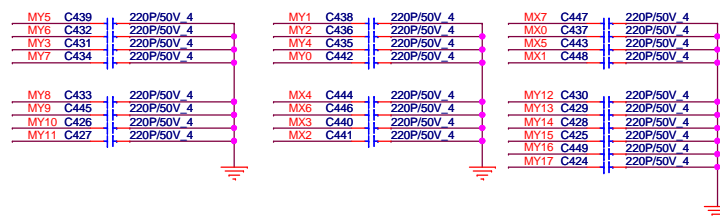
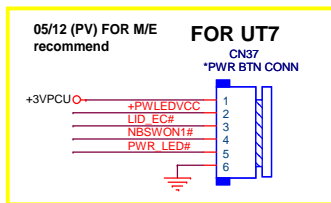
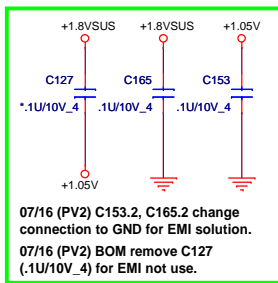
Table with 4 columns: MODEL, UT7 120W (H), UT6 90W (L), UT6 65W (0.5V). Rows include R694 and R695 with component values.



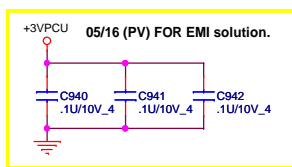
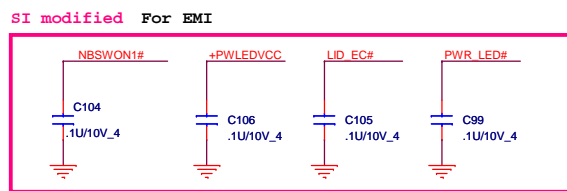
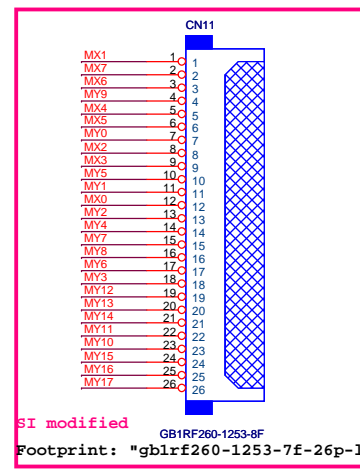
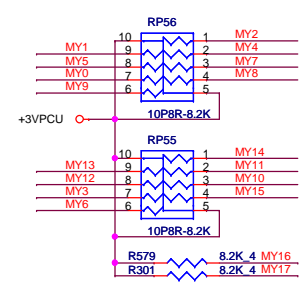
Socket: DG008000031
MXIC: AKE5GFK0Z09
AIT: AKE3GZP0801



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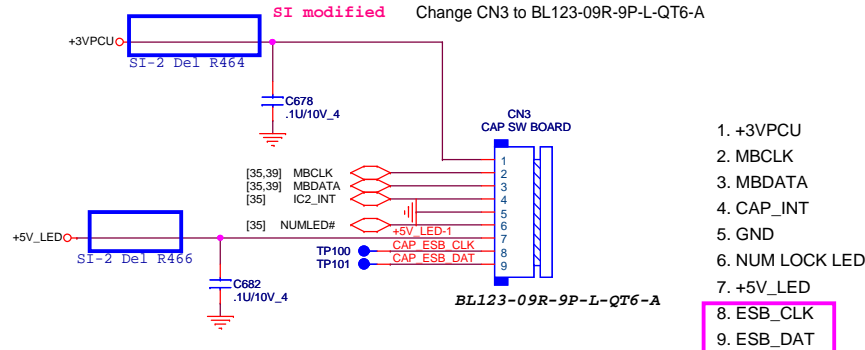


KEYBOARD PULL-UP

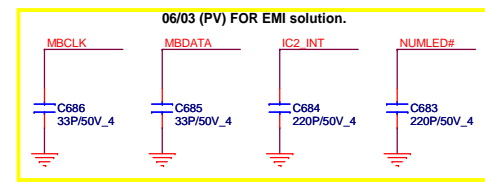
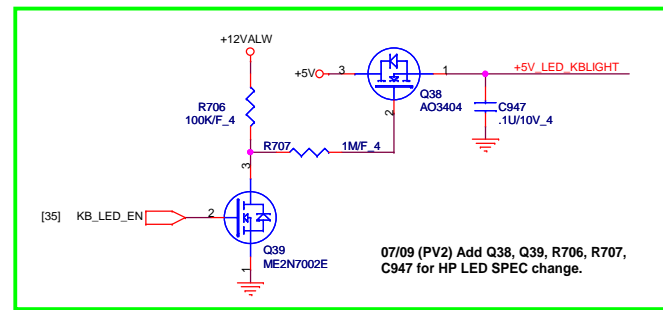
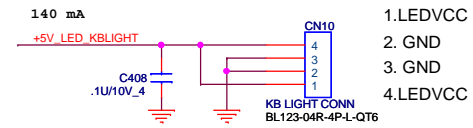


POWER BOTTON CONNECT

CAP SW CONNECT

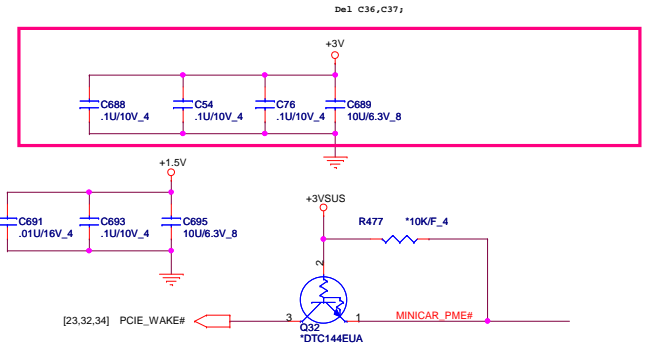
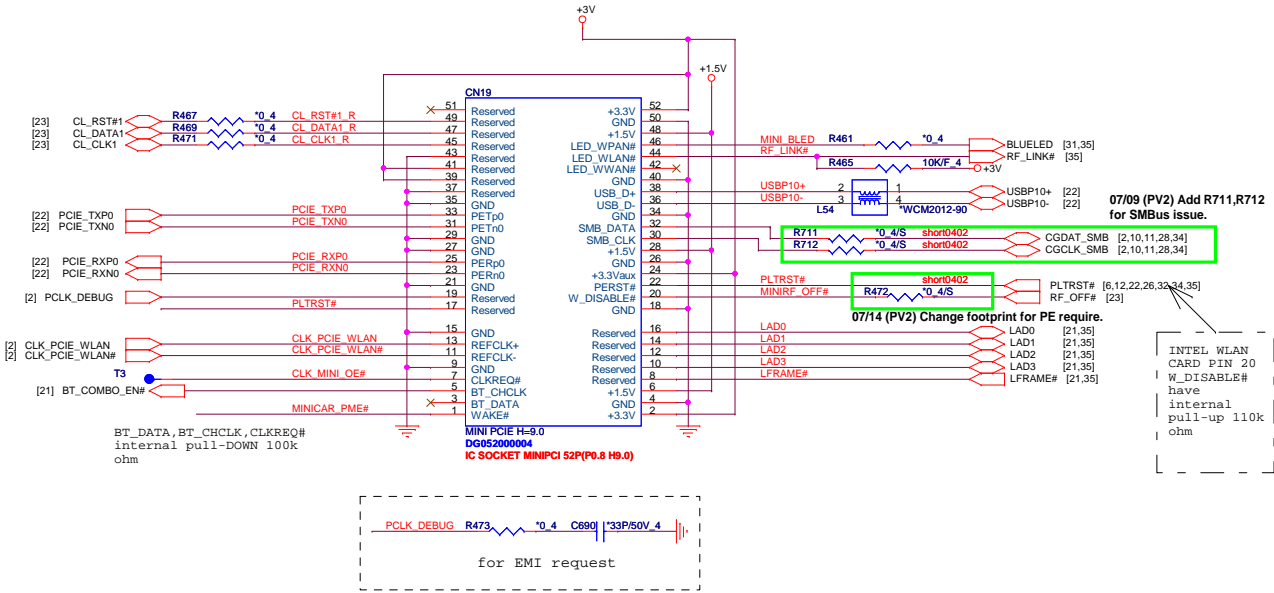


07/14 (PV2) Delete L69,L70,C922,C923 for EMI solution.



Mini PCI-E Card 1 WLAN

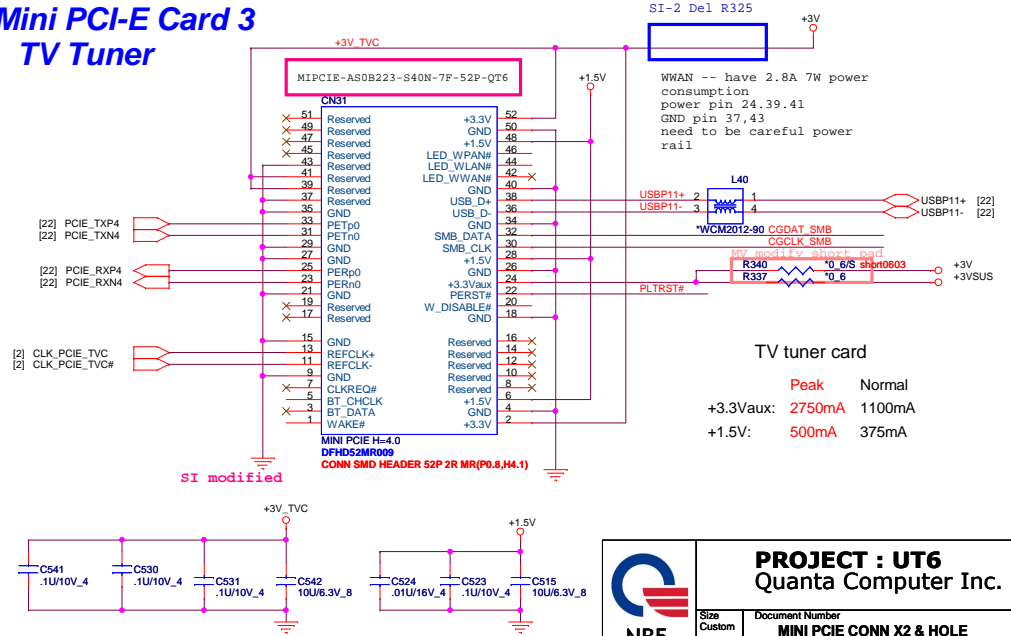
Delete R110,R78
+3V must have a 120mil plane
Each pin 25mil



Mini PCI-E Card 2 ROBSON

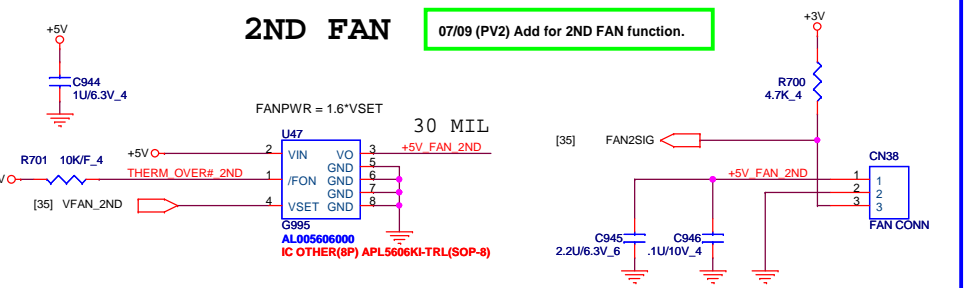
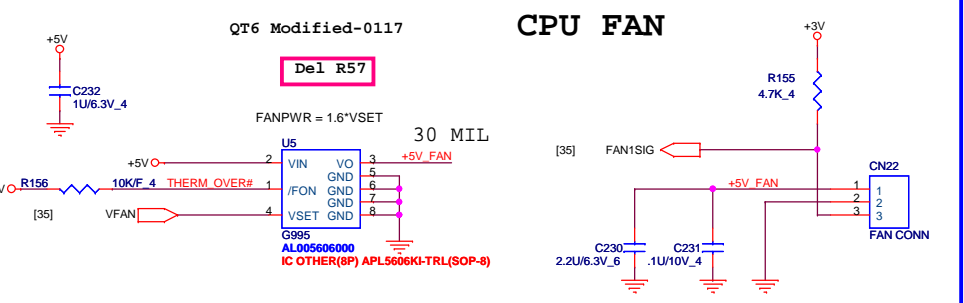
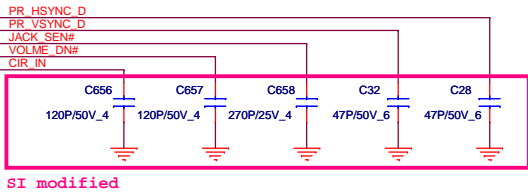
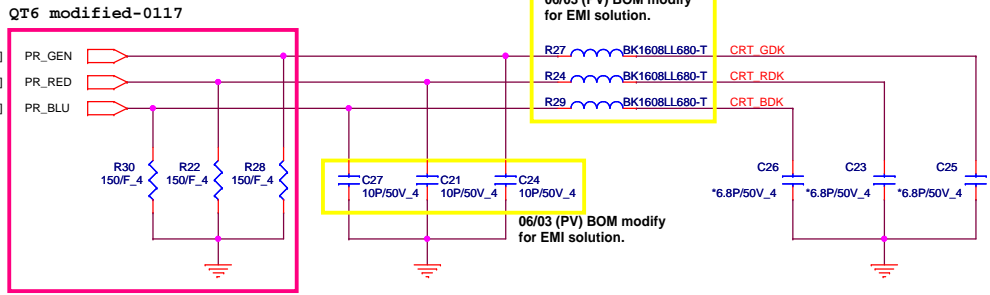
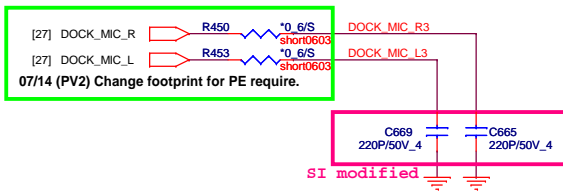
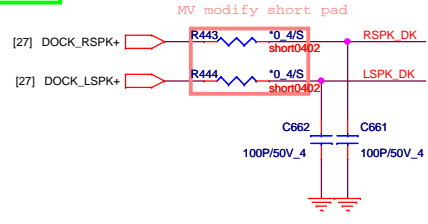
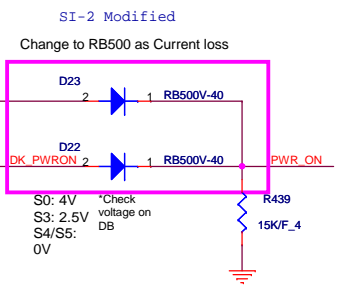
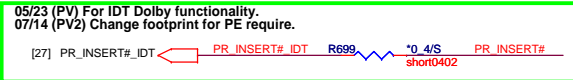
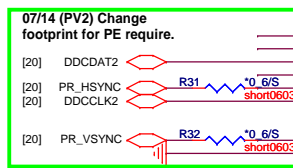
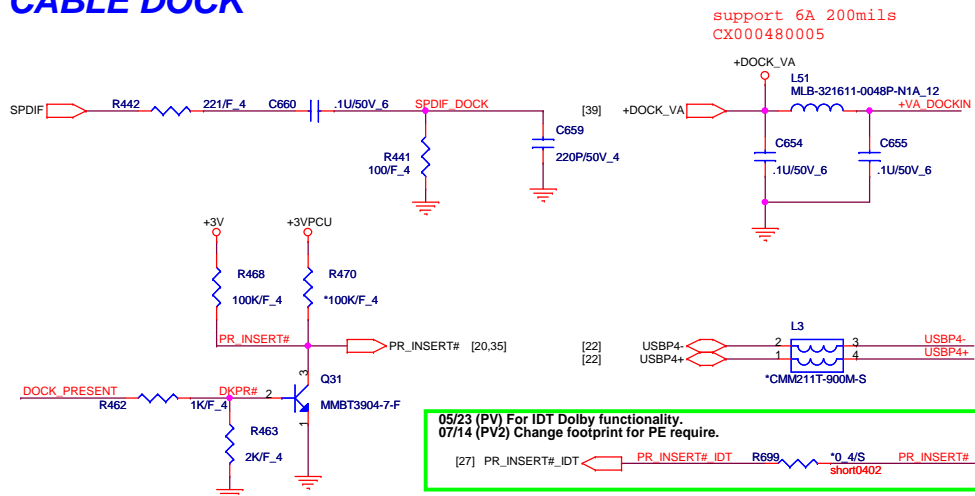
07/09 (PV2) Delete for no support ROBSON card.

Mini PCI-E Card 3 TV Tuner



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Size Custom	Document Number MINI PCIE CONN X2 & HOLE	Rev E3A
Date: Wednesday, August 06, 2008	Sheet 37 of 46	



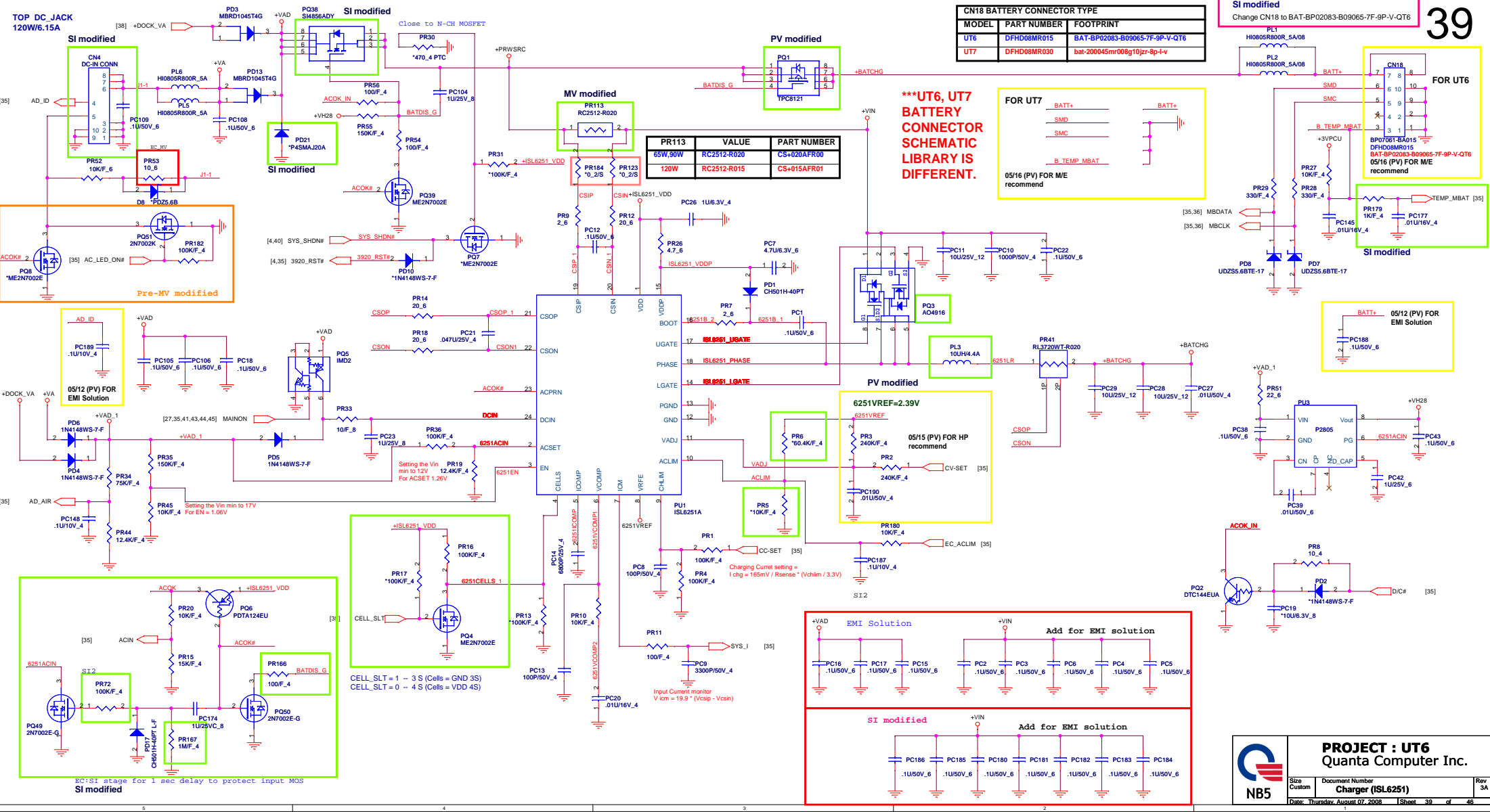
PROJECT : UT6
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Size Custom	Document Number CABLE DOCKING/FAN	Rev E3A
Date: Wednesday, August 06, 2008	Sheet 38	of 46

TOP DC JACK
120W/6.15A

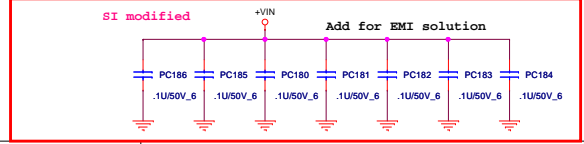
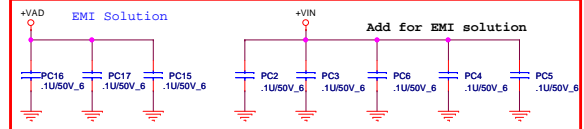
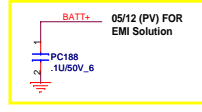
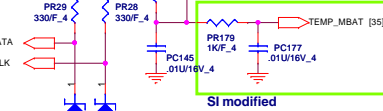
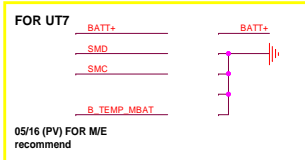
CN18 BATTERY CONNECTOR TYPE		
MODEL	PART NUMBER	FOOTPRINT
UT6	DFHD08MR015	BAT-BP02083-B09065-7F-9P-V-QT6
UT7	DFHD08MR030	bat-20045mr009g10zr-8p-l-v

SI modified
Change CN18 to BAT-BP02083-B09065-7F-9P-V-QT6



PR113	VALUE	PART NUMBER
65W_90W	RC2512-R020	CS-020AFR00
120W	RC2512-R015	CS-015AFR01

*****UT6, UT7
BATTERY CONNECTOR
SCHEMATIC
LIBRARY IS
DIFFERENT.**



CELL_SLT = 1 - 3 S (Cells = GND 3S)
CELL_SLT = 0 - 4 S (Cells = VDD 4S)

Charging Current setting =
Ichg = 165mV / Rsense * (Vohlim / 3.3V)

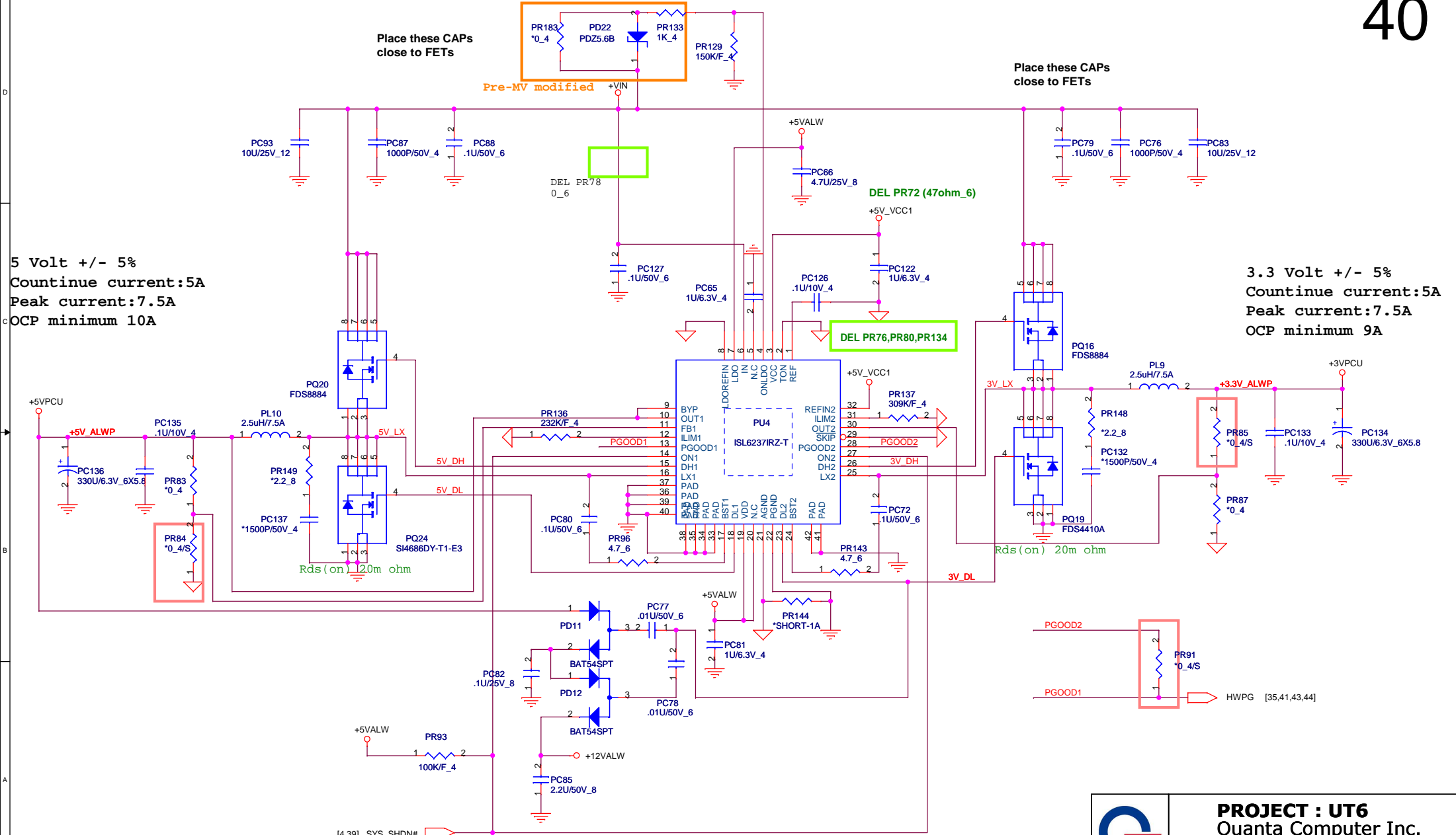
Input Current monitor
V_{icm} = 19.9 * (V_{csip} - V_{csin})

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Size Custom Document Number **Charger (ISL6251)** Rev 3A

Date: Thursday, August 07, 2008 Sheet 39 of 46

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW



Place these CAPs close to FETs

Place these CAPs close to FETs

5 Volt +/- 5%
 Countinue current:5A
 Peak current:7.5A
 OCP minimum 10A

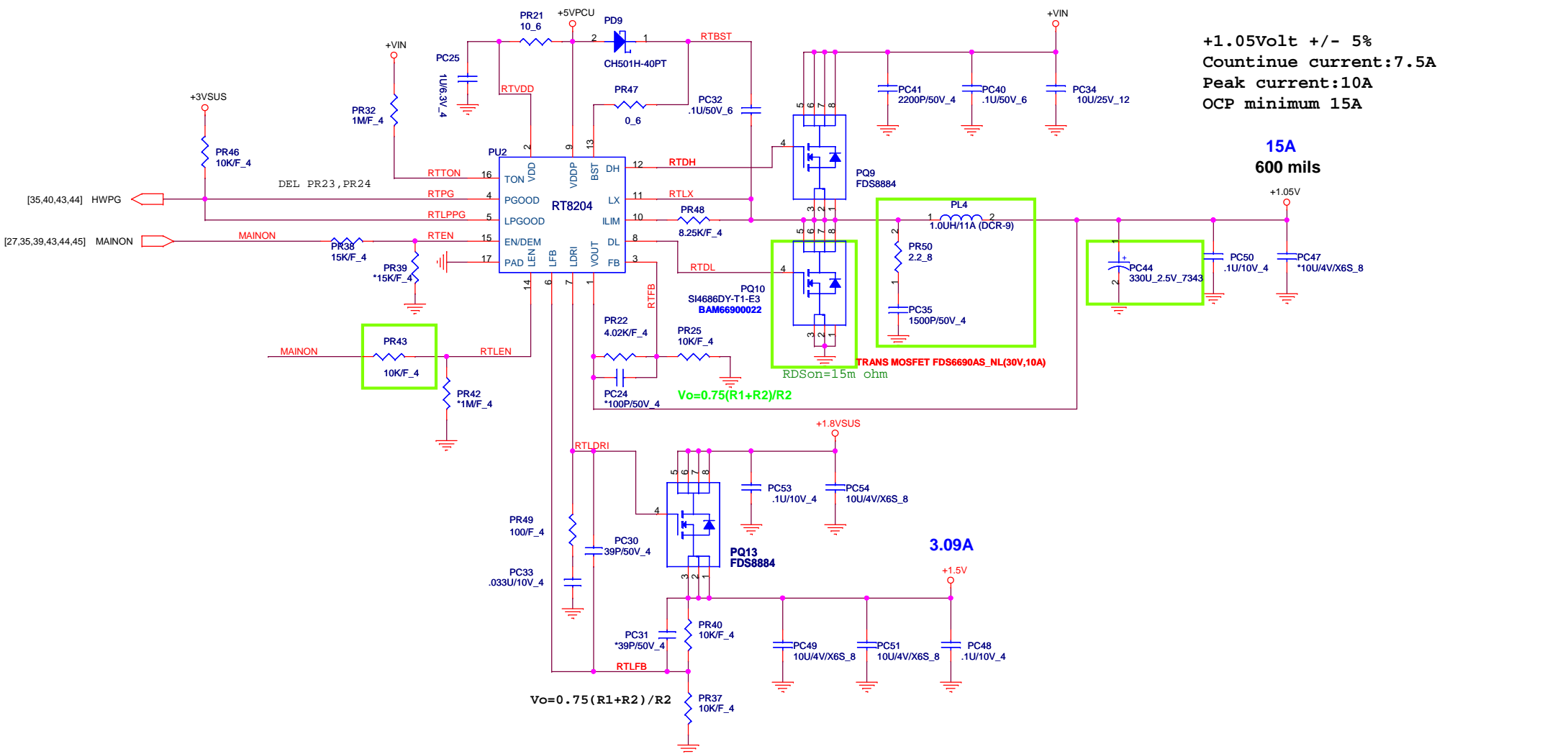
3.3 Volt +/- 5%
 Countinue current:5A
 Peak current:7.5A
 OCP minimum 9A



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Size B	Document Number +5V/+3V (ISL6237)	Rev 3A
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VCCP1.05V & +1.5V




+1.05Volt +/- 5%
 Countinue current:7.5A
 Peak current:10A
 OCP minimum 15A

15A
 600 mils

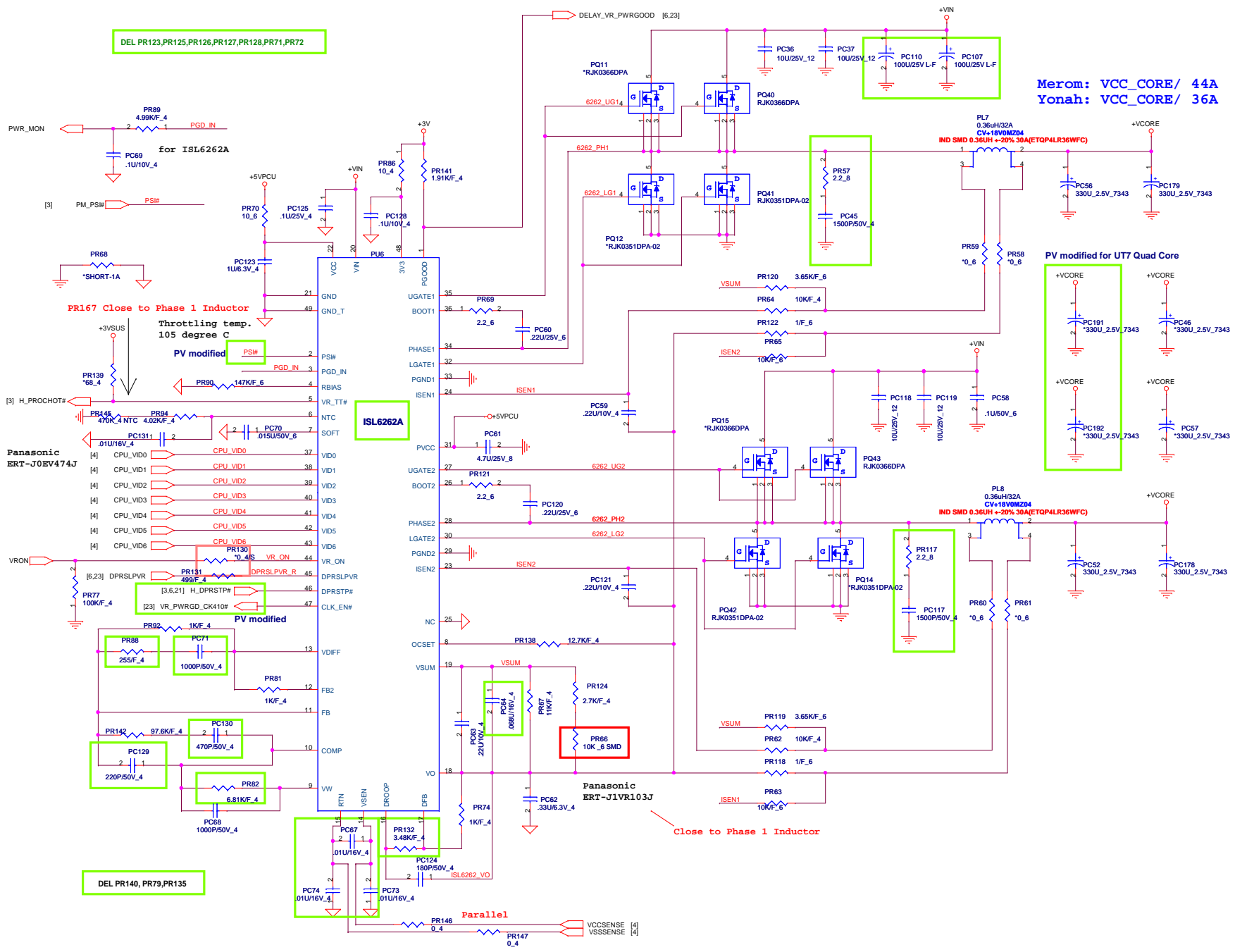
3.09A

$$V_o = 0.75(R1+R2)/R2$$

$$V_o = 0.75(R1+R2)/R2$$

	PROJECT : UT6 Quanta Computer Inc.	
	Size B	Document Number +1.05V/+1.5V (RT8204)
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Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A



DEL PR123,PR125,PR126,PR127,PR128,PR71,PR72

for ISL6262A
PC69 .1u/10V_4
PS#

PR167 Close to Phase 1 Inductor
Throttling temp.
105 degree C
PV modified
PS#

ISL6262A

Panasonic
ERT-J0EV474J

PV modified
PR92 1K/F_4
PR88 255/F_4
PC71 1000P/50V_4

DEL PR140, PR79, PR135

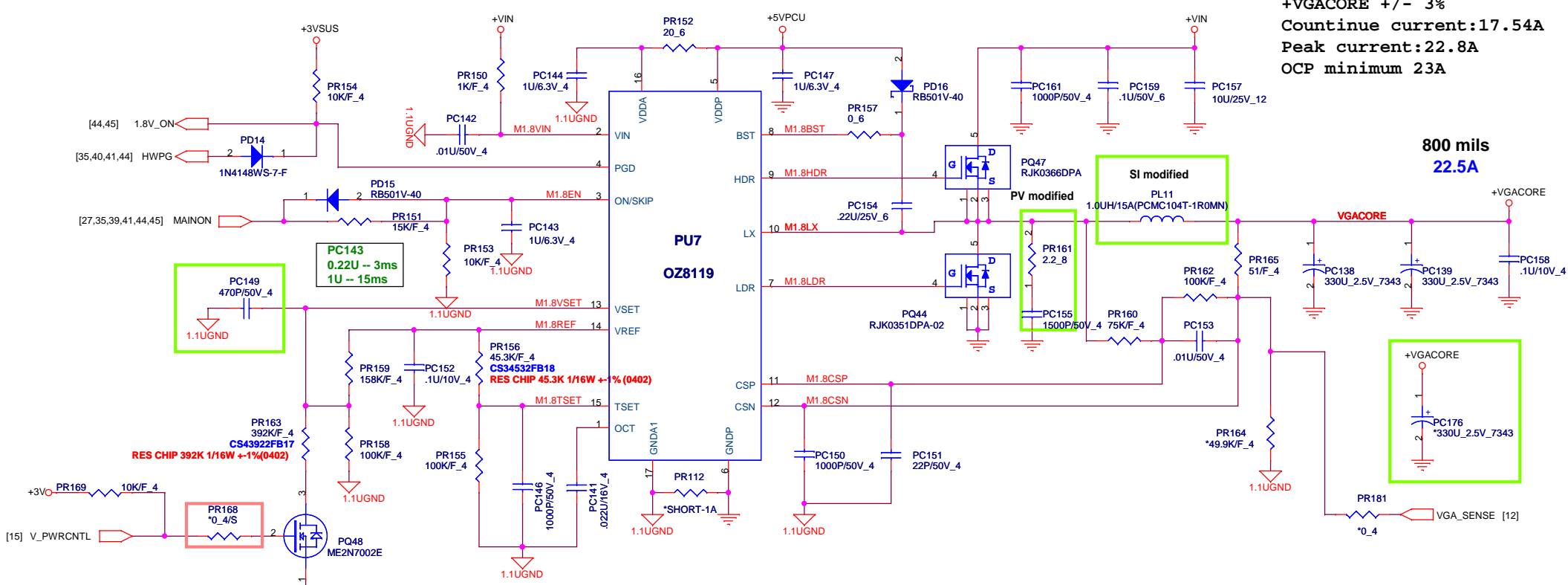
Close to Phase 1 Inductor

PV modified for UT7 Quad Core



PROJECT : UT6
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Size Custom	Document Number CPU Core (ISL6266A)	Rev 3A
Date: Thursday, August 07, 2008	Sheet 42	of 48



+VGACORE +/- 3%
 Countinue current:17.54A
 Peak current:22.8A
 OCP minimum 23A

800 mils
 22.5A

VREF=2.75V +/-1.5%

NB9P-GS: PR163=392Kohm
 Output = 0.9V

NB9M-GE: PR203=590Kohm
 NB9P-GS: PR203=768Kohm

CS45902FB10 RES CHIP 590K 1/16W +/-1%(0402)
 CS47682FB10 RES CHIP 768K 1/16W +/-1%(0402)

V_PWRCNTL	NB9P-GS
GPIO5	1.05V
Low	1.05V
High	0.9V

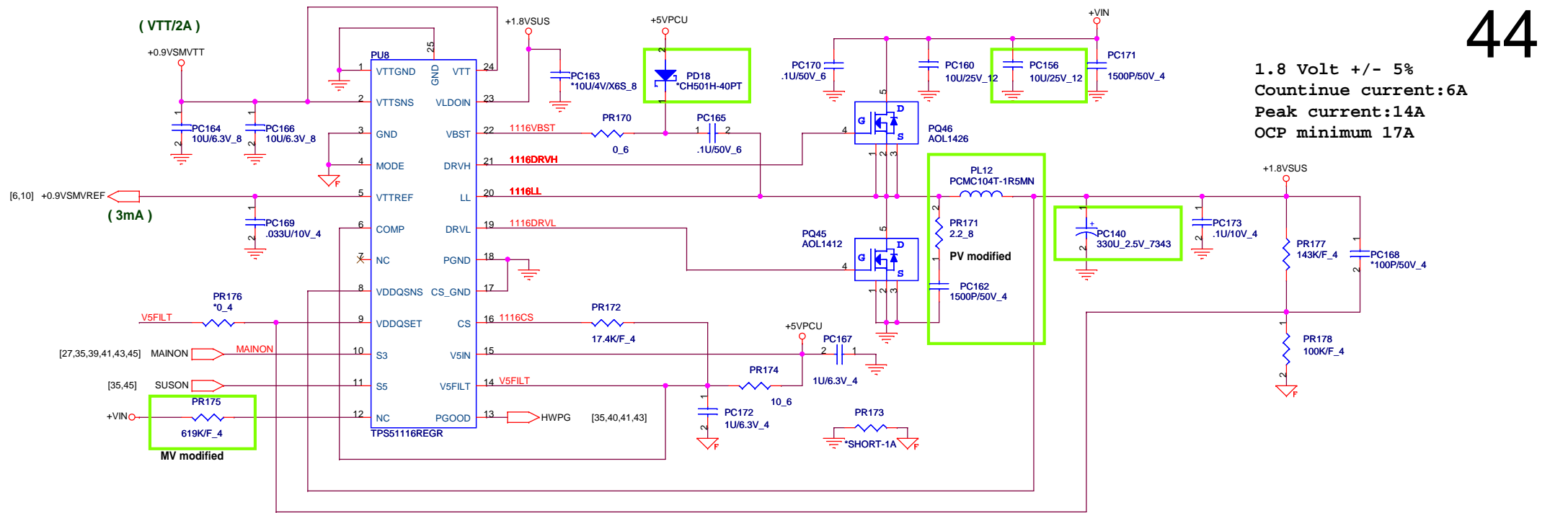
VGA_GPIO6	V_PWRCNTL		NB9P-GS	NB9M-GE
GPIO6	GPIO5			
Low	Low	MAX BAT	0.9V	0.9V
Low	High	SD DVD	0.9V	0.9V
High	Low	HD DVD	0.9V	0.9V
High	High	MAX PERF	1.05V	1.09V

03/21 remove PD22, PR180, PR181

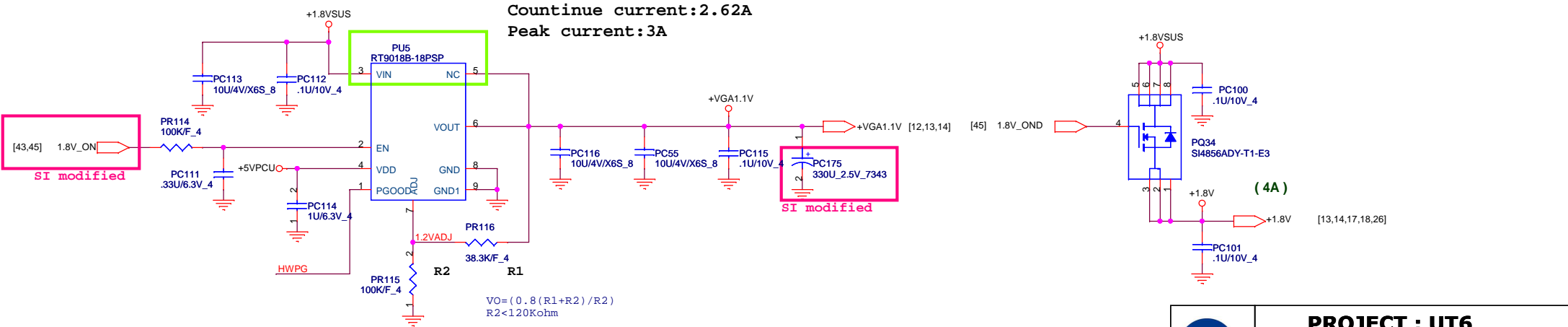


PROJECT : UT6
 Quanta Computer Inc.

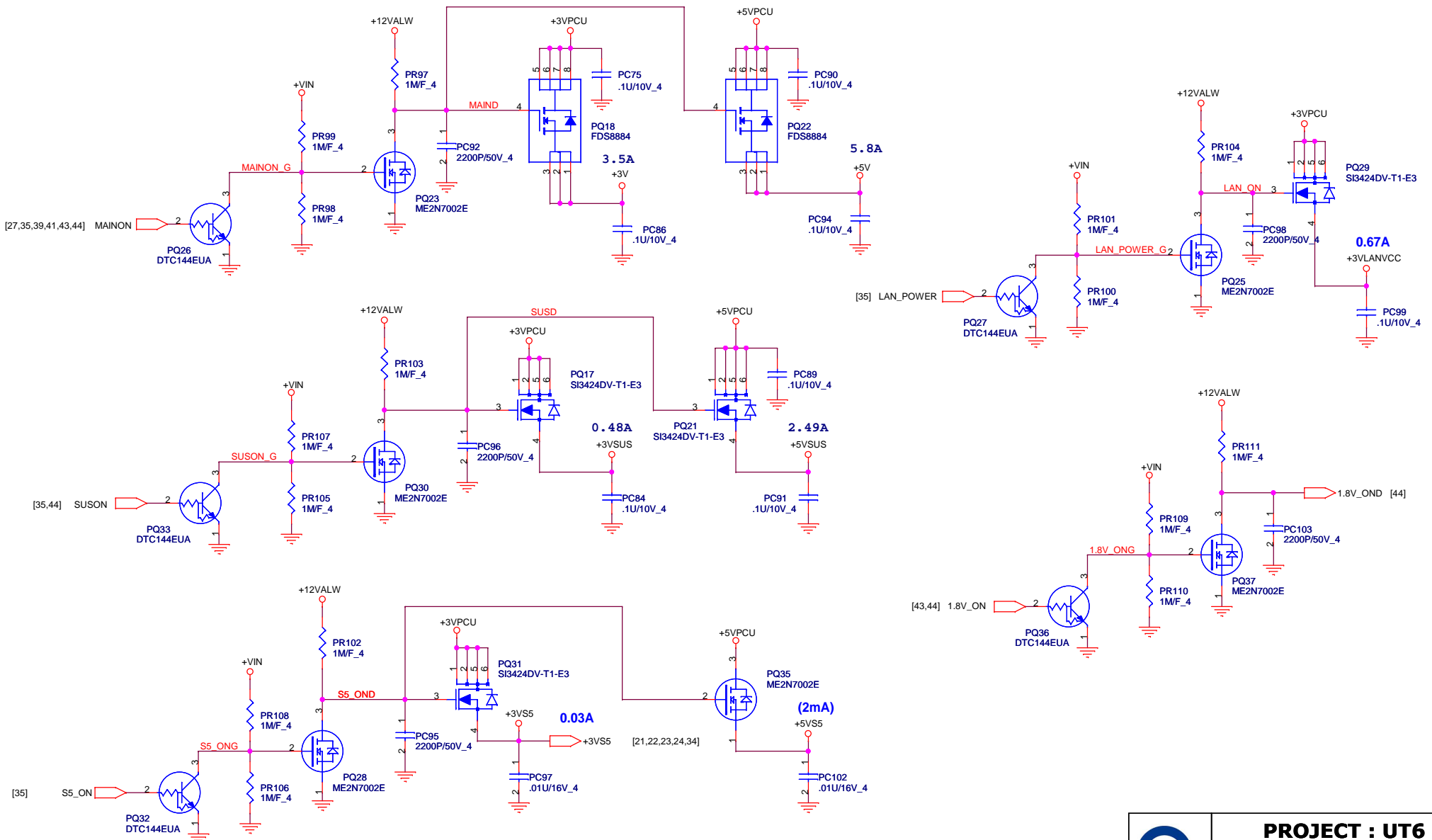
Size B	Document Number VGA CORE OZ8118	Rev 3A
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1.1 Volt +/- 5%
 Continue current: 2.62A
 Peak current: 3A



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	Size B	Document Number 1.8V/DDR_VTER/+1.8v/+1.1V
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Quanta Computer Inc.

Size B	Document Number DISCHARGE/3VS5/5VS5/LAN	Rev 3A
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	Voltage level	AC MODE				DC MODE			
		S0	S3	S4	S5	S0	S3	S4	S5
+3VPCU	3.3V +/- 5%	V	V	V	V	V	V	V	V
+5VPCU	5V +/- 5%	V	V	V	V	V	V	V	V
+3VRTC	3.3V +/- 5%	V	V	V	V	V	V	V	V
+3VS5	3.3V +/- 5%	V	V	V	V	V	V		
+5VS5	5V +/- 5%	V	V	V	V	V	V		
+3VSUS	3.3V +/- 5%	V	V			V	V		
+5VSUS	5V +/- 5%	V	V			V	V		
+1.8VSUS	1.8V +/- 5%	V	V			V	V		
+0.9VSMVTT	0.9V +/- 5%	V	V			V	V		
+1.5V	1.5V +/- 5%	V				V			
+1.05V	1.05V +/- 5%	V				V			
+VCORE	0.9~1.15V	V				V			
+VGA_CORE	0.9~1.2V	V				V			
+VGA1.1V	1.1V +/- 5%	V				V			
+1.8V	1.8V +/- 5%	V				V			
+3VLAVCC	3.3V +/- 5%	V				V			



PROJECT : UT6
 Quanta Computer Inc.

Size Custom	Document Number Voltage	Rev E3A
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