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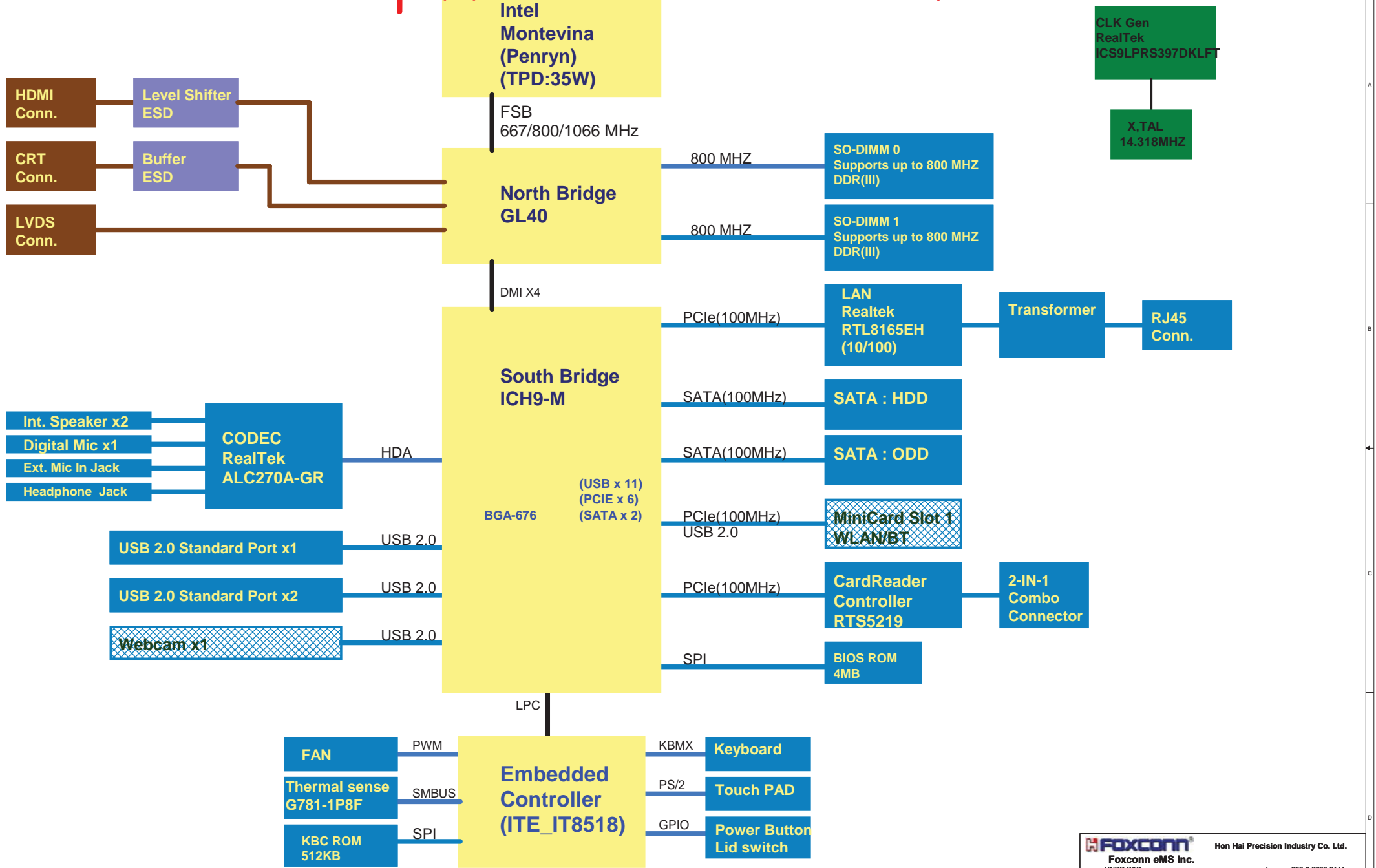
P. Leader	Check by	Design by

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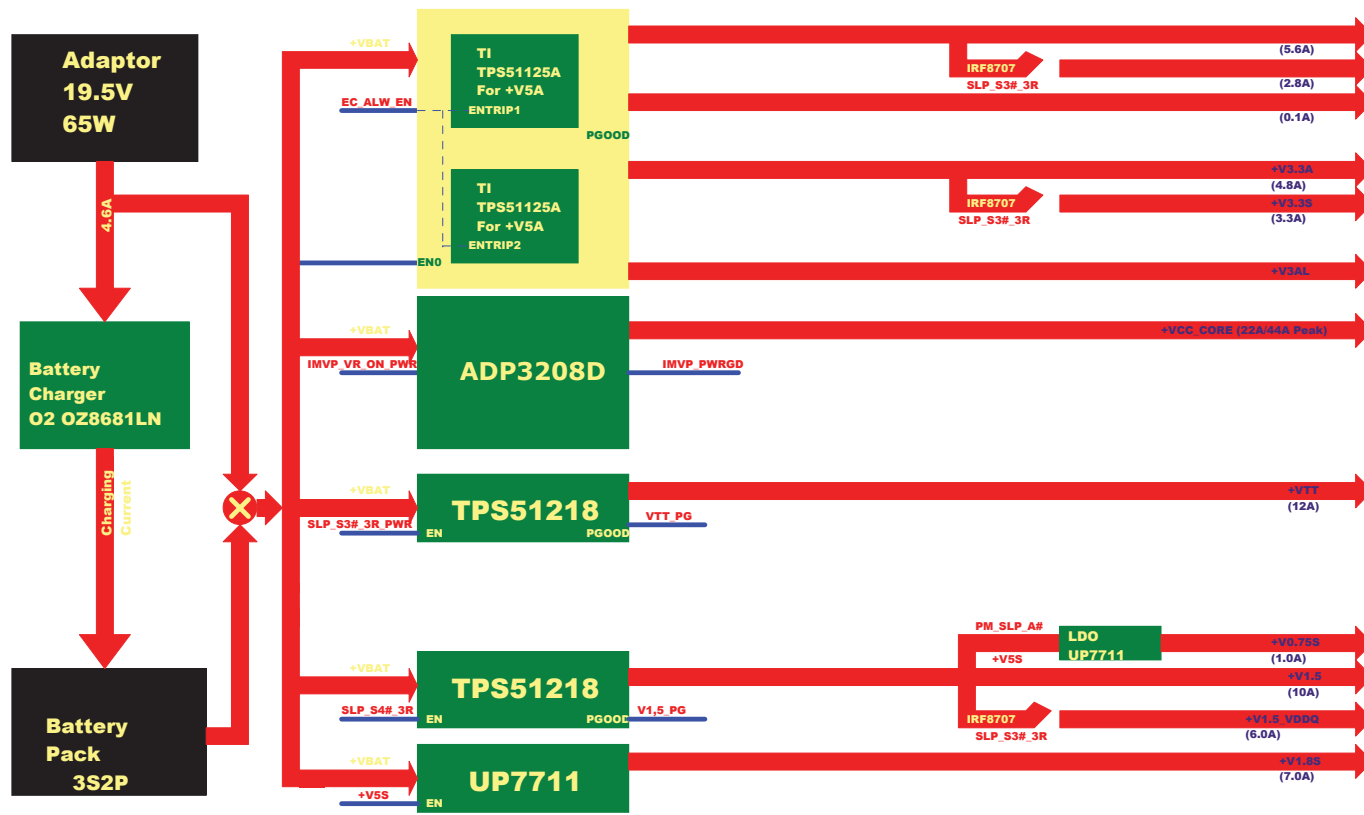
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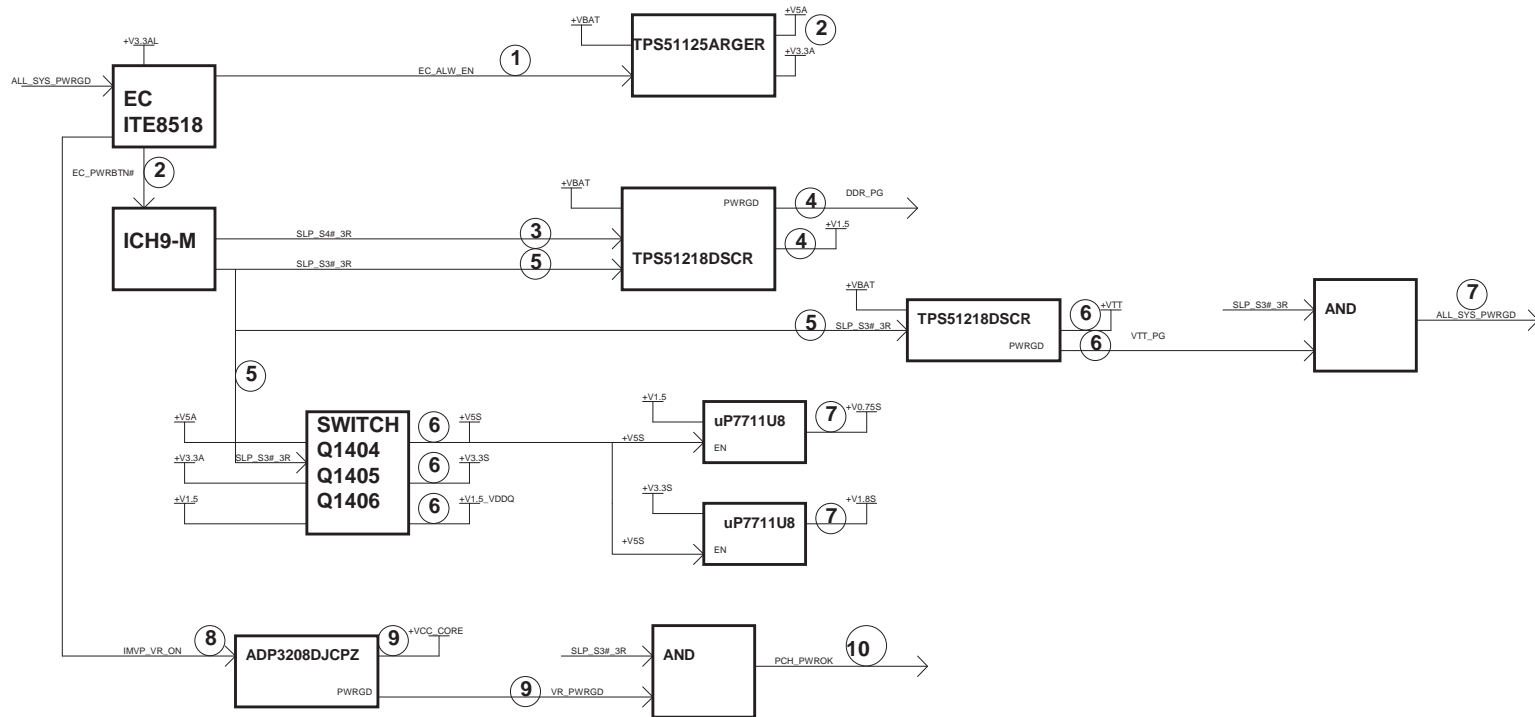
Size	Document Number	Rev
Custom	<b>TPN-F101/TPN-F102 Montevina</b>	

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### POWER MAP





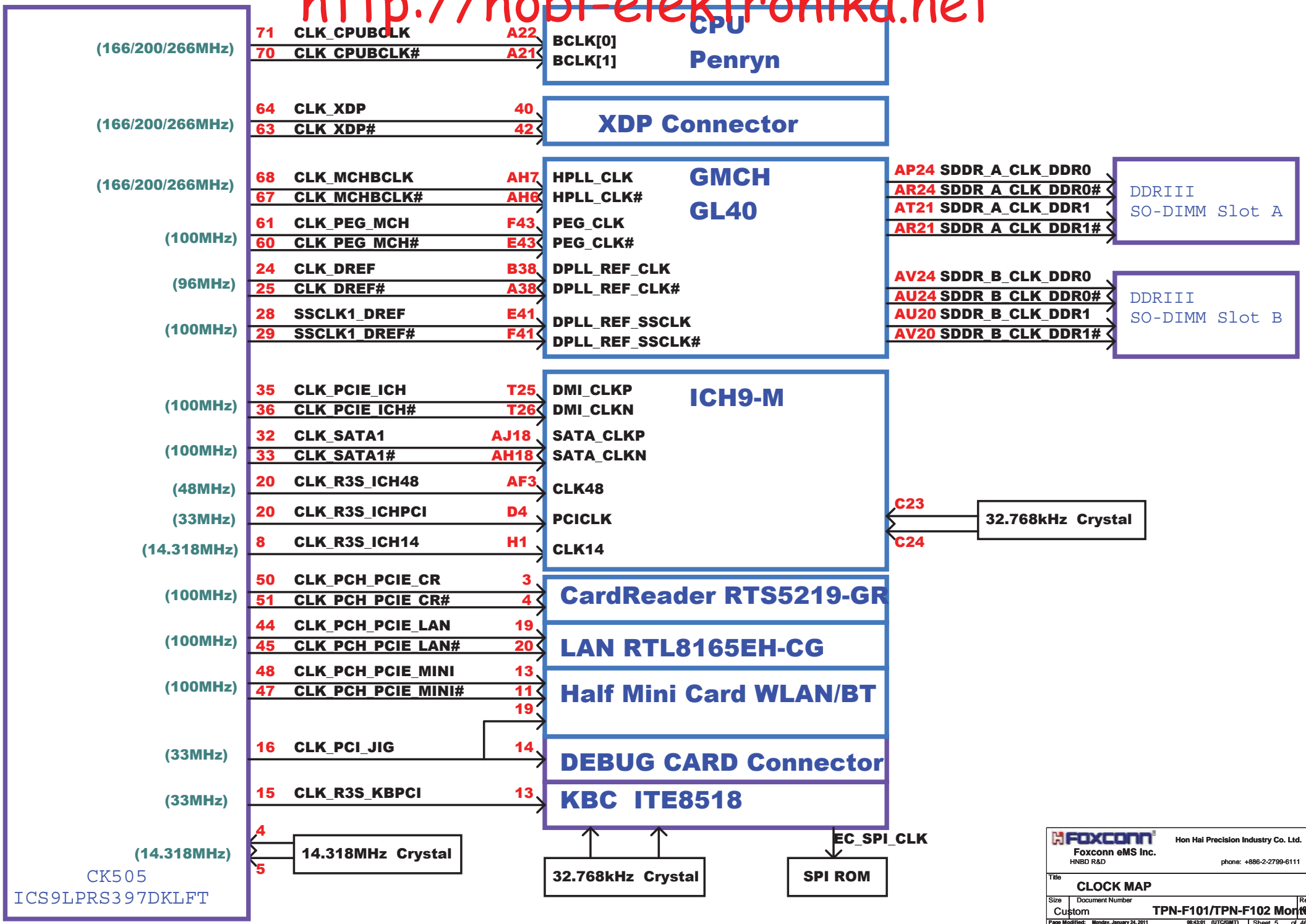
Power on Sequence required:

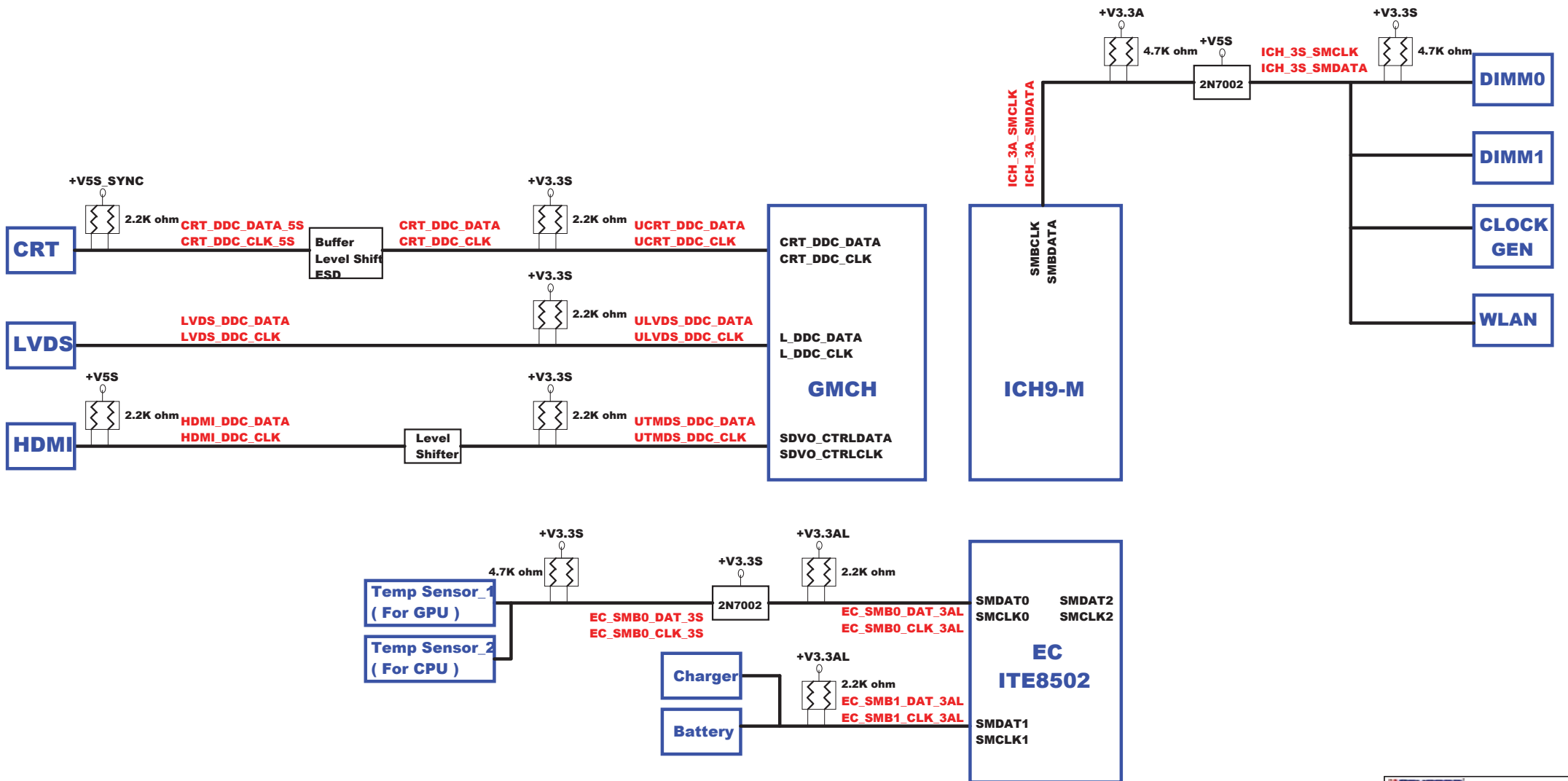
GL40:

- 1, +V3.3A ramp before +V1.1A
- 2, +V3.3S ramp before +V1.8S
- 3, +V1.8S ramp before +V1.1S
- 4, +V3.3S ramp before +V1.1S

ICH9-M:

- 1, 0 < (+V3.3S) - (+V1.8S) < 2.1
- 2, +V1.8S ramp before +V1.1S
- 3, +V1.1S ramp before VCC\_NB





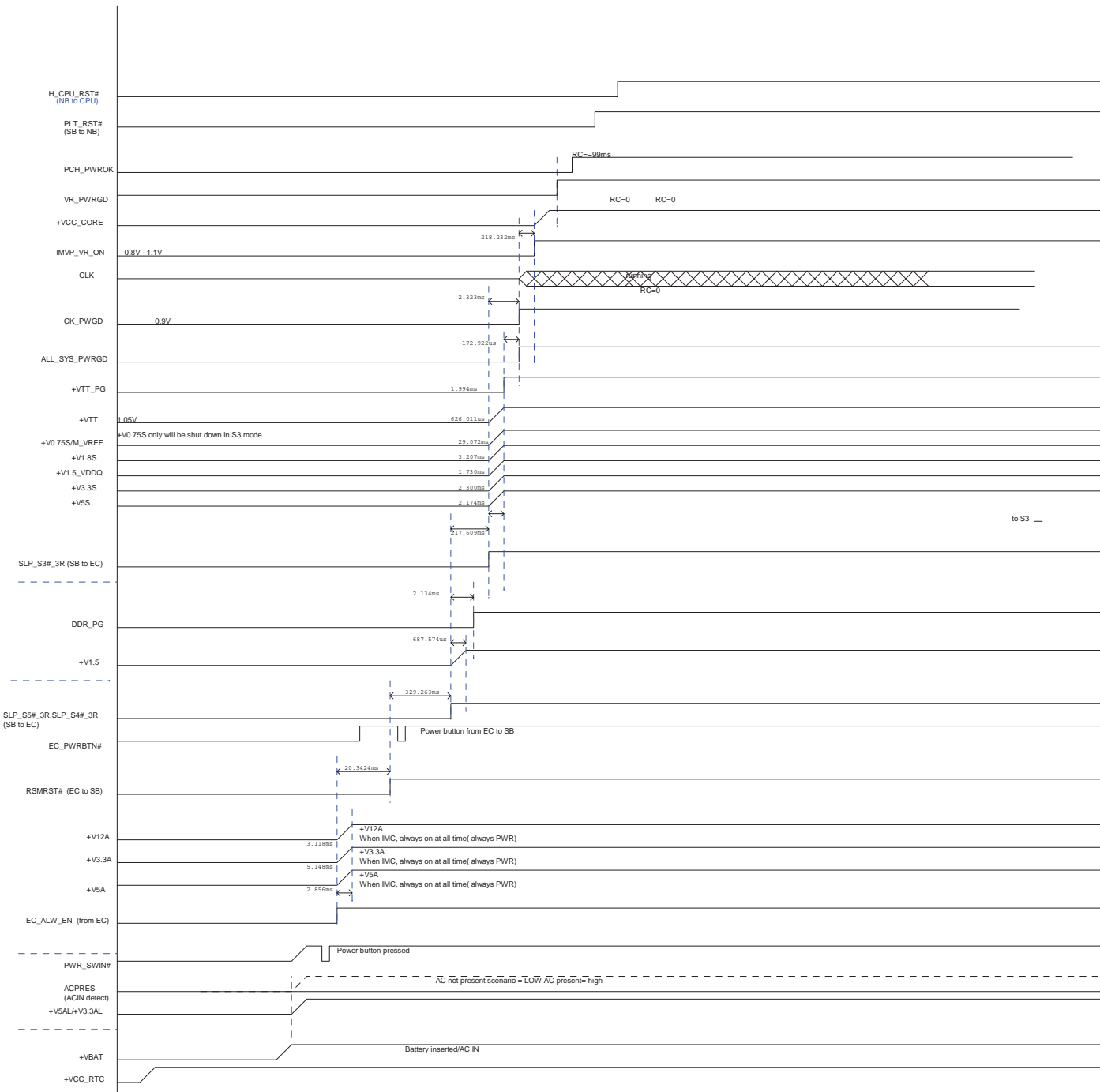
**Power on Sequence required:**

**ICH9M:**

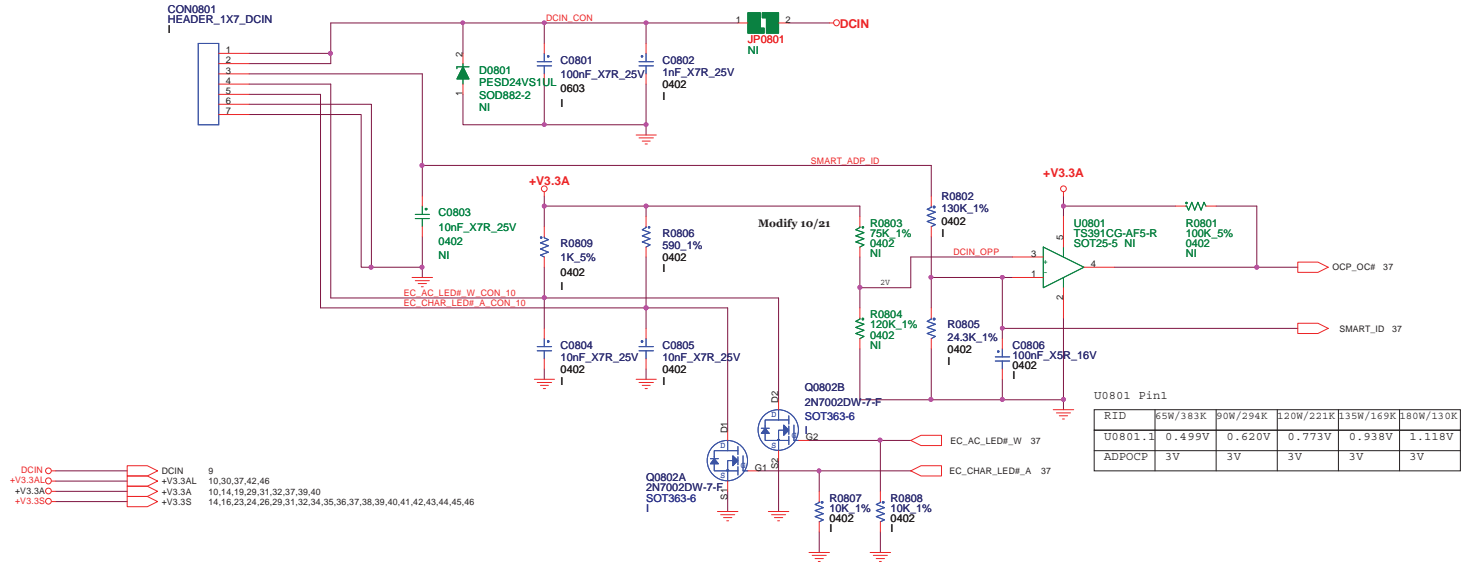
- 1, +V3.3A ramp before +V1.1A
- 2, +V3.3S ramp before +V1.8S
- 3, +V1.8S ramp before +V1.1S
- 5, +V3.3A ramping down time > 300us
- 6, 50uS <= All power rails except +V3.3A <= 40mS
- 7, 100uS <= +V3.3A <= 40mS

**GMCH:**

- 1, 0 < (+V3.3S) - (+V1.8S) < 2.1
- 2, +V1.8S ramp before +V1.1S
- 3, +V1.1S ramp before +VCC\_NB

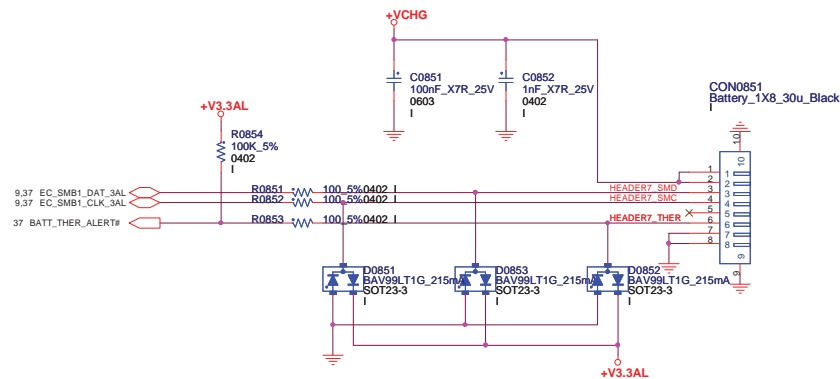


## DC\_JACK WIRE to BOARD CONNECTOR



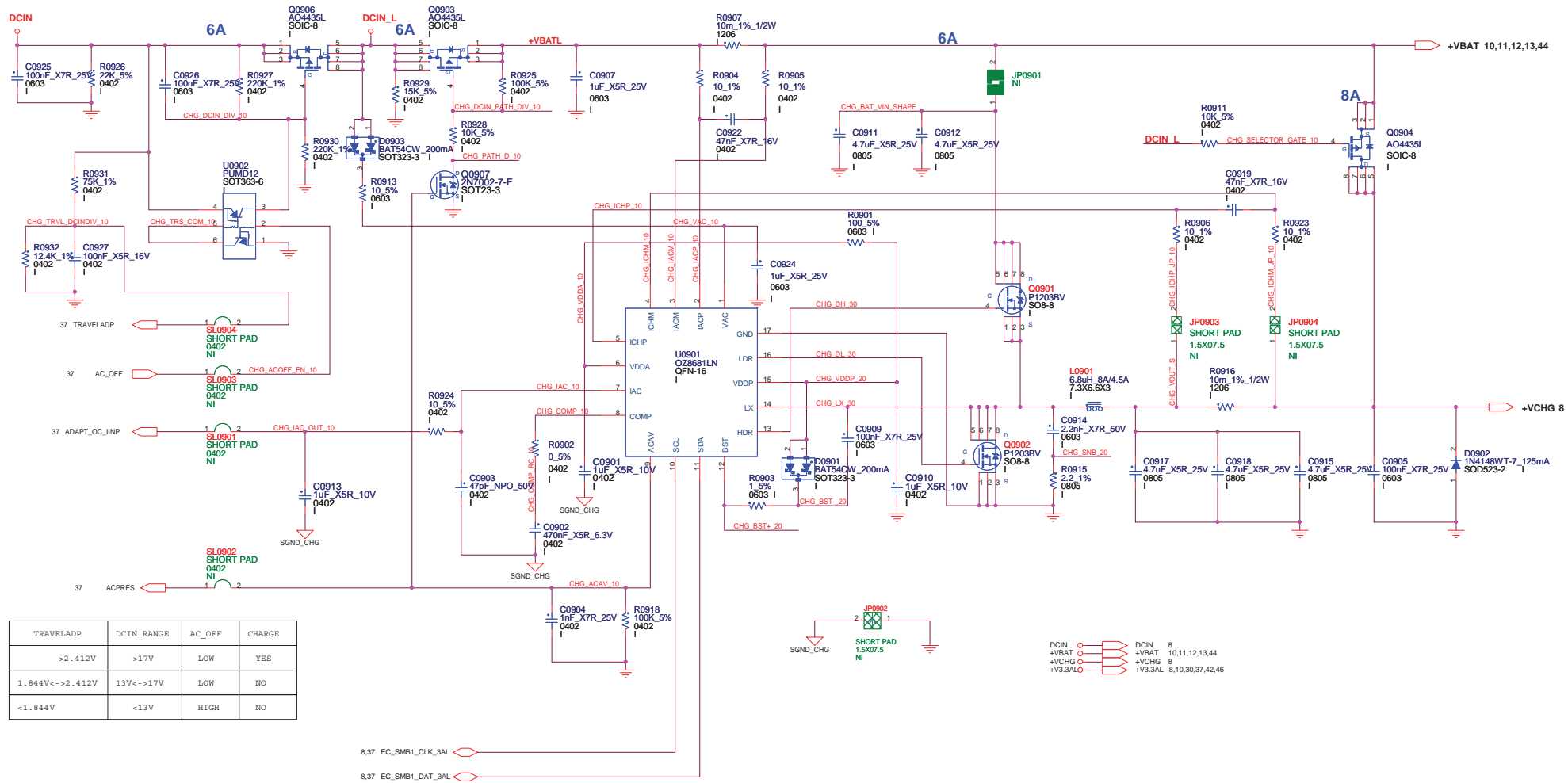
## BATTERY CONNECTOR

2010.0914.0





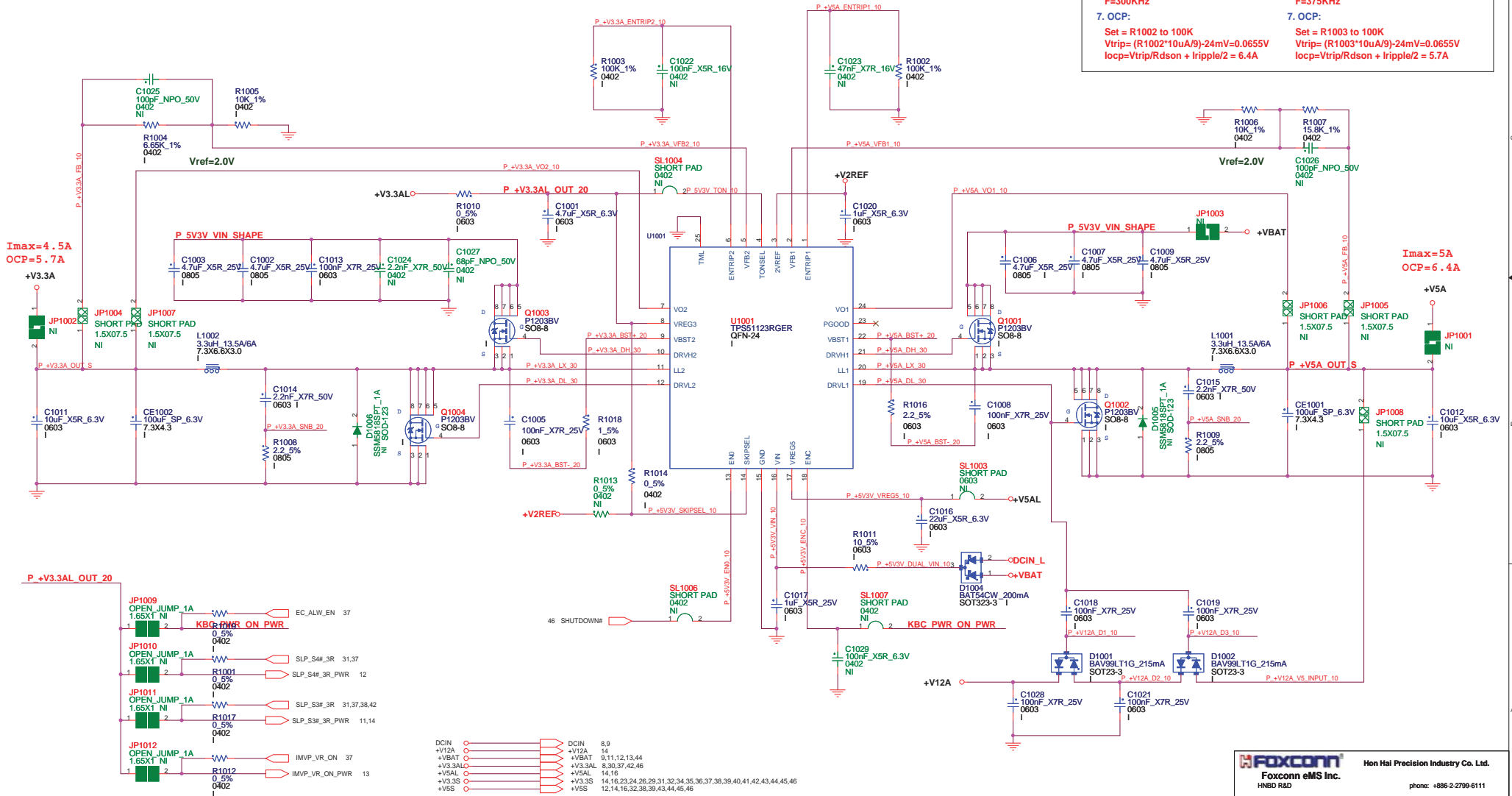
# BATTERY CHARGER



## +V5A / +V3.3A POWER SUPPLY

2010.1103.0

<p>1. I/P Current:  <math>I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 3.7A</math></p> <p>2. Ripple Current:  <math>I_{rip} = 3.72A</math></p> <p>3. Ripple Voltage:  <math>ESR/1 = 15mohm</math>  <math>V_{rip} = 55.8mV</math></p> <p>4. Inductor Spec:  <math>I_{sat} = 13.5A</math>  <math>I_{dc} = 6A</math>  <math>DCR = 30mohm</math></p> <p>5. MOSFET Spec:  <b>H-side MOSFET: IRF8707PBF</b>  <math>R_{ds(ON)} = 17.5mohm</math> (<math>V_{gs} = 4.5V</math>)  <math>I_{cont} = 11A</math> (<math>T = 25^\circ C</math>)  <math>I_{peak} = 88A</math> (Pause = 10 us)</p> <p>6. Frequency:  <math>F = 300KHz</math></p> <p>7. OCP:  <math>Set = R1002 \text{ to } 100K</math>  <math>V_{trip} = (R1002 \cdot 10uA/9) - 24mV = 0.0655V</math>  <math>I_{ocp} = V_{trip} / R_{dson} + I_{ripple} / 2 = 6.4A</math></p>	<p>1. I/P Current:  <math>I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.2A</math></p> <p>2. Ripple Current:  <math>I_{rip} = 2.21A</math></p> <p>3. Ripple Voltage:  <math>ESR/1 = 15mohm</math>  <math>V_{rip} = 33.15mV</math></p> <p>4. Inductor Spec:  <math>I_{sat} = 13.5A</math>  <math>I_{dc} = 6A</math>  <math>DCR = 30mohm</math></p> <p>5. MOSFET Spec:  <b>L-side MOSFET: IRF8707PBF</b>  <math>R_{ds(ON)} = 17.5mohm</math> (<math>V_{gs} = 4.5V</math>)  <math>I_{cont} = 11A</math> (<math>T = 25^\circ C</math>)  <math>I_{peak} = 88A</math> (Pause = 10 us)</p> <p>6. Frequency:  <math>F = 375KHz</math></p> <p>7. OCP:  <math>Set = R1003 \text{ to } 100K</math>  <math>V_{trip} = (R1003 \cdot 10uA/9) - 24mV = 0.0655V</math>  <math>I_{ocp} = V_{trip} / R_{dson} + I_{ripple} / 2 = 5.7A</math></p>
---	--



DCIN	8,9
+V12A	14
+VBAT	8,11,12,13,44
+V3.3AL	8,30,37,42,46
+V5AL	14,16
+V3.3S	14,16,23,24,26,29,31,32,34,35,36,37,38,39,40,41,42,43,44,45,46
+V5S	12,14,16,32,38,39,43,44,45,46

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Title: **5V/3.3V**

Size: Document Number

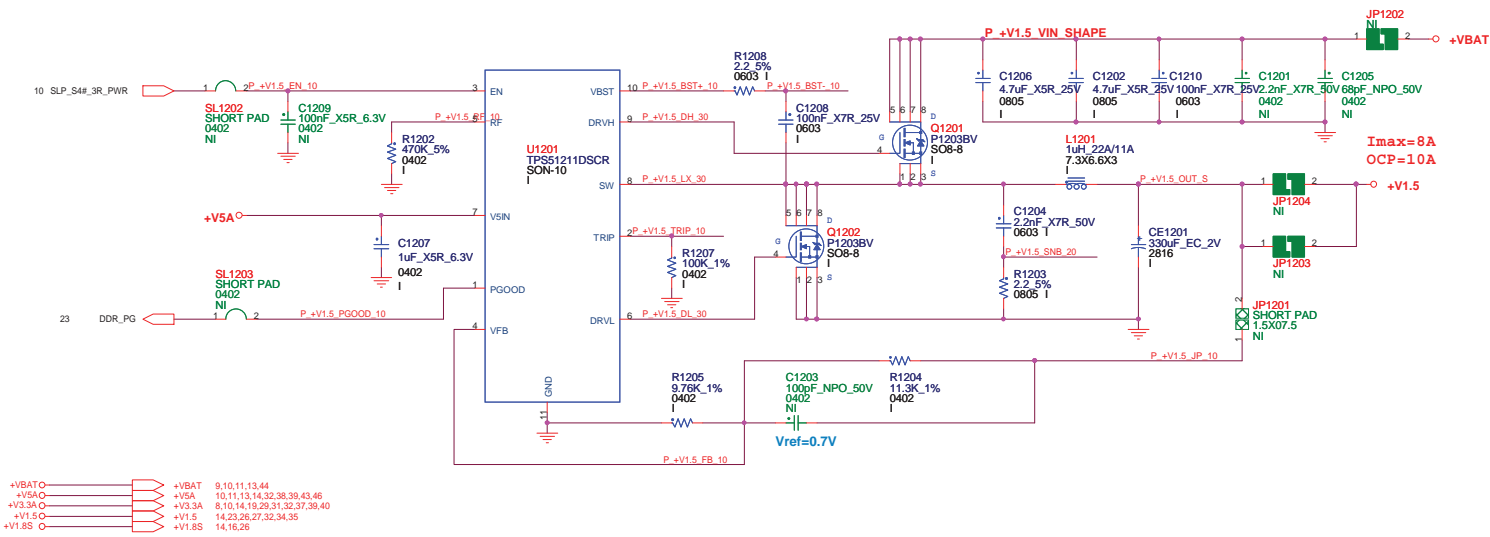
C **CHICAGO**

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Rev: **0.1**

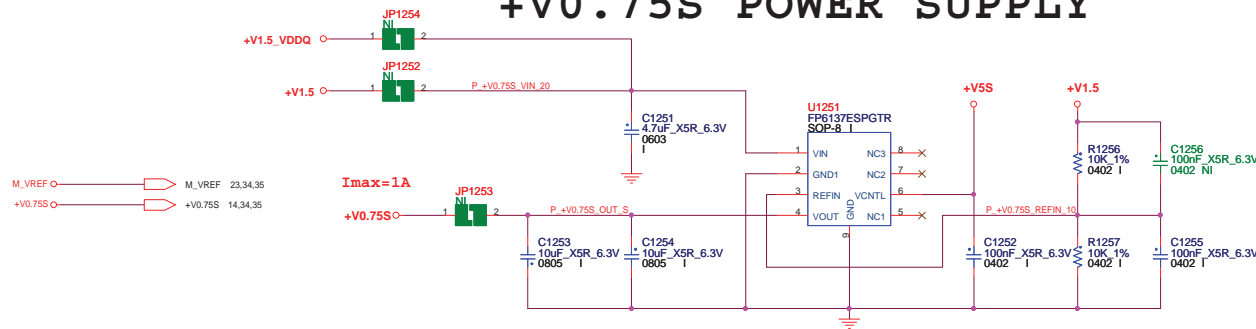


## +V1.5 POWER SUPPLY

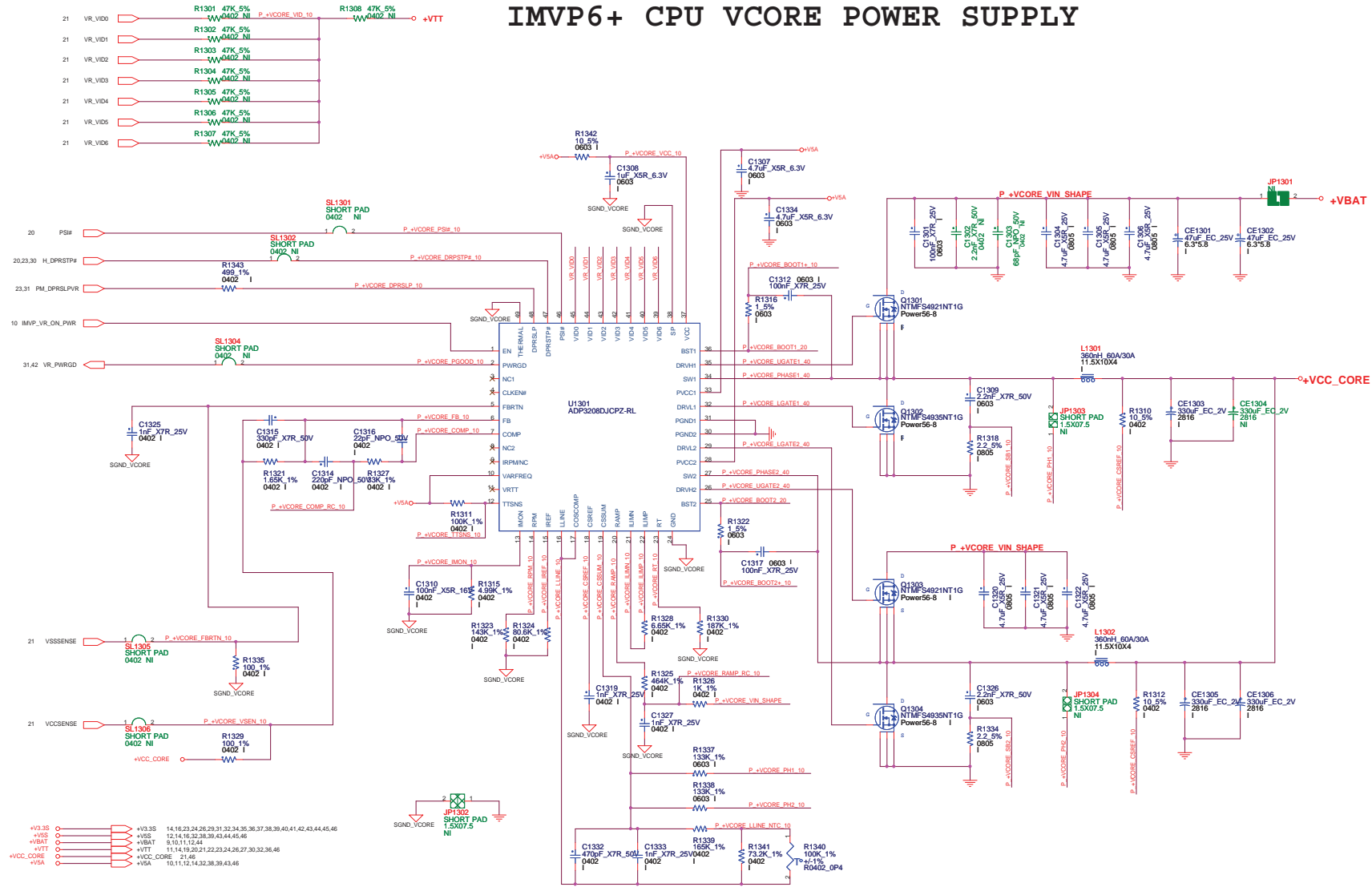


- +V1.5:**
- I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.78A$
  - Ripple Current:**  
 $I_{rip} = 3.34A$
  - Ripple Voltage:**  
 $ESR/1 = 9m\Omega$   
 $V_{rip} = 30.6mV$
  - Inductor Spec:**  
 $I_{sat} = 36A$   
 $I_{dc} = 18A$   
 $DCR = 3.3m\Omega$
  - MOSFET Spec:**  
**H-side MOSFET: IRF8707PBF**  
 $R_{ds(ON)} = 17.5m\Omega$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 11A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 88A$  (Pause = 10 us)  
**L-side MOSFET: IRF8707PBF**  
 $R_{ds(ON)} = 17.5m\Omega$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 11A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 88A$  (Pause = 10 us)
  - Frequency:**  
 $F = 290KHz$  ( $R_{0902} = 470K$ )
  - OCp:**  
 $Set = R_{0907} \text{ to } 100K$   
 $V_{trip} = R_{0907} \cdot 10\mu A = 1V$   
 $I_{ocp} = (V_{trip} / 8 \cdot R_{dson}) + I_{ripple} / 2 = 9.5A$

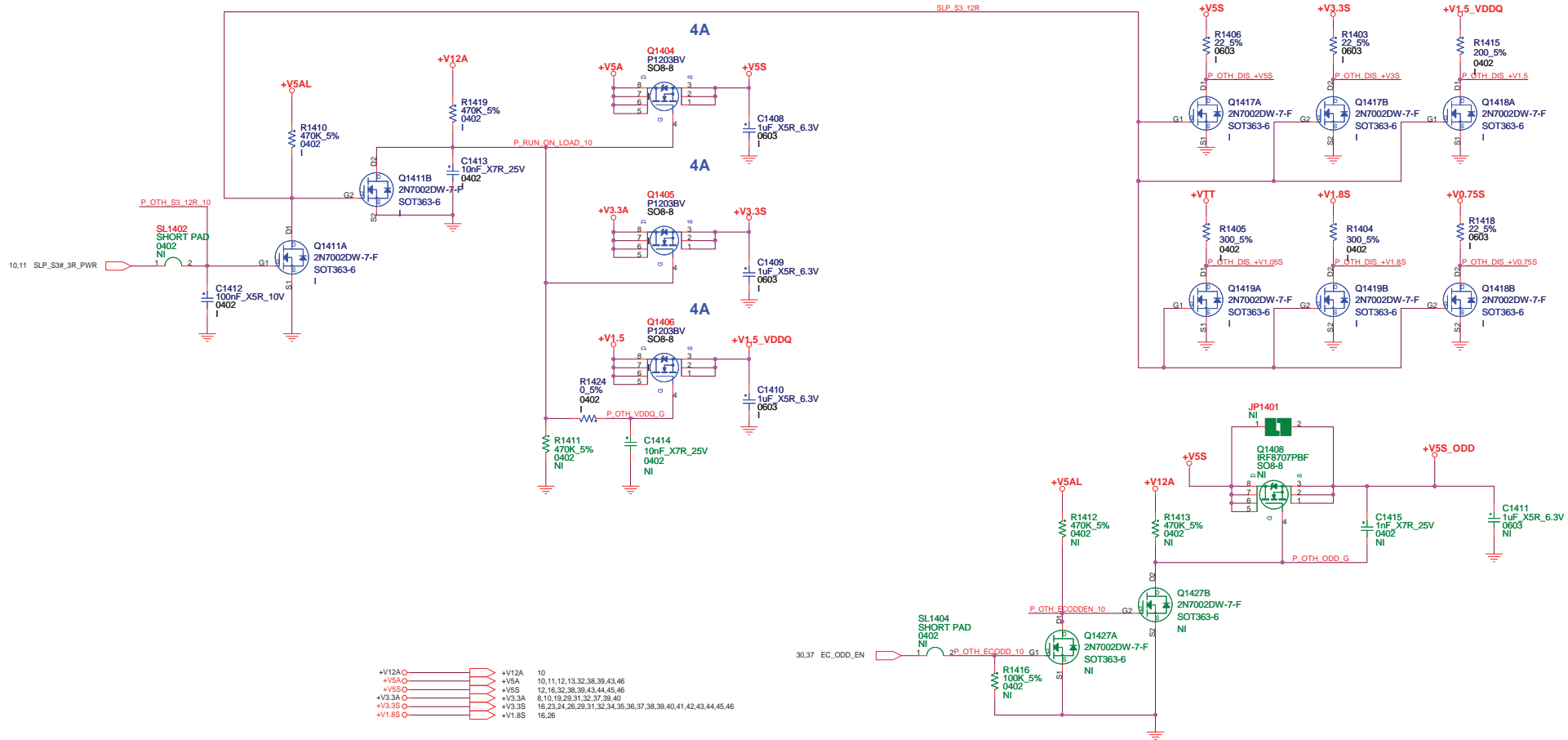
## +V0.75S POWER SUPPLY



## IMVP6+ CPU VCORE POWER SUPPLY



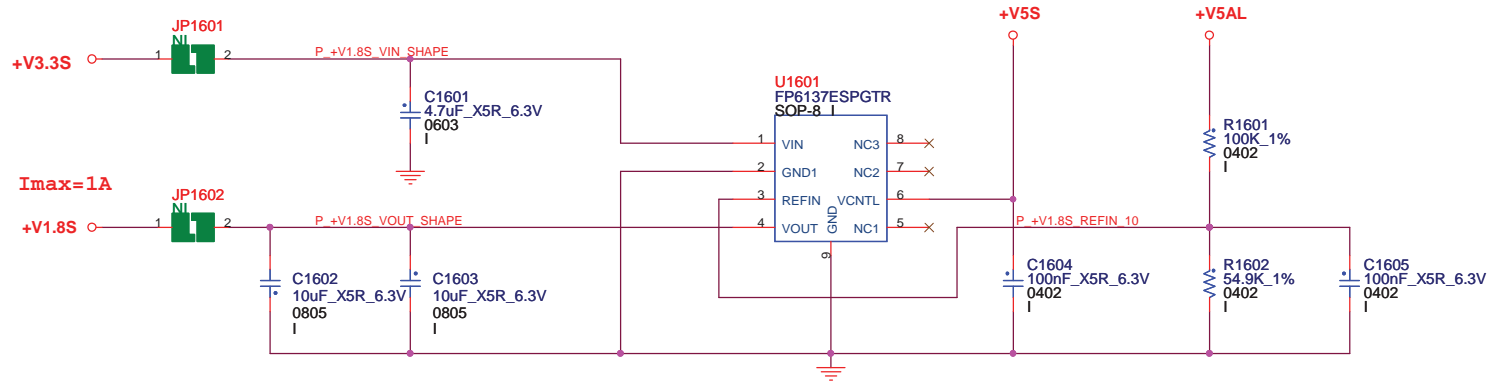
OTHER POWER / DISCHARGE CIRCUITS



+V12A	10
+V5A	10, 11, 12, 13, 32, 38, 39, 43, 46
+V5S	12, 16, 32, 38, 39, 43, 44, 45, 46
+V3.3A	8, 10, 19, 29, 31, 32, 37, 39, 40
+V3.3S	16, 23, 24, 26, 29, 31, 32, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46
+V1.8S	16, 26

<http://hobi-elektronika.net>

# +V1.8S POWER SUPPLY

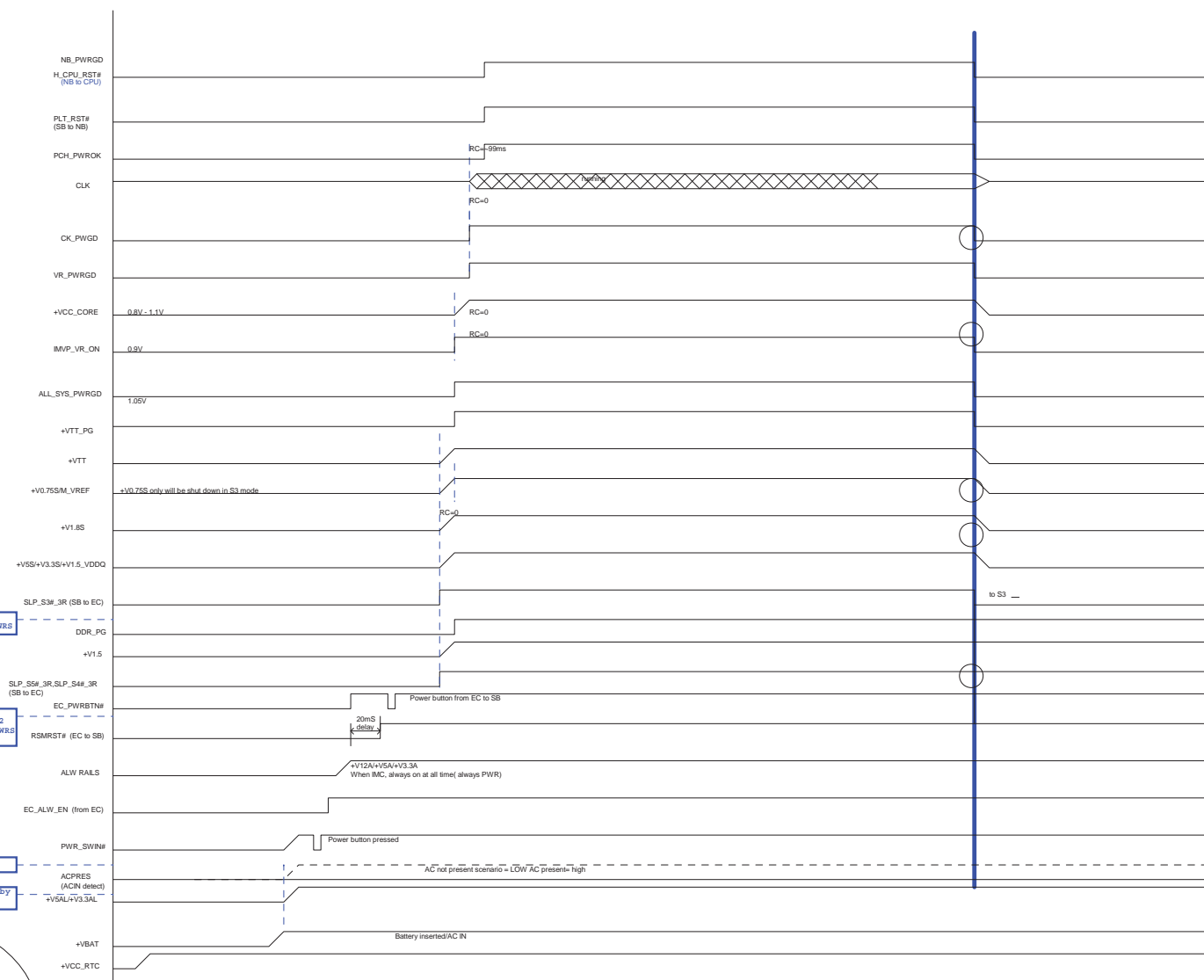


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Size CUSTOMER	Document Number CHICAGO	Page Modified: Monday, January 24, 2011 08:43:02 (UTC/GMT) Sheet 16 of 46	



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Signals	Test Point
LDT_RST#	CX61
LDT_PG	RX23
CPU_CLKP/N	CX72 ; CX73
NB_PWRGD	RX30
SB_PWRGD	DS63
+VCC_NB	PJ212
+VLDT	PJP15/2
+V1.1S	PJP15/1
VRM_PWRGD	DB72
+VDOR_CPU	PJ16/1
+VCC_CORE	PCE12
+VDDNB_CPU	PJ17/2
VDDA_PWRGD	PR211
+VDDA_CPU	PJ22/2
+V1.5S	PJ28/1
V1.8S_PWRGD	DS71
+V1.8S	PJ21
+V3.3S	PC170
+V5S	PC175
+V12S	PQ41/D
SLP_S3M_3R	RS60
+V0.75S	PJ8/2
M_VREF	PC182
+V1.5	RS76
SLP_S5M_3R	DB/2
EC_PWRBTN#	DB/2
RSMRST#	RS61
+V1.1A	PJ23/2
+V3.3A	PC109
+V5A	PJ25
+V12A	PC169
EC_ALW_EN	PQ27/G
PWR_SWIN#	HEADER2/B
ACPRES	RS51
+V5AL	PC164
+V3.3AL	PJ24
MS1ALDO	PC61
+VBAT	PJ19/2
+VCC_RTC	CS48



CPU MEM CTL & DDR3 SODIMM PWRs

CPU TMM/SB/SB\_SCL1/2 SB\_KB/SPI/LPC ROM PWRs

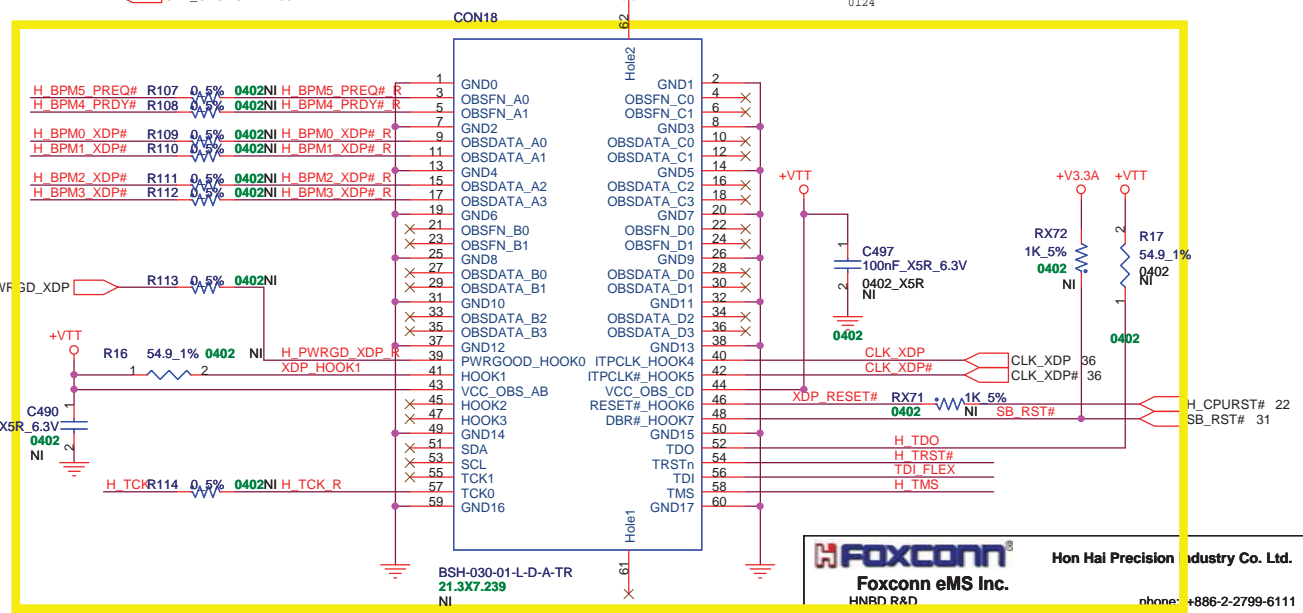
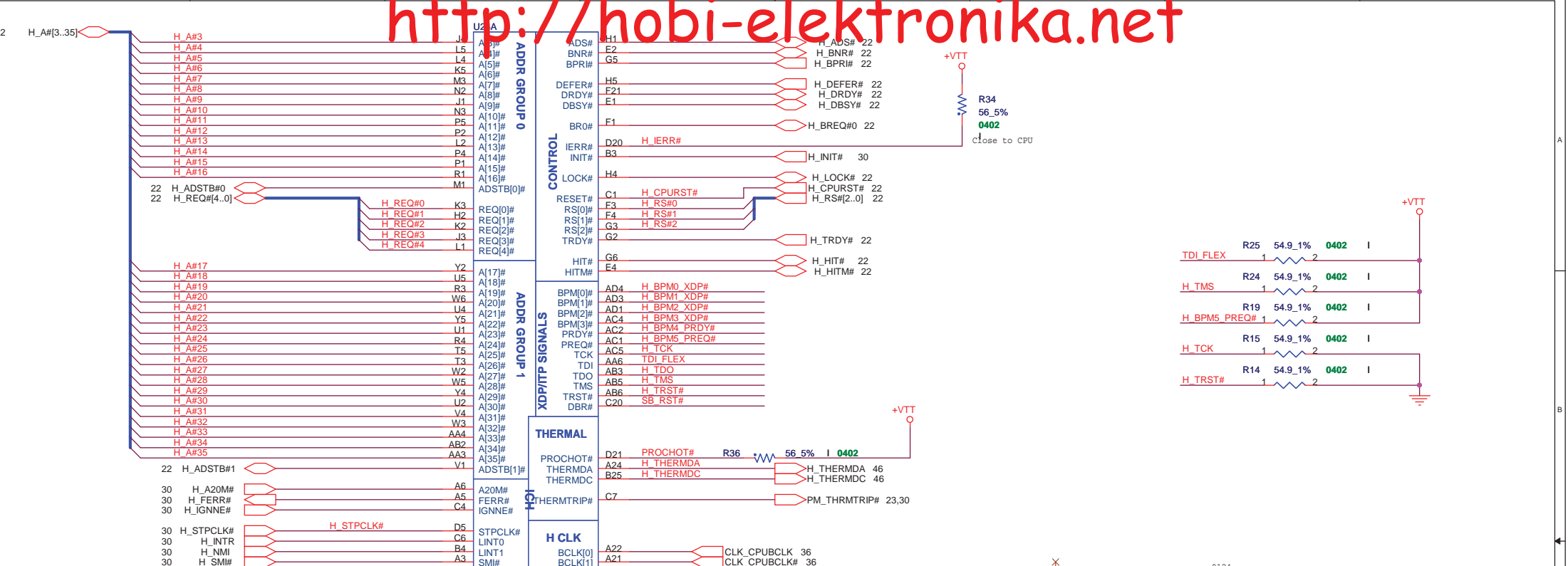
KBC is ready

KBC is powered by +V3.3AL

**Power on Sequence required:**

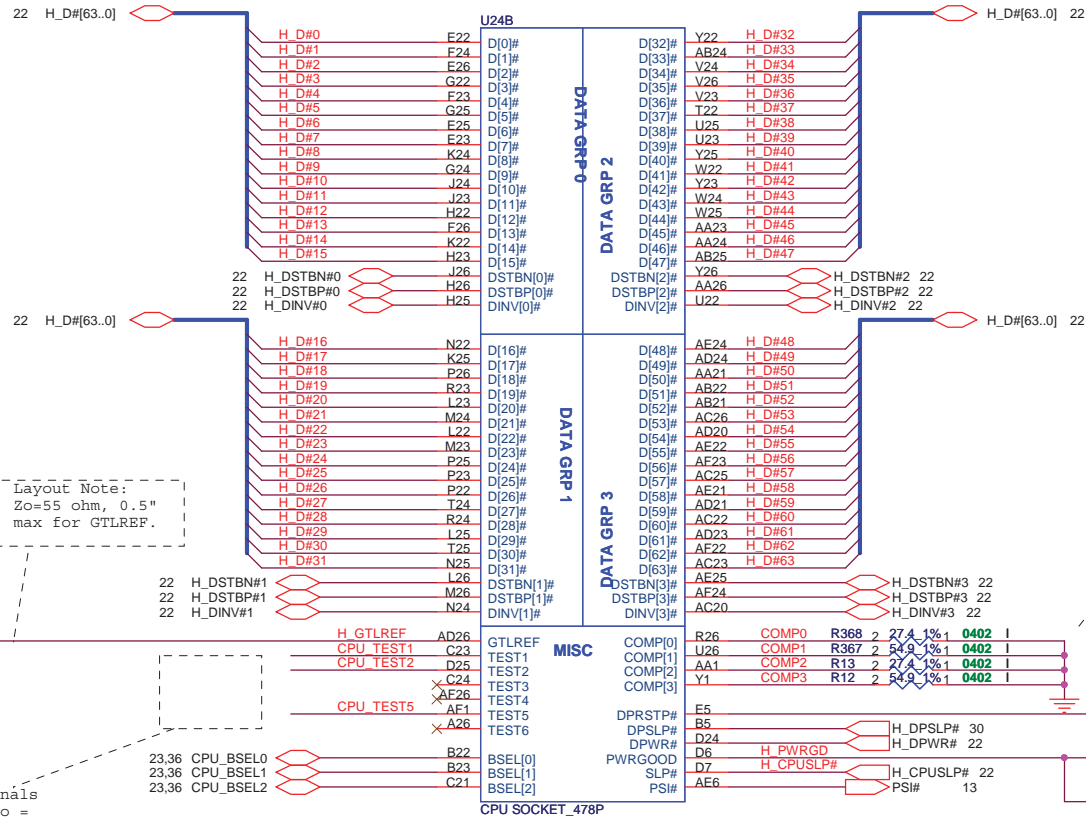
**ICHM:**  
 1. +V3.3A ramp before +V1.1A  
 2. +V3.3S ramp before +V1.8S  
 3. +V1.8S ramp before +V1.1S  
 5. +V3.3A ramping down time > 300us  
 6. 50us <= All power rails except +V3.3A <= 40mS  
 7. 100us <= +V3.3A <= 40mS

**GMCH:**  
 1. 0 <= (+V3.3S) - (+V1.8S) < 2.1  
 2. +V1.8S ramp before +V1.1S  
 3. +V1.1S ramp before +VCC\_NB



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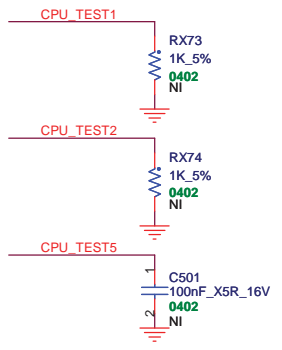
Title		
Penryn (HOST BUS) 1/3		
Size	Document Number	Rev
Custom	TPN-F101/TPN-F102 Montevina	
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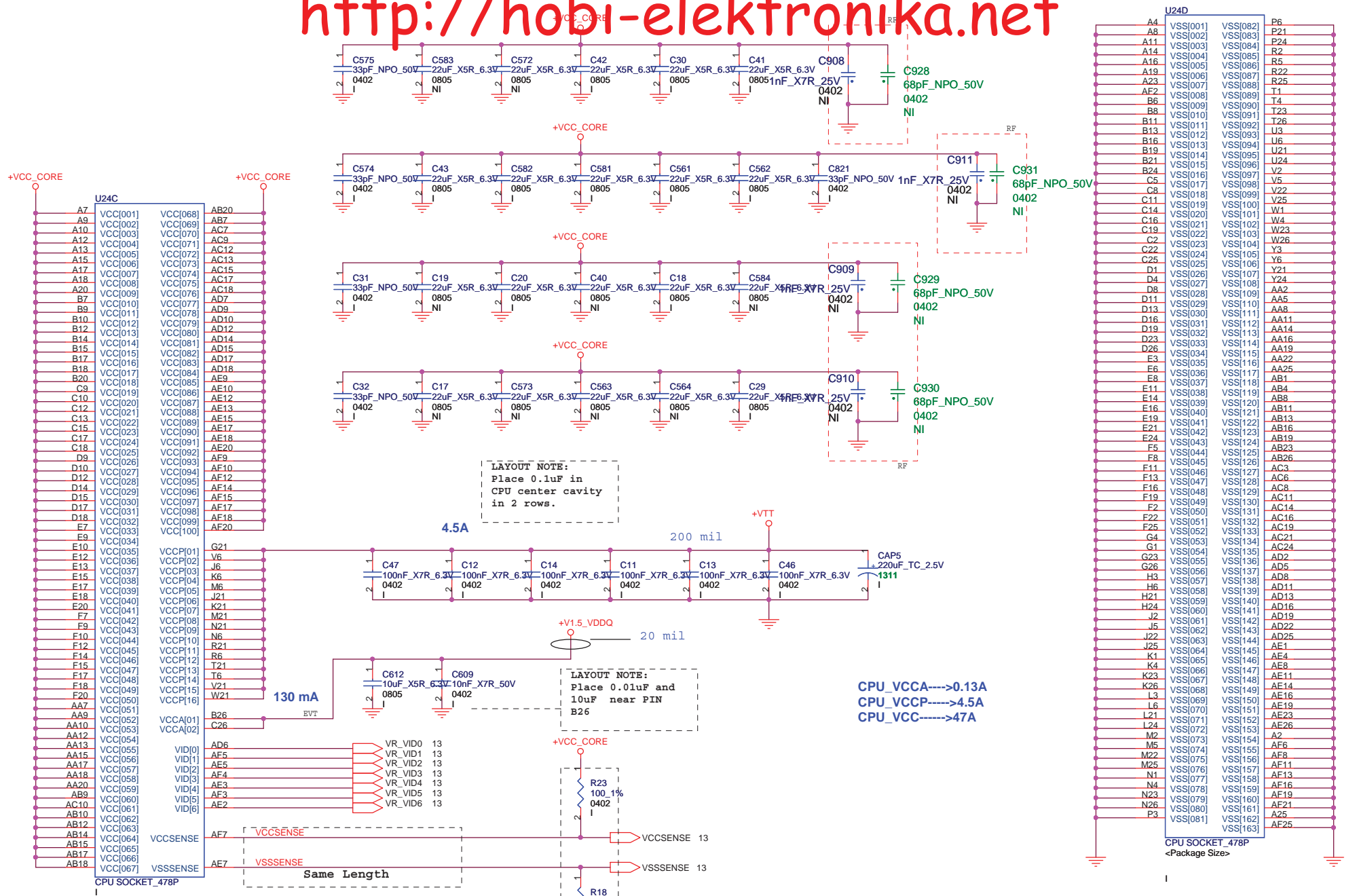
Layout Note:  
 Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5". Width=18mil(MS)  
 Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5". Width=5mil(MS)

Place close to CPU

Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. TEST4 and TEST6 and TEST7 pins can be left NC.



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Title: <b>Penryn (HOST BUS) 2/3</b>			
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Custom	<b>TPN-F101/TPN-F102 Montevina</b>		
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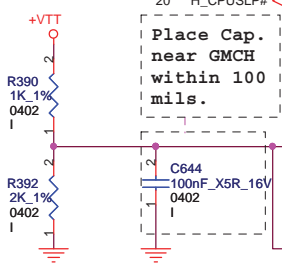
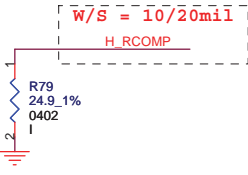
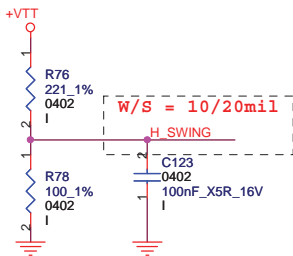
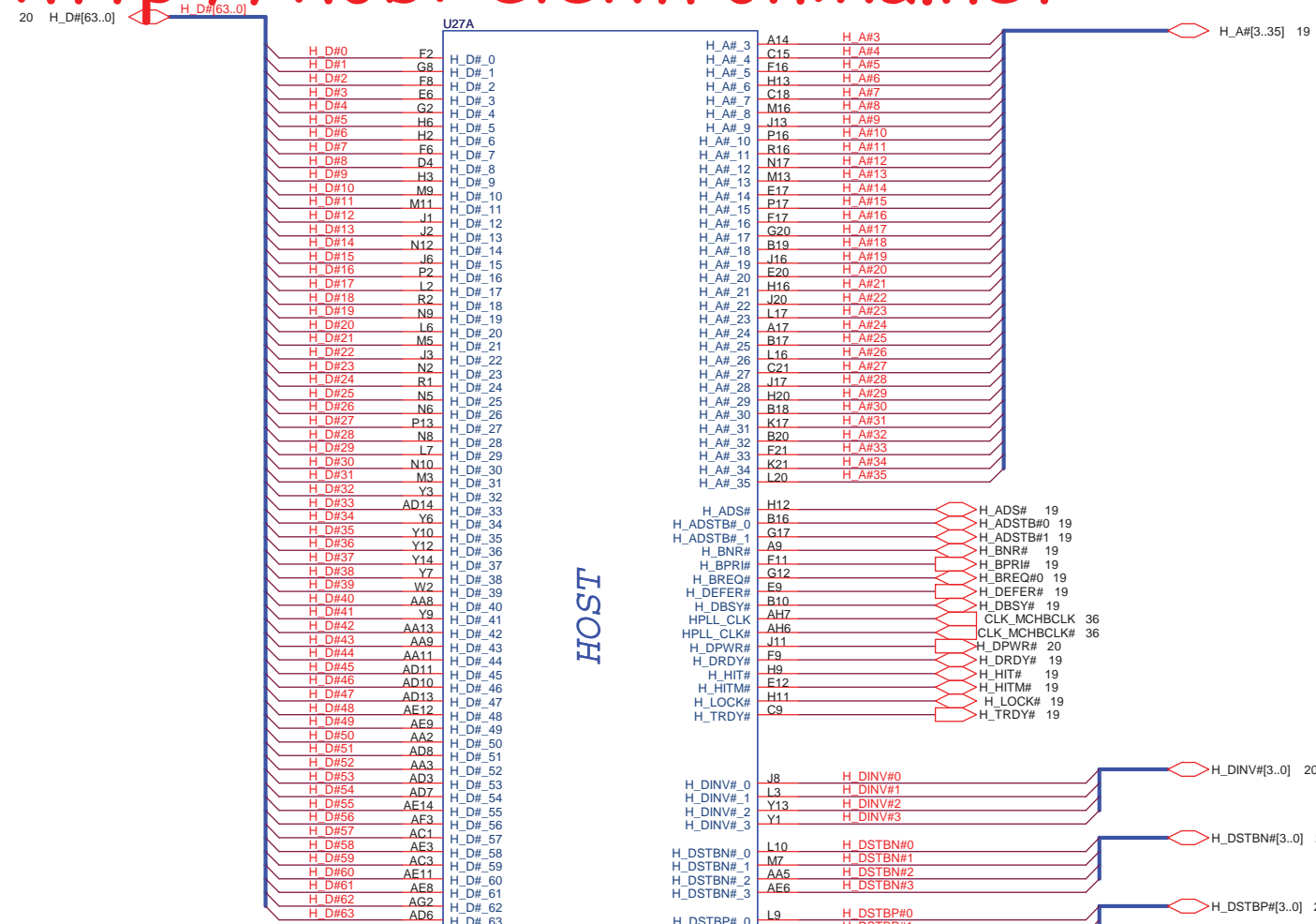
Outer width=18 mil spacing=7 mil  
 Inner width=14 mil spacing=7 mil  
 Length match < 25 mil

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Title: **Penryn (POWER/GROUND) 3/3**

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Traces width 10 mils.

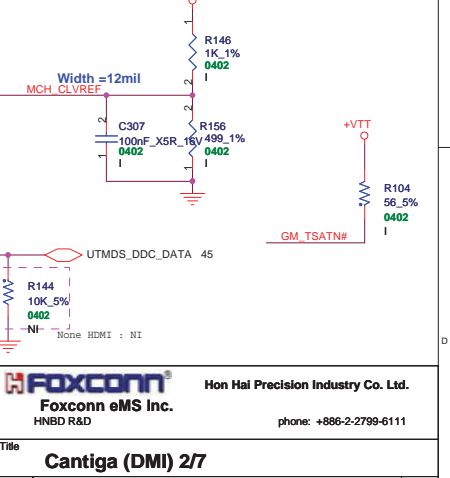
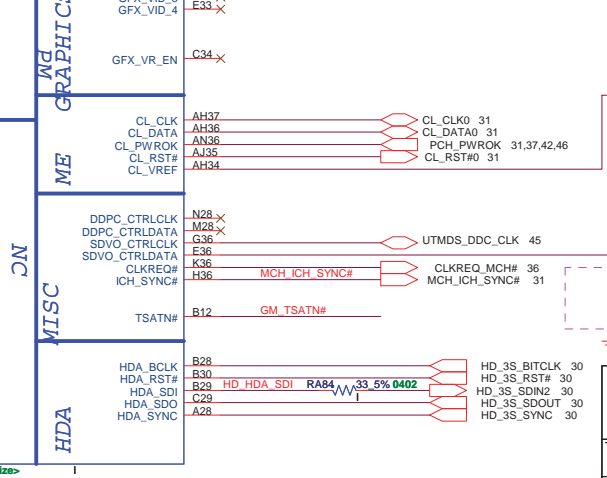
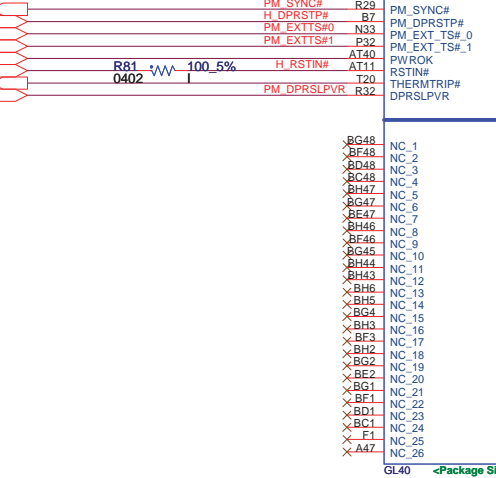
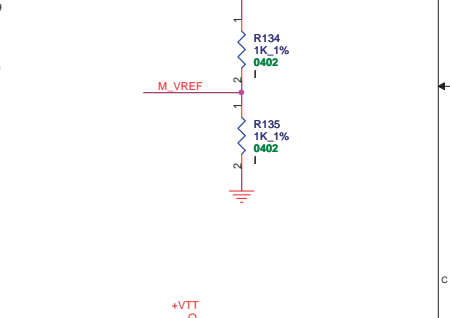
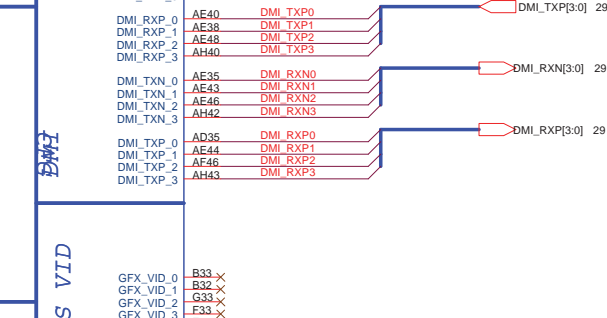
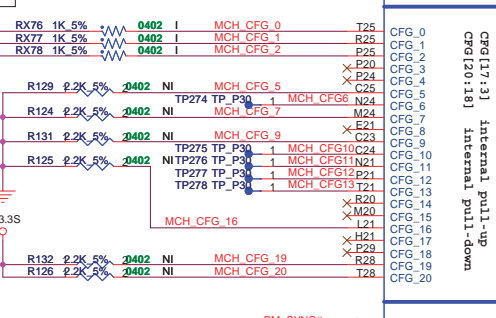
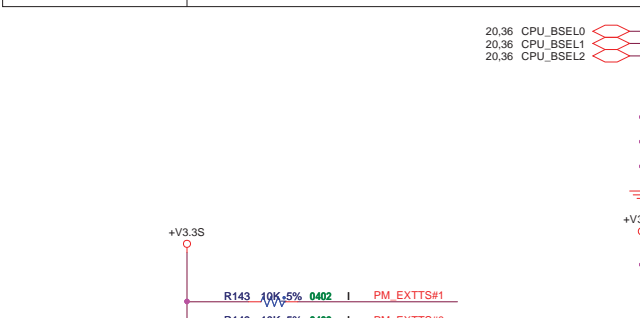
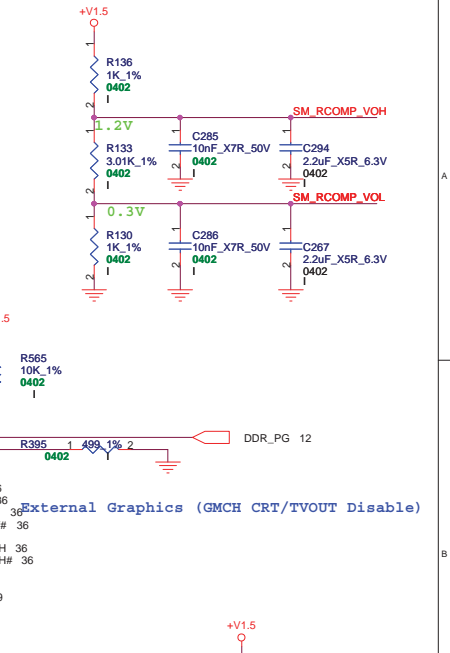
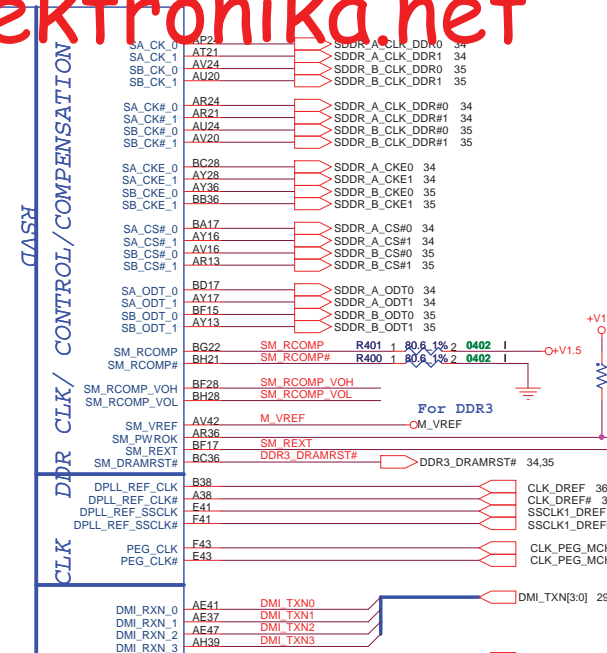
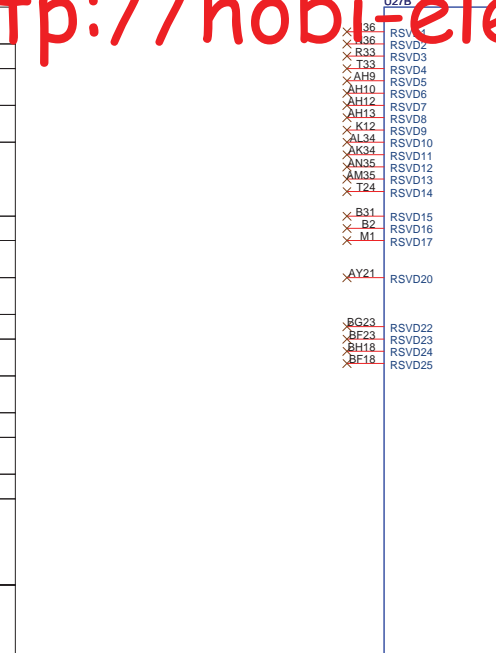
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Title: **Cantiga (HOST) 1/7**

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Custom	<b>TPN-F101/TPN-F102 Montevina</b>	

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MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low = The ITPM Host Interface is enabled High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Transport Layer Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Reverse Lane High = Normal operation (default)
MCH_CFG_10 PCIe Loopback enable	Low = Enabled High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode ([G]MCH->ICH): (3->0, 2-> 1, 1->2 and 0->3) DMI x2 mode ([G]MCH ->ICH): (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/ DP/iHDMI)	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port



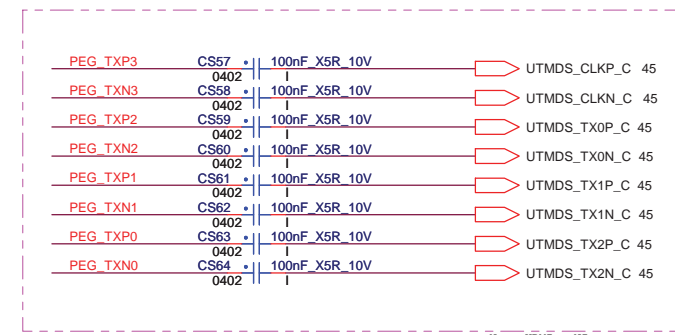
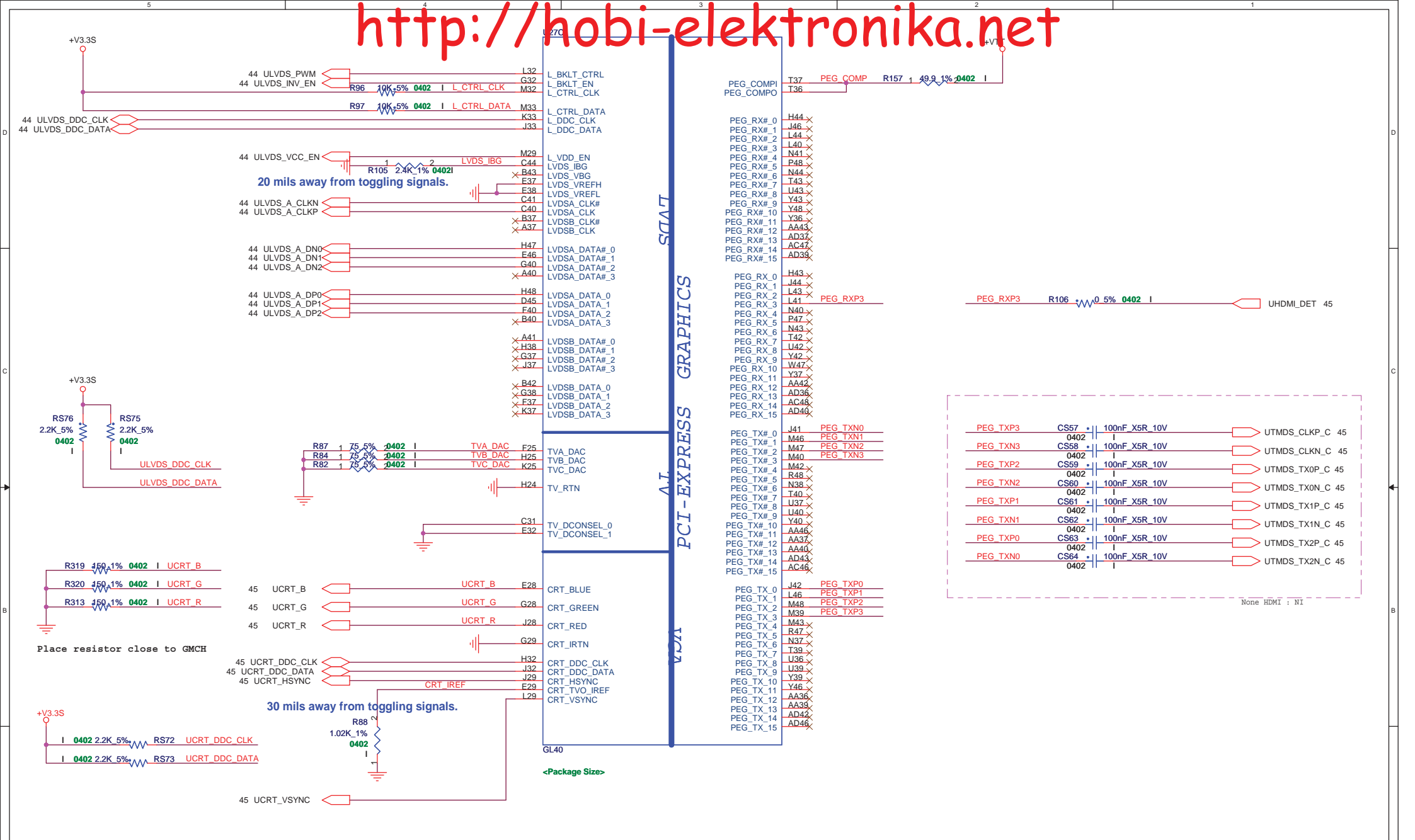
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Foxconn eMS Inc.  
HNBD R&D phone: +886-2-2799-6111

Title: **Cantiga (DMI) 2/7**

Size: Document Number  
Custom TPN-F101/TPN-F102 Montevina pl

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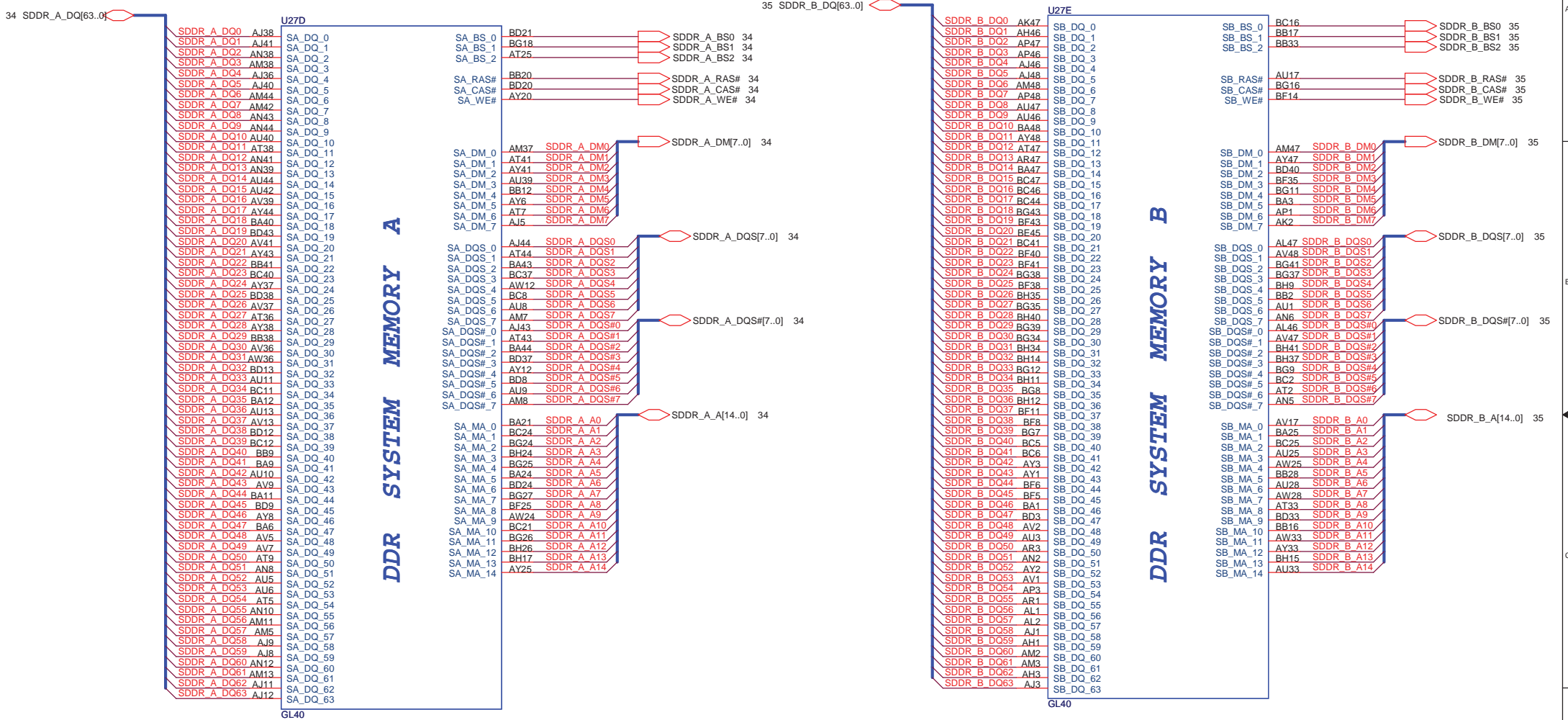
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 HNBD R&D phone: +886-2-2799-6111

Title: **Cantiga (GRAPHIC) 3/7**

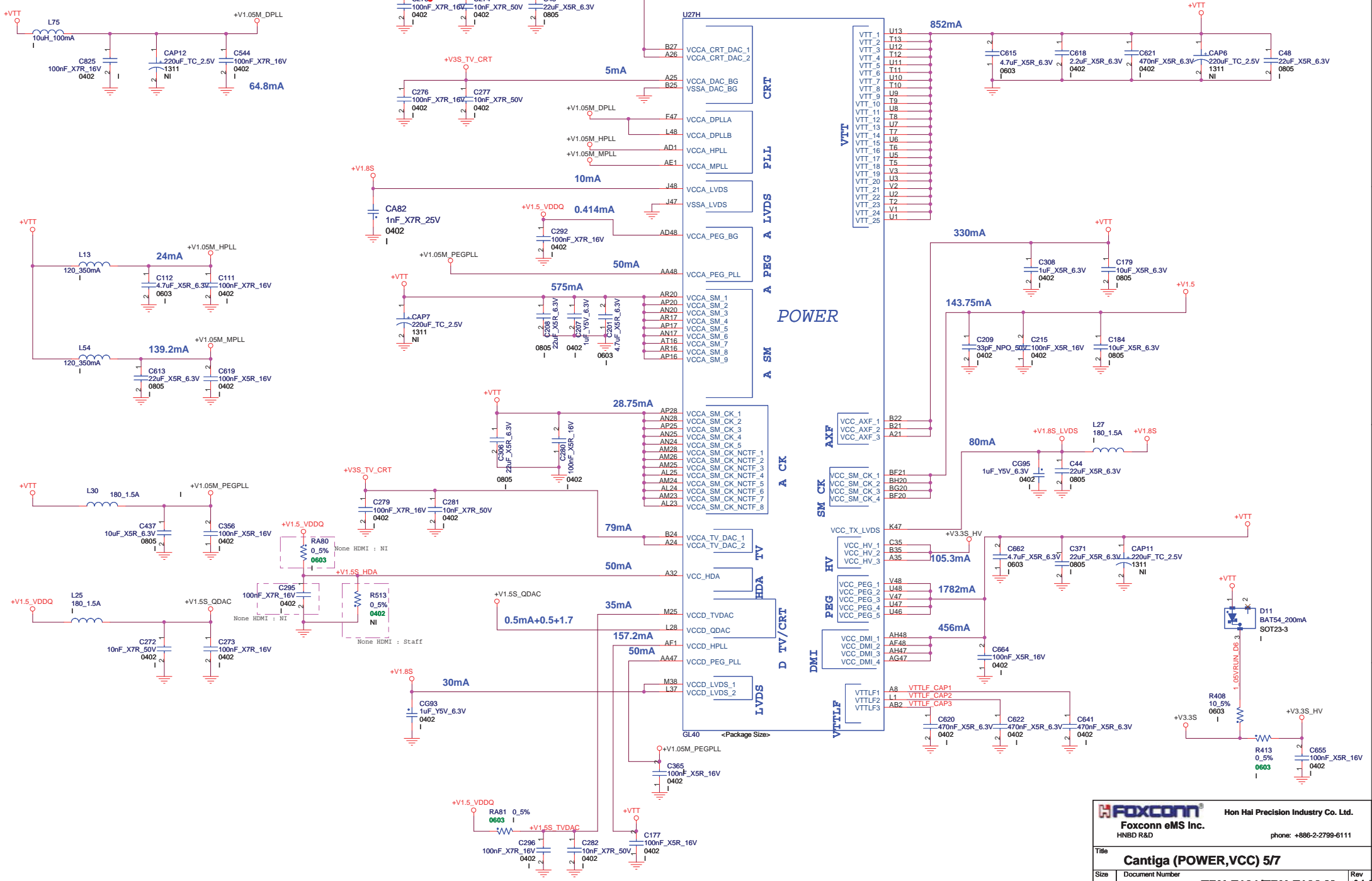
Size	Document Number	Rev
Custom	TPN-F101/TPN-F102 Montevina	

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Title			
Cantiga (DDR3) 4/7			
Size	Document Number	Rev	
Custom	TPN-F101/TPN-F102	Montevina	
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Title: **Cantiga (POWER,VCC) 5/7**

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 Custom **TPN-F101/TPN-F102** Montevina pl Rev

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A48	VSS_1	VSS_100	AM6	RG21	VSS_199	VSS_297	AH8
AR48	VSS_2	VSS_101	AE36	L12	VSS_200	VSS_298	Y8
AL48	VSS_3	VSS_102	AW21	AW21	VSS_201	VSS_299	L8
BB47	VSS_4	VSS_103	P36	AU21	VSS_202	VSS_300	E8
AW47	VSS_5	VSS_104	L36	AP21	VSS_203	VSS_301	B8
AN47	VSS_6	VSS_105	J36	AN21	VSS_204	VSS_302	AY7
AJ47	VSS_7	VSS_106	F36	AH21	VSS_205	VSS_303	AU7
AF47	VSS_8	VSS_107	AF21	E36	VSS_206	VSS_304	AN7
AD47	VSS_9	VSS_108	AH35	AB21	VSS_207	VSS_305	AJ7
AB47	VSS_10	VSS_109	AA35	R21	VSS_208	VSS_306	AE7
Y47	VSS_11	VSS_110	Y35	M21	VSS_209	VSS_307	AA7
T47	VSS_12	VSS_111	U35	J21	VSS_210	VSS_308	N7
N47	VSS_13	VSS_112	G21	T35	VSS_211	VSS_309	U7
L47	VSS_14	VSS_113	BF34	BC20	VSS_212	VSS_310	BG6
BD46	VSS_15	VSS_114	AM34	BA20	VSS_213	VSS_311	BD6
BA46	VSS_16	VSS_115	VSS_114	AW20	VSS_214	VSS_312	AV6
AY46	VSS_17	VSS_116	AJ34	AT20	VSS_215	VSS_313	AM6
AV46	VSS_18	VSS_117	AF34	AJ20	VSS_216	VSS_314	AT6
AR46	VSS_19	VSS_118	AE34	AG20	VSS_217	VSS_315	M6
AM46	VSS_20	VSS_119	W34	N20	VSS_218	VSS_316	C6
V46	VSS_21	VSS_120	B34	A44	VSS_219	VSS_317	BA5
H46	VSS_22	VSS_121	K20	N20	VSS_220	VSS_318	AH5
R46	VSS_23	VSS_122	BC33	F20	VSS_221	VSS_319	AD5
P46	VSS_24	VSS_123	BA33	C20	VSS_222	VSS_320	Y5
H46	VSS_25	VSS_124	AV33	A20	VSS_223	VSS_321	L5
F46	VSS_26	VSS_125	AR33	RG19	VSS_224	VSS_322	J5
BF44	VSS_27	VSS_126	AL33	A18	VSS_225	VSS_323	H5
AH44	VSS_28	VSS_127	AH33	BG17	VSS_226	VSS_324	F5
AD44	VSS_29	VSS_128	AB33	BC17	VSS_227	VSS_325	BE4
AA44	VSS_30	VSS_129	P33	AW17	VSS_228		
Y44	VSS_31	VSS_130	L33	AI17	VSS_229	VSS_327	BC3
U44	VSS_32	VSS_131	H33	R17	VSS_230	VSS_328	AV3
T44	VSS_33	VSS_132	N32	M17	VSS_231	VSS_329	AL3
M44	VSS_34	VSS_133	K32	H17	VSS_232	VSS_330	R3
F44	VSS_35	VSS_134	F32	C17	VSS_233	VSS_331	P3
BC43	VSS_36	VSS_135	C32		VSS_234	VSS_332	F3
AV43	VSS_37	VSS_136	A31	BA16	VSS_235	VSS_333	BA2
AJ43	VSS_38	VSS_137	AN29			VSS_334	AW2
AM43	VSS_39	VSS_138	T29	AL16	VSS_237	VSS_335	T2
J43	VSS_40	VSS_139	N29	AN16	VSS_238	VSS_336	AR2
C43	VSS_41	VSS_140	K29	N16	VSS_239	VSS_337	AP2
BG42	VSS_42	VSS_141	H29	K16	VSS_240	VSS_338	AJ2
AY42	VSS_43	VSS_142	E16	G16	VSS_241	VSS_339	AH2
AN42	VSS_44	VSS_143	BG28	A29	VSS_242	VSS_340	AF2
AJ42	VSS_45	VSS_144	BD28	BG15	VSS_243	VSS_341	AE2
AE42	VSS_46	VSS_145	BA28	AC15	VSS_244	VSS_342	AD2
N42	VSS_47	VSS_146	AV28	W15	VSS_245	VSS_343	AC2
L42	VSS_48	VSS_147	AT28	AI15	VSS_246	VSS_344	Y2
RD41	VSS_49	VSS_148	AR28	BG14	VSS_247	VSS_345	M2
AL41	VSS_50	VSS_149	AJ28	AA14	VSS_248	VSS_346	K2
AM41	VSS_51	VSS_150	AE28	C14	VSS_249	VSS_347	AM1
AH41	VSS_52	VSS_151	AB28	BG13	VSS_250	VSS_348	AA1
AD41	VSS_53	VSS_152	Y28	BC13	VSS_251	VSS_349	P1
AA41	VSS_54	VSS_153	P28	BA13	VSS_252	VSS_350	H1
Y41	VSS_55	VSS_154	H28			VSS_351	U24
U41	VSS_56	VSS_155	F28	AN13	VSS_255	VSS_352	U28
T41	VSS_57	VSS_156	C28	AL13	VSS_256	VSS_353	U25
M41	VSS_58	VSS_157	BF28	AE13	VSS_257	VSS_354	U29
G41	VSS_59	VSS_158	L13	N13	VSS_258		
B41	VSS_60	VSS_159	GH26	G13	VSS_259		
RG40	VSS_61	VSS_160	E13	E13	VSS_260	VSS_NCTF_1	AF32
BB40	VSS_62	VSS_161	AF26	AF12	VSS_261	VSS_NCTF_2	AB32
AV40	VSS_63	VSS_162	AB26	AV12	VSS_262	VSS_NCTF_3	V32
AN40	VSS_64	VSS_163	AA26	C26	VSS_263	VSS_NCTF_4	AJ30
H40	VSS_65	VSS_164	B26	AM12	VSS_264	VSS_NCTF_5	AM29
E40	VSS_66	VSS_165	BH25	AA12	VSS_265	VSS_NCTF_6	AF29
AT39	VSS_68	VSS_166	BD25	J12	VSS_266	VSS_NCTF_7	AB29
AM39	VSS_69	VSS_167	BB25	A12	VSS_267	VSS_NCTF_8	U26
AJ39	VSS_70	VSS_168	AV25	BD11	VSS_268	VSS_NCTF_9	U23
AE39	VSS_71	VSS_169	AR25	BB11	VSS_269	VSS_NCTF_10	AL20
N39	VSS_72	VSS_170	AJ25	AY11	VSS_270	VSS_NCTF_11	V20
L39	VSS_73	VSS_171	AC25	AN11	VSS_271	VSS_NCTF_12	AC19
B39	VSS_74	VSS_172	Y25	AH11	VSS_272	VSS_NCTF_13	AL17
BH38	VSS_75	VSS_173	N25		VSS_273	VSS_NCTF_14	AJ17
BC38	VSS_76	VSS_174	L25	Y11	VSS_275	VSS_NCTF_15	AA17
BA38	VSS_77	VSS_175	J25	N11	VSS_276	VSS_NCTF_16	U17
AJ38	VSS_78	VSS_176	G25	G11	VSS_277		
AH38	VSS_79	VSS_177	E25	C11	VSS_278		
AD38	VSS_80	VSS_178	BF24	BG10	VSS_279	VSS_SCB_1	BH48
AA38	VSS_81	VSS_179	AD12	AV10	VSS_280	VSS_SCB_2	BH1
Y38	VSS_82	VSS_180	AY24	AJ10	VSS_281	VSS_SCB_3	A48
U38	VSS_83	VSS_181	AT24	AE10	VSS_282	VSS_SCB_4	C1
T38	VSS_84	VSS_182	AJ24	AA10	VSS_283	VSS_SCB_5	A3
J38	VSS_85	VSS_183	AH24		VSS_284		
F38	VSS_86	VSS_184	AF24	M10	VSS_285	NC_26	E1
C38	VSS_87	VSS_185	AB24	BF9	VSS_286	NC_27	D2
BF37	VSS_88	VSS_186	R24	BC9	VSS_287	NC_28	C3
BB37	VSS_89	VSS_187	L24	AN9	VSS_288	NC_29	B4
AW37	VSS_90	VSS_188	K24	AM9	VSS_289	NC_30	A5
AT37	VSS_91	VSS_189	J24	AD9	VSS_290	NC_31	A6
AN37	VSS_92	VSS_190	G24	G9	VSS_291	NC_32	A4
AJ37	VSS_93	VSS_191	F24	B9	VSS_292	NC_33	A4
H37	VSS_94	VSS_192	E24	BH8	VSS_293	NC_34	B45
C37	VSS_95	VSS_193	BH23	BB8	VSS_294	NC_35	C46
PG36	VSS_96	VSS_194	AV8	AG23	VSS_295	NC_36	D47
BD36	VSS_97	VSS_195	Y23	ATR	VSS_296	NC_37	A46
AK15	VSS_98	VSS_196	B23			NC_38	A46
AU36	VSS_99	VSS_197	A23			NC_39	F48
		VSS_198	AJ6			NC_40	E48
		VSS_199				NC_41	C48
						NC_42	B48

VSS

VSS

VSS NCTF

VSS SCB

NC

GL40

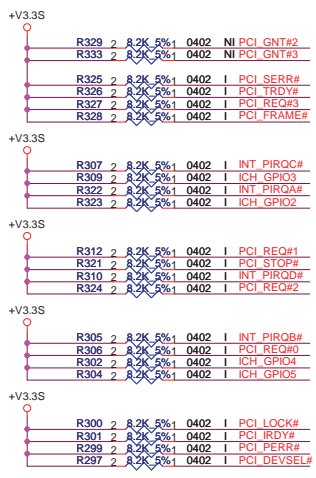
GL40

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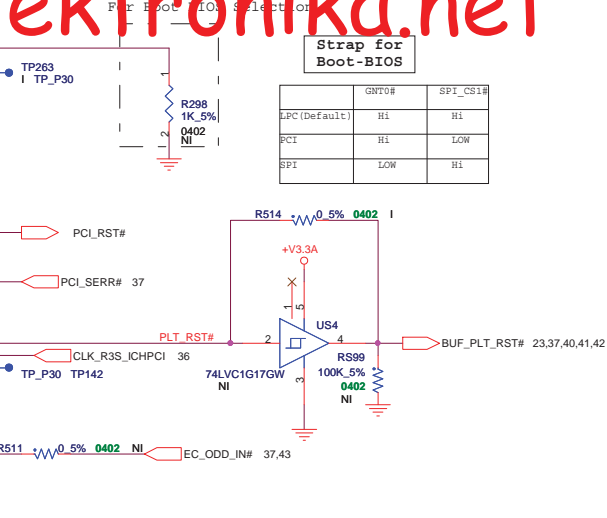
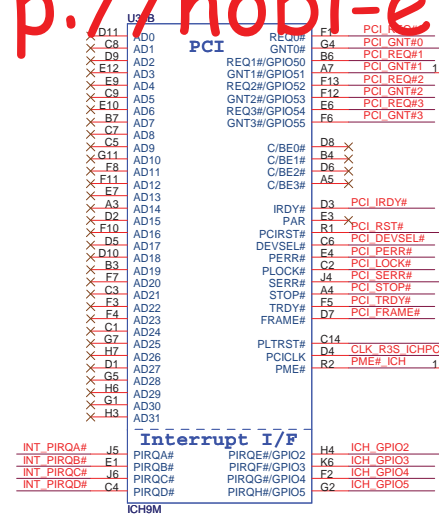
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 Custom **TPN-F101/TPN-F102 Montevina pl**

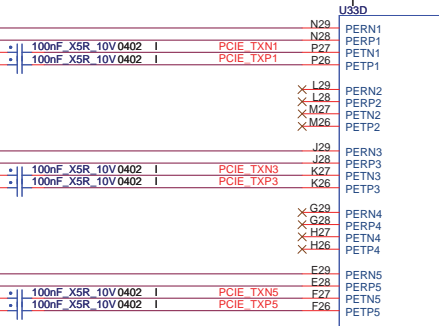
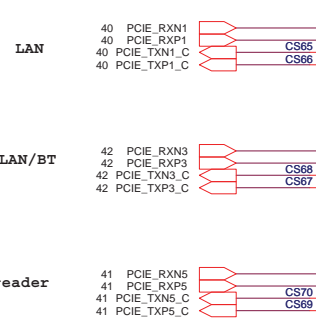
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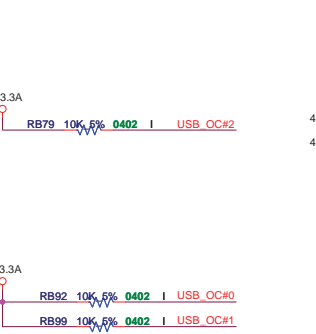
PCI Pullups



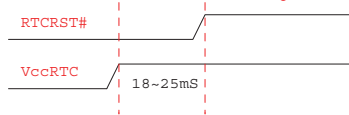
USB PORT	Function	OC pin
PORT-0	Ext. USB 0	
PORT-1	Ext. USB 1	
PORT-2	Ext. USB 2	
PORT-3		
PORT-4		
PORT-5		
PORT-6		
PORT-7		
PORT-8		
PORT-9		
PORT-10	Camera	
PORT-11	WLAN/BT	
PORT-12		
PORT-13		



Place within 500 mils of ICH

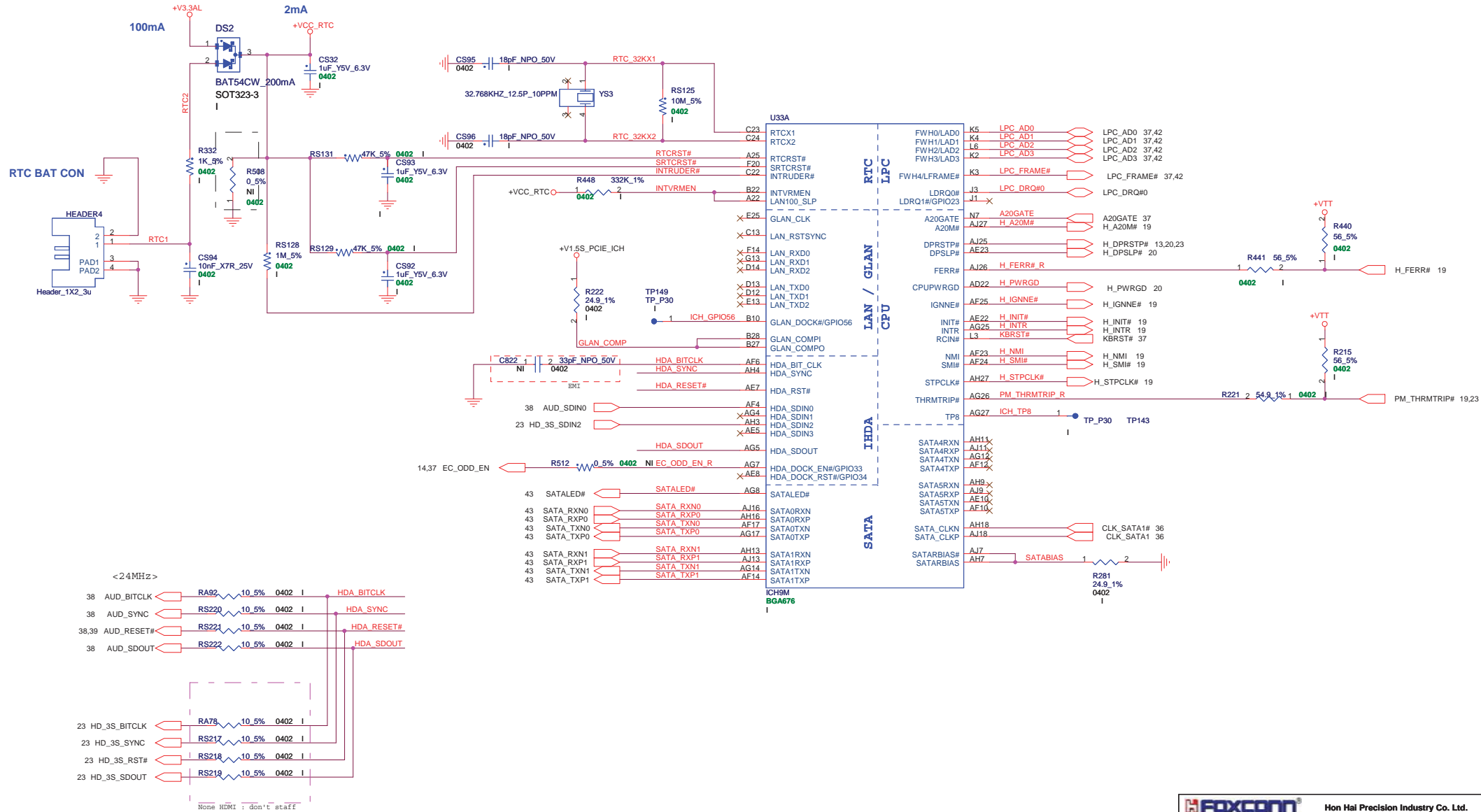


Place within 500 mils of ICH and don't routing next to high speed signals

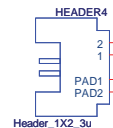


Internal VRM enabled for VccSui1\_05, VccSui1\_5, VccCl1\_5, VccLAN1\_05 and VccCl1\_05

INTVRMEN	Low= Internal VR Disabled High= Internal VR Enabled(Default)
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RTC BAT CON



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Title: <b>ICH9-M (LPC,IDE,SATA) 2/5</b>			
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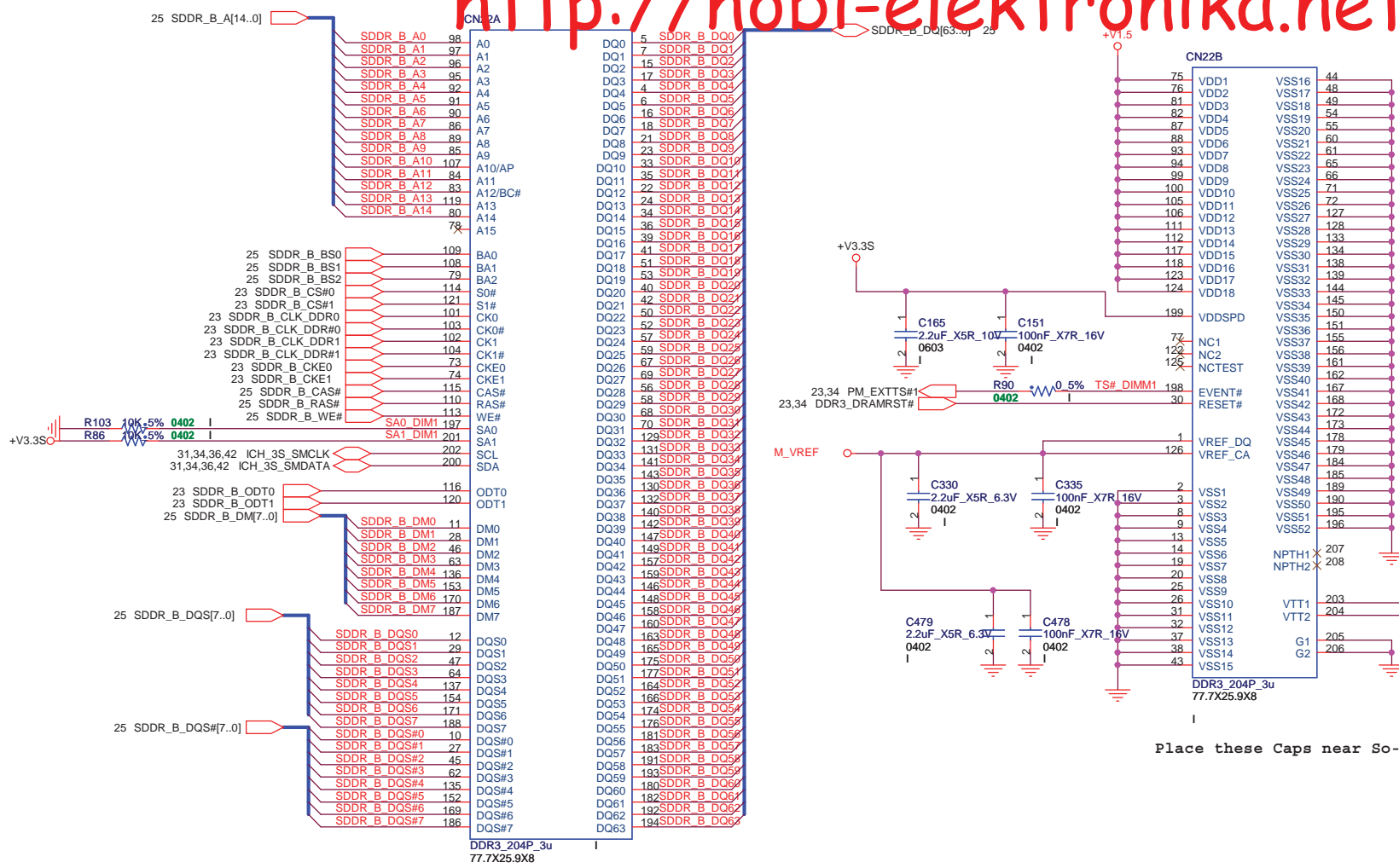


AA26	VSS(00)	VSS(07)	H5
AA27	VSS(002)	VSS(08)	J23
AA3	VSS(003)	VSS(09)	J26
AA6	VSS(004)	VSS(10)	J27
AB1	VSS(005)	VSS(11)	AC22
AA23	VSS(006)	VSS(12)	K28
AB28	VSS(007)	VSS(13)	K29
AB29	VSS(008)	VSS(14)	L13
AB4	VSS(009)	VSS(15)	L15
AB5	VSS(010)	VSS(16)	L2
AC17	VSS(011)	VSS(17)	L26
AC26	VSS(012)	VSS(18)	L27
AC27	VSS(013)	VSS(19)	L5
AC3	VSS(014)	VSS(20)	L7
AD1	VSS(015)	VSS(21)	M12
AD10	VSS(016)	VSS(22)	M13
AD12	VSS(017)	VSS(23)	M14
AD13	VSS(018)	VSS(24)	M15
AD14	VSS(019)	VSS(25)	M16
AD17	VSS(020)	VSS(26)	M17
AD18	VSS(021)	VSS(27)	M23
AD21	VSS(022)	VSS(28)	M28
AD28	VSS(023)	VSS(29)	M29
AD29	VSS(024)	VSS(30)	N11
AD4	VSS(025)	VSS(31)	N12
AD5	VSS(026)	VSS(32)	N13
AD6	VSS(027)	VSS(33)	N14
AD7	VSS(028)	VSS(34)	N15
AD9	VSS(029)	VSS(35)	N16
AE12	VSS(030)	VSS(36)	N17
AE13	VSS(031)	VSS(37)	N18
AE14	VSS(032)	VSS(38)	N26
AE16	VSS(033)	VSS(39)	N27
AE17	VSS(034)	VSS(40)	P12
AE2	VSS(035)	VSS(41)	P13
AE20	VSS(036)	VSS(42)	P14
AE24	VSS(037)	VSS(43)	P15
AE3	VSS(038)	VSS(44)	P16
AE4	VSS(039)	VSS(45)	P17
AE6	VSS(040)	VSS(46)	P2
AE9	VSS(041)	VSS(47)	P23
AF13	VSS(042)	VSS(48)	P28
AF16	VSS(043)	VSS(49)	P29
AF18	VSS(044)	VSS(50)	P4
AF22	VSS(045)	VSS(51)	P7
AH26	VSS(046)	VSS(52)	R11
AF26	VSS(047)	VSS(53)	R12
AF27	VSS(048)	VSS(54)	R13
AF5	VSS(049)	VSS(55)	R14
AF7	VSS(050)	VSS(56)	R15
AF9	VSS(051)	VSS(57)	R16
AG13	VSS(052)	VSS(58)	R17
AG16	VSS(053)	VSS(59)	R18
AG18	VSS(054)	VSS(60)	R28
AG20	VSS(055)	VSS(61)	T12
AG23	VSS(056)	VSS(62)	T13
AG3	VSS(057)	VSS(63)	T14
AG6	VSS(058)	VSS(64)	T15
AG9	VSS(059)	VSS(65)	T16
AH14	VSS(060)	VSS(66)	T17
AH17	VSS(061)	VSS(67)	T23
AH19	VSS(062)	VSS(68)	B26
AH2	VSS(063)	VSS(69)	U12
AH22	VSS(064)	VSS(70)	U13
AH25	VSS(065)	VSS(71)	U14
AH28	VSS(066)	VSS(72)	U15
AH5	VSS(067)	VSS(73)	U16
AH8	VSS(068)	VSS(74)	U17
AJ12	VSS(069)	VSS(75)	AD23
AJ14	VSS(070)	VSS(76)	U26
AJ17	VSS(071)	VSS(77)	U27
AJ8	VSS(072)	VSS(78)	U3
B11	VSS(073)	VSS(79)	V1
B14	VSS(074)	VSS(80)	V13
B17	VSS(075)	VSS(81)	V15
B2	VSS(076)	VSS(82)	V23
B20	VSS(077)	VSS(83)	V28
B23	VSS(078)	VSS(84)	V29
B5	VSS(079)	VSS(85)	V4
B8	VSS(080)	VSS(86)	V5
C26	VSS(081)	VSS(87)	W26
C27	VSS(082)	VSS(88)	W27
E11	VSS(083)	VSS(89)	W3
E14	VSS(084)	VSS(90)	Y1
E18	VSS(085)	VSS(91)	Y28
E2	VSS(086)	VSS(92)	Y29
E21	VSS(087)	VSS(93)	Y4
E24	VSS(088)	VSS(94)	Y5
E5	VSS(089)	VSS(95)	AG28
E8	VSS(090)	VSS(96)	AH6
F16	VSS(091)	VSS(97)	AF2
F28	VSS(092)	VSS(98)	B25
F29	VSS(093)	VSS_NCTF(01)	A1
G12	VSS(094)	VSS_NCTF(02)	A2
G14	VSS(095)	VSS_NCTF(03)	A28
G18	VSS(096)	VSS_NCTF(04)	A29
G21	VSS(097)	VSS_NCTF(05)	AH1
G24	VSS(098)	VSS_NCTF(06)	AH29
G26	VSS(099)	VSS_NCTF(07)	AJ1
G27	VSS(100)	VSS_NCTF(08)	AJ2
G8	VSS(101)	VSS_NCTF(09)	AJ28
H2	VSS(102)	VSS_NCTF(10)	AJ29
H23	VSS(103)	VSS_NCTF(11)	B1
H28	VSS(104)	VSS_NCTF(12)	B29
H29	VSS(105)		
	VSS(106)		

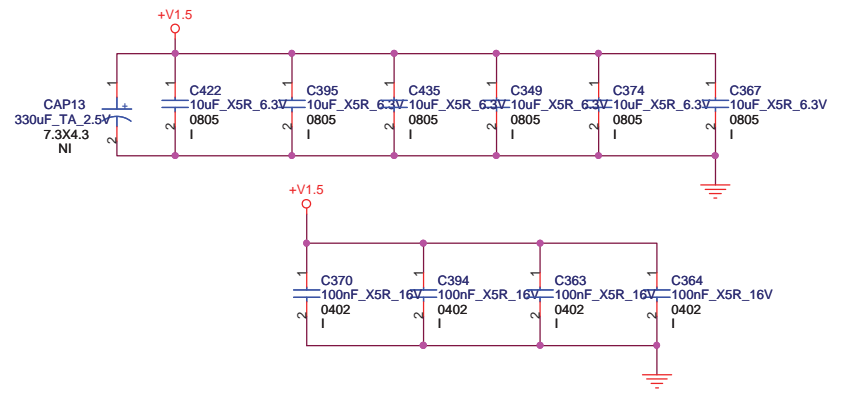
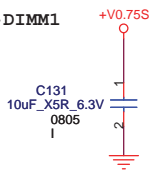
ICH9M

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		phone: +886-2-2799-6111	
Title: ICH9-M ( GND) 5/5			
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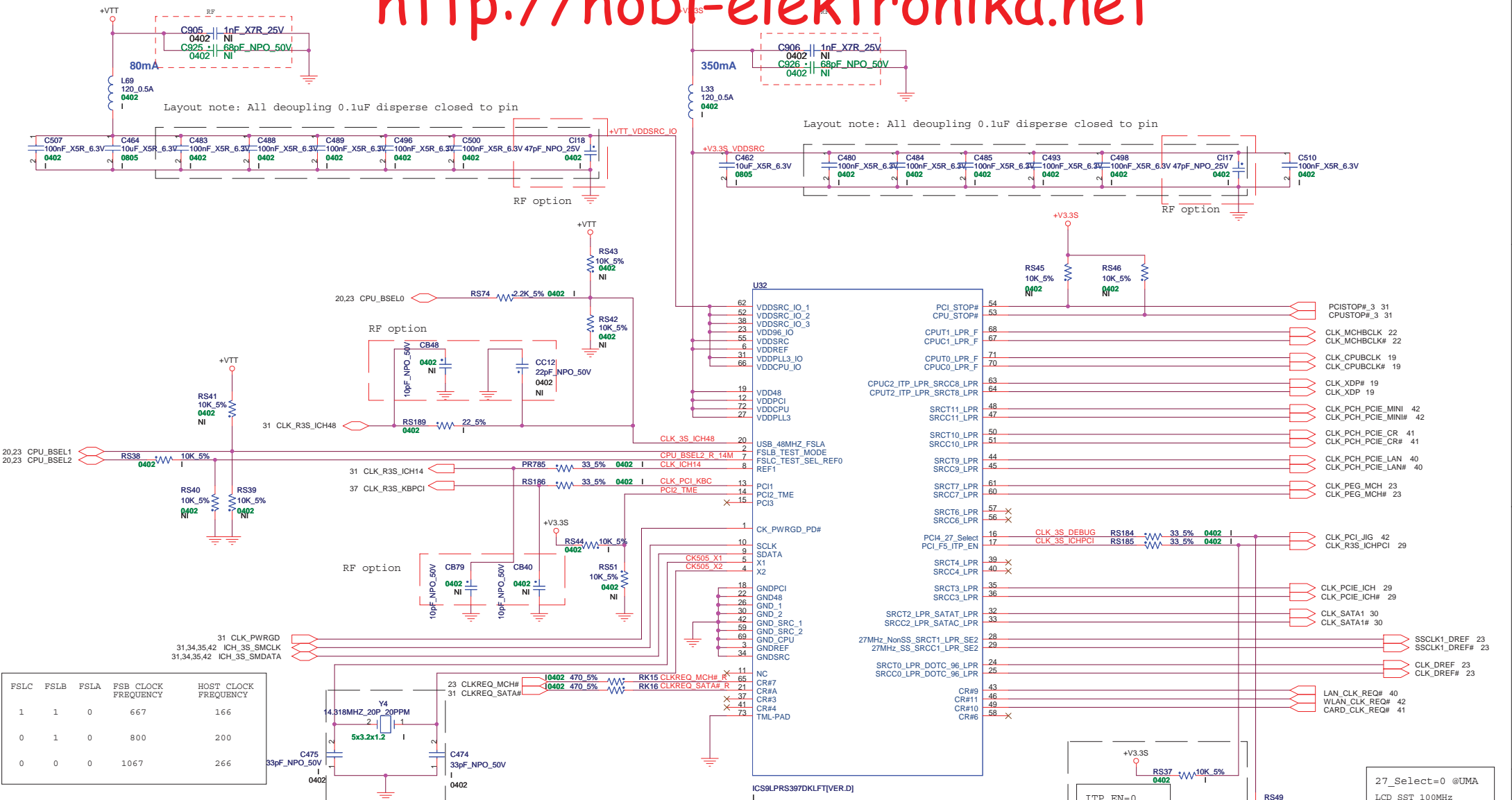
Place these Caps near So-DIMM1



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 Foxconn eMS Inc.  
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Title: **DDR3 SO-DIMM\_1**

Size	Document Number	Rev
Custom	<b>TPN-F101/TPN-F102 Montevina</b>	
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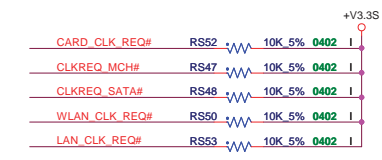


FSLC	FSLB	FSLA	FSB	CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166	
0	1	0	800	200	
0	0	0	1067	266	

\*CLKREQ# pin controls SRC Table.

CR#_A	Byte5:bit7=0, disable CR#_A; 1 enable CR#_A	CR#_3	Byte5:bit5=0 (PWD), disable CR#3; 1, enable CR#_3
CR#_4	Byte5:bit6=0 (PWD)	CR#_6	Byte5:bit3=0 (PWD), disable CR#6; 1, enable CR#6
	SRC0		SRC2
CR#_4	Byte5:bit4=0 (PWD), disable CR#4; 1, enable CR#4	CR#_6	Byte5:bit3=0 (PWD), disable CR#6; 1, enable CR#6
	SRC4		SRC6

CR#_7	Byte5:bit2=0 (PWD), disable CR#7; 1, enable CR#7
SRC7	
CR#_9	Byte5:bit1=0 (PWD), disable CR#9; 1, enable CR#9
SRC9	
CR#_10	Byte5:bit0=0 (PWD), disable CR#10; 1, enable CR#10
SRC10	
CR#_11	Byte6:bit7=0 (PWD), disable CR#11; 1, enable CR#11
SRC11	



27\_Select=0 @UMA  
LCD\_SST 100MHz  
27\_Select=1 @DIS  
27Mhz non-spread clock

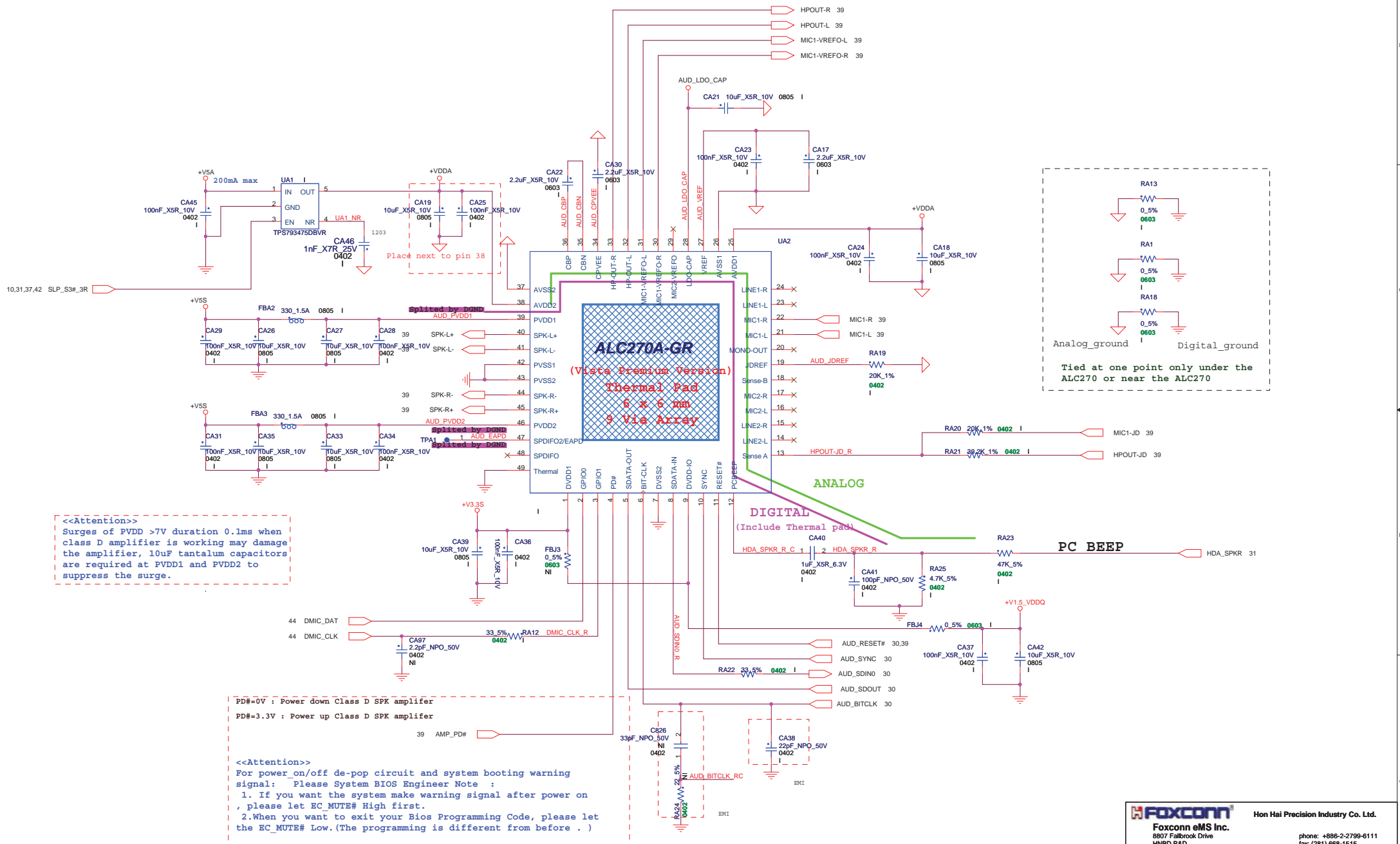
**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
Foxconn eMS Inc.  
HNBD R&D phone: +886-2-2799-6111

Title: **CLOCK GEN**

Size: Document Number: **TPN-F101/TPN-F102** Rev: **Montevina pl**

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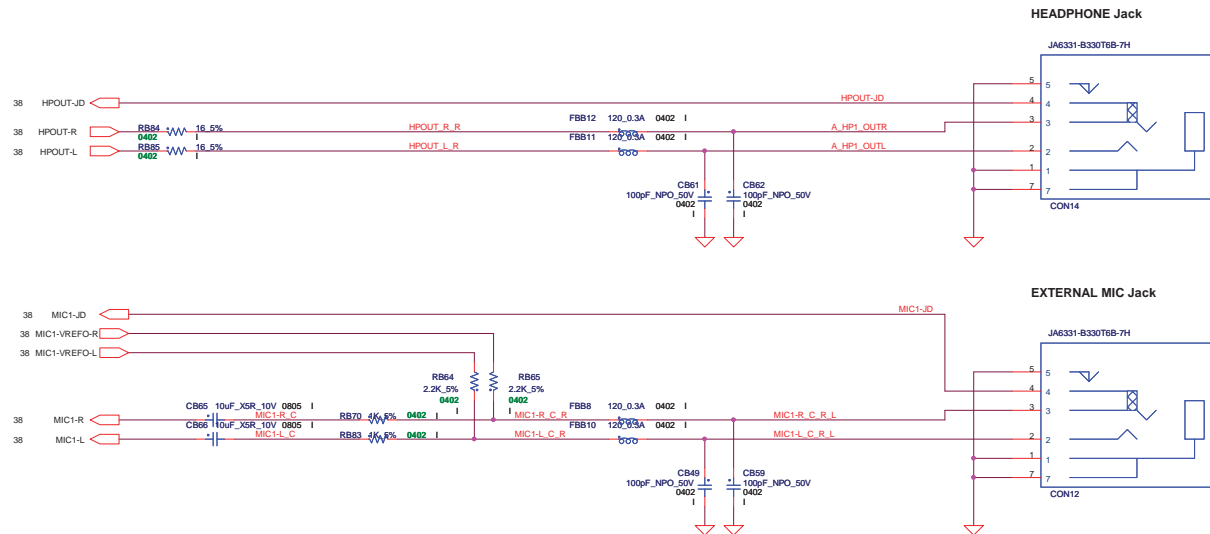
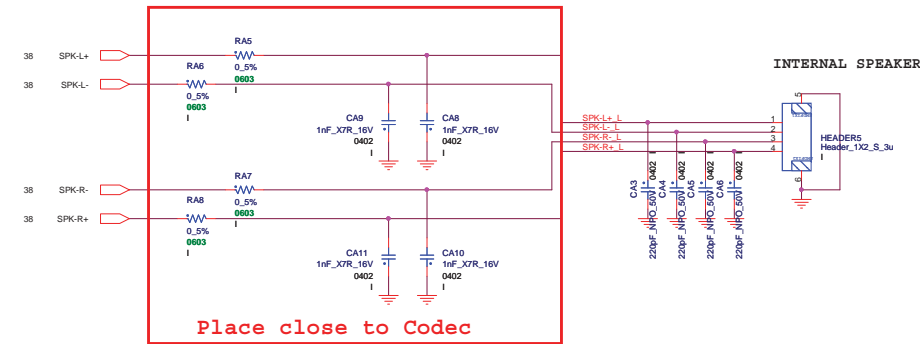
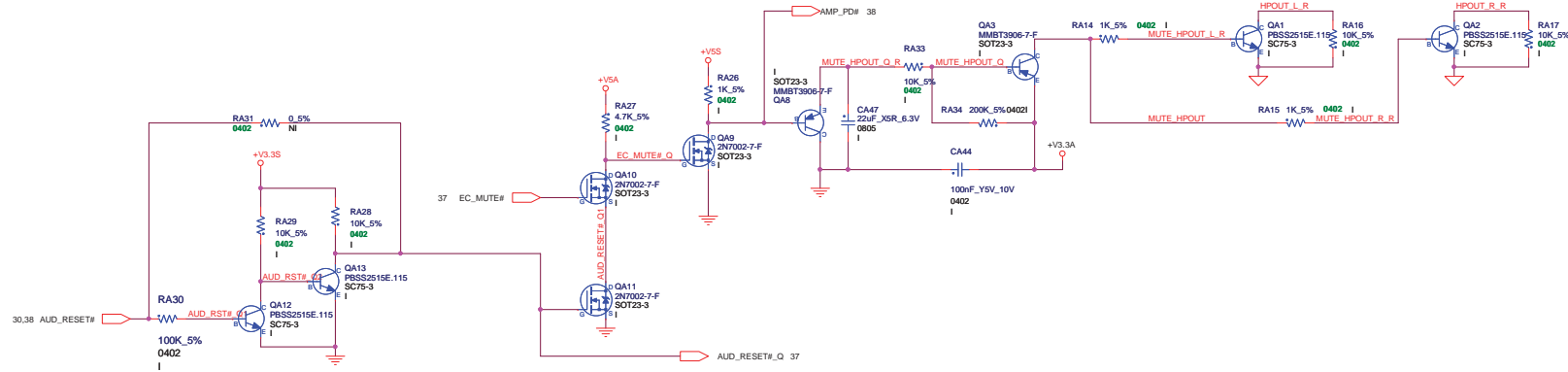
<<Attention>>  
 Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

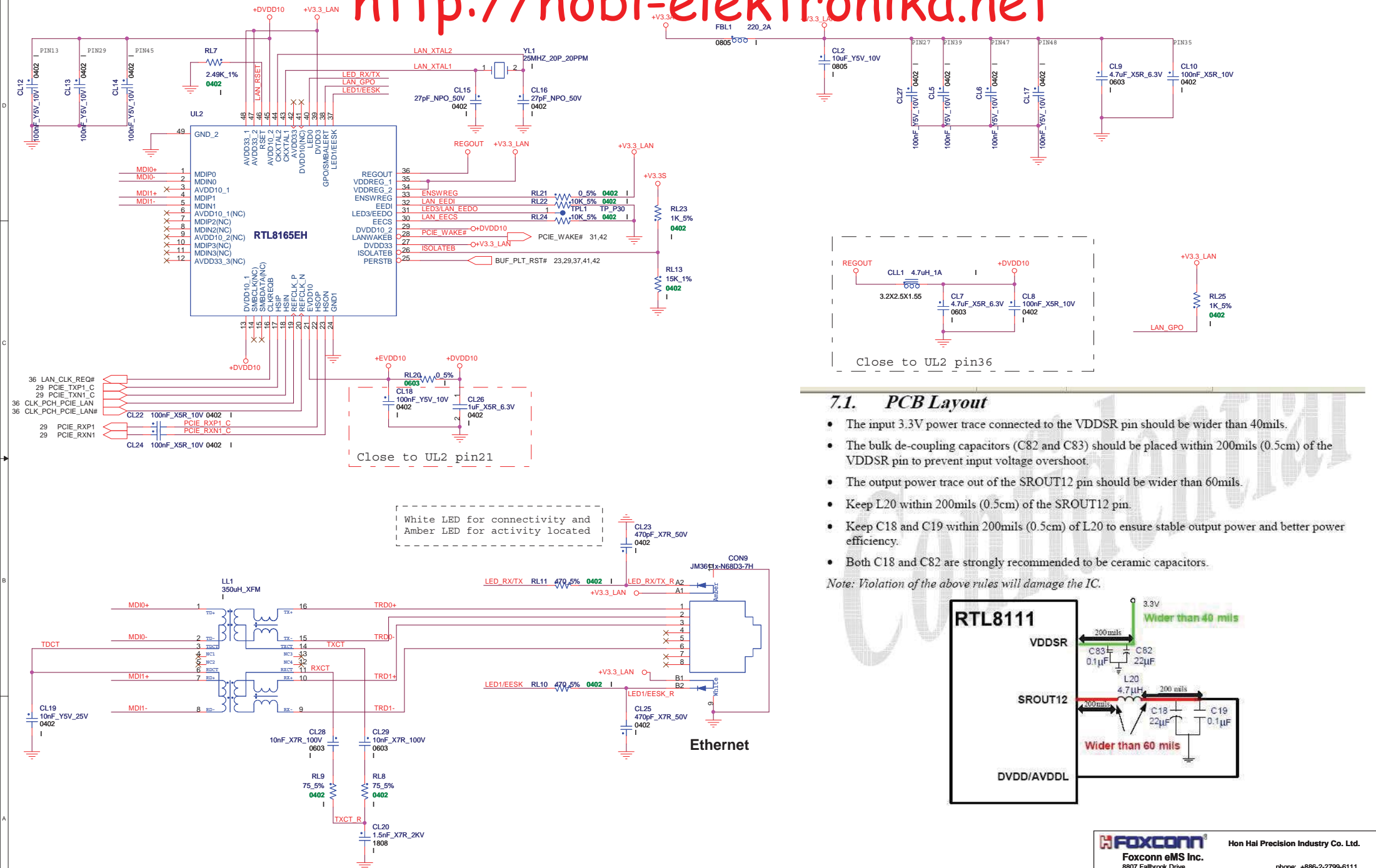
PD#=0V : Power down Class D SPK amplifier  
 PD#=3.3V : Power up Class D SPK amplifier

<<Attention>>  
 For power on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :  
 1. If you want the system make warning signal after power on , please let EC MUTE# High first.  
 2. When you want to exit your Bios Programming Code, please let the EC MUTE# Low. (The programming is different from before .)



Mute

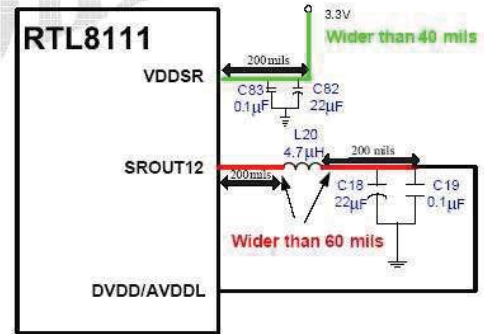




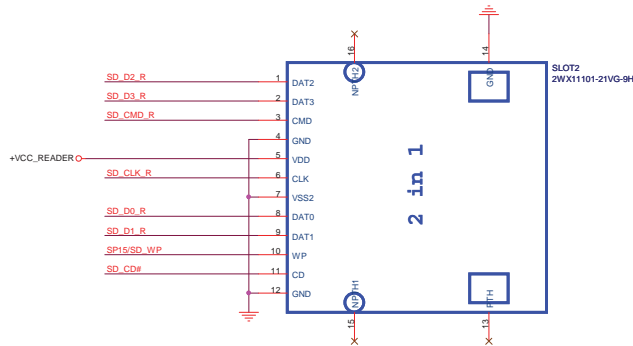
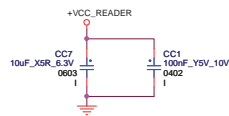
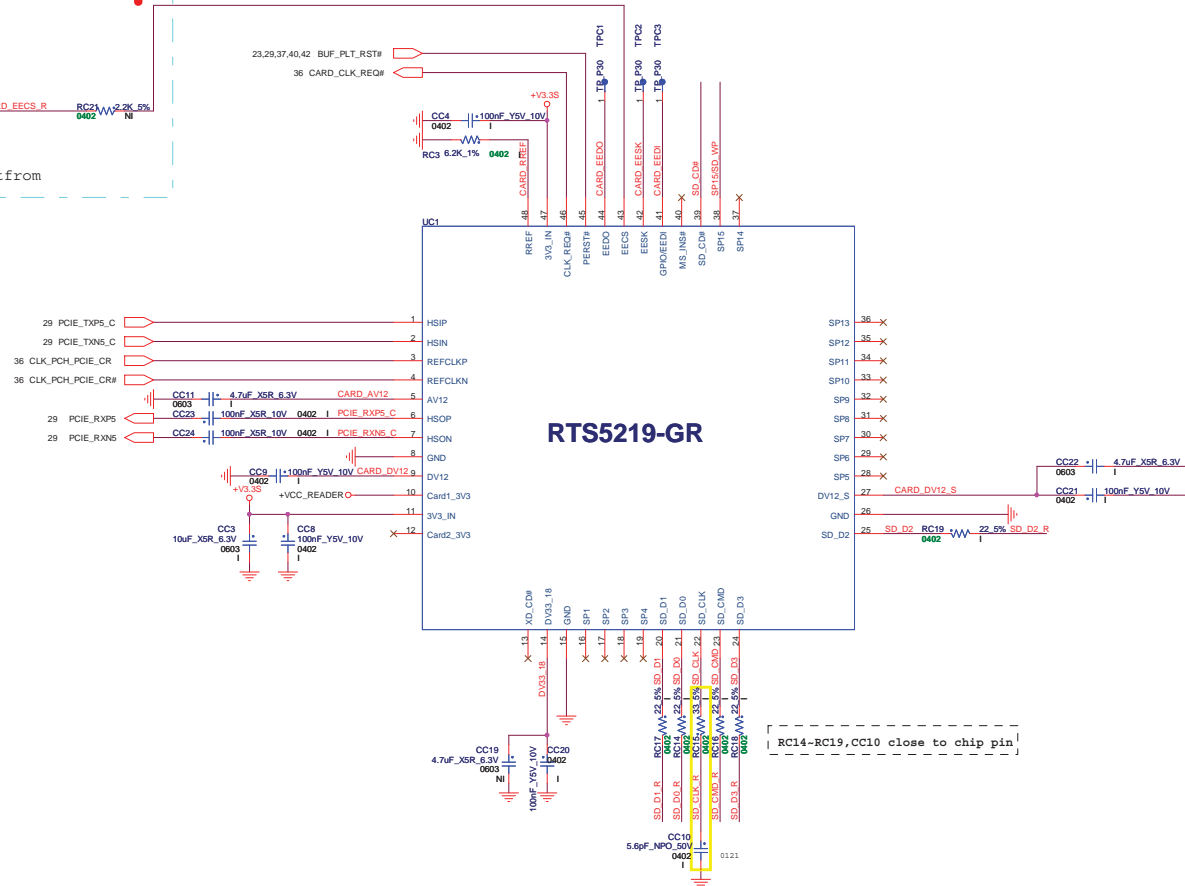
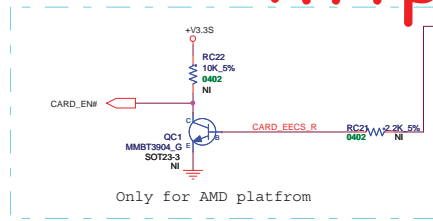
## 7.1. PCB Layout

- The input 3.3V power trace connected to the VDDSR pin should be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200mils (0.5cm) of the VDDSR pin to prevent input voltage overshoot.
- The output power trace out of the SROUT12 pin should be wider than 60mils.
- Keep L20 within 200mils (0.5cm) of the SROUT12 pin.
- Keep C18 and C19 within 200mils (0.5cm) of L20 to ensure stable output power and better power efficiency.
- Both C18 and C82 are strongly recommended to be ceramic capacitors.

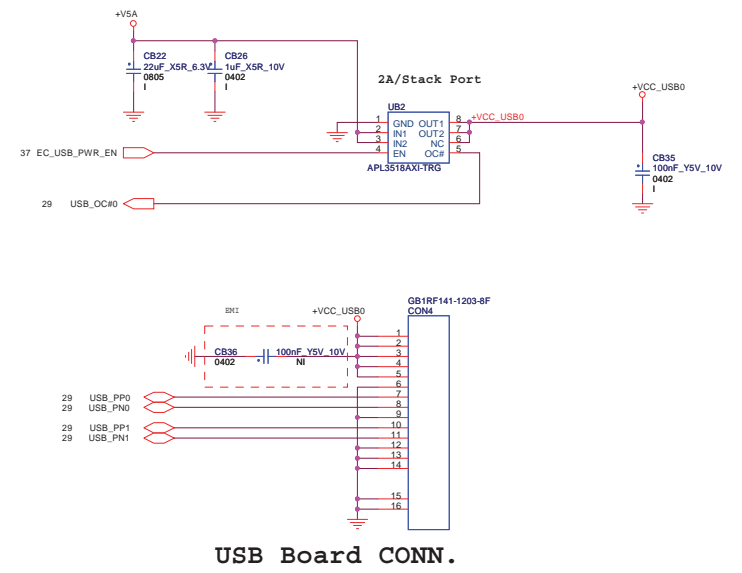
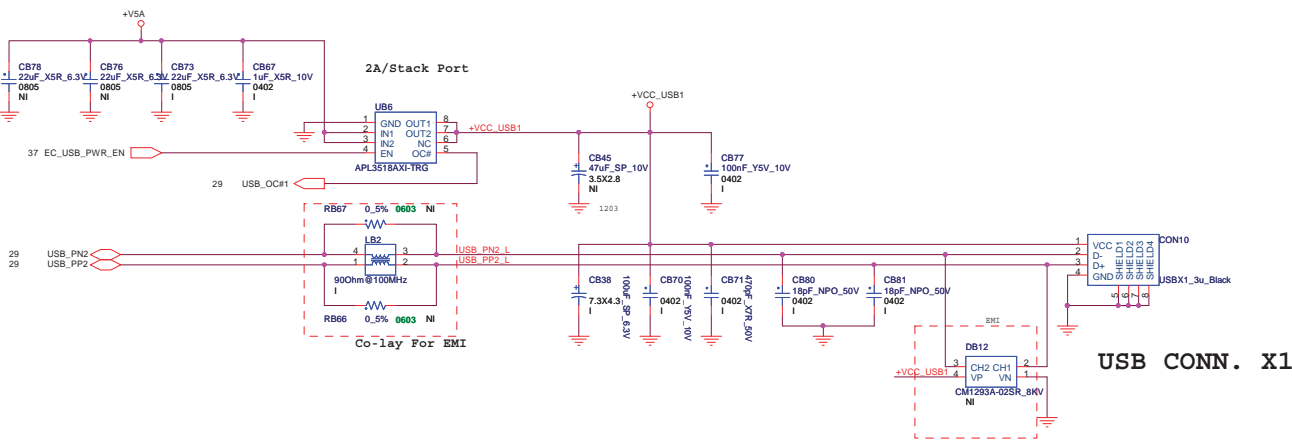
Note: Violation of the above rules will damage the IC.



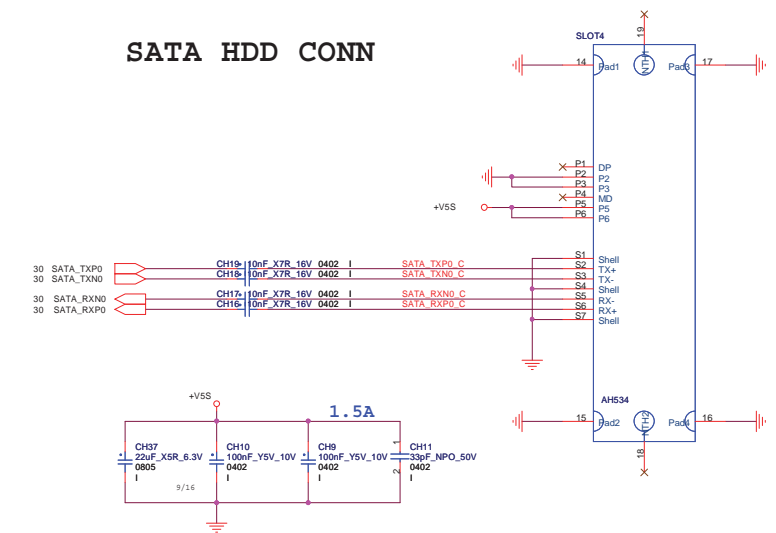




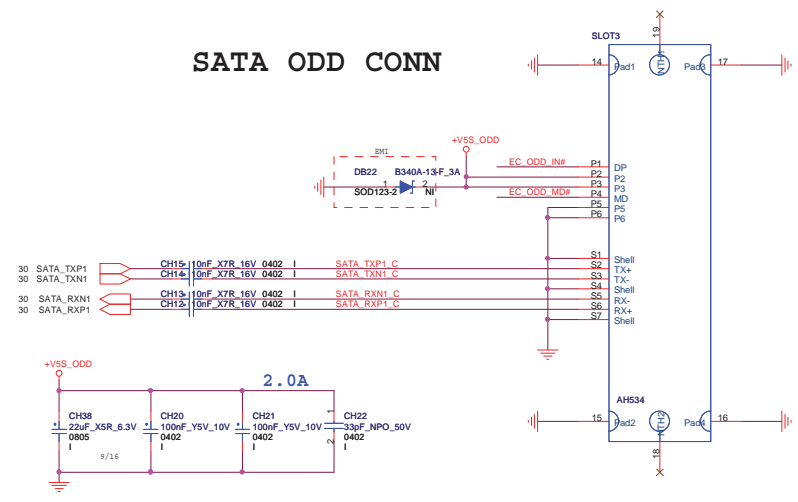




## SATA HDD CONN

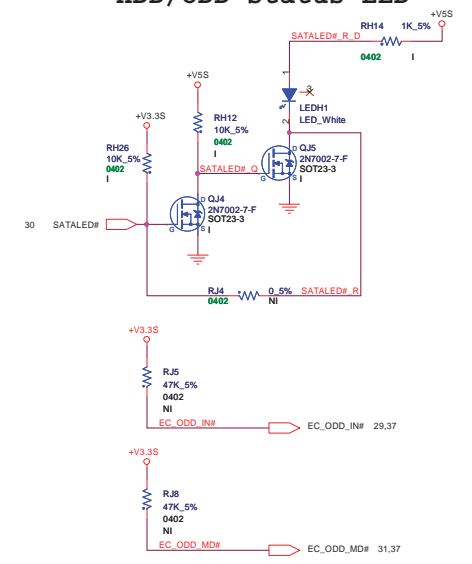


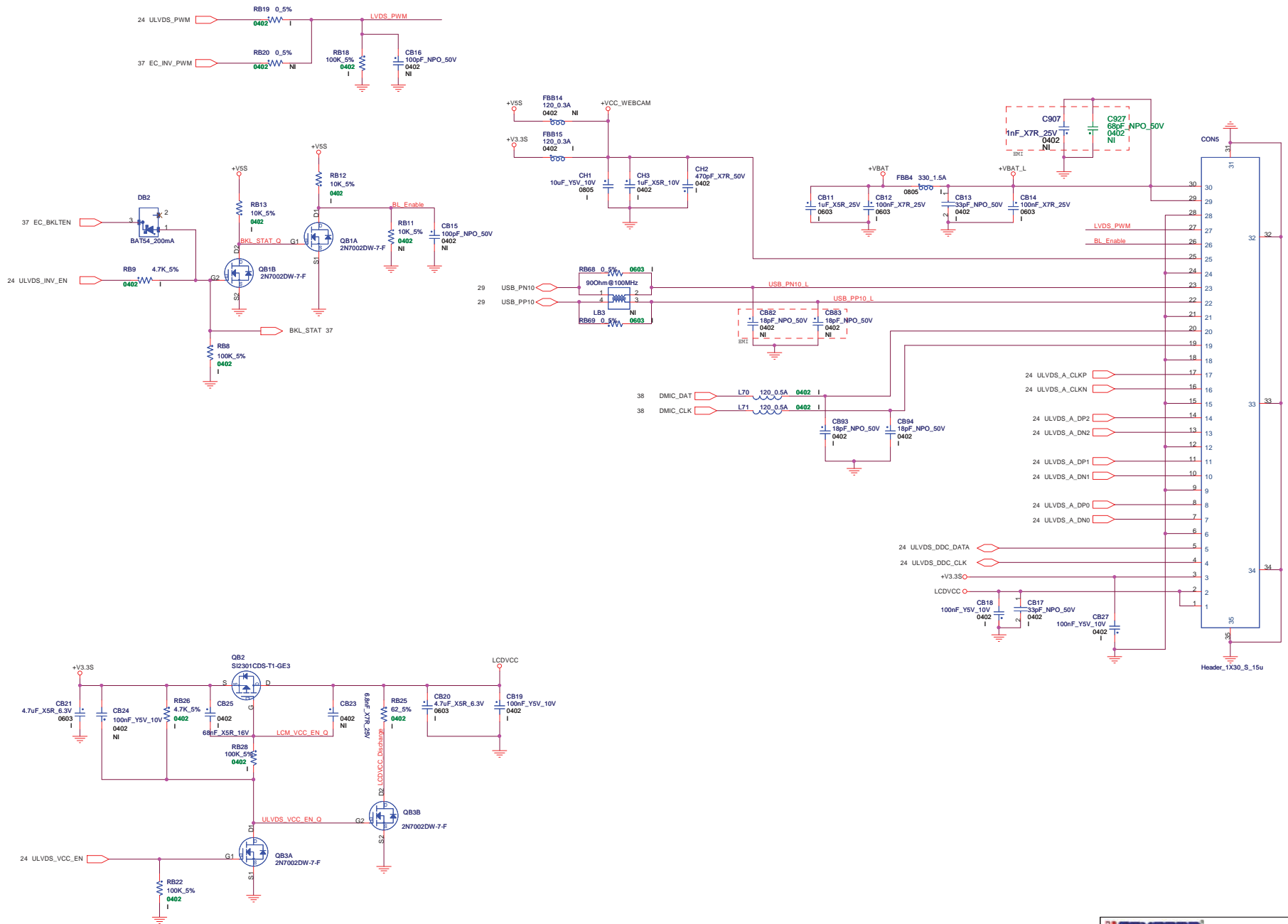
## SATA ODD CONN

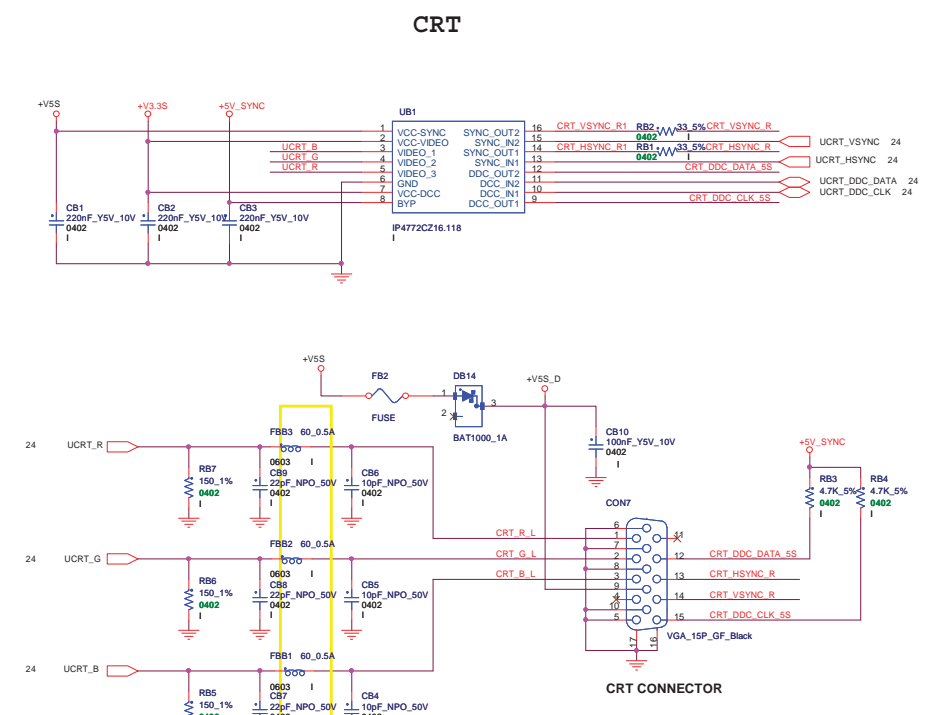
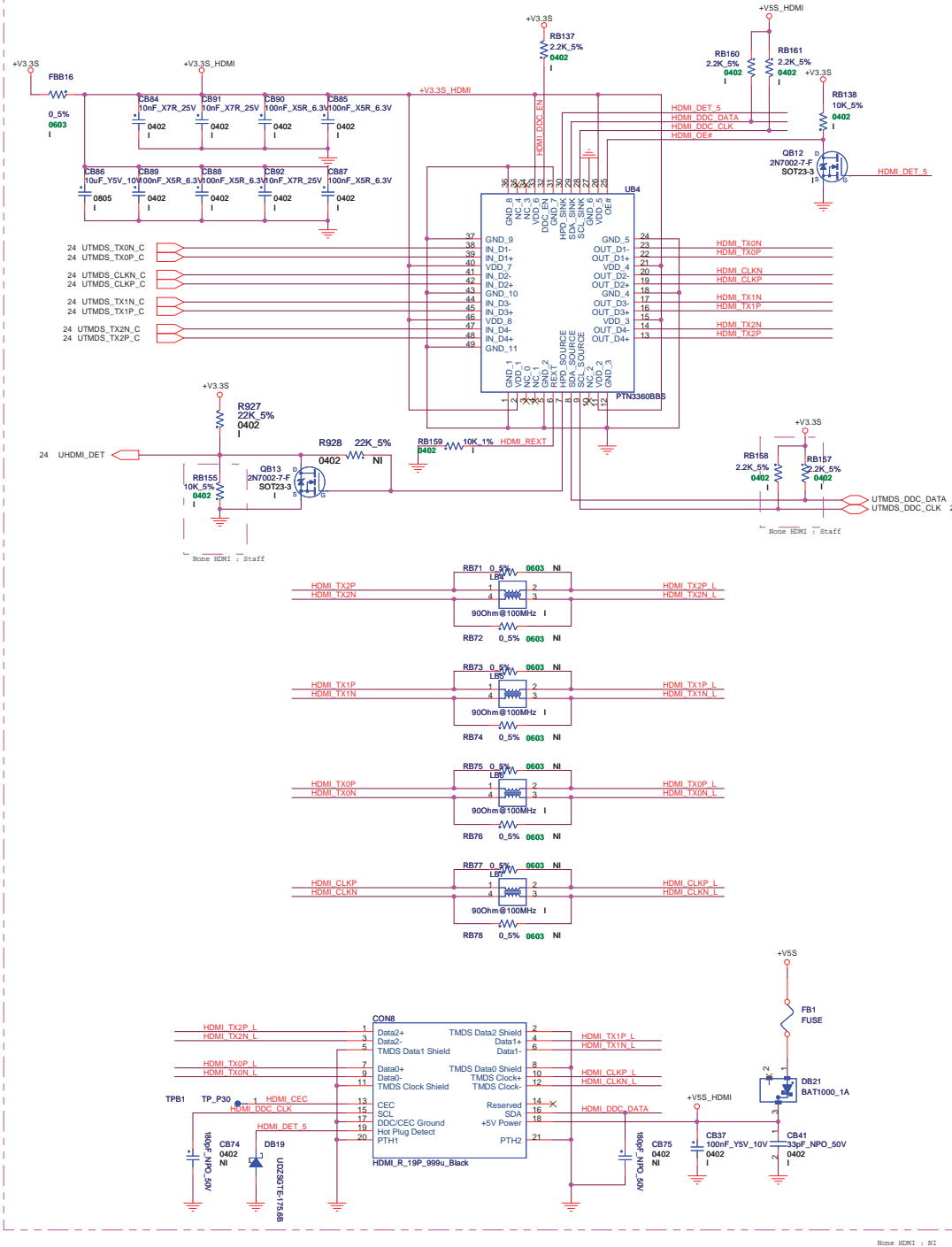


Power pin current  
max. 1300 mA (less 2ms)

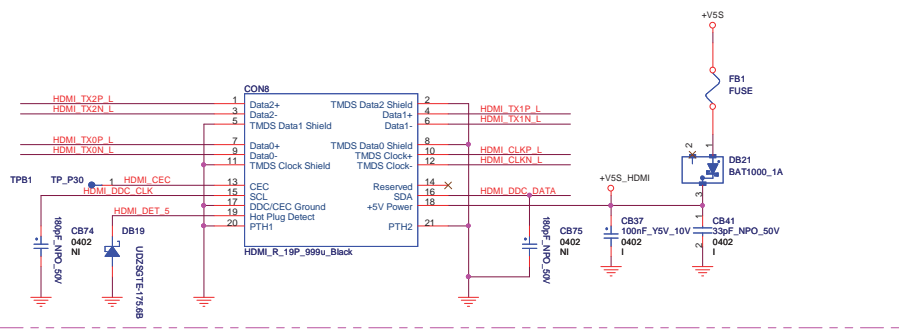
## HDD/ODD Status LED



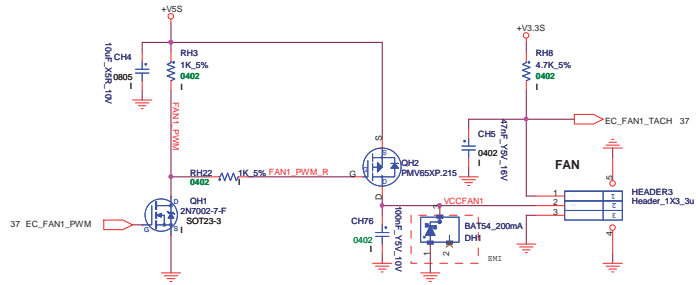




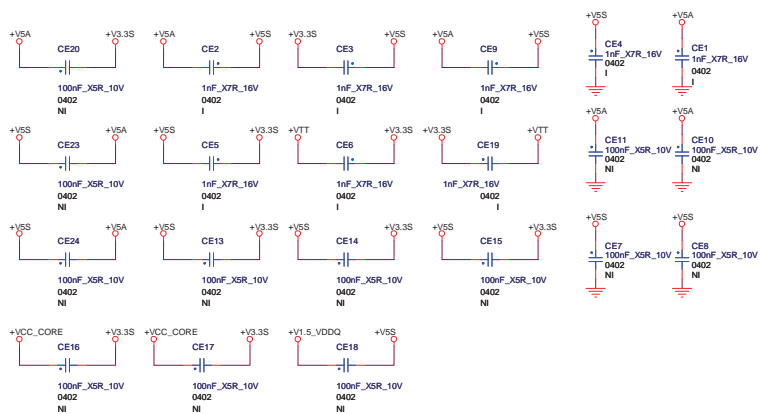
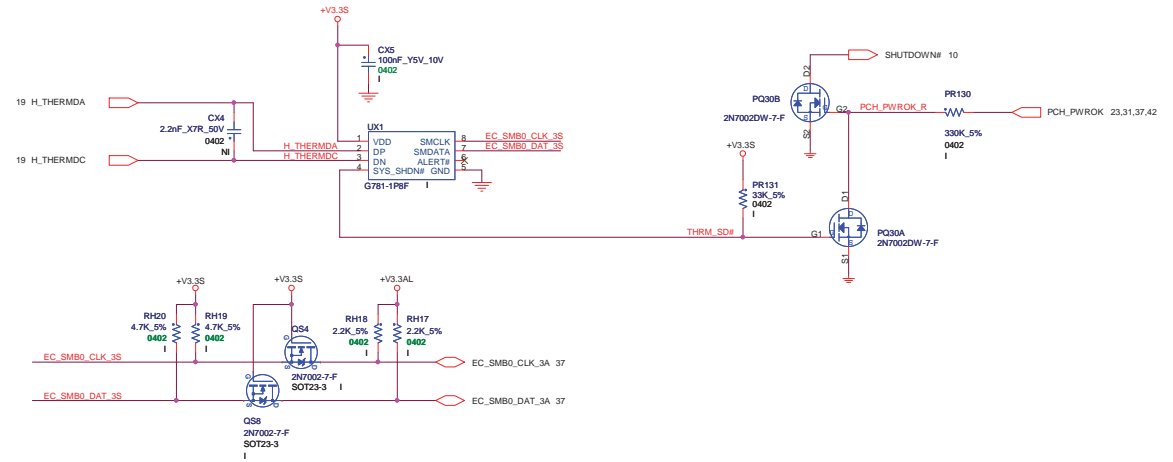
CRT CONNECTOR



## FAN



## THERMAL SENSOR



stitch cap

RF Solution