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Title: **Index Page**

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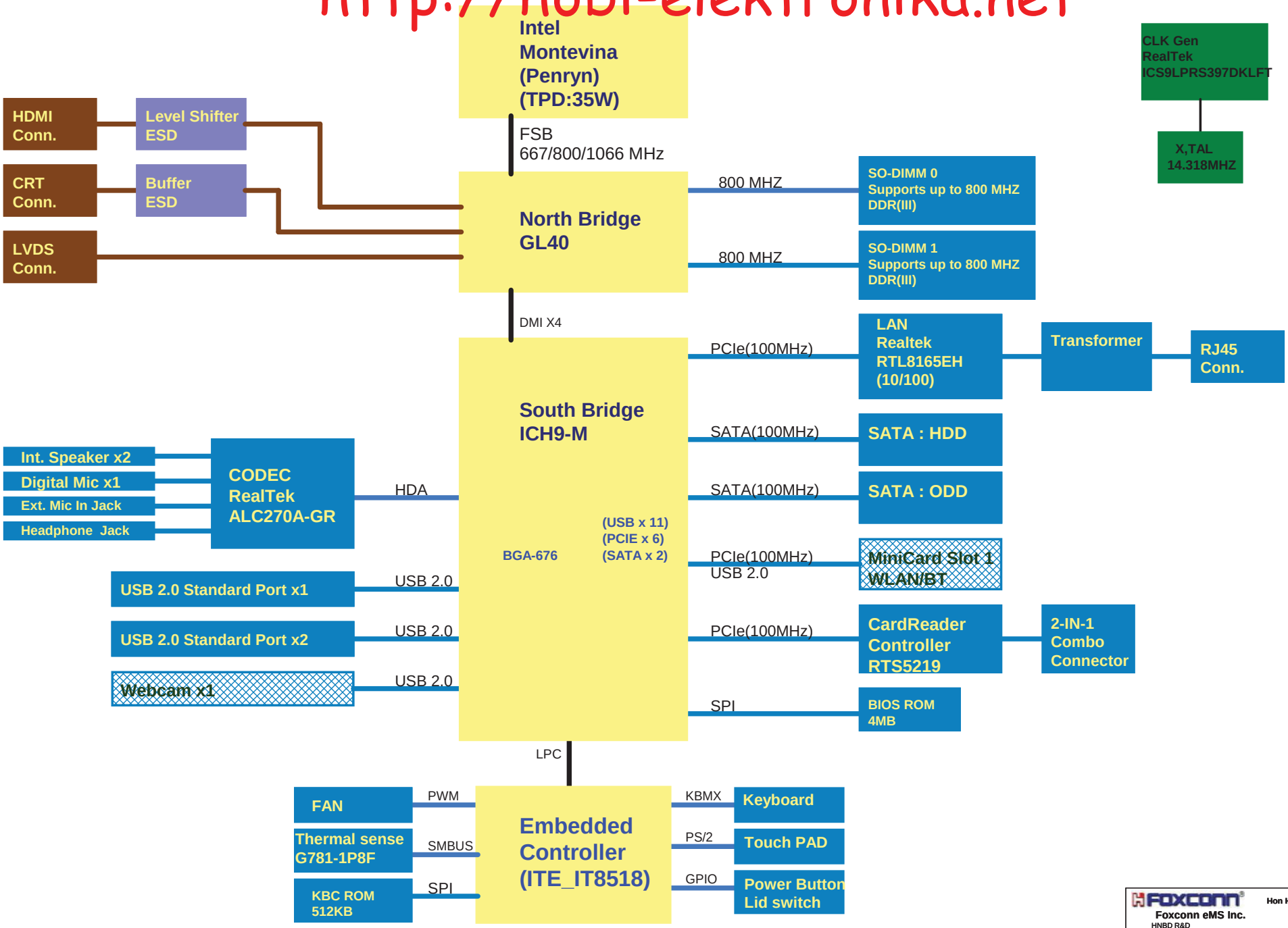

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Title: SYSTEM BLOCK DIAGRAM

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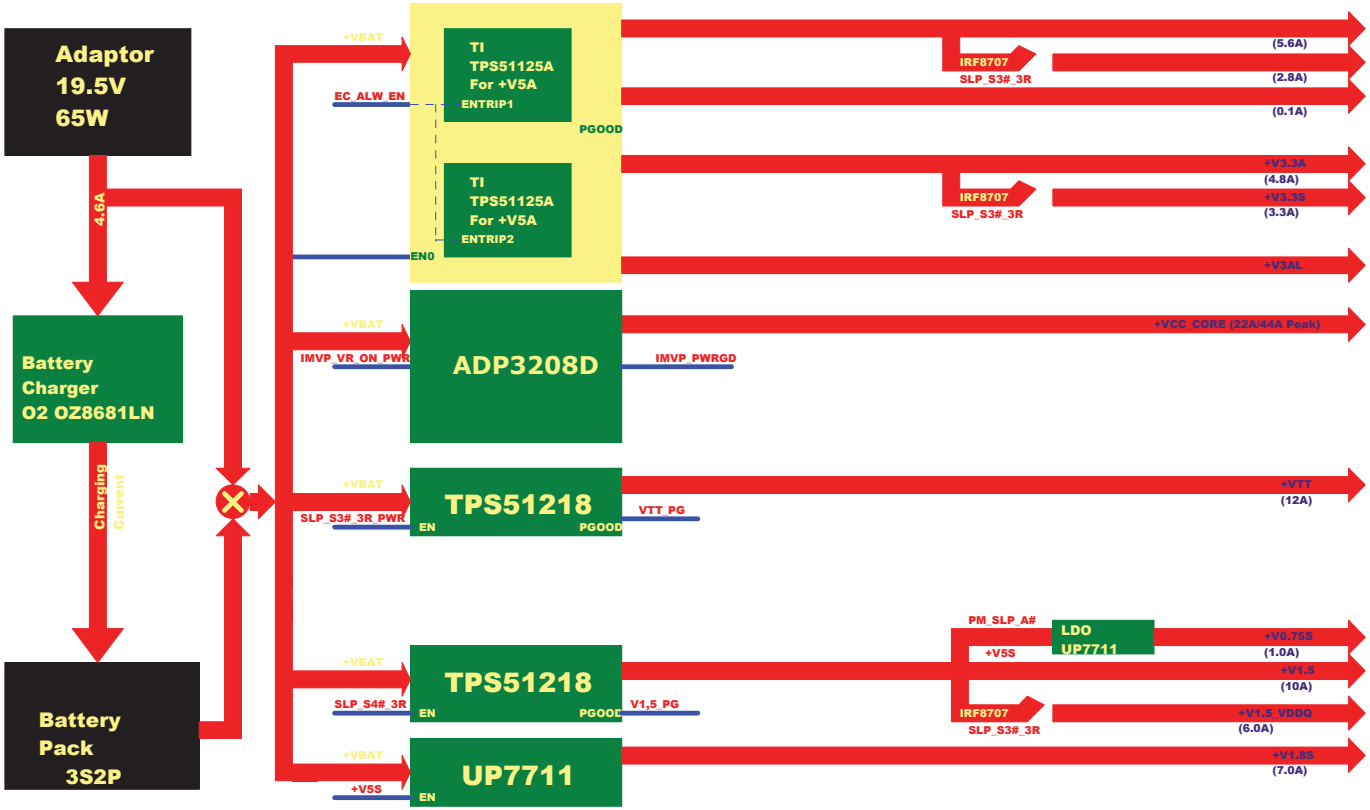
POWER MAP



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Title: History
Size: Custom
Document Number: TPN-F101/TPN-F102 Montevina
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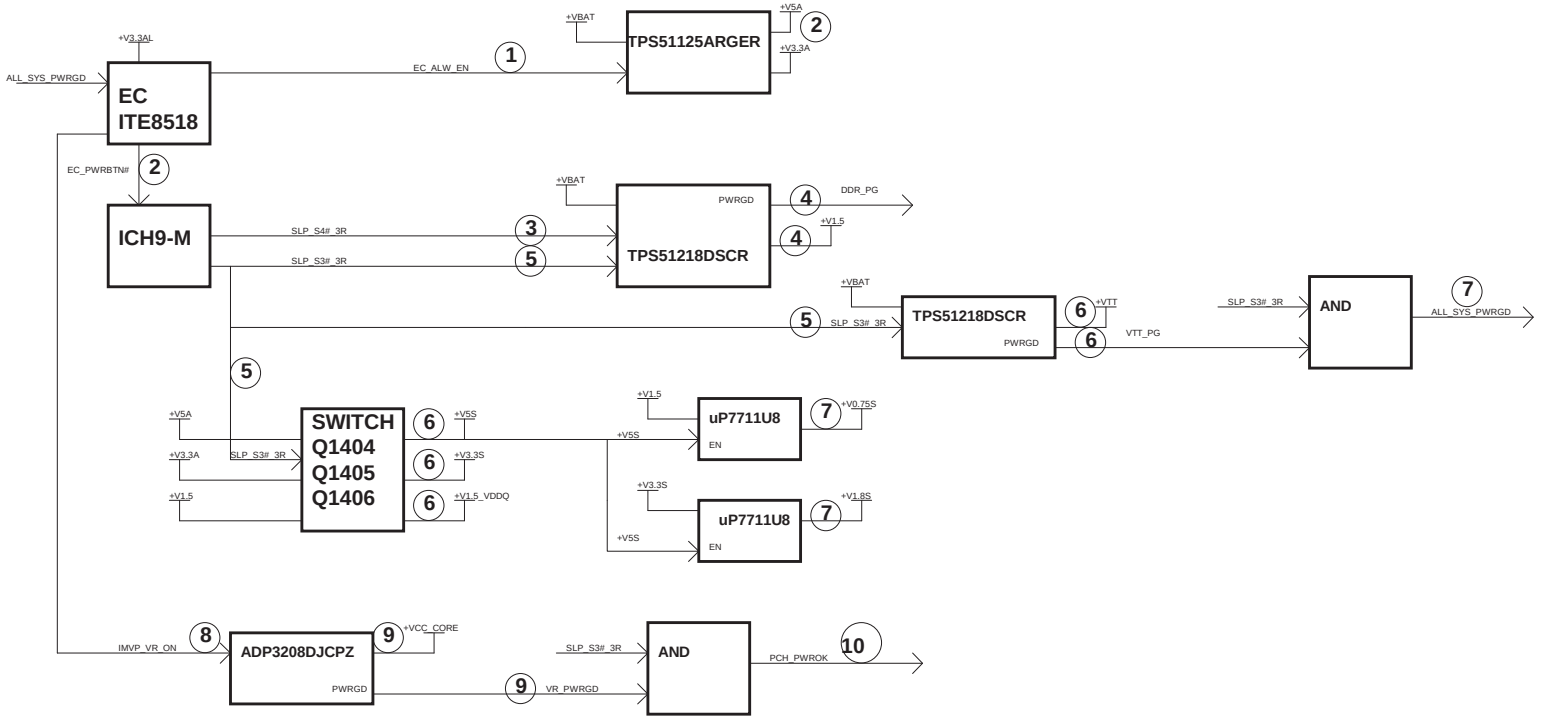

Power on Sequence required:

GL40:
1, +V3.3A ramp before +V1.1A
2, +V3.3S ramp before +V1.8S
3, +V1.8S ramp before +V1.1S
4, +V3.3S ramp before +V1.1S

ICH9-M:
1, 0 <(+V3.3S) - (+V1.8S) < 2.1
2, +V1.8S ramp before +V1.1S
3. +V1.1S ramp before VCC_NB

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Title: POWER SEQUENCY DIAGRAM

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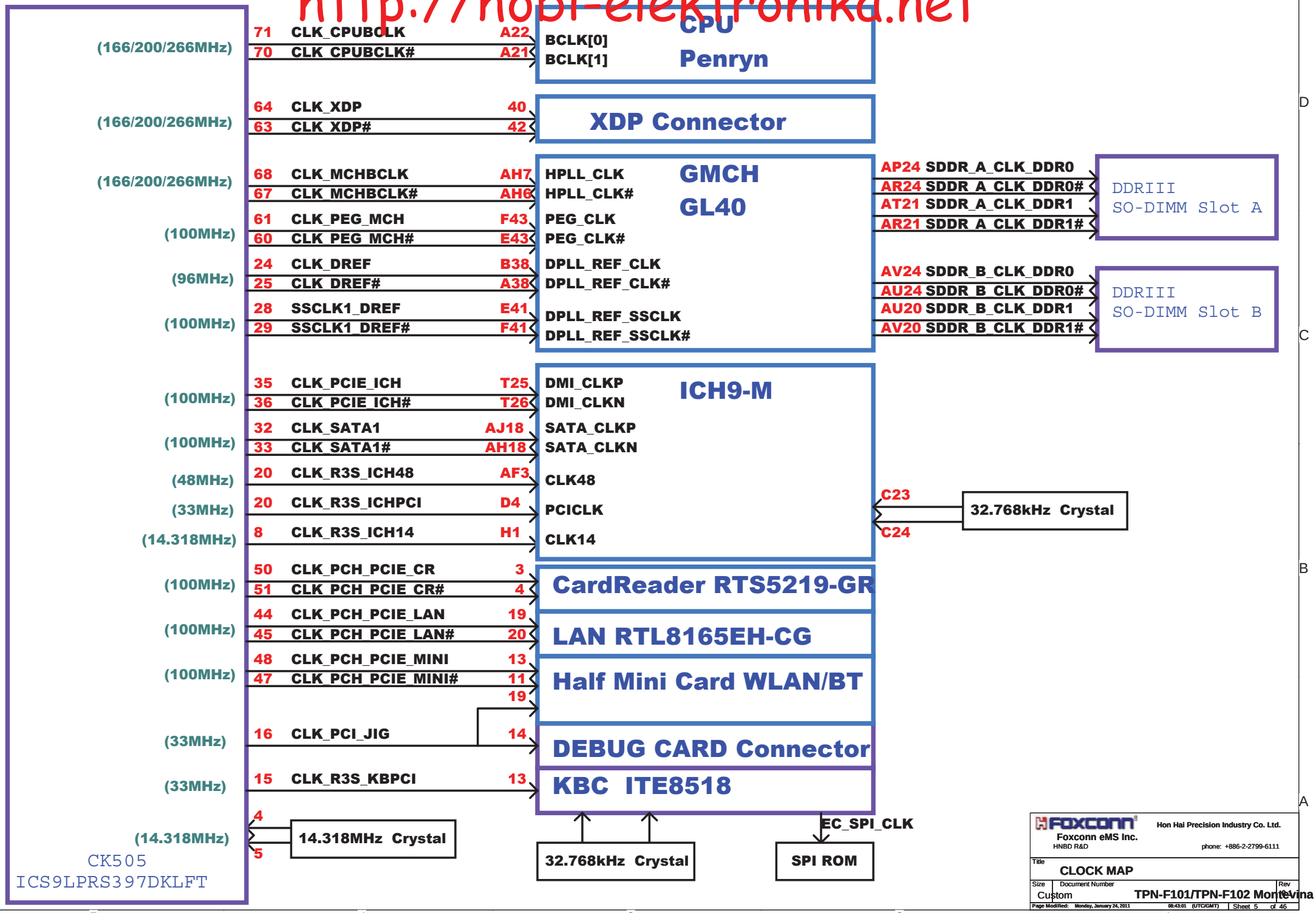

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Title: CLOCK MAP
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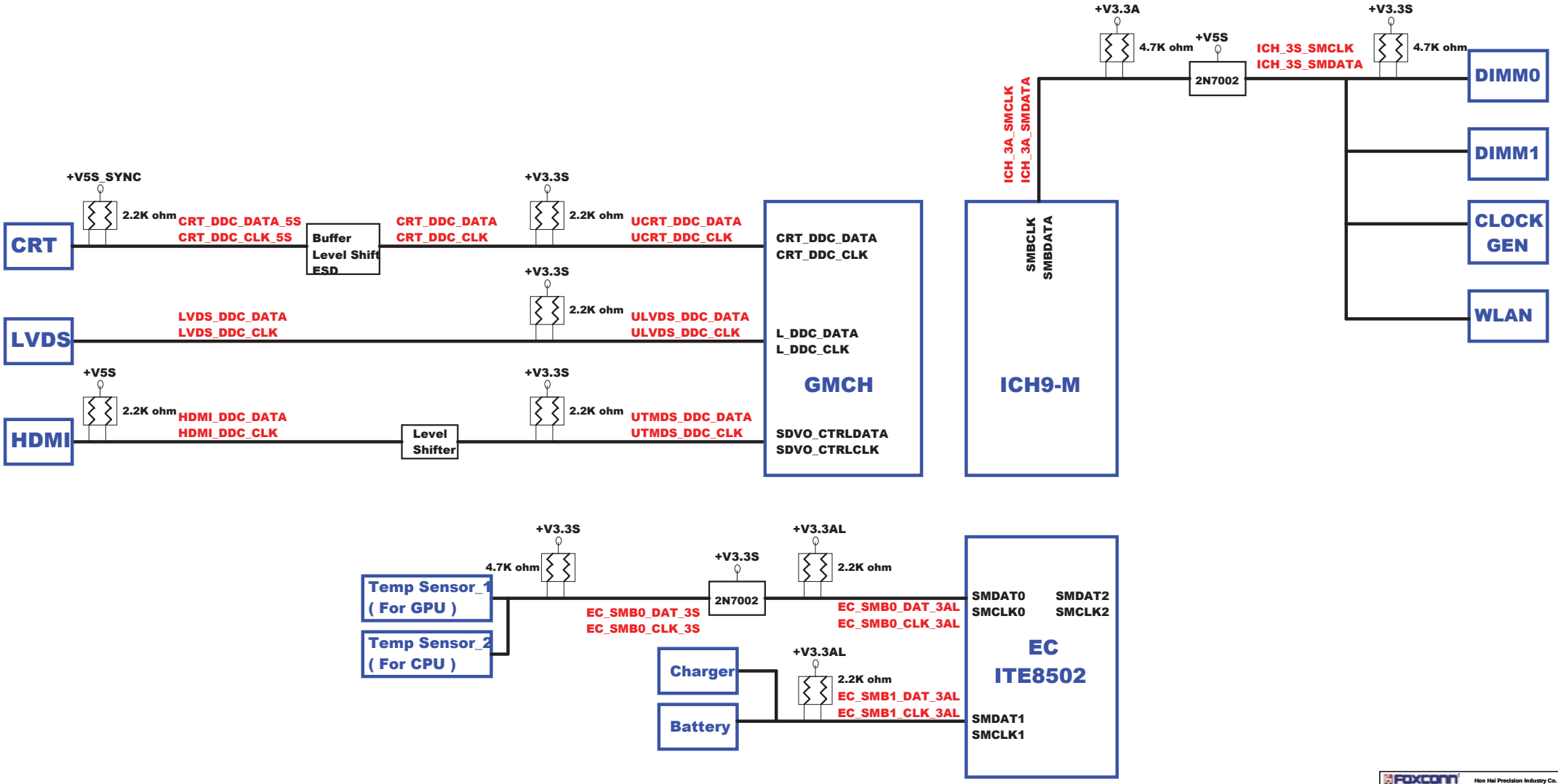

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Title: SMBUS&I2C MAP
Size: Custom
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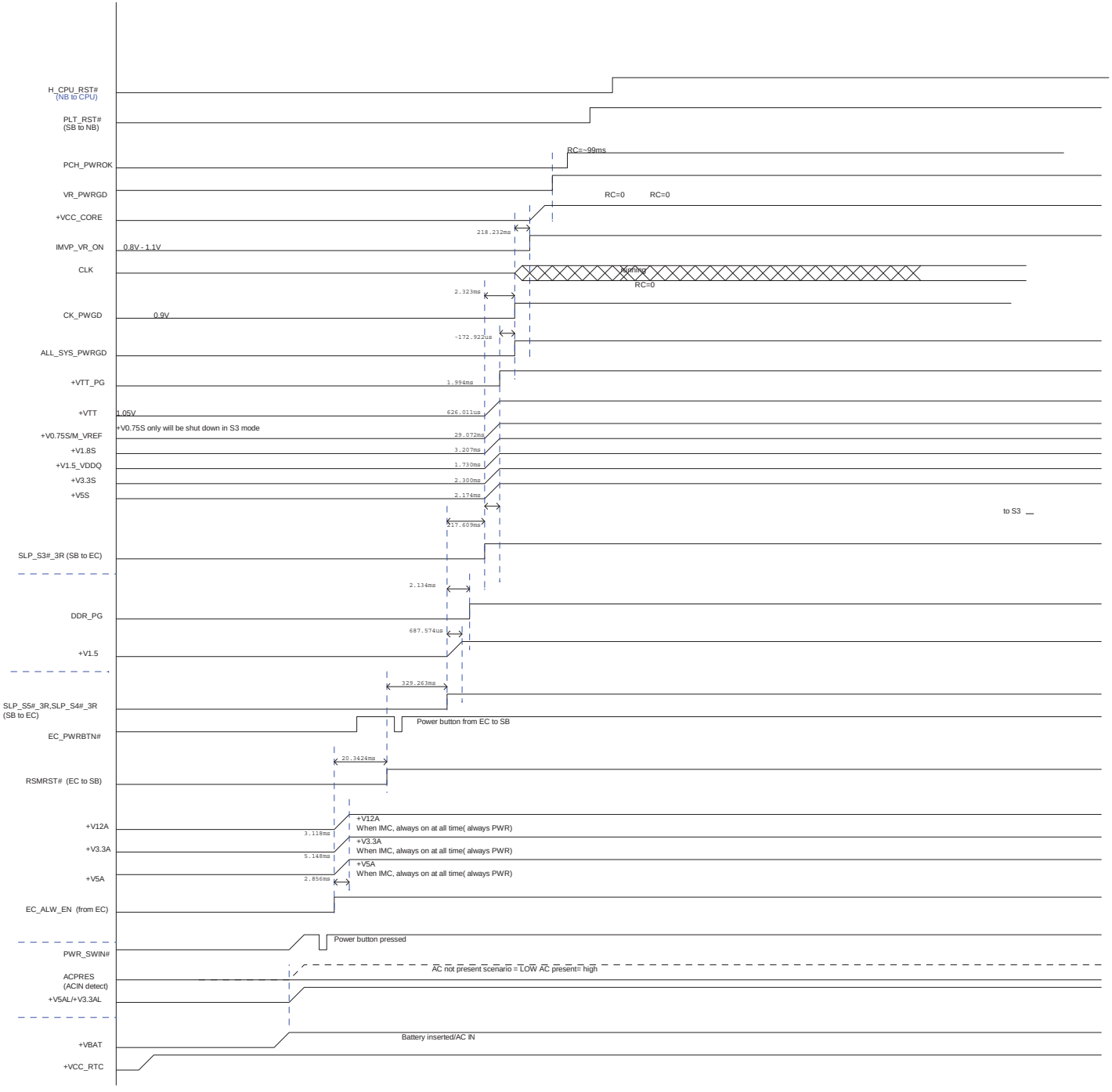

Power on Sequence required:

ICH9M:
1, +V3.3A ramp before +V1.1A
2, +V3.3S ramp before +V1.8S
3, +V1.8S ramp before +V1.1S
5, +V3.3A ramping down time > 300us
6, 50uS <= All power rails except +V3.3A <= 40mS
7, 100uS <= +V3.3A <= 40mS

GMCH:
1, 0 <(+V3.3S) - (+V1.8S) < 2.1
2, +V1.8S ramp before +V1.1S
3. +V1.1S ramp before +VCC_NB

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Title: POWER SEQUENCE

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Custom	TPN-F101/TPN-F102 Montevina platform	0.1

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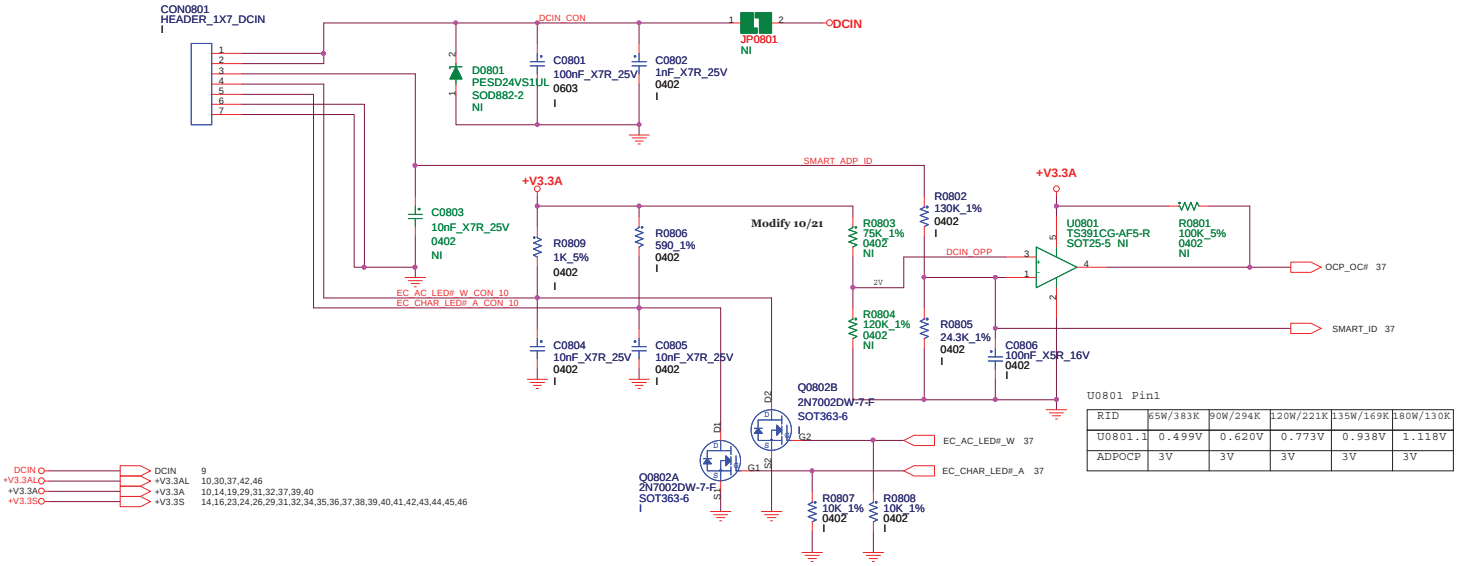
DC_JACK WIRE to BOARD CONNECTOR

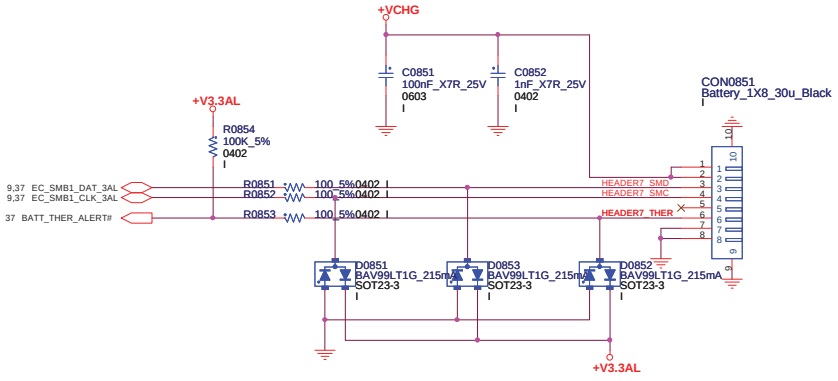


U0801 Pin1

RID	65W/383K	90W/294K	120W/221K	135W/169K	180W/130K
U0801.1	0.499V	0.620V	0.773V	0.938V	1.118V
ADPOCP	3V	3V	3V	3V	3V

BATTERY CONNECTOR

2010.0914.0



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Title: DCIN/Battery/OCP/FAN

Size: Custom | Document Number: Hopkins/Penn montevina platf | Rev: A0

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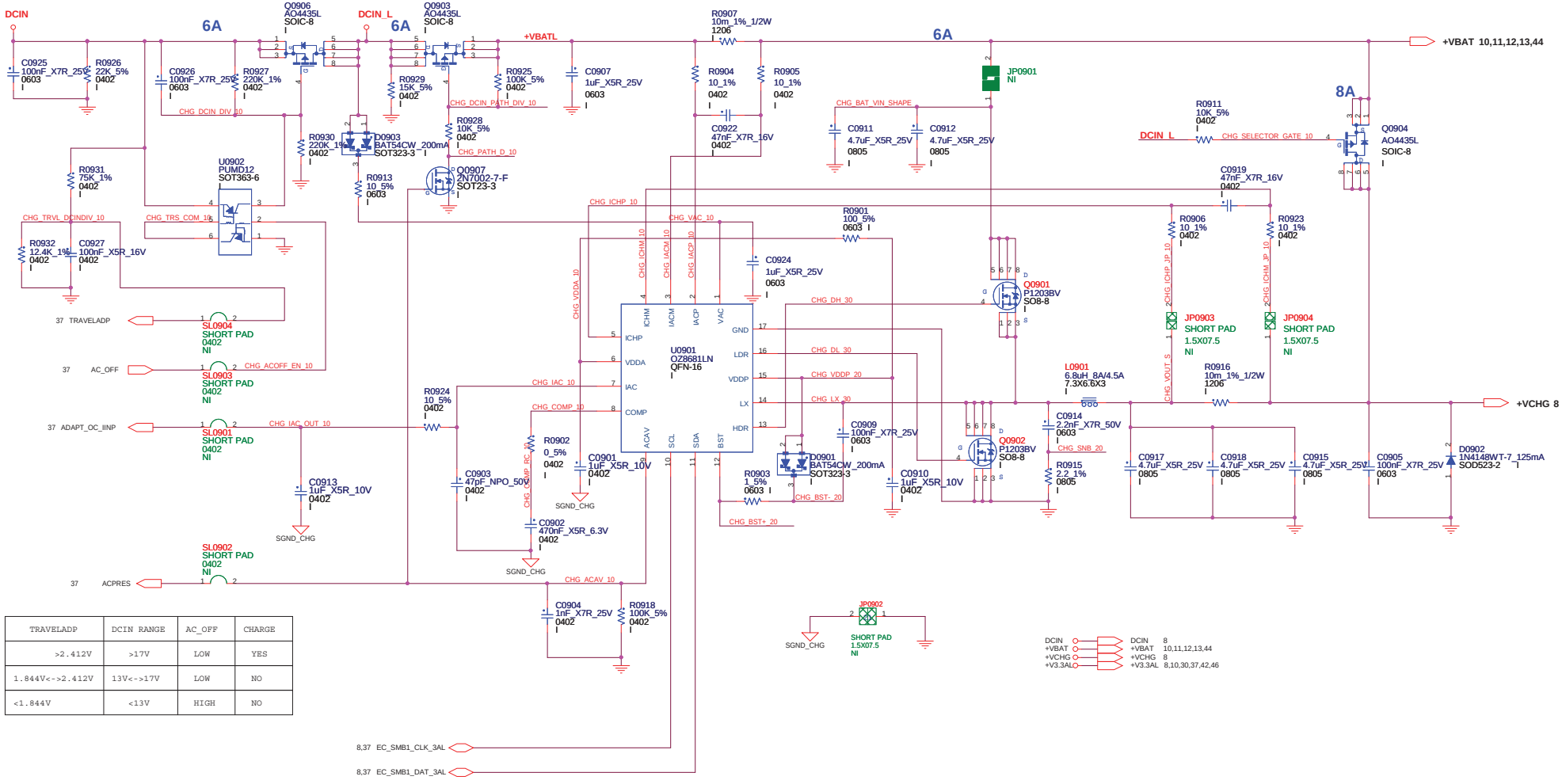
BATTERY CHARGER



TRAVELADP	DCIN RANGE	AC_OFF	CHARGE
>2.412V	>17V	LOW	YES
1.844V<->2.412V	13V<->17V	LOW	NO
<1.844V	<13V	HIGH	NO

DCIN		DCIN	8
+VBAT		+VBAT	10,11,12,13,44
+VCHG		+VCHG	8
+V3.3AL		+V3.3AL	8,10,30,37,42,46

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Size	Custom
Document Number	Hopkins/Penn montevina platform
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+V5A / +V3.3A POWER SUPPLY

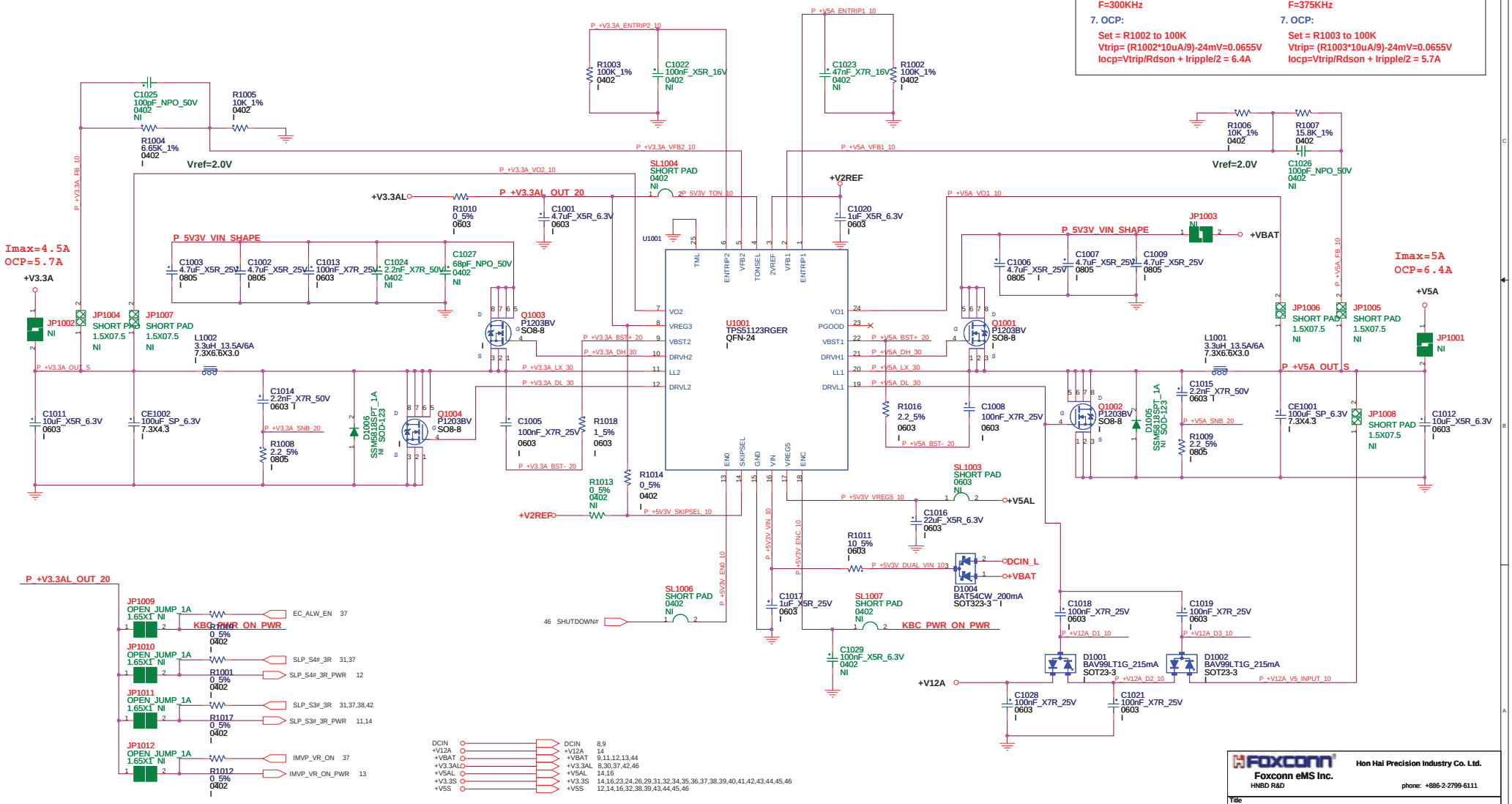
2010.1103.0

+V5A:

1. I/P Current:
   lin=Vo*Io/(0.75*Vin)=3.7A
2. Ripple Current:
   Irip=3.72A
3. Ripple Voltage:
   ESR/1=15mohm
   Vrip=55.8mV
4. Inductor Spec:
   Isat=13.5A
   Idc=6A
   DCR=30mohm
5. MOSFET Spec:
   H-side MOSFET: IRF8707PBF
   Rds(ON)=17.5mohm (Vgs=4.5 V)
   I cont = 11A (T =25 ℃)
   I peak = 88A (Pause =10 us)
6. Frequency:
   F=300KHz
7. OCP:
   Set = R1002 to 100K
   Vtrip= (R1002*10uA/9)-24mV=0.0655V
   Iocp=Vtrip/Rdson + Iripple/2 = 6.4A

+V3.3A:

1. I/P Current:
   lin=Vo*Io/(0.75*Vin)=2.2A
2. Ripple Current:
   Irip=2.21A
3. Ripple Voltage:
   ESR/1=15mohm
   Vrip=33.15mV
4. Inductor Spec:
   Isat=13.5A
   Idc=6A
   DCR=30mohm
5. MOSFET Spec:
   L-side MOSFET: IRF8707PBF
   Rds(ON)=17.5mohm (Vgs=4.5 V)
   I cont = 11A (T =25 ℃)
   I peak = 88A (Pause =10 us)
6. Frequency:
   F=375KHz
7. OCP:
   Set = R1003 to 100K
   Vtrip= (R1003*10uA/9)-24mV=0.0655V
   Iocp=Vtrip/Rdson + Iripple/2 = 5.7A



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Title: 5V/3.3V	
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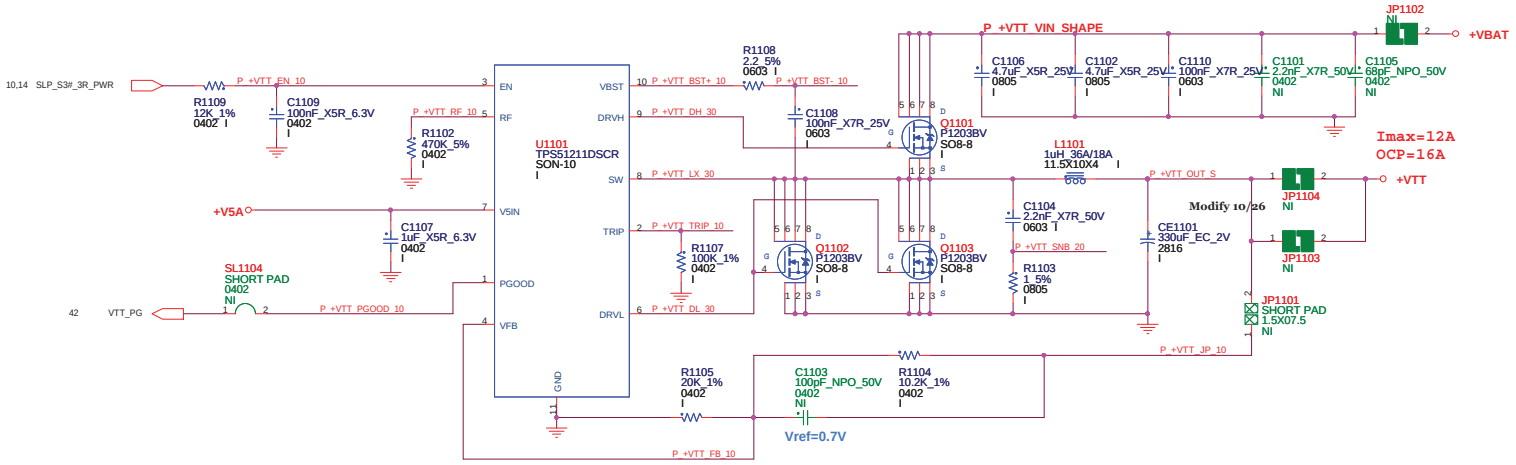
+VTT POWER SUPPLY



+V3.3S	+V3.3S	14,16,23,24,26,29,31,32,34,35,36,37,38,39,40,41,42,43,44,45,46
+V5S	+V5S	12,14,16,32,38,39,43,44,45,46
+VBAT	+VBAT	9,10,12,13,44
+VTT	+VTT	13,14,19,20,21,22,23,24,26,27,30,32,36,46

+VTT:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.86A
2. Ripple Current:
   Irip=3.42A
3. Ripple Voltage:
   ESR/1=9mohm
   Vrip=30.78mV
4. Inductor Spec:
   Isat=36A
   Idc=18A
   DCR=3.3mohm
5. MOSFET Spec:
   H-side MOSFET: IRF8707PBF
   Rds(ON)=17.5mohm (Vgs=4.5 V)
   I cont = 11A (T =25 ℃)
   I peak = 88A (Pause =10 us)

   L-side MOSFET: IRF8707PBF
   Rds(ON)=17.5mohm (Vgs=4.5 V)
   I cont = 11A (T =25 ℃)
   I peak = 88A (Pause =10 us)
6. Frequency:
   F=290KHz (R0802=470K)
7. OCP:
   Set = R0807 to 100K
   Vtrip= R0807*10uA=1V
   Iocp=(Vtrip/8*Rdson) + Iripple/2 = 16A

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Title: TPS51124 +V1.5/+V1.05

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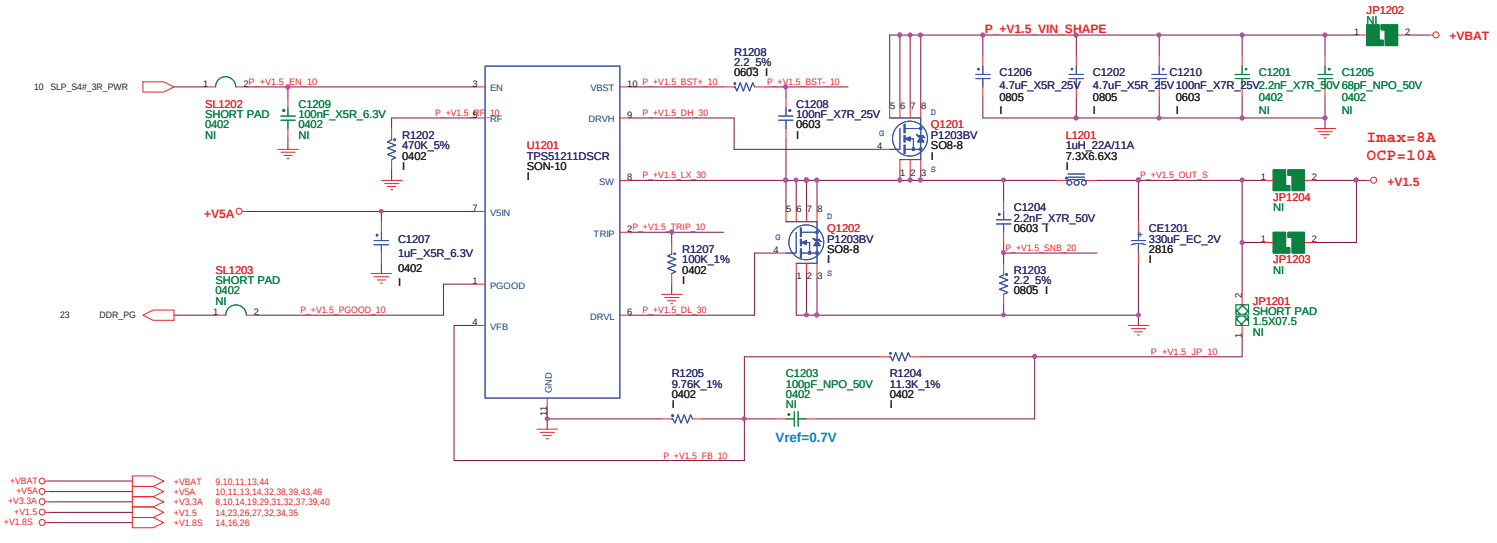
+V1.5 POWER SUPPLY



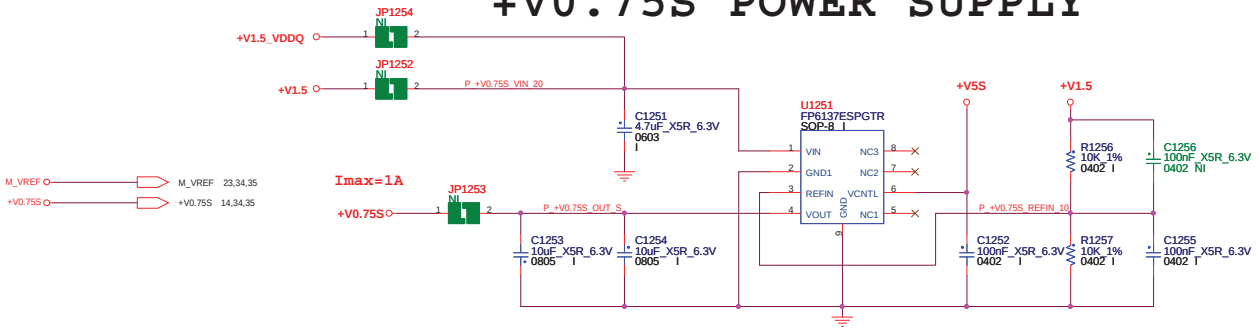
+V1.5:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.78A
2. Ripple Current:
   Irip=3.34A
3. Ripple Voltage:
   ESR/1=9mohm
   Vrip=30.6mV
4. Inductor Spec:
   Isat=36A
   Idc=18A
   DCR=3.3mohm
5. MOSFET Spec:

H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)	Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)	I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)	I peak = 88A (Pause =10 us)

6. Frequency:
   F=290KHz (R0902=470K)
7. OCP:
   Set = R0907 to 100K
   Vtrip= R0907*10uA=1V
   Iocp=(Vtrip/8*Rdson) + Iripple/2 = 9.5A

+V0.75S POWER SUPPLY



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Title: +V0.75/+V1.8S		
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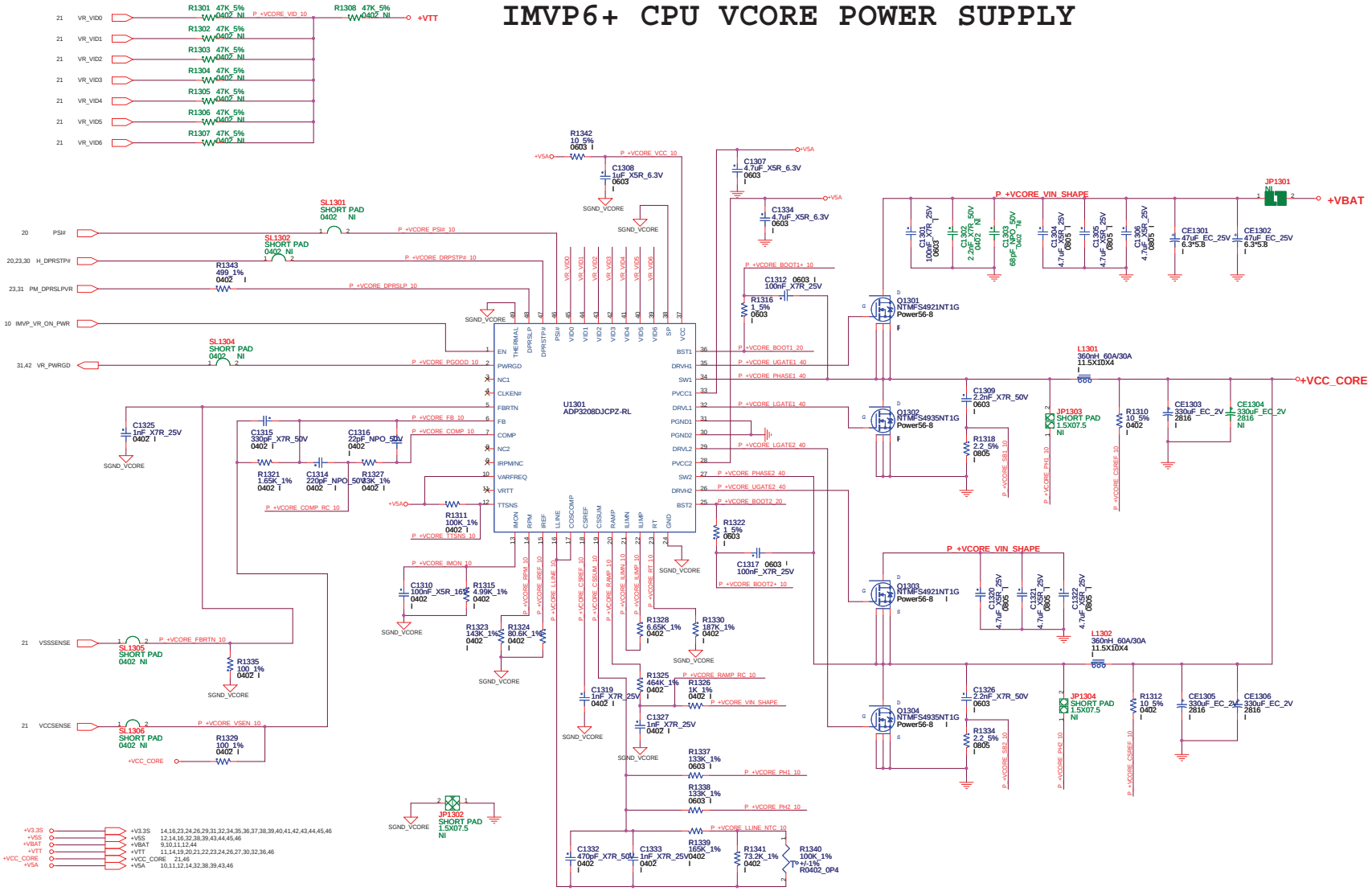
IMVP6+ CPU VCORE POWER SUPPLY



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Title: VCC_CORE TPS51620

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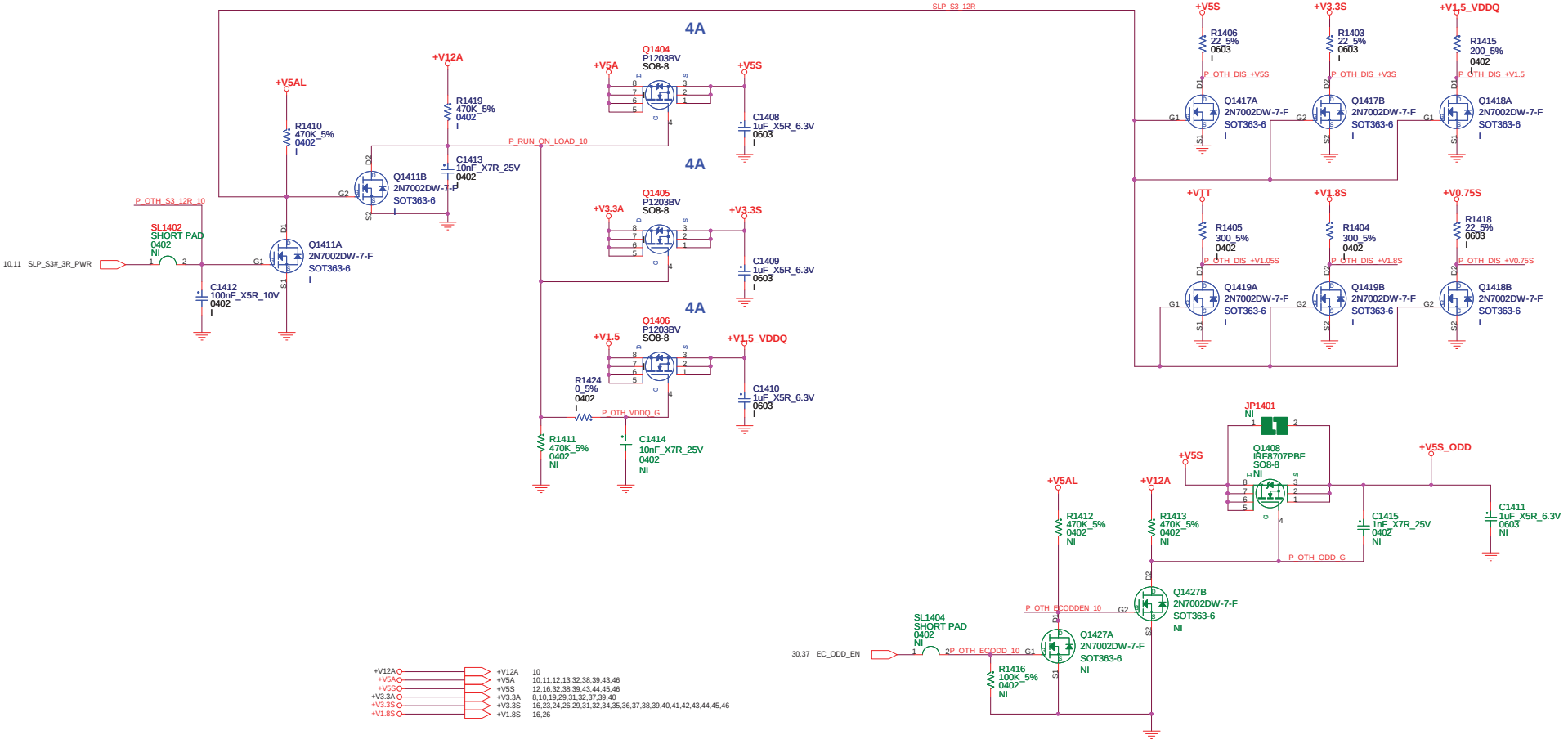
OTHER POWER / DISCHARGE CIRCUITS



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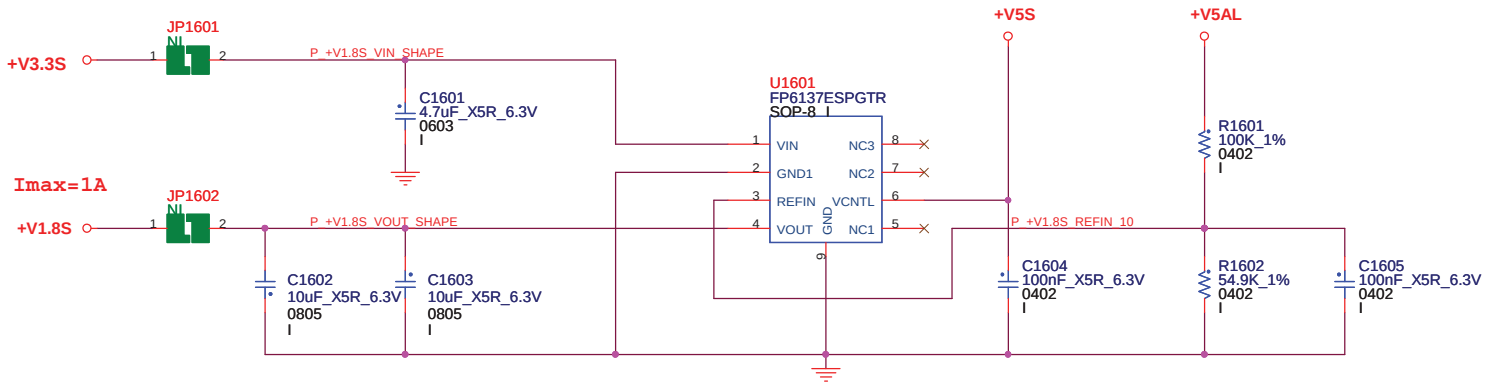
+V1.8S POWER SUPPLY



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Title: PWR_1.8VS		
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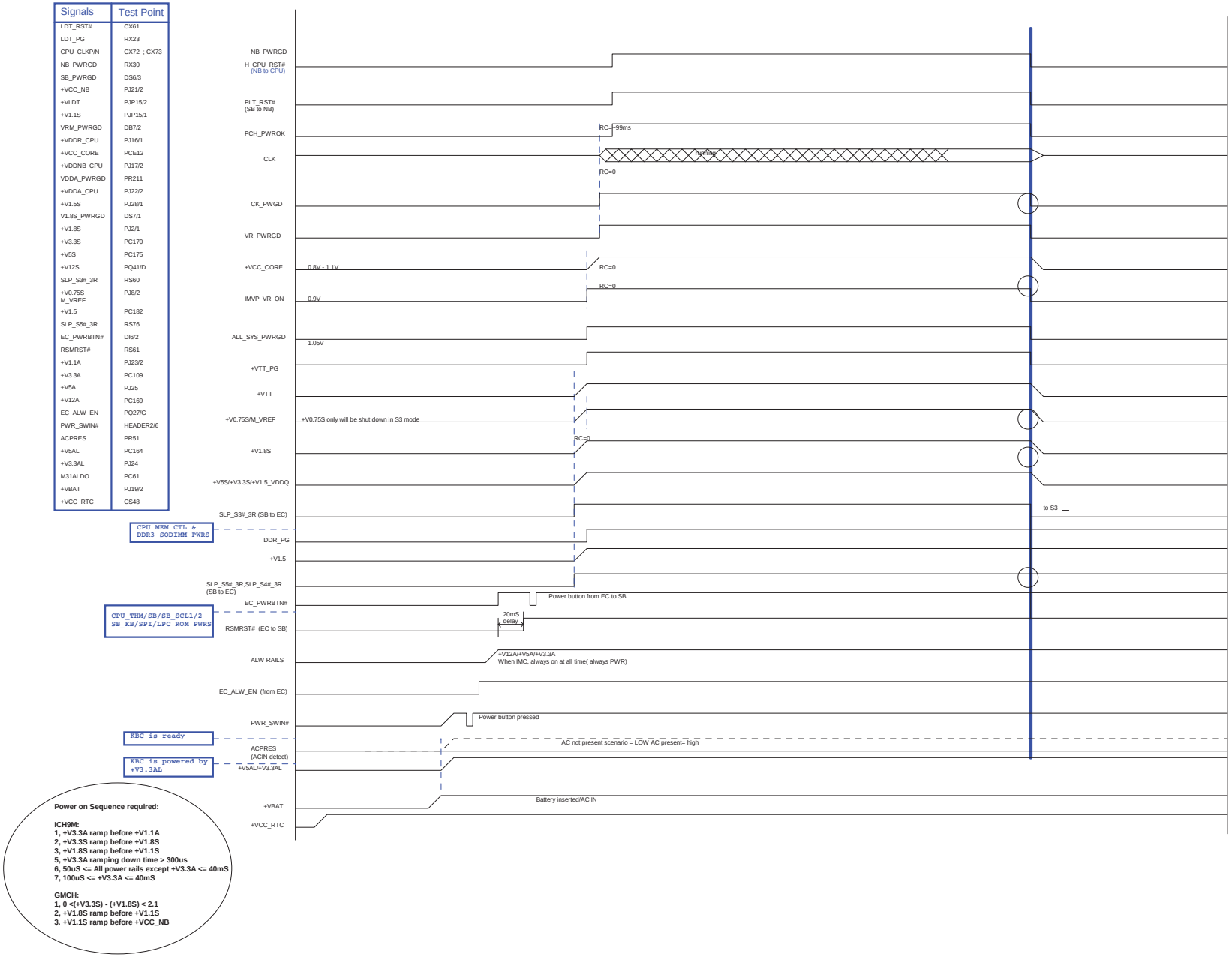
Signals	Test Point
LDT_RST#	CX61
LDT_PG	RX23
CPU_CLKP/N	CX72 ; CX73
NB_PWRGD	RX30
SB_PWRGD	DS6/3
+VCC_NB	PJ21/2
+VLDT	PJP15/2
+V1.1S	PJP15/1
VRM_PWRGD	DB7/2
+VDDR_CPU	PJ16/1
+VCC_CORE	PCE12
+VDDNB_CPU	PJ17/2
VDDA_PWRGD	PR211
+VDDA_CPU	PJ22/2
+V1.5S	PJ28/1
V1.8S_PWRGD	DS7/1
+V1.8S	PJ2/1
+V3.3S	PC170
+V5S	PC175
+V12S	PQ41/D
SLP_S3#_3R	RS60
+V0.75S M_VREF	PJ8/2
+V1.5	PC182
SLP_S5#_3R	RS76
EC_PWRBTN#	DI6/2
RSMRST#	RS61
+V1.1A	PJ23/2
+V3.3A	PC109
+V5A	PJ25
+V12A	PC169
EC_ALW_EN	PQ27/G
PWR_SWIN#	HEADER2/6
ACPRES	PR51
+V5AL	PC164
+V3.3AL	PJ24
M31ALDO	PC61
+VBAT	PJ19/2
+VCC_RTC	CS48



Power on Sequence required:

ICH9M:
1, +V3.3A ramp before +V1.1A
2, +V3.3S ramp before +V1.8S
3, +V1.8S ramp before +V1.1S
5, +V3.3A ramping down time > 300us
6, 50uS <= All power rails except +V3.3A <= 40mS
7, 100uS <= +V3.3A <= 40mS

GMCH:
1, 0 <(+V3.3S) - (+V1.8S) < 2.1
2, +V1.8S ramp before +V1.1S
3. +V1.1S ramp before +VCC_NB

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Title: **POWER SEQUENCE TIMING**

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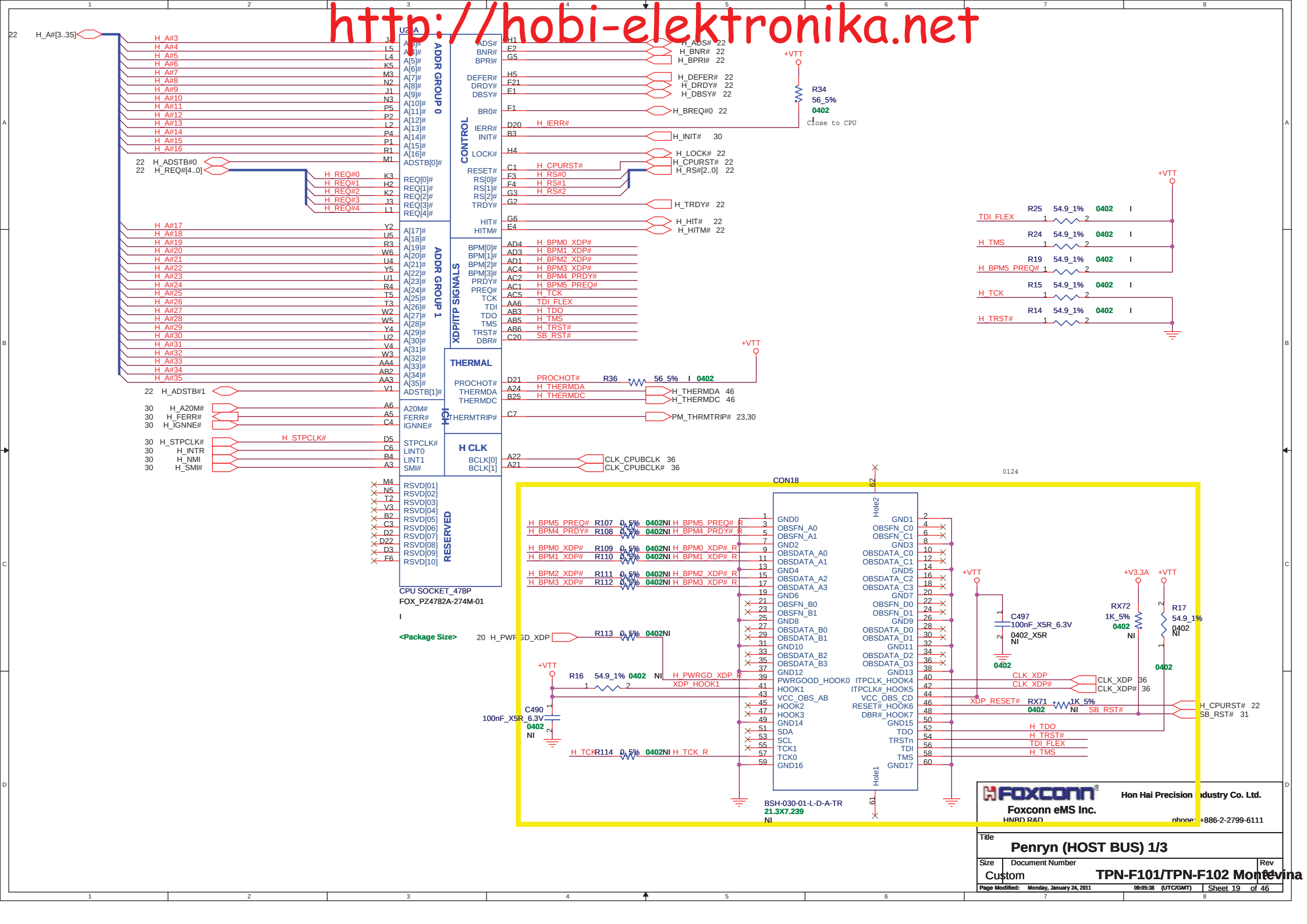

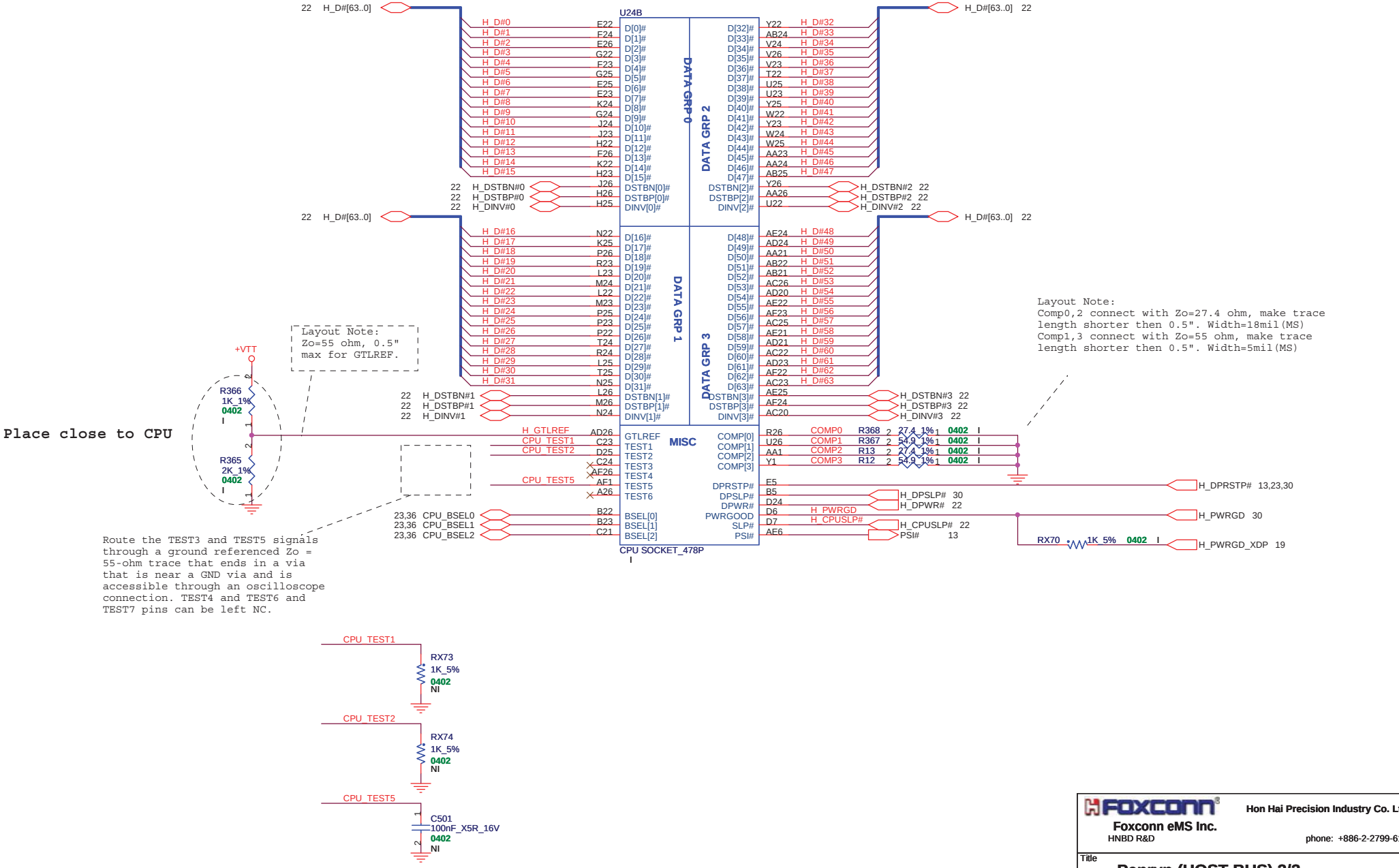

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Title: Penryn (HOST BUS) 2/3		
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina	Rev: 1A
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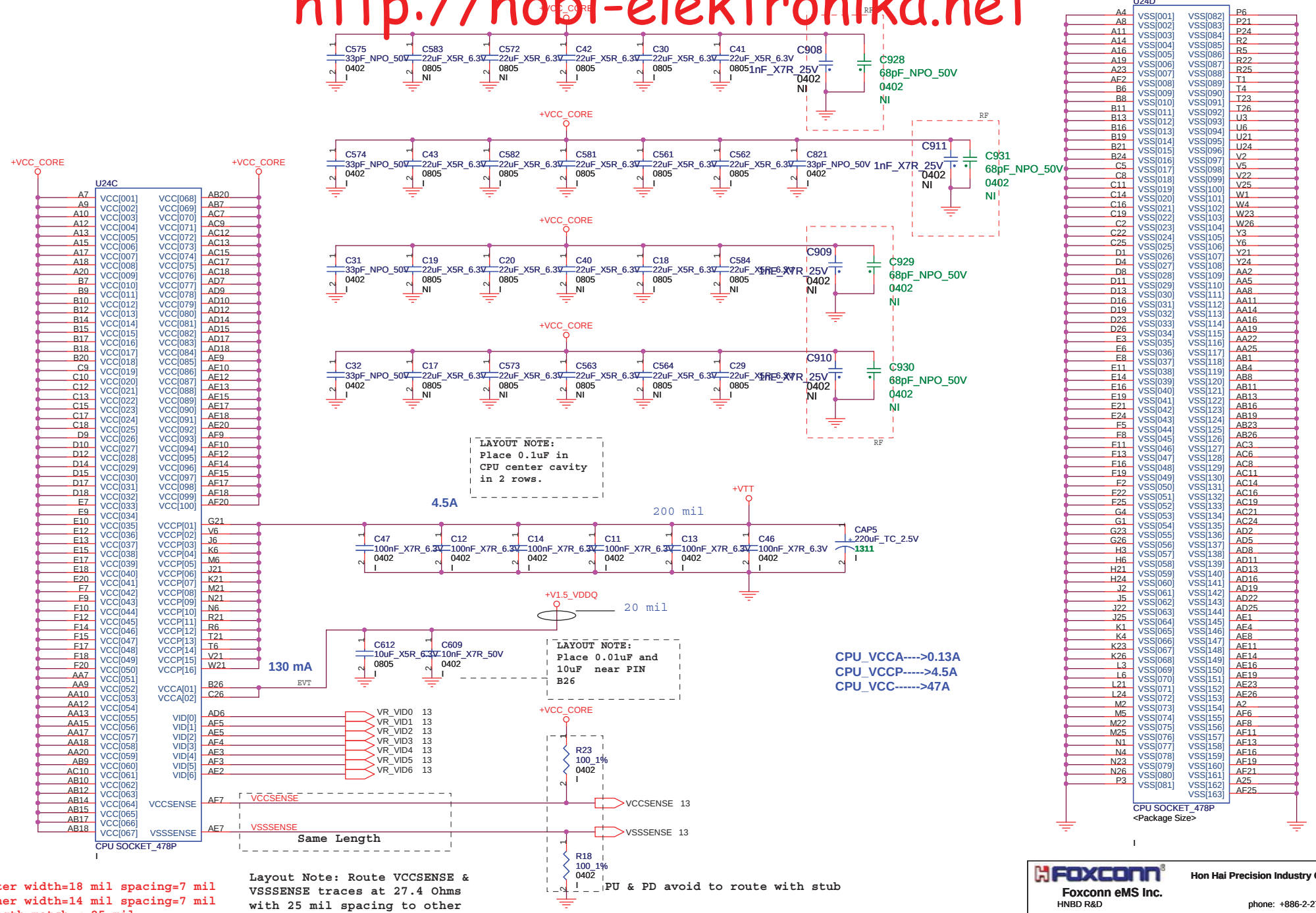

Outer width=18 mil spacing=7 mil
Inner width=14 mil spacing=7 mil
Length match < 25 mil

Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 1 inch of CPU.

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Title: Penryn (POWER/GROUND) 3/3

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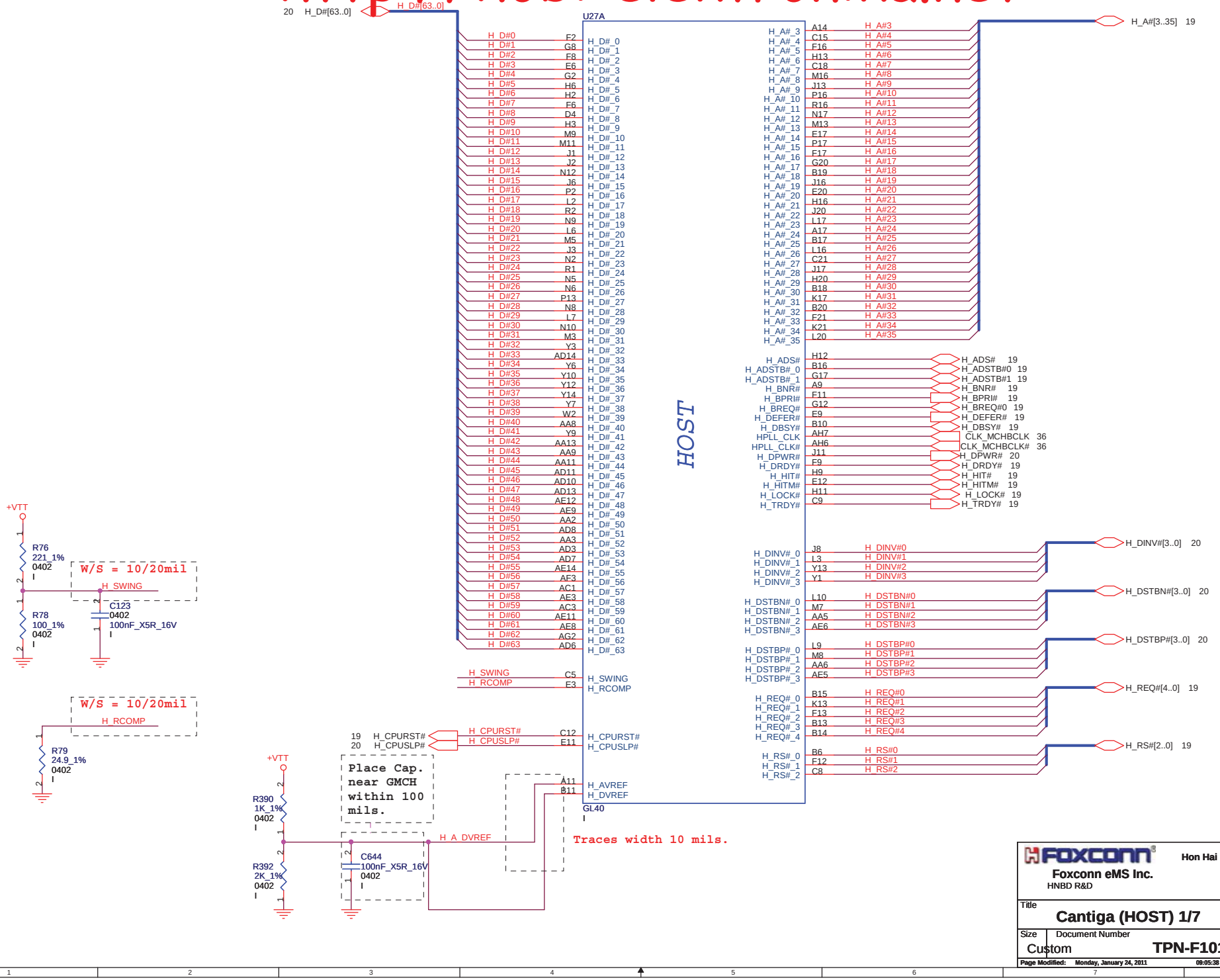

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Title: Cantiga (HOST) 1/7		
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MCH_CFG_0~2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3~4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low =The ITPM Host Interface is enabled2 High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIE Graphics Lane	Low = Reverse Lane High = Normal operation (default)
MCH_CFG_10 PCIE Loopback enable	Low = Enabled3 High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled3 High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled3 High = Disabled (default)
MCH_CFG_14~15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17~18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2-> 1, 1->2 and 0->3) DMI x2 mode [(G)MCH ->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/ DP/iHDMI) Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port

U27B

RSVD
RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10 RSVD11 RSVD12 RSVD13 RSVD14 RSVD15 RSVD16 RSVD17 RSVD20 RSVD22 RSVD23 RSVD24 RSVD25

DDR CLK/ CONTROL/COMPENSATION
SA_CK_0 SA_CK_1 SB_CK_0 SB_CK_1 SA_CK#_0 SA_CK#_1 SB_CK#_0 SB_CK#_1 SA_CKE_0 SA_CKE_1 SB_CKE_0 SB_CKE_1 SA_CS#_0 SA_CS#_1 SB_CS#_0 SB_CS#_1 SA_ODT_0 SA_ODT_1 SB_ODT_0 SB_ODT_1 SM_RCOMP SM_RCOMP# SM_RCOMP_VOH SM_RCOMP_VOL SM_VREF SM_PWROK SM_REXT SM_DRAMRST#

CLK
DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK# PEG_CLK PEG_CLK#

DMI
DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3 DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3

PM
GRAPHICS VID
GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VID_4 GFX_VR_EN

ME
CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF

MISC
DDPC_CTRLCLK DDPC_CTRLDATA SDVO_CTRLCLK SDVO_CTRLDATA CLKREQ# ICH_SYNC# TSATN#

HDA
HDA_BCLK HDA_RST# HDA_SDI HDA_SDO HDA_SYNC

CFG
CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20
CFG[17:3] internal pull-up
CFG[20:18] internal pull-down

PM
PM_SYNC# PM_DPRSTP# PM_EXT_TS#_0 PM_EXT_TS#_1 PWROK RSTIN# THERMTRIP# DPRSLPVR

NC
NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7 NC_8 NC_9 NC_10 NC_11 NC_12 NC_13 NC_14 NC_15 NC_16 NC_17 NC_18 NC_19 NC_20 NC_21 NC_22 NC_23 NC_24 NC_25 NC_26

GL40 <Package Size>

For DDR3

External Graphics (GMCH CRT/TVOUT Disable)

Width =12mil

None HDMI : NI

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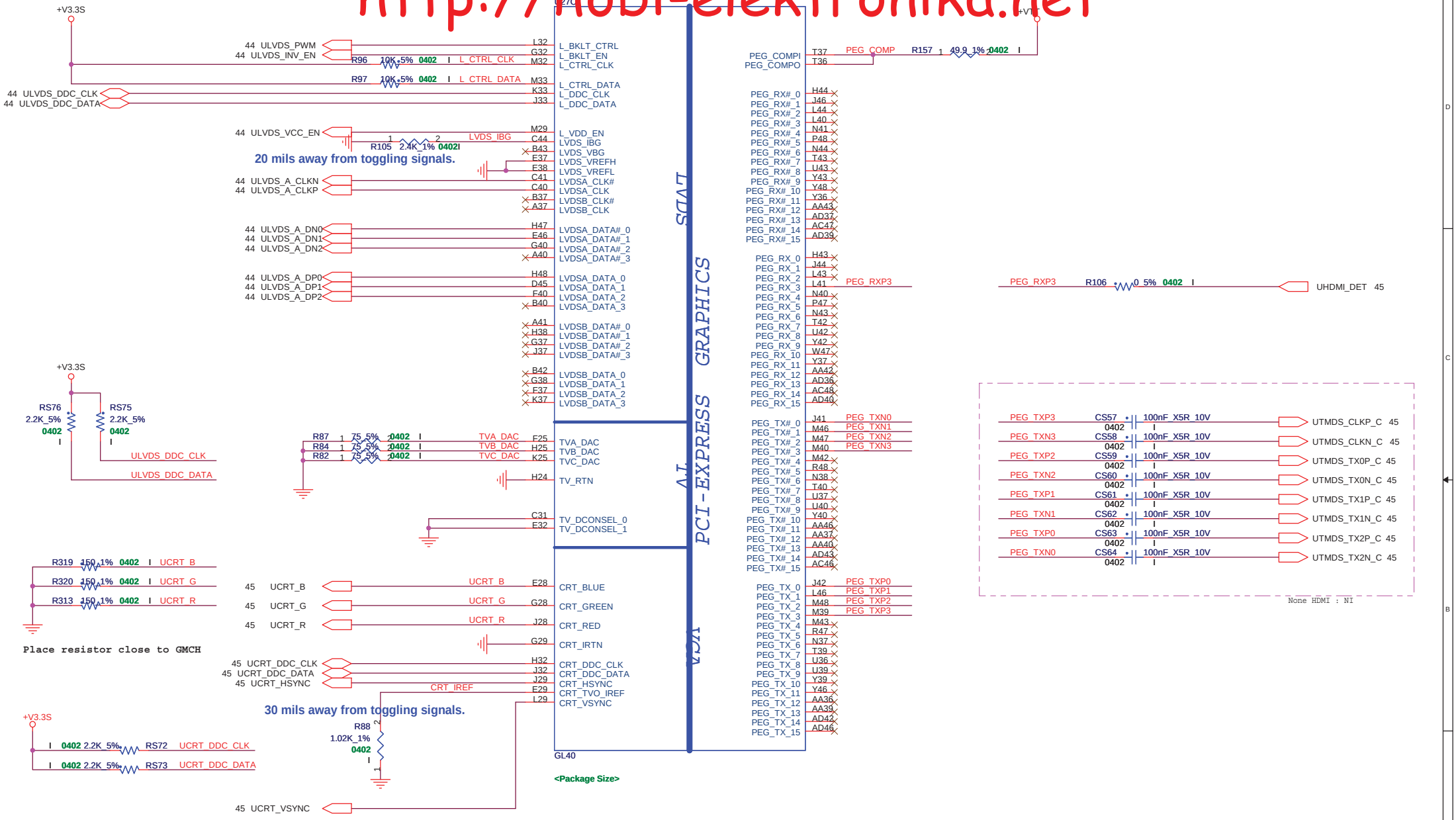
phone: +886-2-2799-6111	
Title	Cantiga (DMI) 2/7
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina pl
Rev: 0.1	
Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT)	Sheet 23 of 46



FOXCONN	Hon Hai Precision Industry Co. Ltd.	
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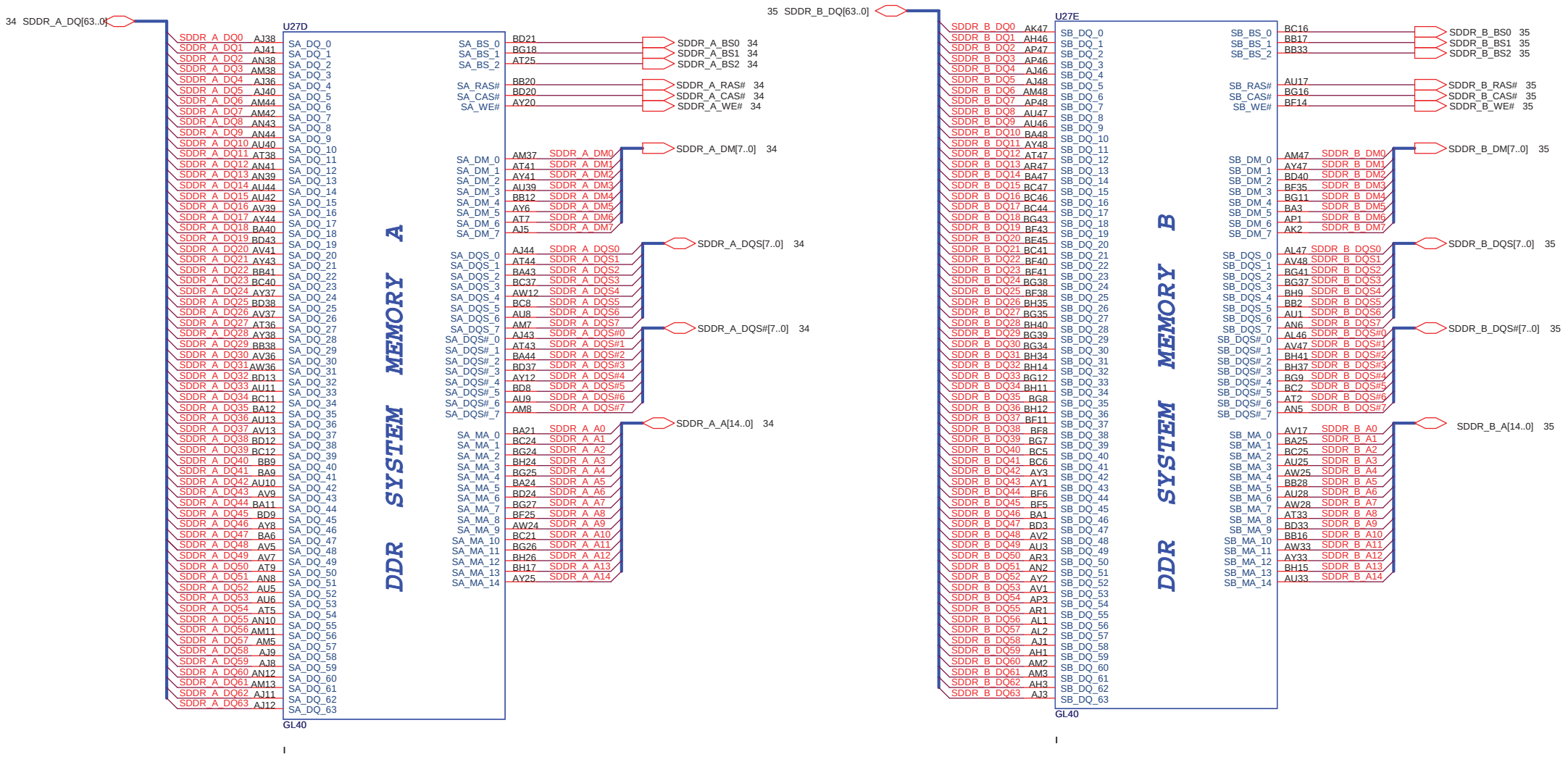
HNBD R&D	phone: +886-2-2799-6111	
Title: Cantiga (GRAPHIC) 3/7		
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina	Rev: 0.4
Page Modified: Monday, January 24, 2011 09:05:39 (UTC/GMT)		Sheet 24 of 46



FOXCONN
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Cantiga (DDR3) 4/7

Size	Document Number	Rev
Custom	TPN-F101/TPN-F102 Montevina	

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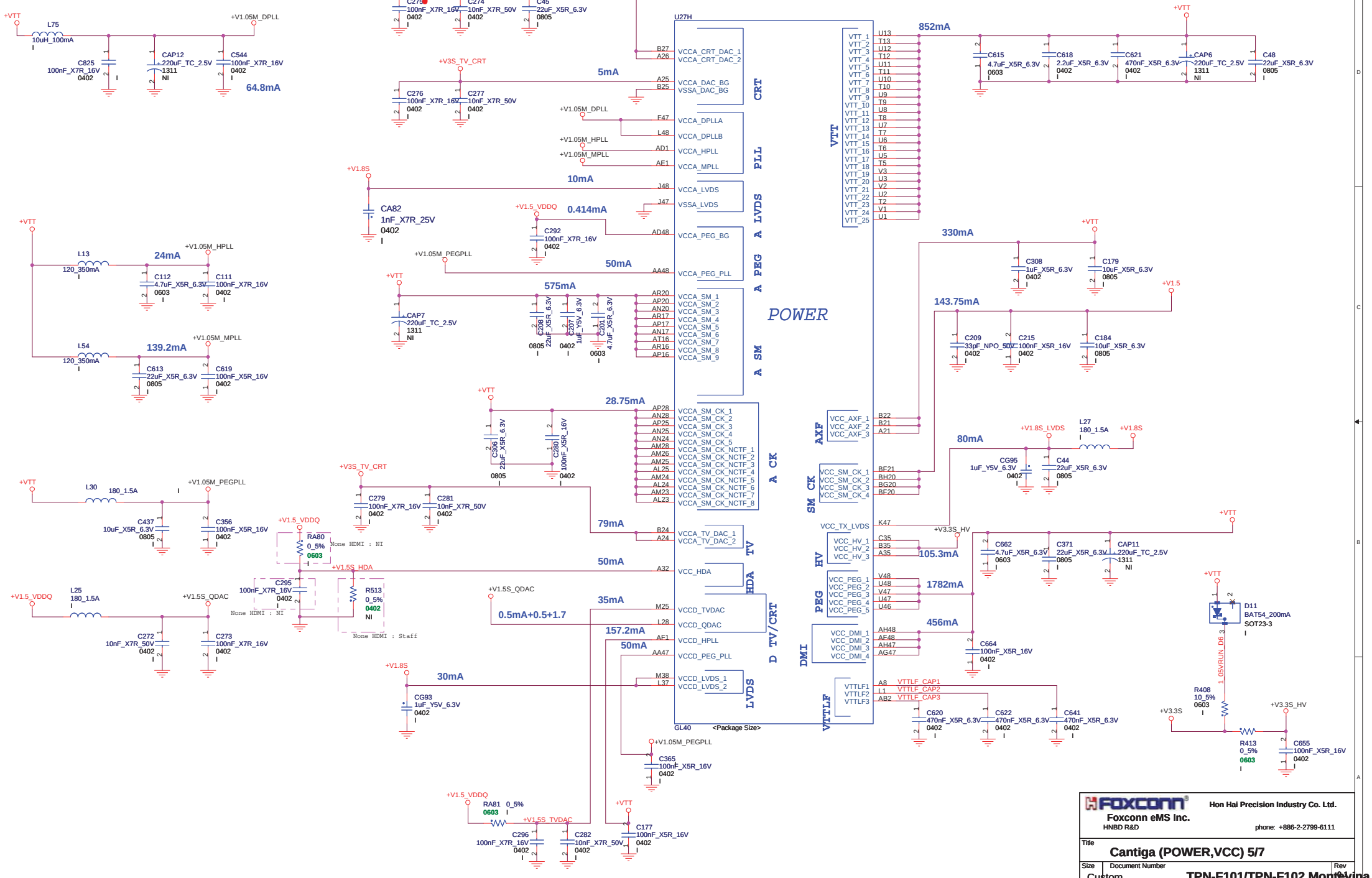
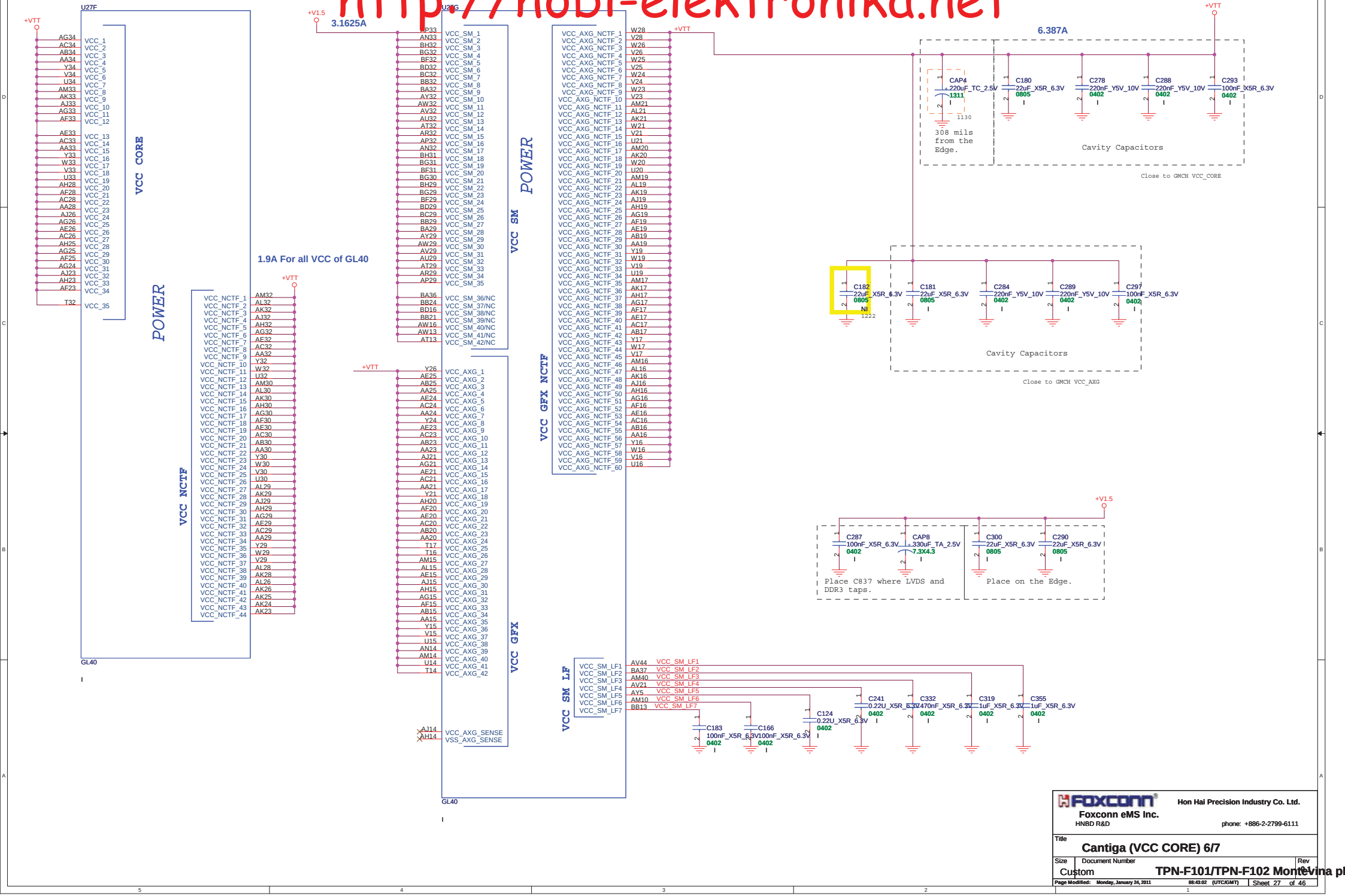


Hon Hai Precision Industry Co. Ltd.	Foxconn eMS Inc.
HNBD R&D	phone: +886-2-2799-6111
Title	Cantiga (POWER,VCC) 5/7
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina pl
Rev: 0.1	
Page Modified: Monday, January 24, 2011 08:43:02 (UTC/GMT)	Sheet 26 of 46



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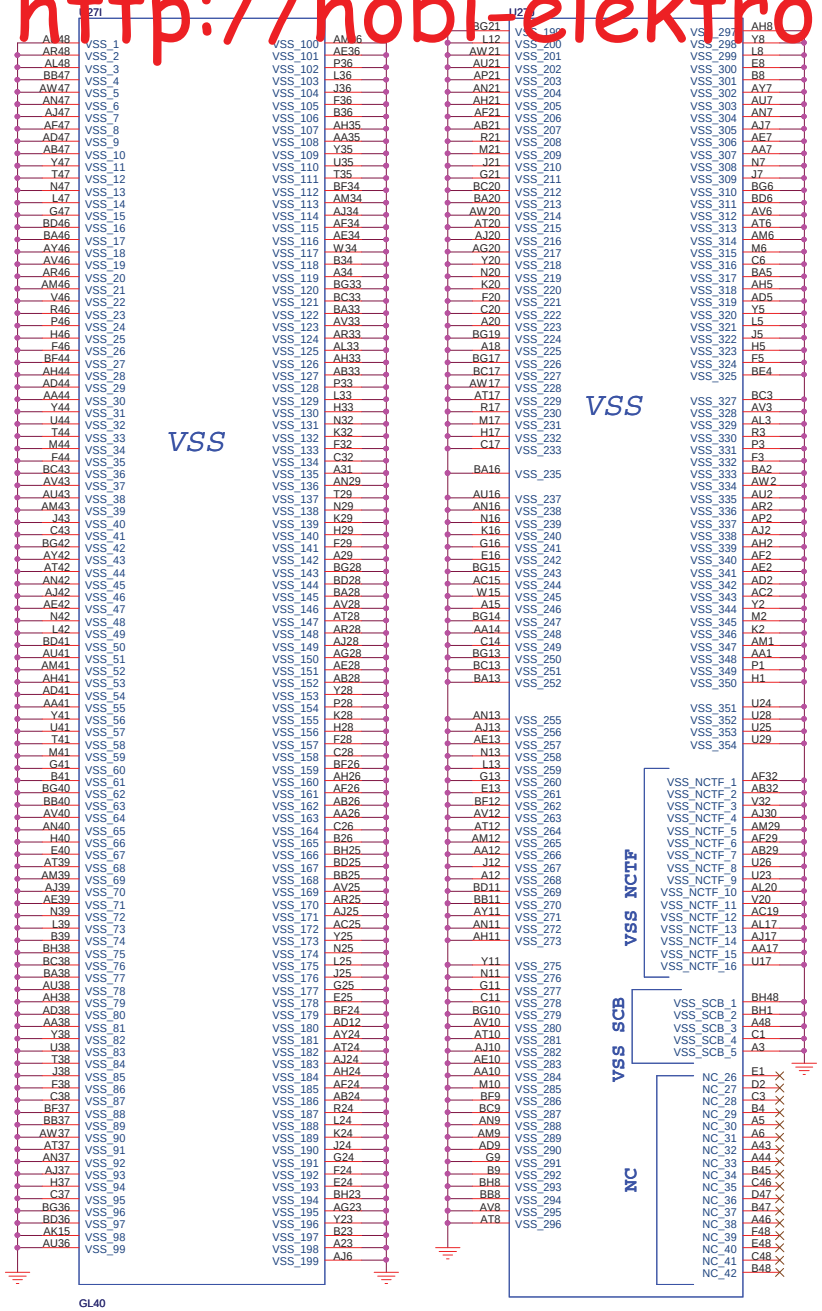
Foxconn eMS Inc.	
HNBD R&D	phone: +886-2-2799-6111
Title	Cantiga (VCC CORE) 6/7
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina pl
Rev: 0.1	
Page Modified: Monday, January 24, 2011 08:43:02 (UTC/GMT)	Sheet 27 of 46

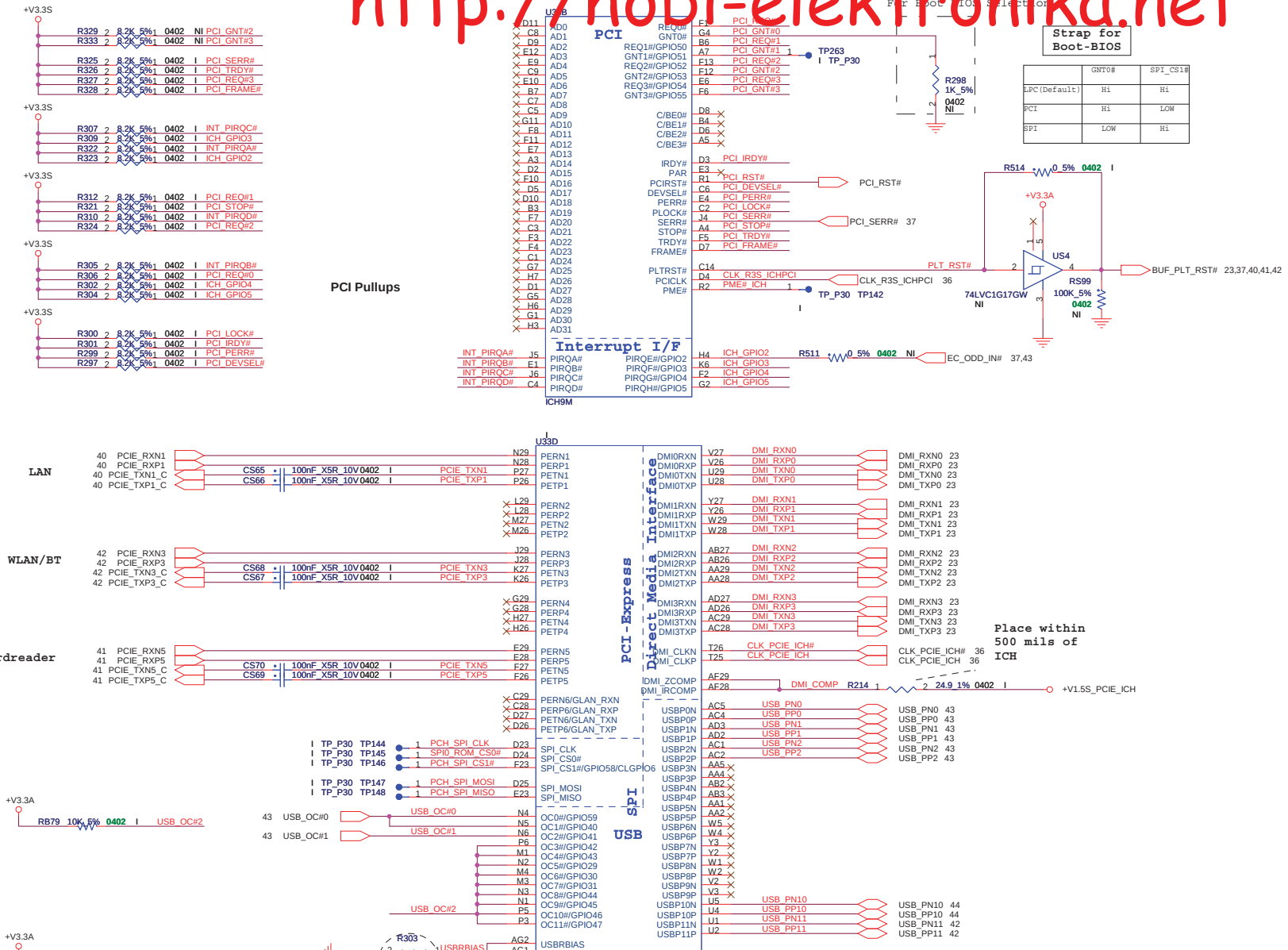


Hon Hai Precision Industry Co. Ltd.
Foxconn eMS Inc.
HNBD R&D
phone: +886-2-2799-6111

Title: Cantiga (VSS) 7/7

Size: Custom | Document Number: TPN-F101/TPN-F102 Montevina pl | Rev: 0.1

Page Modified: Monday, January 24, 2011 08:43:03 (UTC/GMT) | Sheet 28 of 46



USB PORT	Function	OC pin
PORT-0	Ext. USB 0	
PORT-1	Ext. USB 1	
PORT-2	Ext. USB 2	
PORT-3		
PORT-4		
PORT-5		
PORT-6		
PORT-7		
PORT-8		
PORT-9		
PORT-10	Camera	
PORT-11	WLAN/BT	
PORT-12		
PORT-13		

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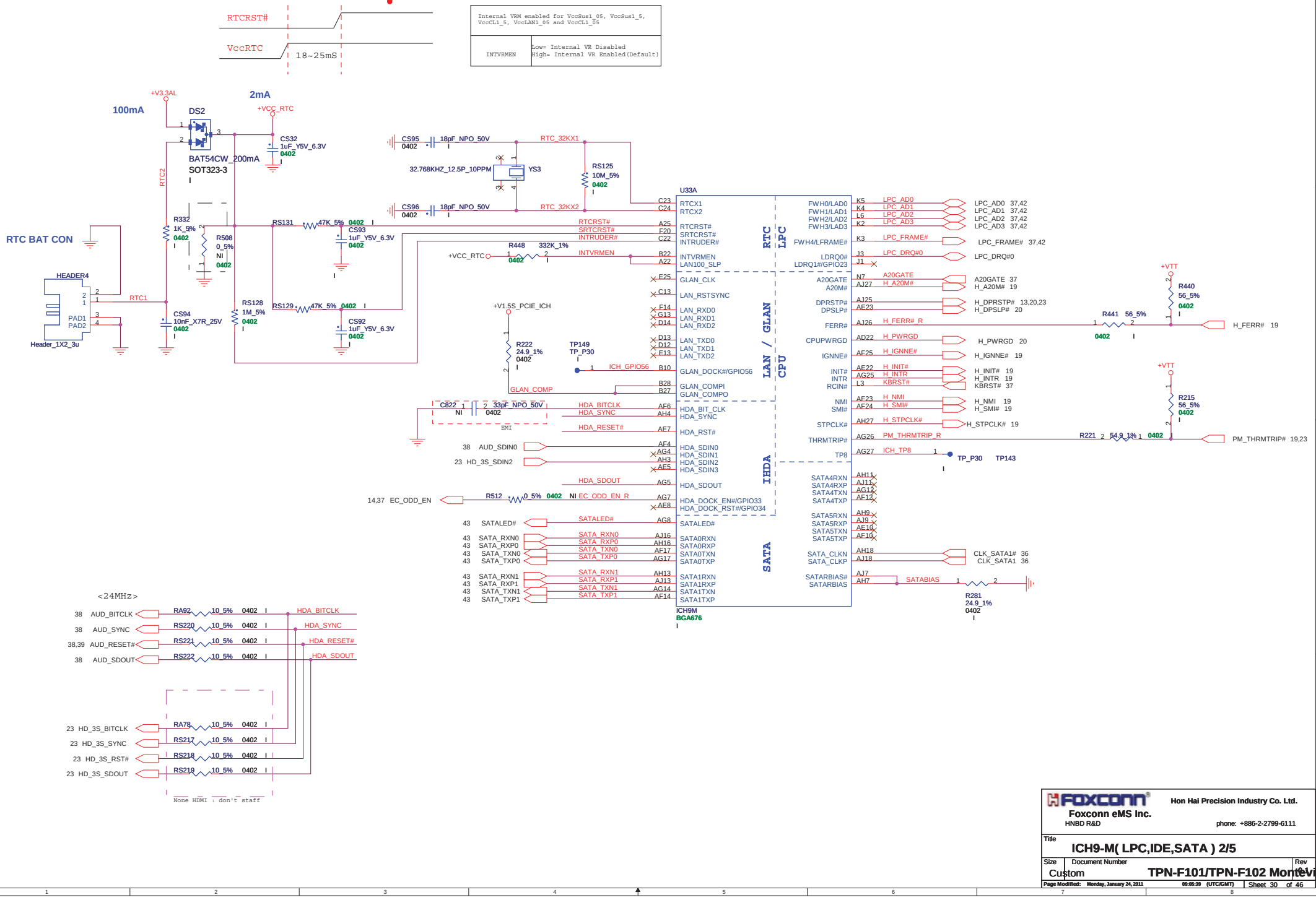
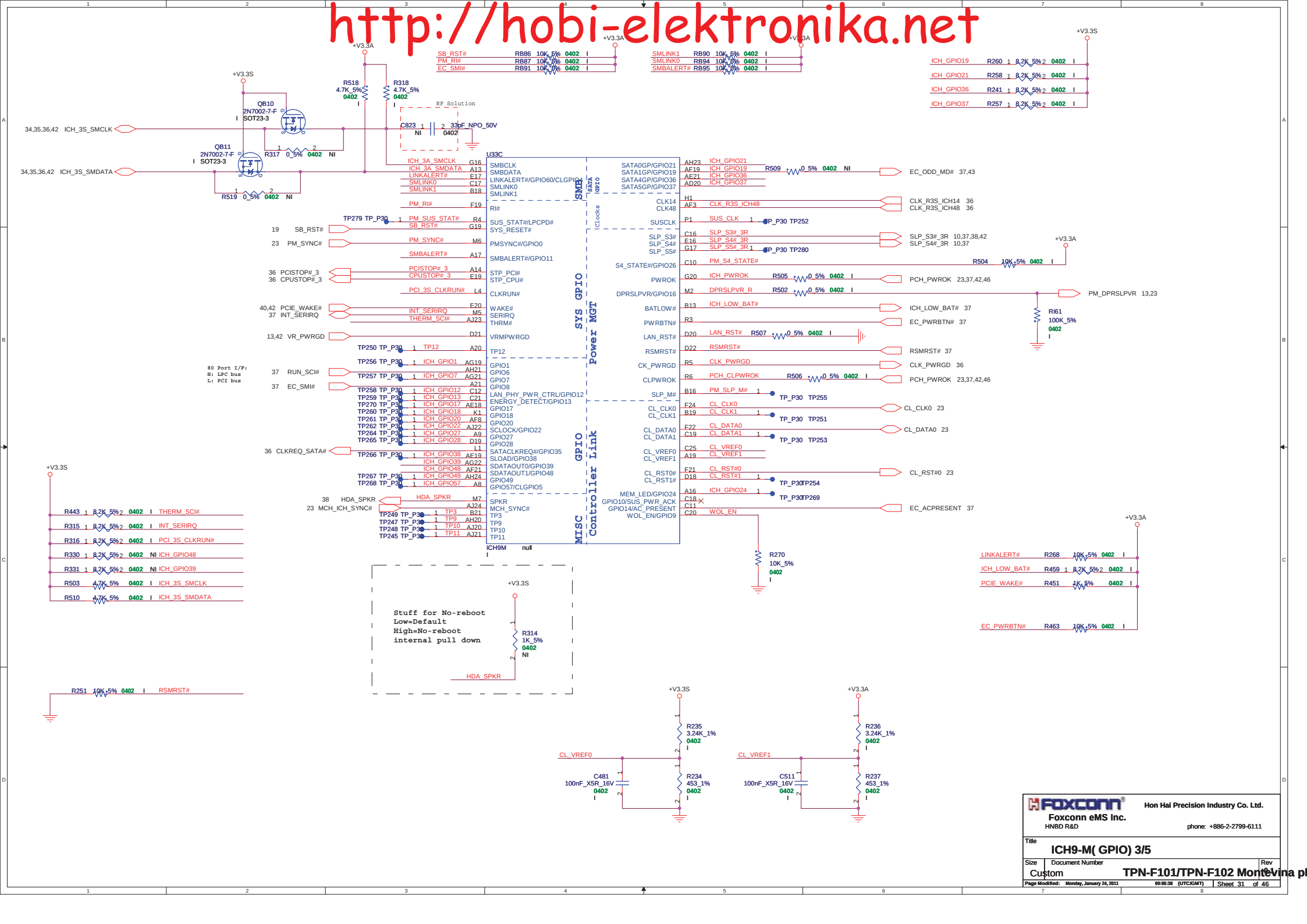
Title: ICH9-M(PCI/DMI/USB/PCIE) 1/5

Size: Custom | Document Number: TPN-F101/TPN-F102 Montevina pl | Rev: 0.1

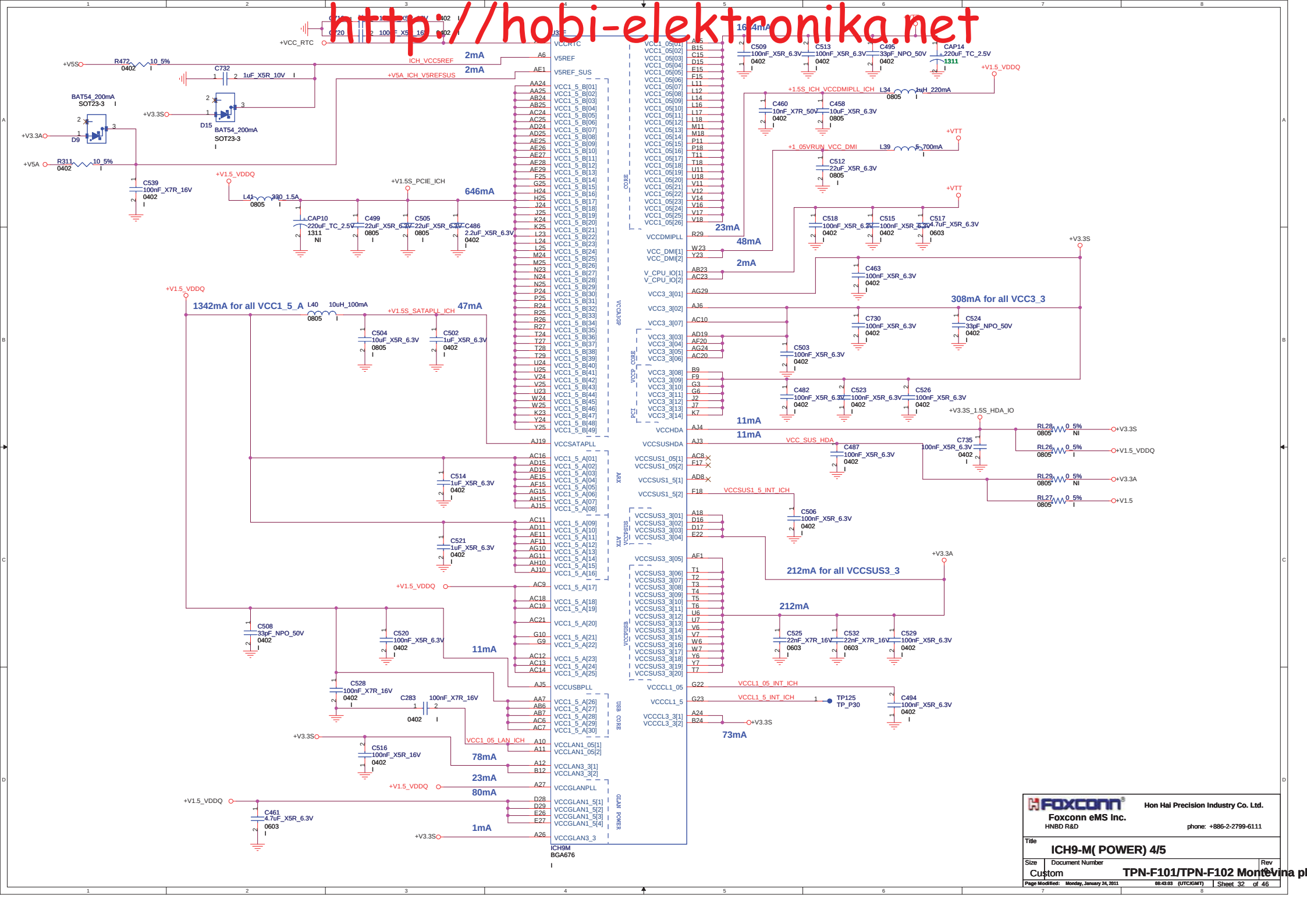
Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT) | Sheet 29 of 46



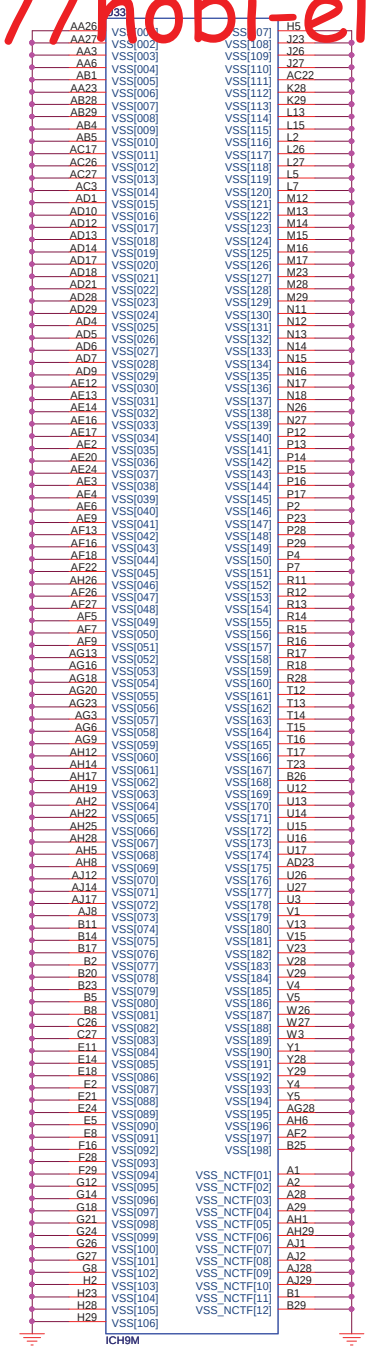
Hon Hai Precision Industry Co. Ltd.	Foxconn eMS Inc.
HNBD R&D	phone: +886-2-2799-6111
Title	ICH9-M(LPC,IDE,SATA) 2/5
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina pl
Rev: 0.1	
Page Modified: Monday, January 24, 2011 09:05:39 (UTC/GMT)	Sheet 30 of 46



Foxconn	Hon Hai Precision Industry Co. Ltd.
Foxconn eMS Inc.	
HNBD R&D	phone: +886-2-2799-6111
Title	ICH9-M(GPIO) 3/5
Size	Custom
Document Number	TPN-F101/TPN-F102 Montevina pl
Rev	0.1
Page Modified:	Monday, January 24, 2011 09:05:38 (UTC/GMT)
Sheet	31 of 46



Hon Hai Precision Industry Co. Ltd.		
Foxconn eMS Inc.		
HNBD R&D	phone: +886-2-2799-6111	
Title: ICH9-M(POWER) 4/5		
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina pl	Rev: 0.1
Page Modified: Monday, January 24, 2011 08:43:03 (UTC/GMT)	Sheet 32 of 46	



FOXCONN	Hon Hai Precision Industry Co. Ltd.	
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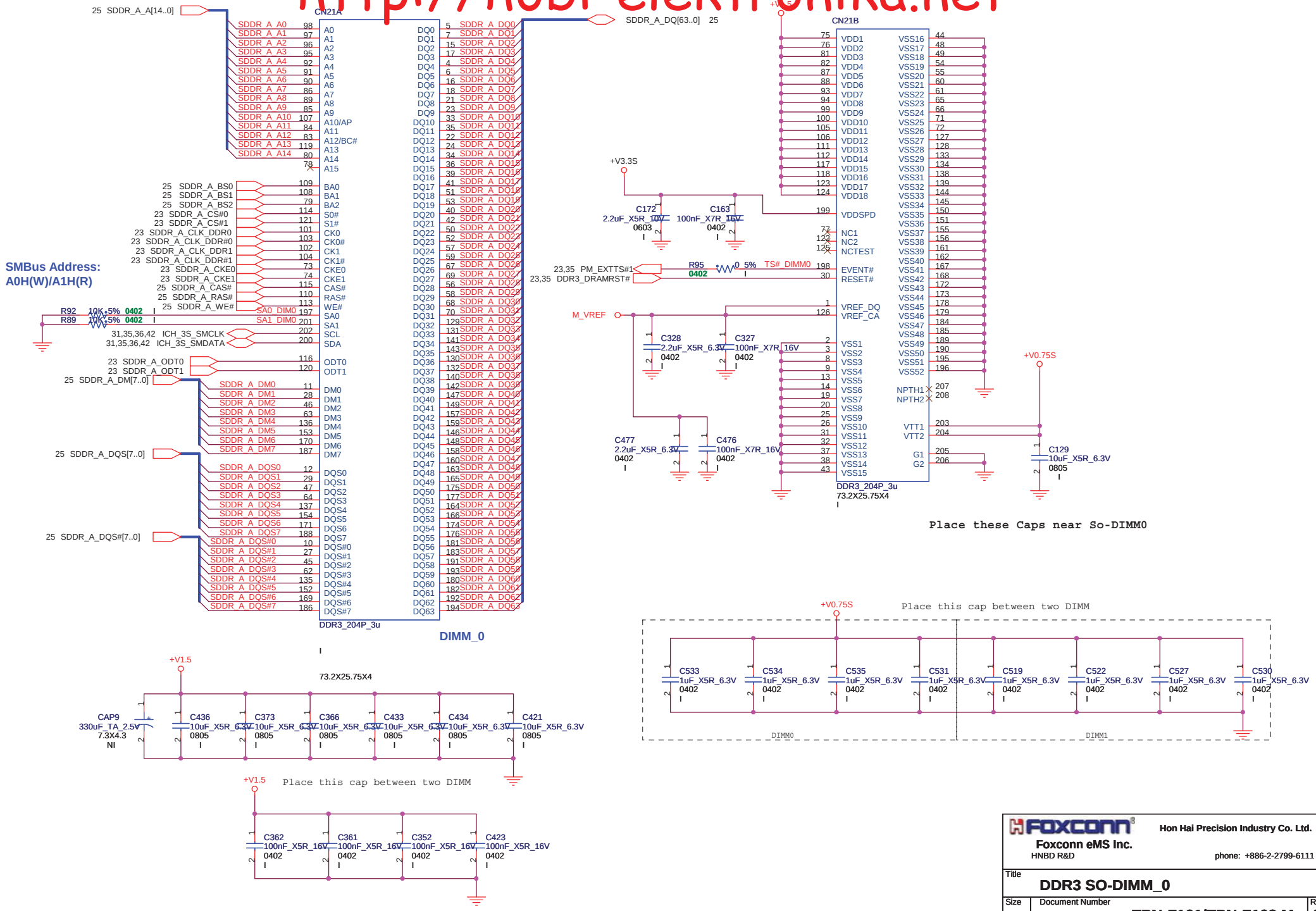
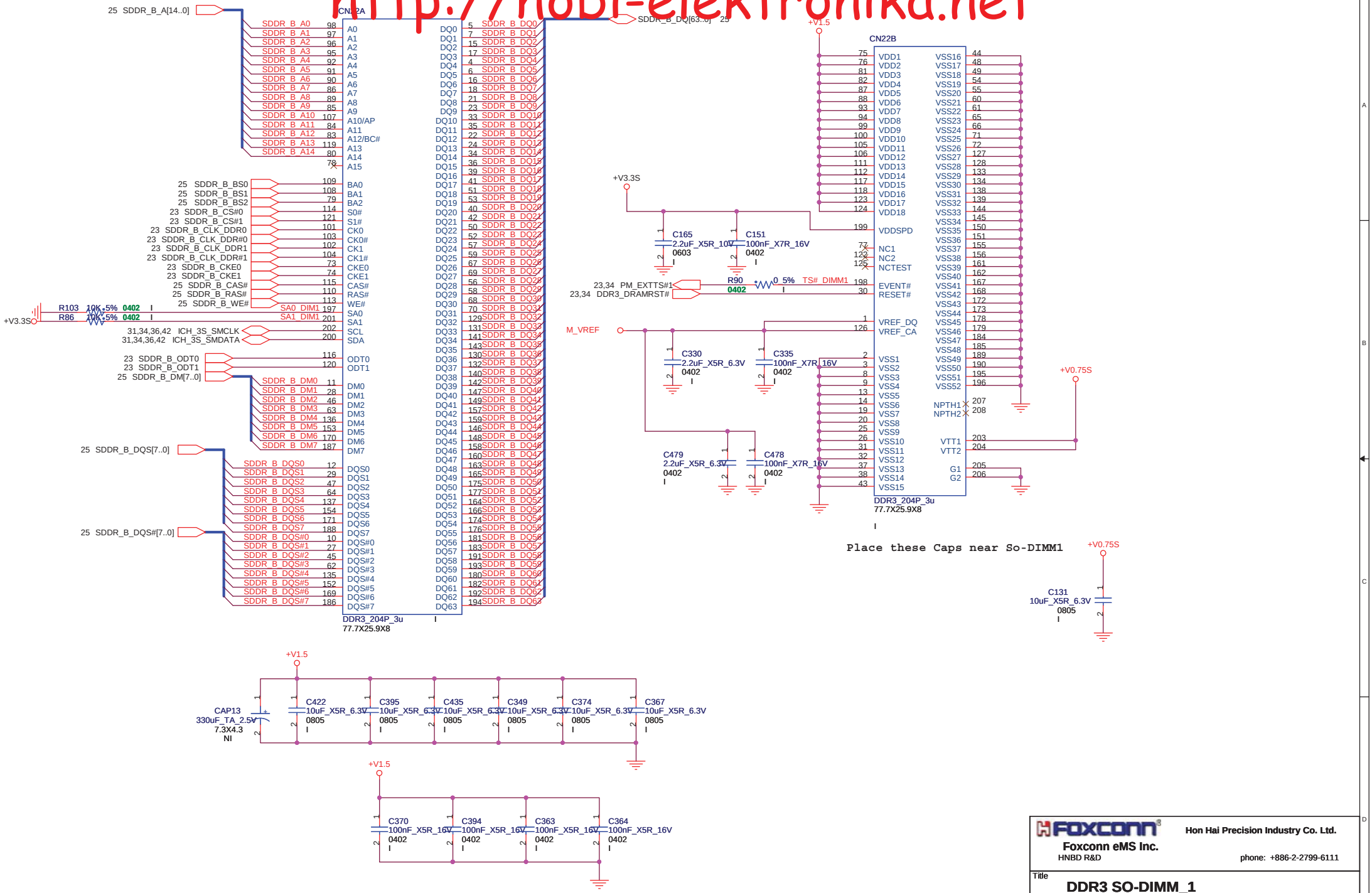
HNBD R&D	phone: +886-2-2799-6111	
Title	ICH9-M(GND) 5/5	
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina pl	Rev: 0.1
Page Modified: Monday, January 24, 2011 08:43:02 (UTC/GMT)	Sheet 33 of 46	





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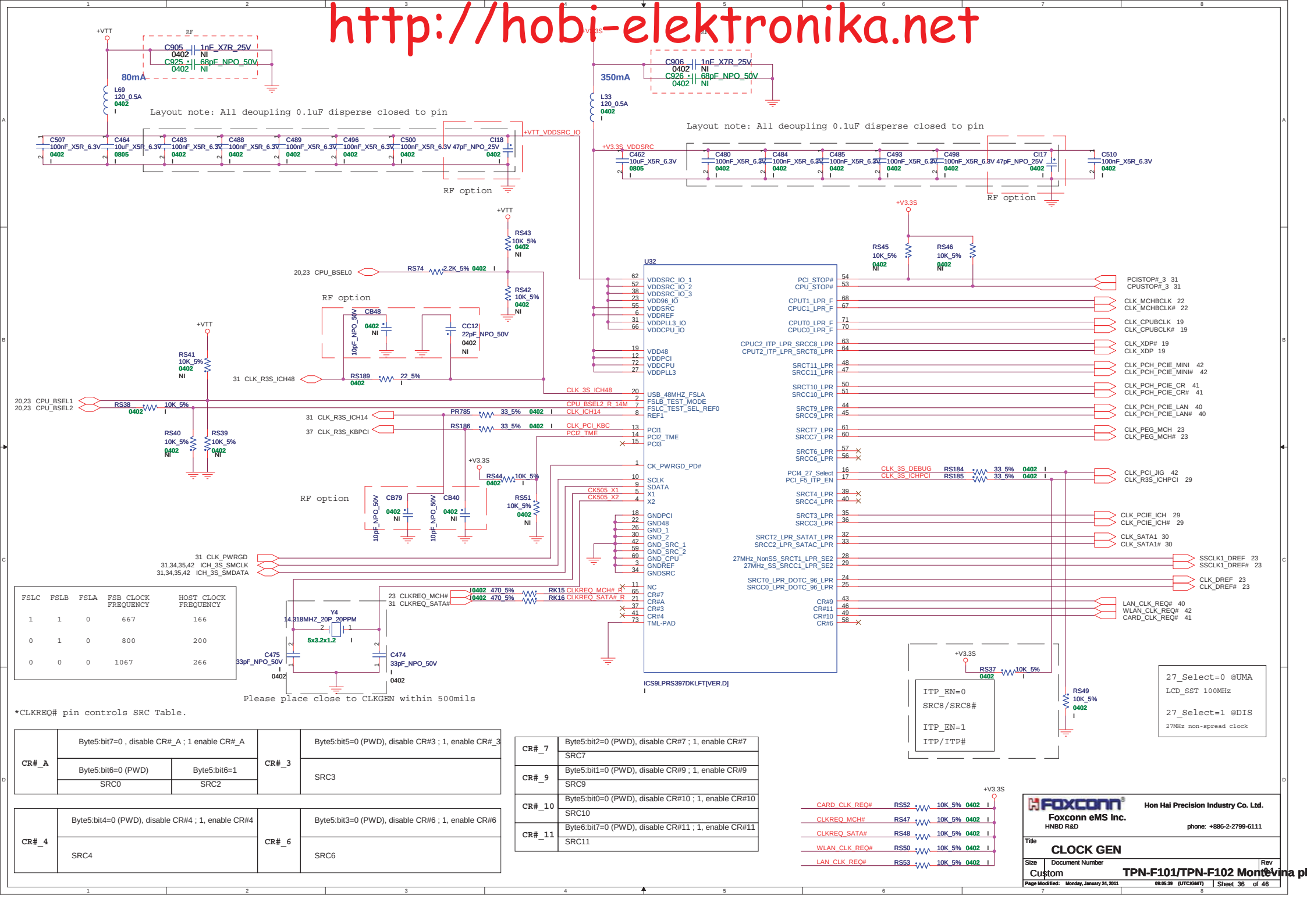
HNBD R&D	phone: +886-2-2799-6111
Title	DDR3 SO-DIMM_1
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina
Rev: 1A	
Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT)	Sheet 35 of 46



FSLC	FSLB	FSLA	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266

*CLKREQ# pin controls SRC Table.

CR#_A	Byte5:bit7=0 , disable CR#_A ; 1 enable CR#_A		CR#_3	Byte5:bit5=0 (PWD), disable CR#3 ; 1, enable CR#_3
	Byte5:bit6=0 (PWD)	Byte5:bit6=1		SRC3
	SRC0	SRC2		

CR#_4	Byte5:bit4=0 (PWD), disable CR#4 ; 1, enable CR#4		CR#_6	Byte5:bit3=0 (PWD), disable CR#6 ; 1, enable CR#6
	SRC4			SRC6

CR#_7	Byte5:bit2=0 (PWD), disable CR#7 ; 1, enable CR#7
	SRC7
CR#_9	Byte5:bit1=0 (PWD), disable CR#9 ; 1, enable CR#9
	SRC9
CR#_10	Byte5:bit0=0 (PWD), disable CR#10 ; 1, enable CR#10
	SRC10
CR#_11	Byte6:bit7=0 (PWD), disable CR#11 ; 1, enable CR#11
	SRC11

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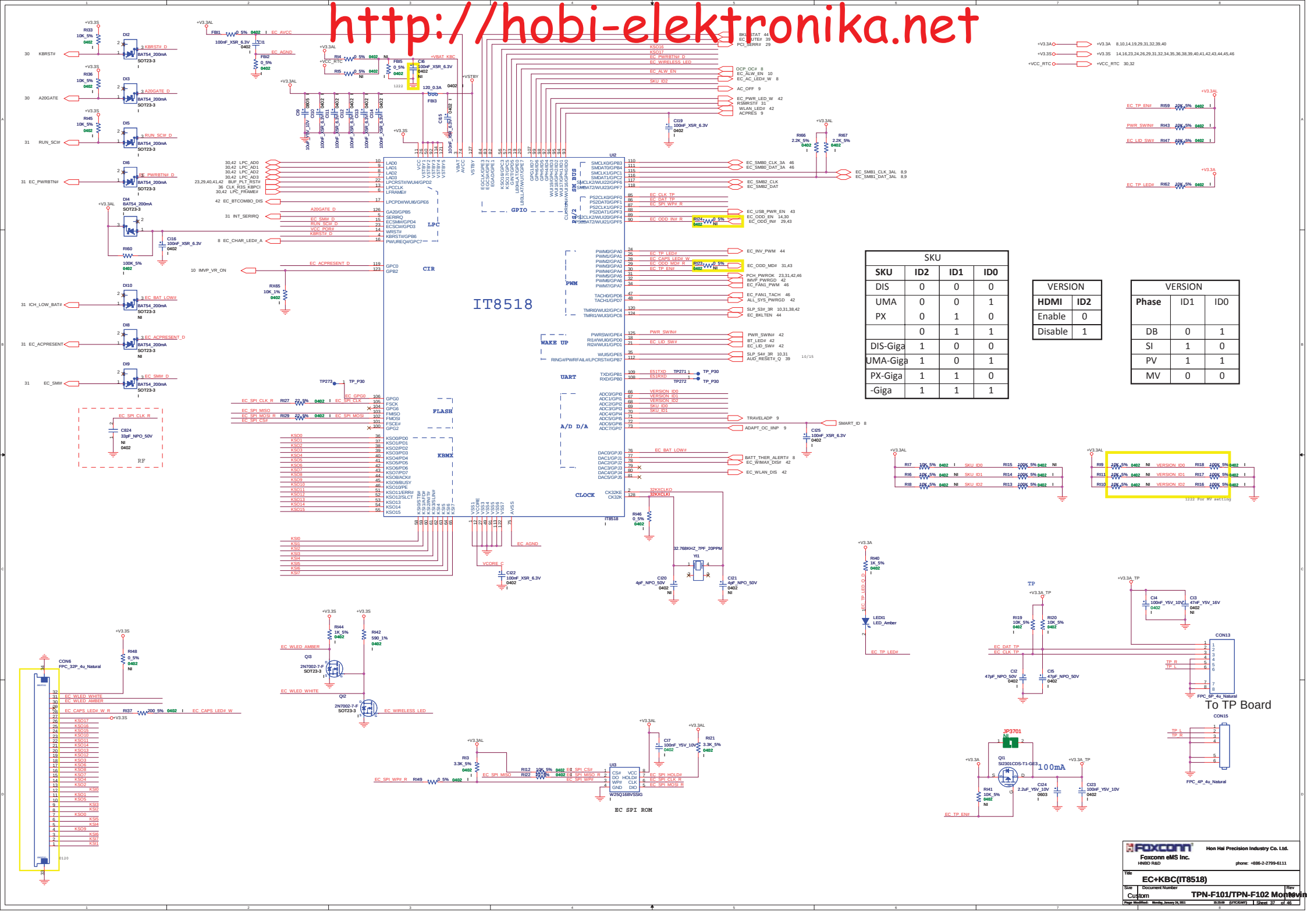

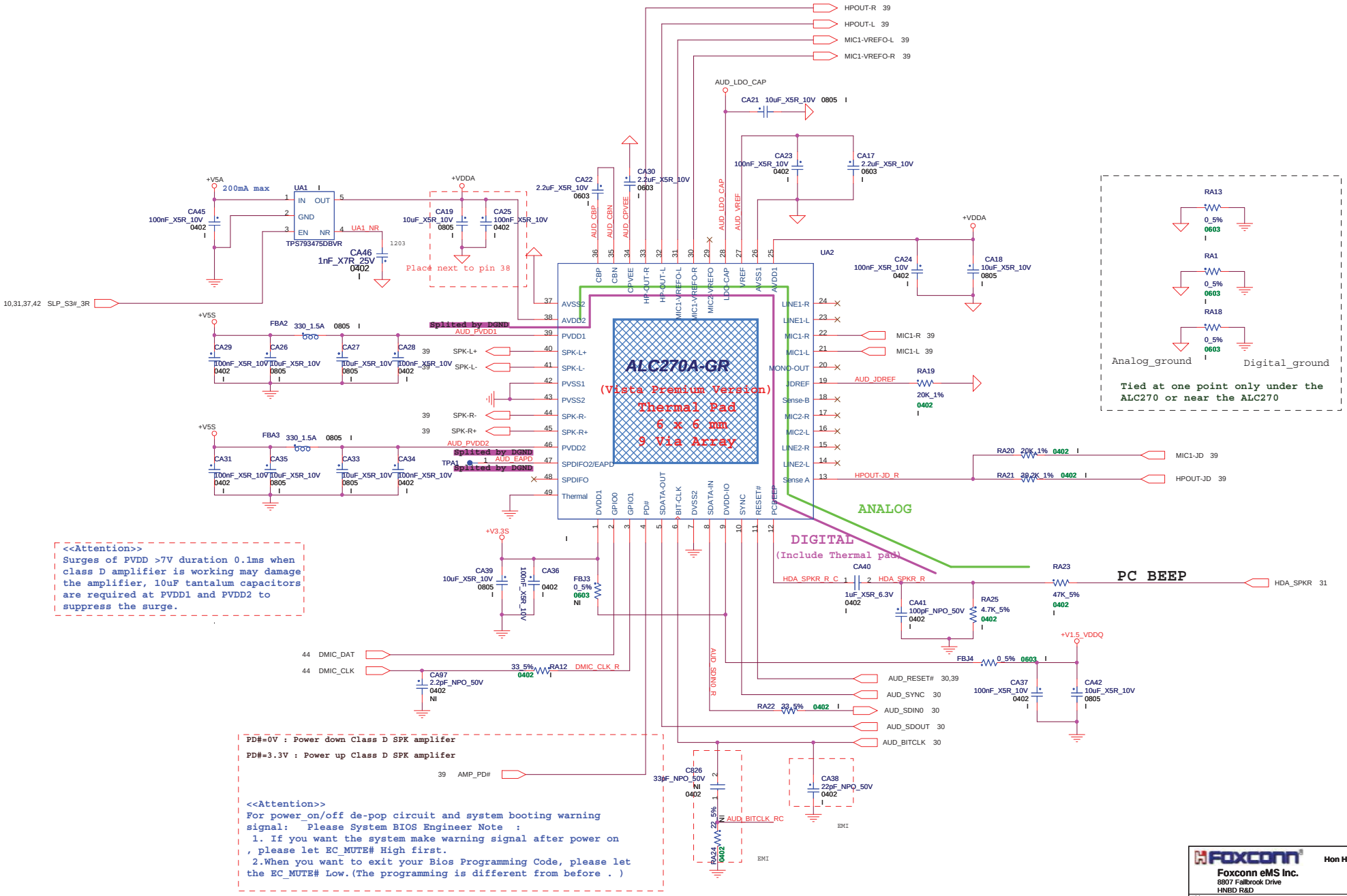

Foxconn
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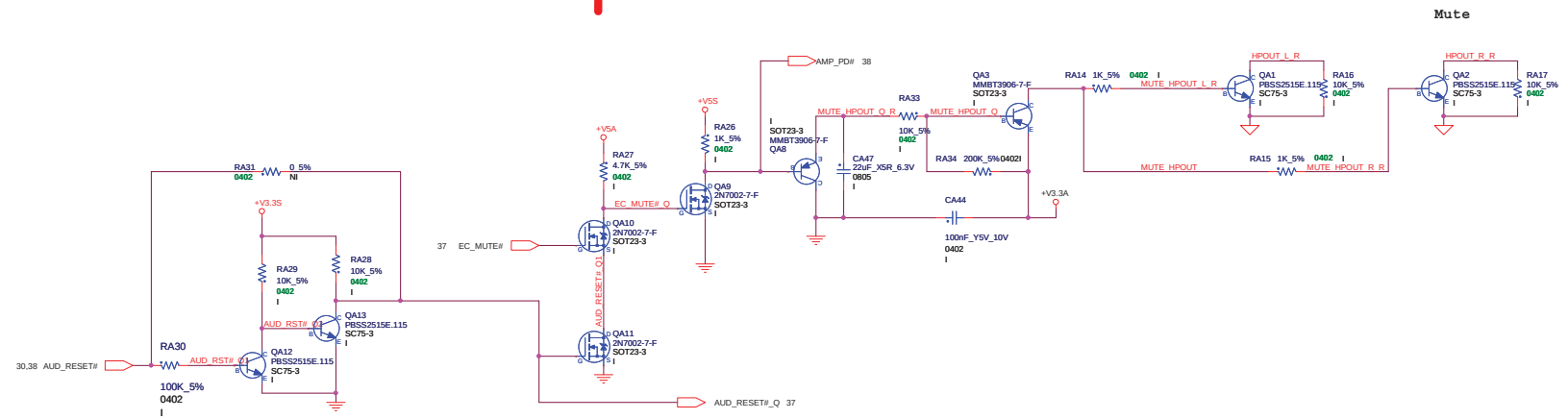
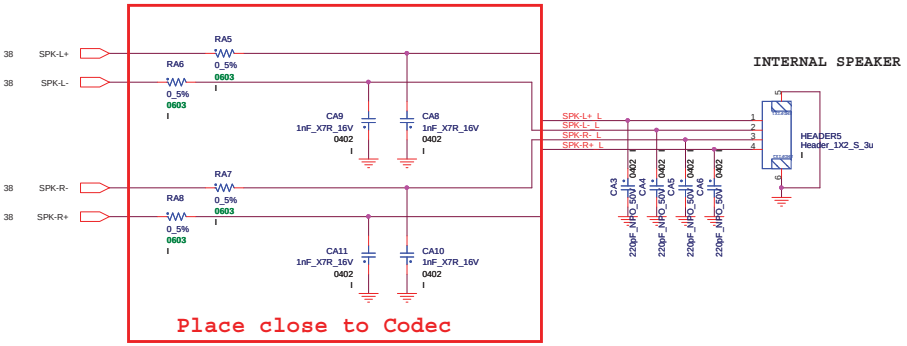
fax: (281) 668-1515

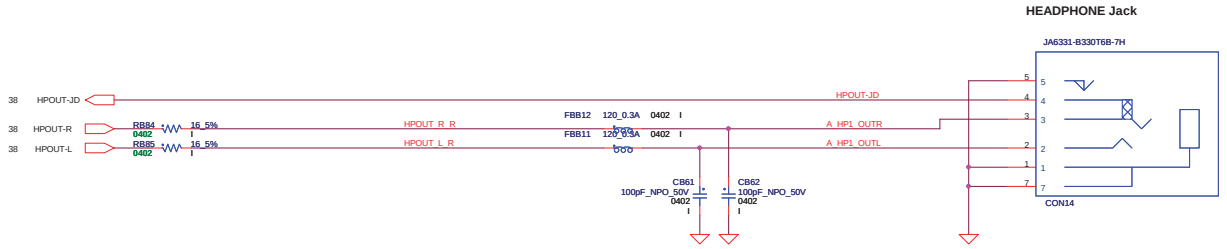
Title: Audio(Codec)

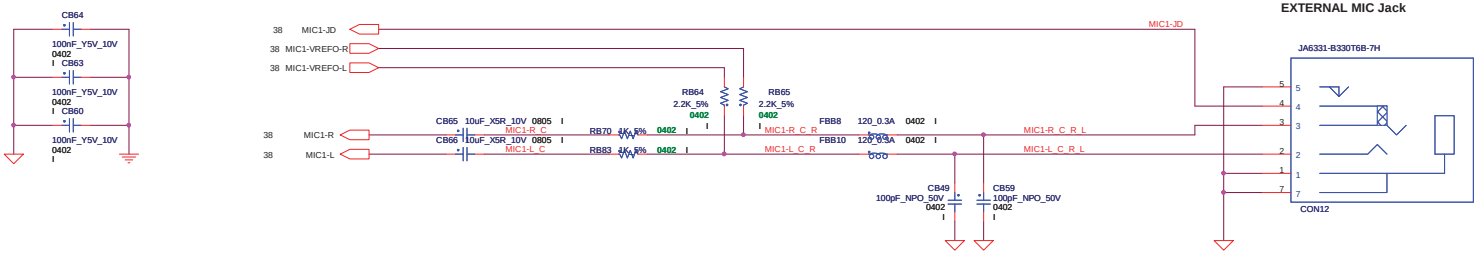
Size: Custom | Document Number: TPN-F101/TPN-F102 Montevina platform | Rev: 0.1

Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT) | Sheet 38 of 46









Foxconn
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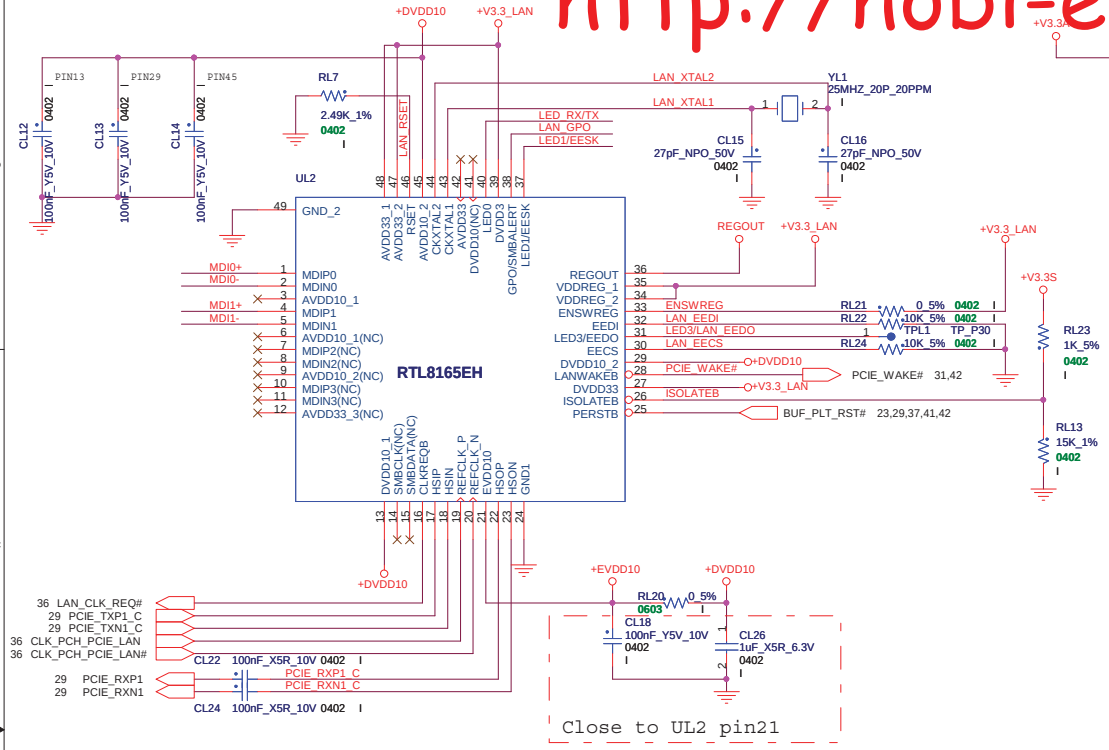
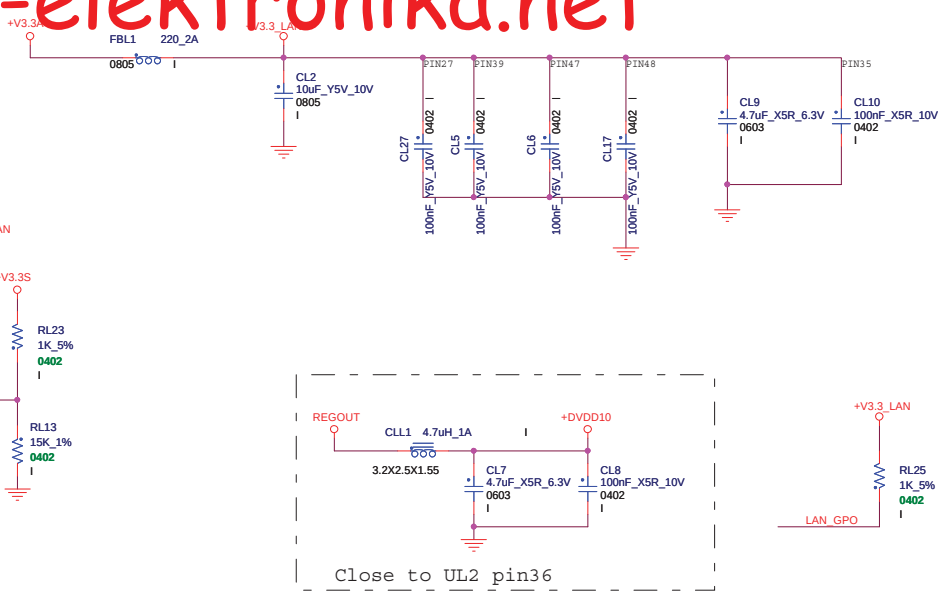
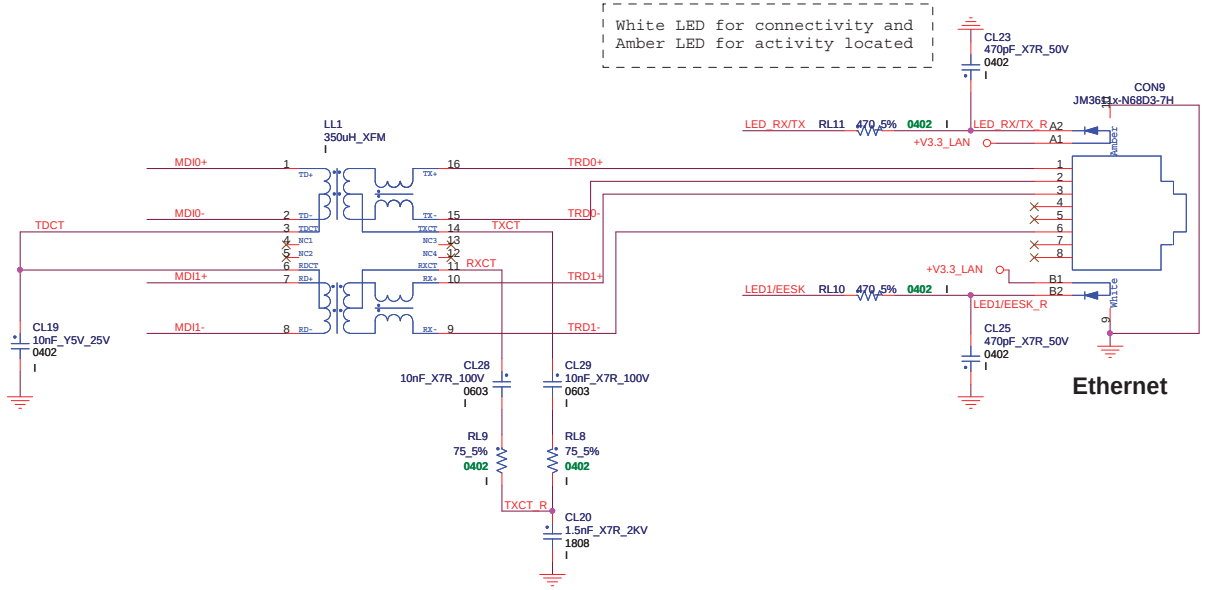
Title: Audio(Jack/Speaker/Mic)

Size | Document Number | Rev
Custom | TPN-F101/TPN-F102 Montevina platform | 0.1

Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT) | Sheet 39 of 46



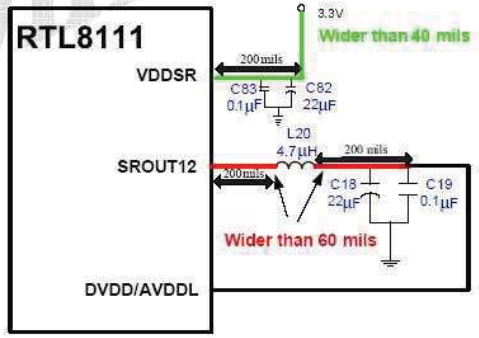




7.1. PCB Layout

- The input 3.3V power trace connected to the VDDSR pin should be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200mils (0.5cm) of the VDDSR pin to prevent input voltage overshoot.
- The output power trace out of the SROUT12 pin should be wider than 60mils.
- Keep L20 within 200mils (0.5cm) of the SROUT12 pin.
- Keep C18 and C19 within 200mils (0.5cm) of L20 to ensure stable output power and better power efficiency.
- Both C18 and C82 are strongly recommended to be ceramic capacitors.

Note: Violation of the above rules will damage the IC.



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Title		
LAN		
Size	Document Number	Rev
Custom	TPN-F101/TPN-F102 Montevina platform	0.2

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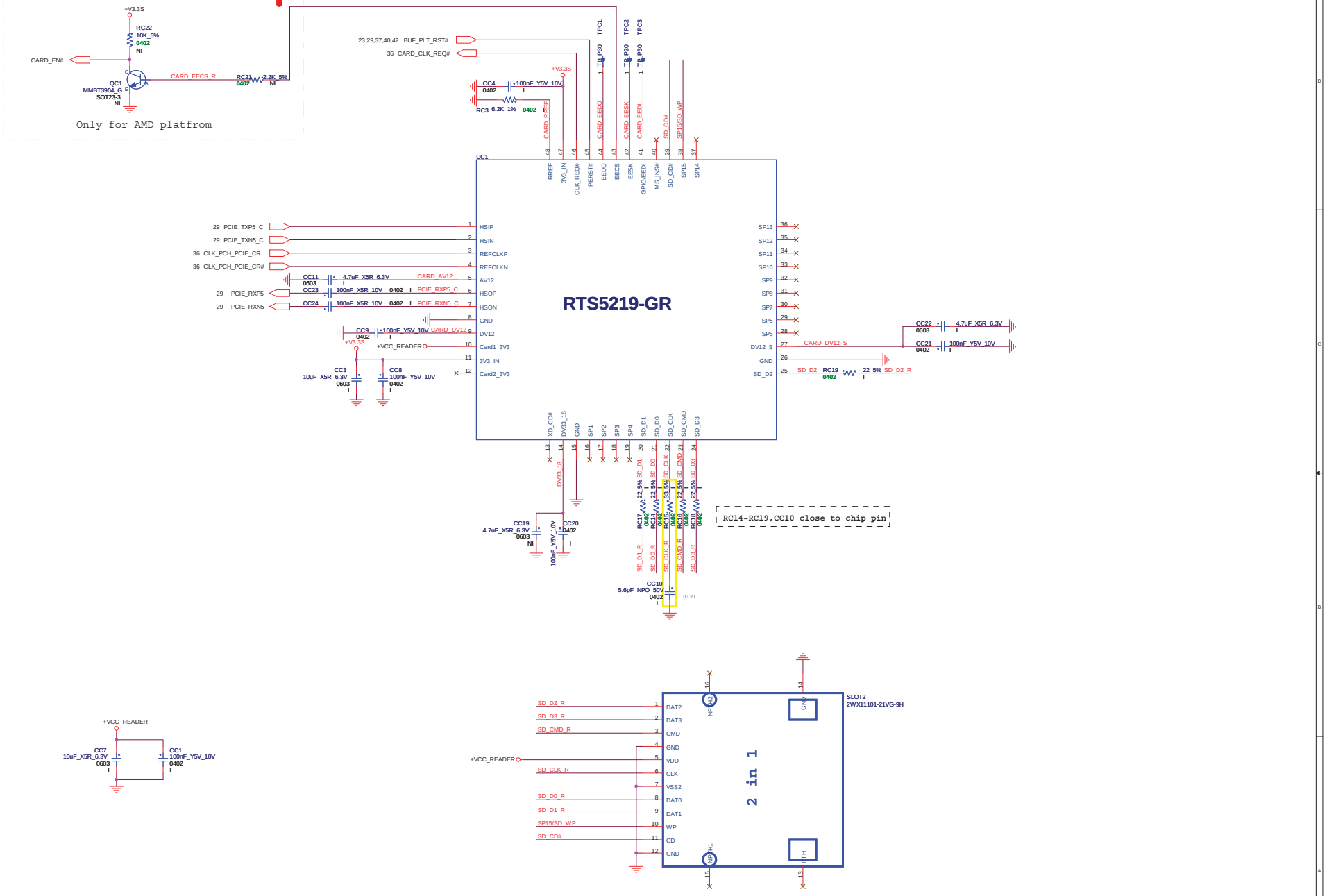
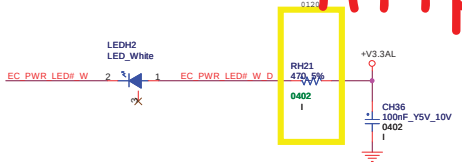
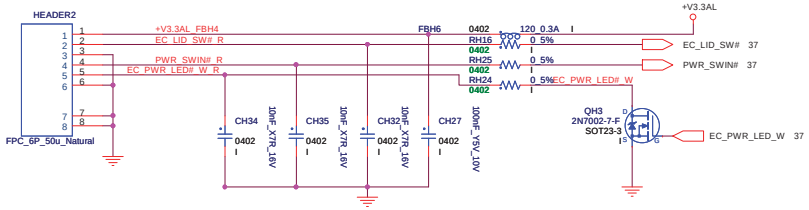


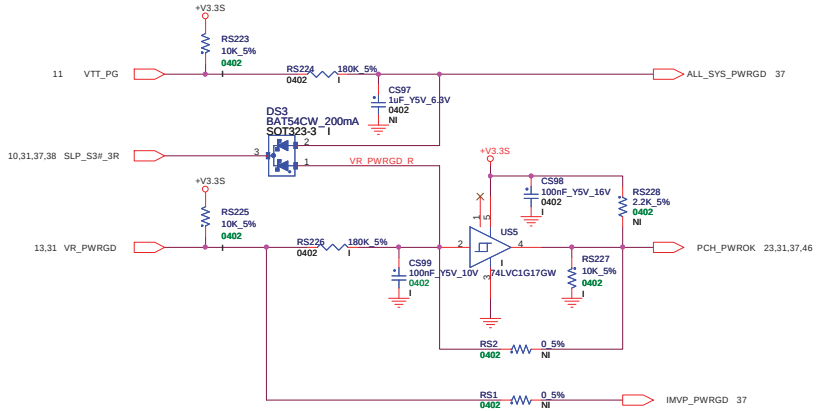


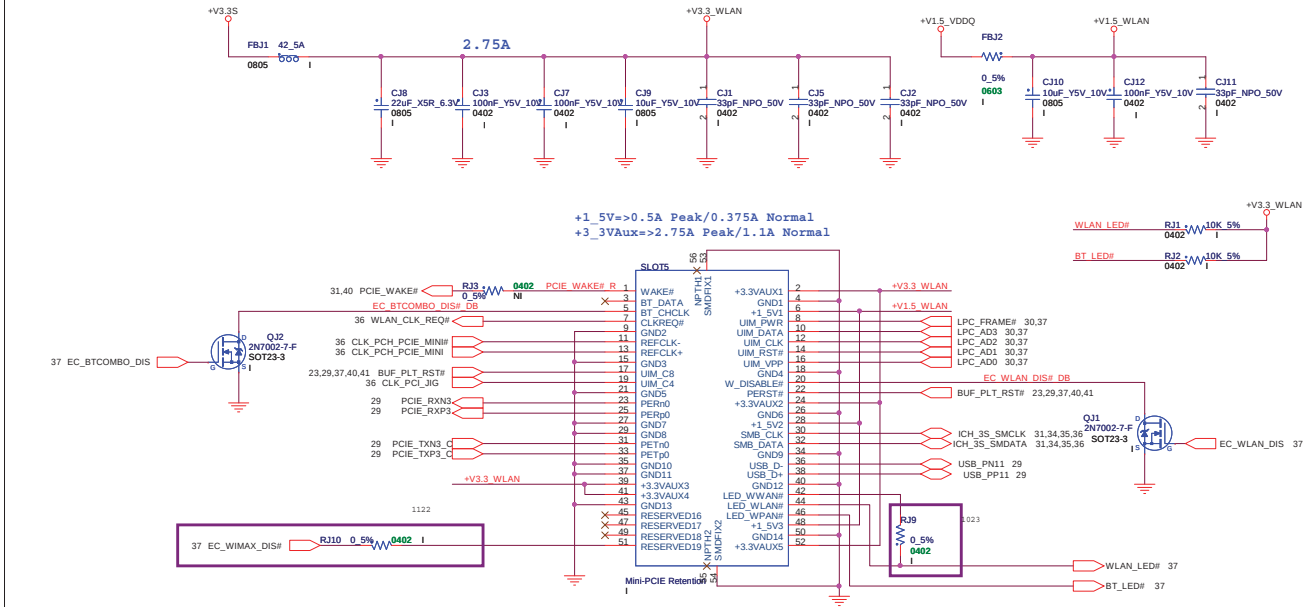
PWR LED

PWR Board CONN.

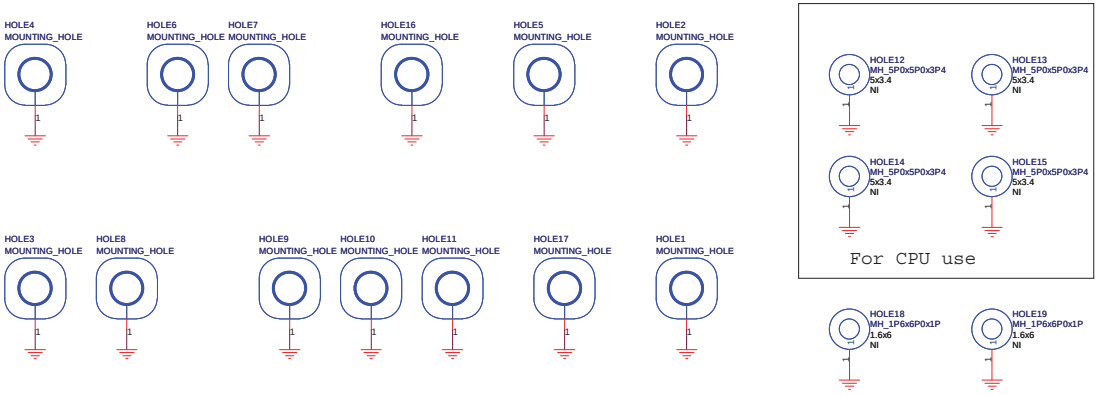


SEQUENCE CIRCULT

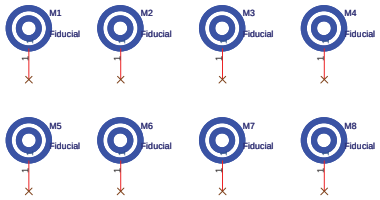




Half Mini Card for WLAN



Mounting HOLE



Fiducial Mark

Foxconn eMS Inc.
8807 Fallbrook Drive
HNBD R&D
Hon Hai Precision Industry Co. Ltd.
phone: +886-2-2799-6111
fax: (281) 668-1515

Title: Mini PCIE&BT

Size | Document Number: Custom TPN-F101/TPN-F102 Montevina platform | Rev: 0.1

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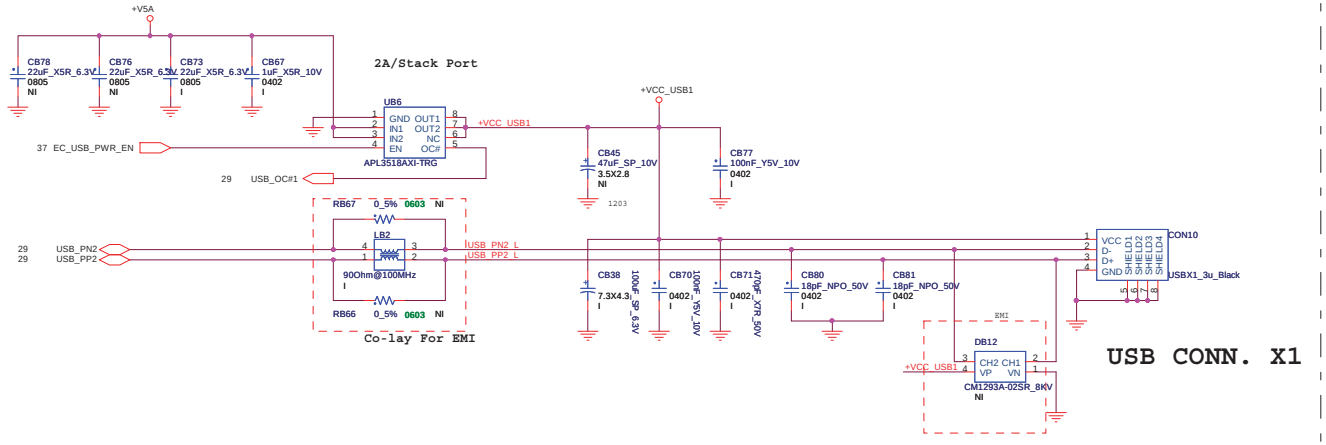
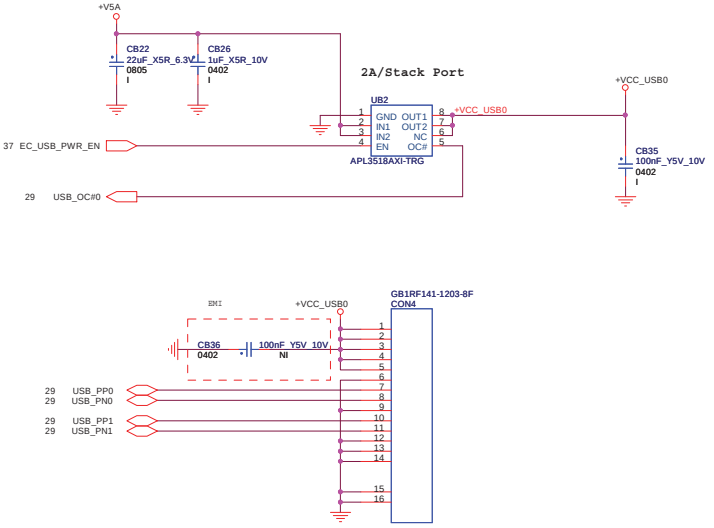
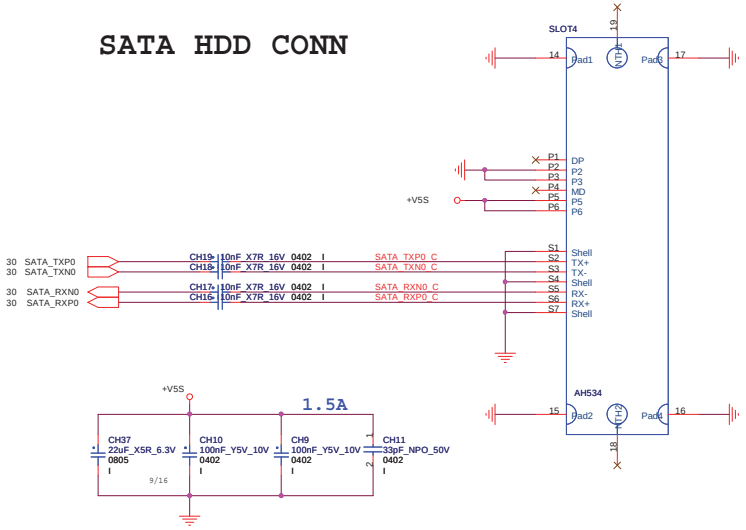


USB CONN. X1

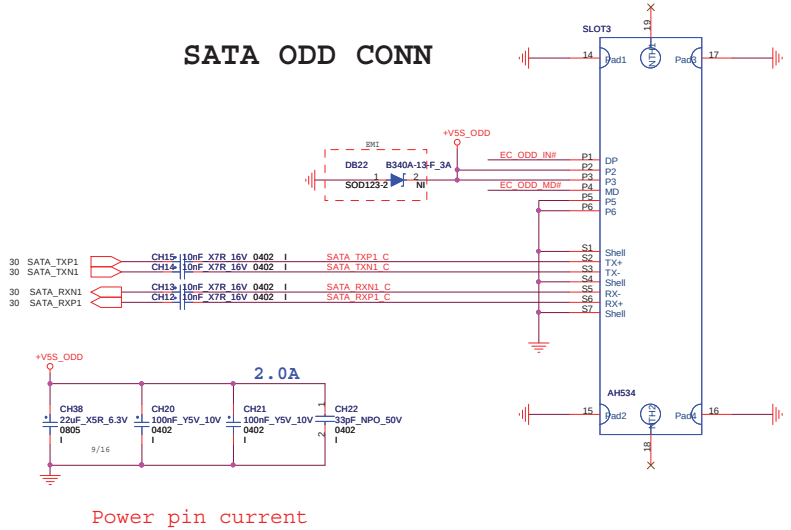


USB Board CONN.

SATA HDD CONN

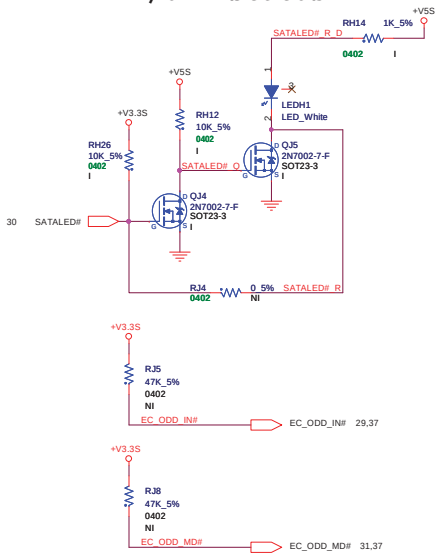


SATA ODD CONN



Power pin current
max. 1300 mA (less 2ms)

HDD/ODD Status LED



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Title: USB/HDD/ODD		
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina platform	Rev: 0.1
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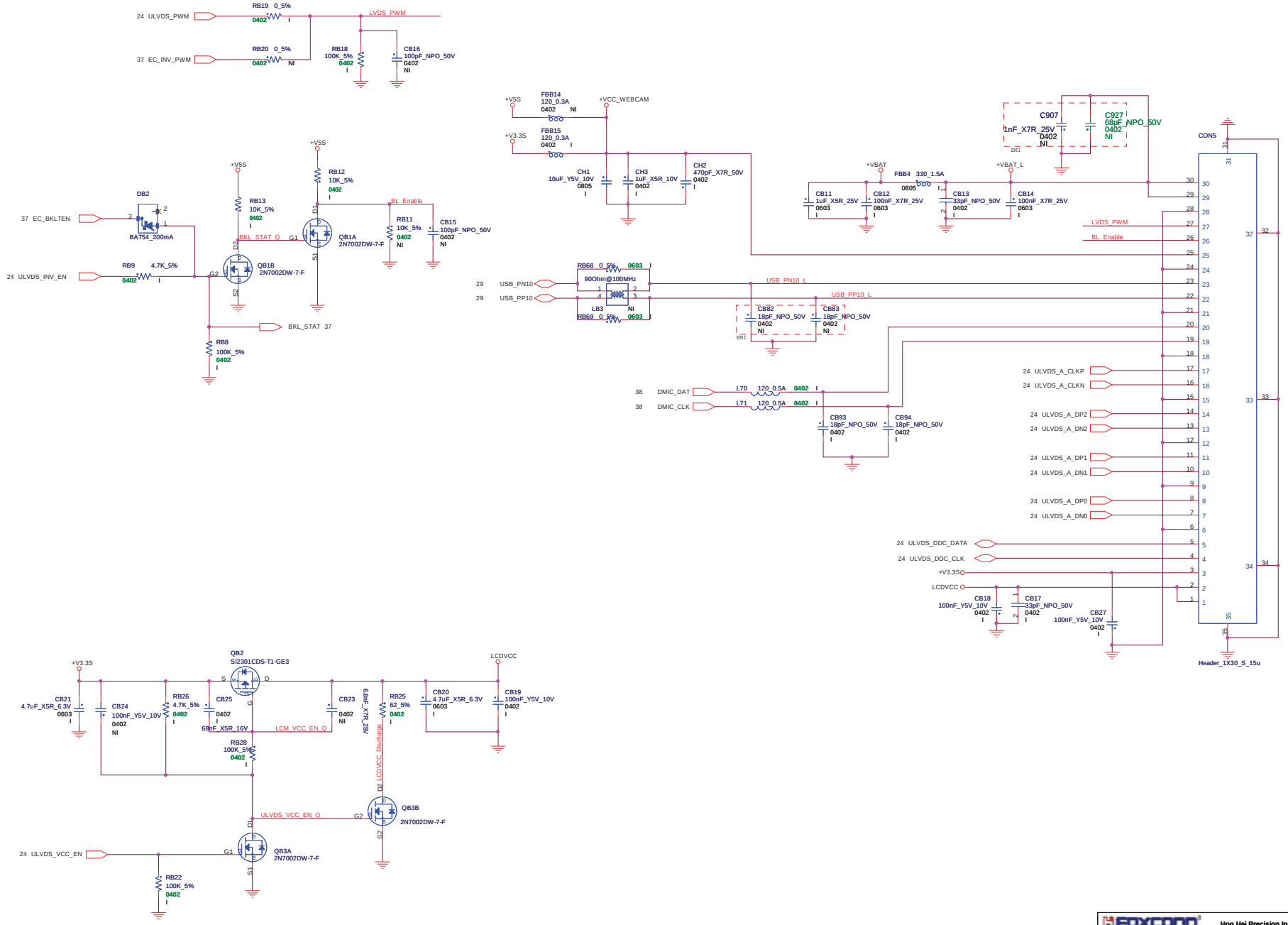

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Title: LVDS/Webcam		
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina platform	Rev: 0.1
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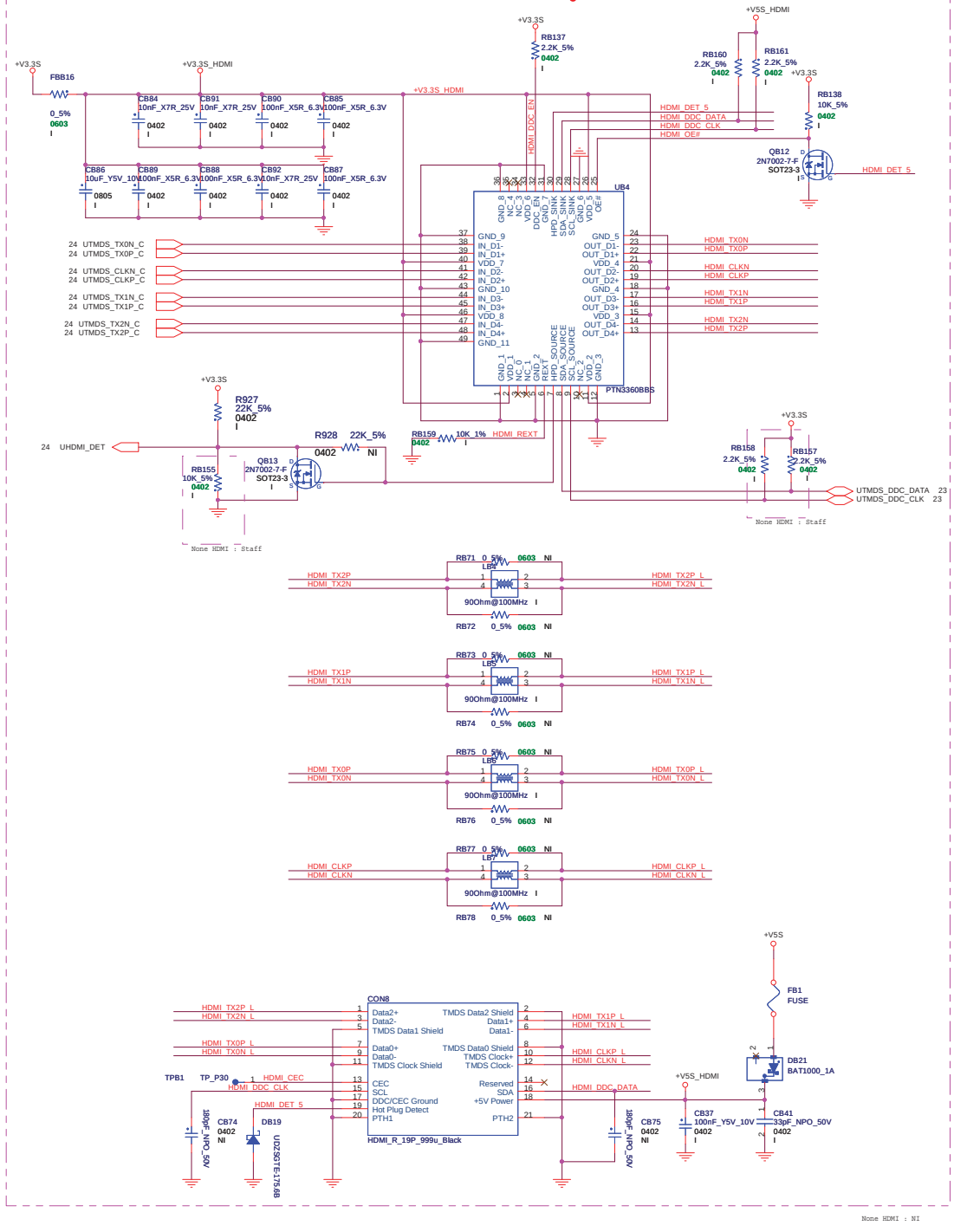
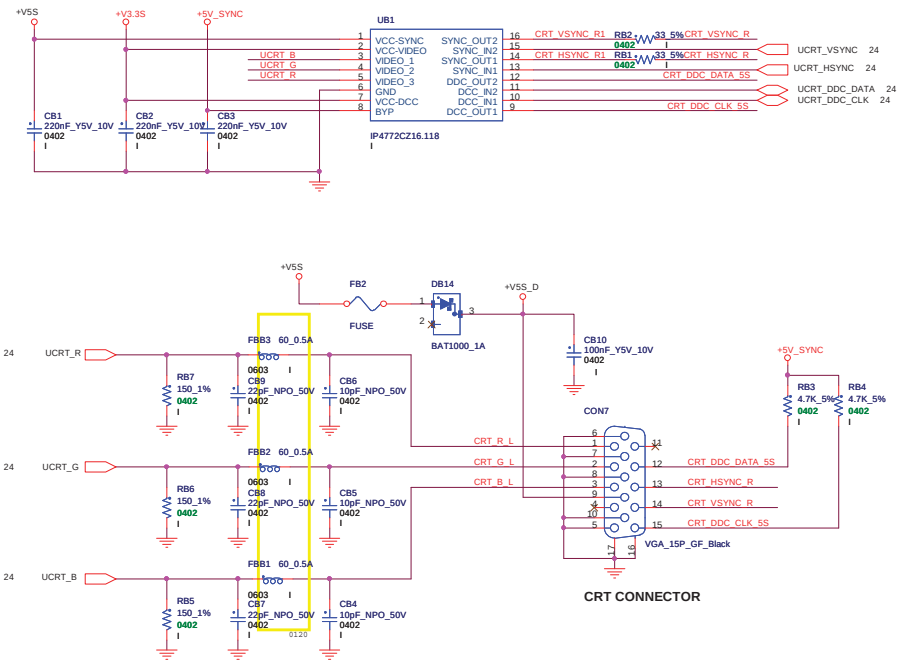


CRT



CRT CONNECTOR

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Title: HDMI/CRT		
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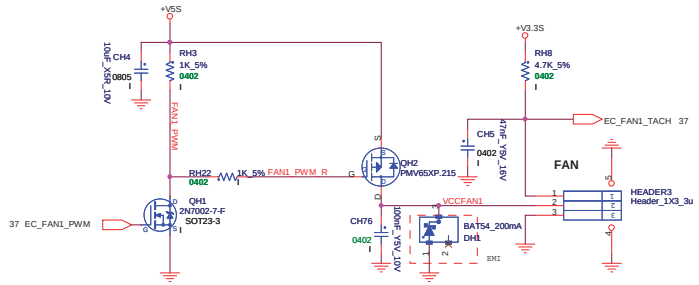
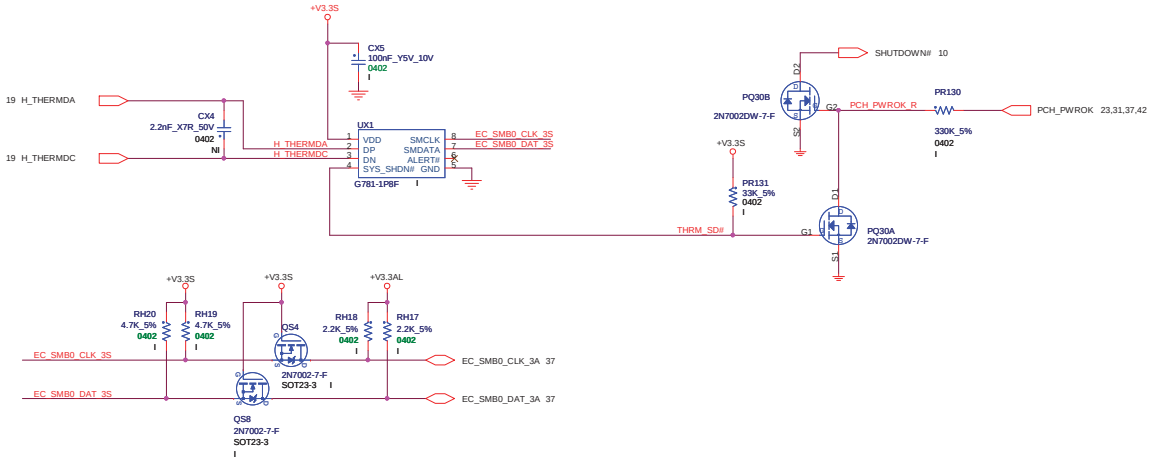
Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT)		Sheet 45 of 46

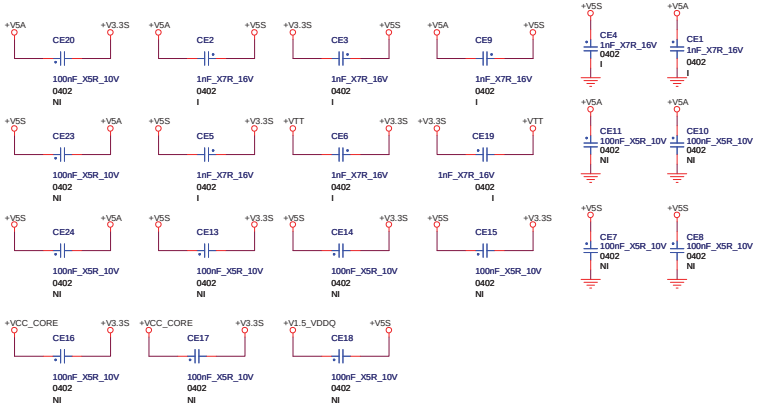
FAN



THERMAL SENSOR



stitch cap



RF Solution

Foxconn eMS Inc. 8807 Fallbrook Drive HNBD R&D	Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111 fax: (281) 668-1515	
Title: Thermal/Fan/Control		
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina platform	Rev: 0.1
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