

MODEL NAME : **KIU20**
PCB NO : **LA-5091P (DA60000BR10)**
BOM P/N : **43169831L02**

Compal Confidential

Bear Schematics Document

Intel Diamondville Processor with Calistoga(945GSE) + DDRII + ICH7M

2009-3-31

REV: 1.0

@ : Nopop Component

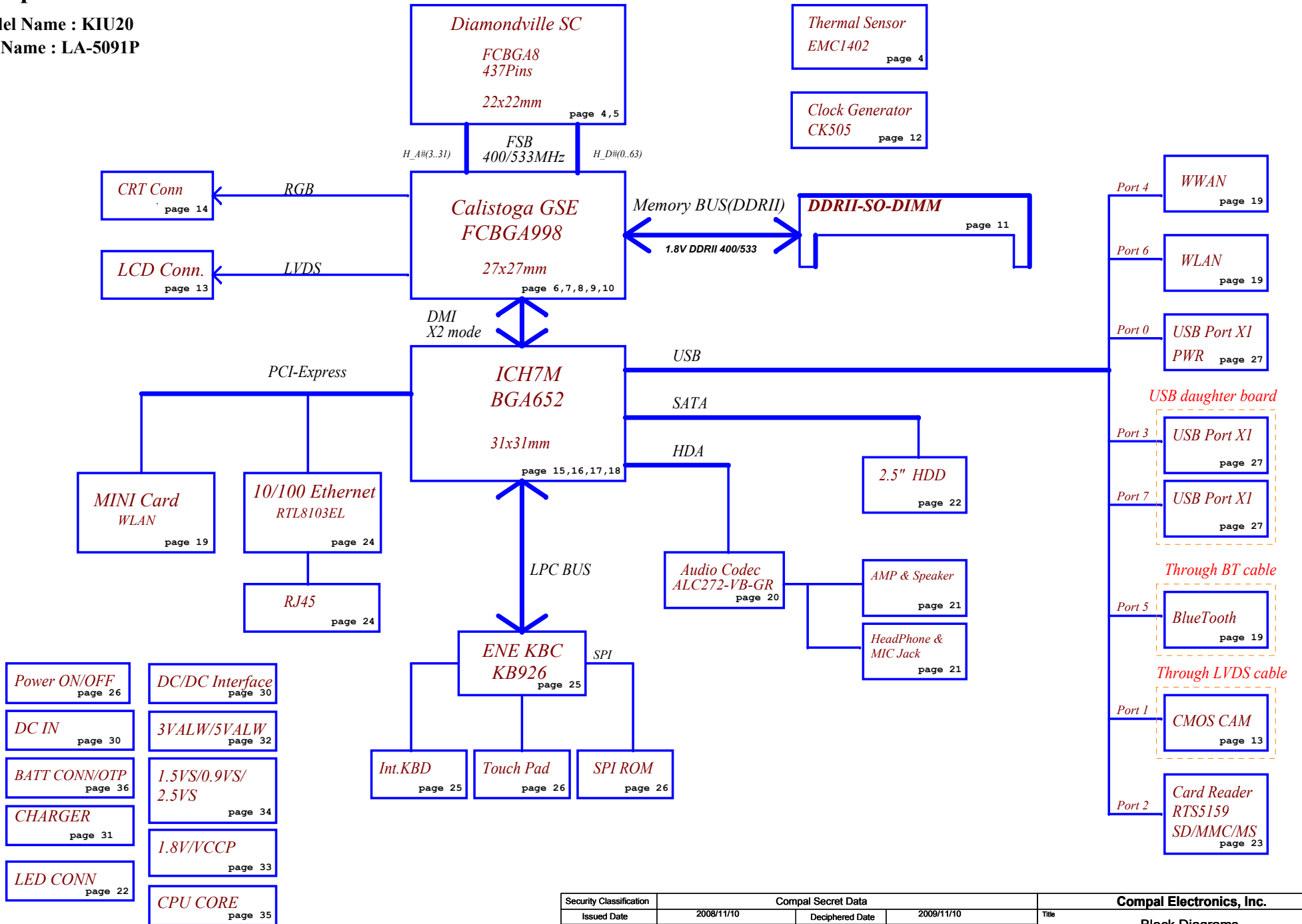
1@ : For N280 only

2@ : For N270 only

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File Name : LA-5091P



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- 3VALW/5VALW page 32
- 1.5VS/0.9VS/2.5VS page 34
- 1.8V/VCCP page 33
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ZZZ



PCB

DA60000BR10

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VS	VS always on power rail	ON	ON	ON*
+RTCBATT	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 25)

ID	BRD ID	Ra	Rb	Vab
0	R01 (SSI)	NC	0	0V
1	R02 (ST)	100K	8.2K	0.25V
2	R10 (X build)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

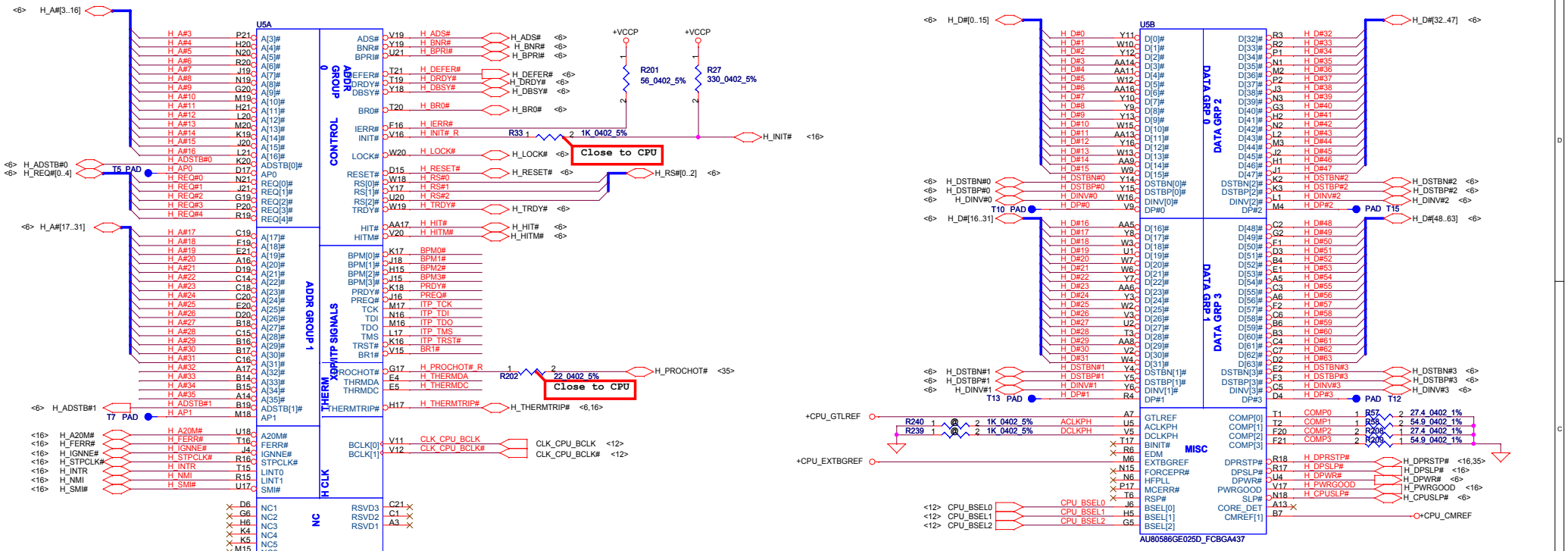
EC SM Bus2 address

Device	Address
EMC1402	1001 100X b

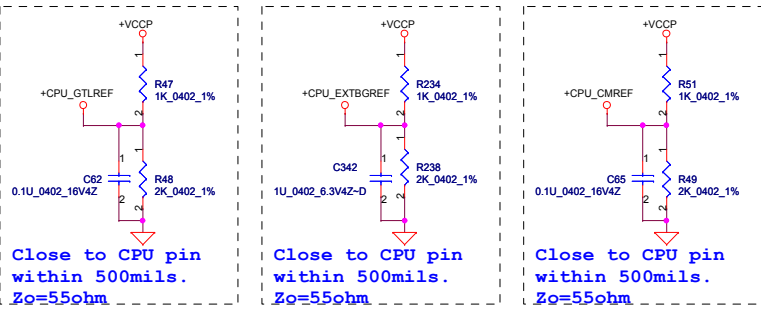
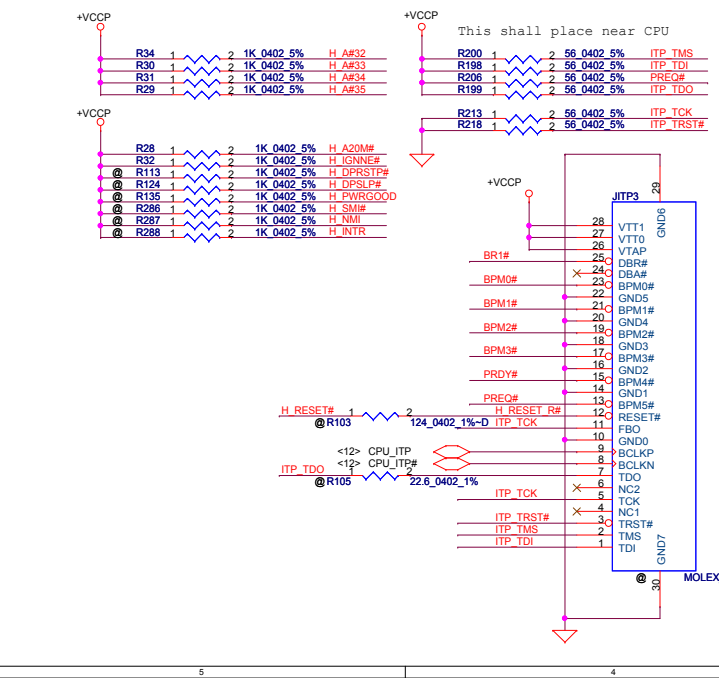
ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

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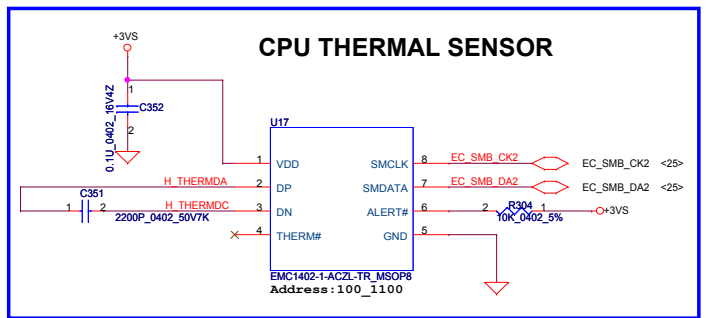


CPU N270 P/N: SA00002031L
 CPU N280 P/N: SA000031F1L



Layout note:
 COMP0,2 connect with Zo=27.4ohm +/-15%, make trace length shorter than 0.5"
 COMP1,3 connect with Zo=55ohm +/-15%, make trace length shorter than 0.5"

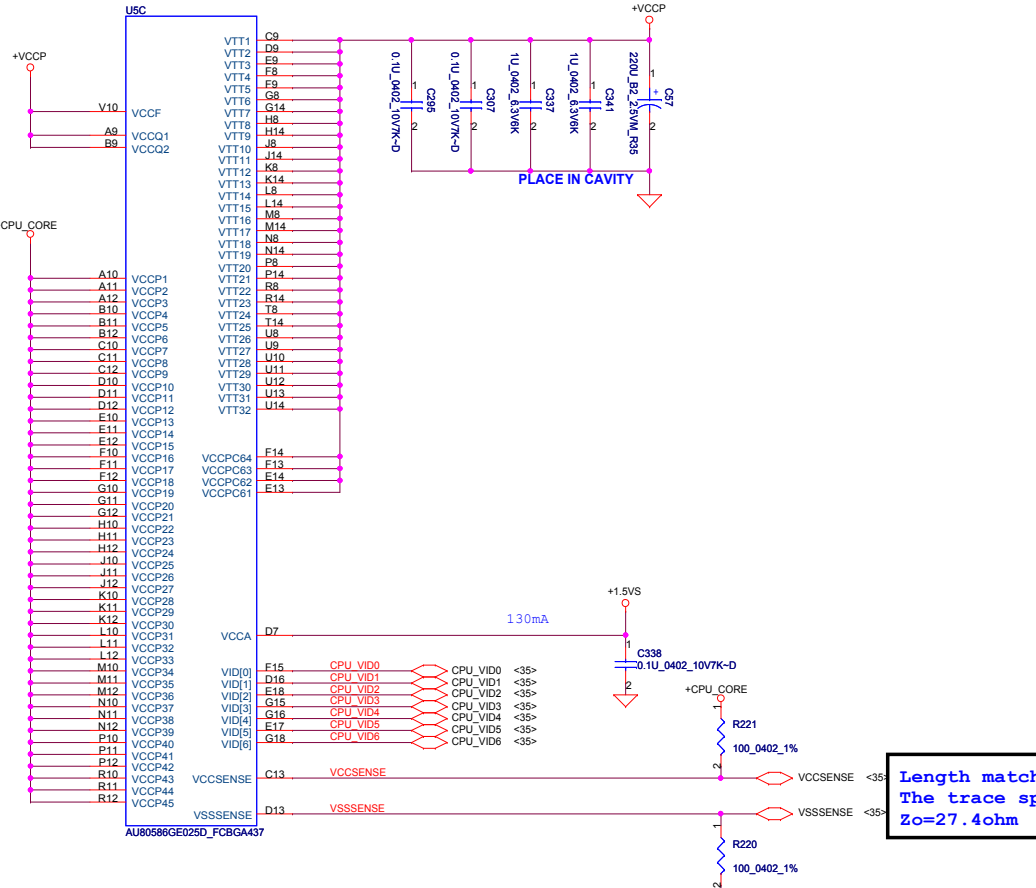
H_THERMDA, H_THERMDC routing together.
 Trace width / Spacing = 10 / 10 mil



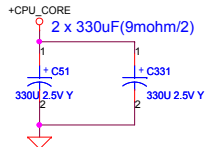
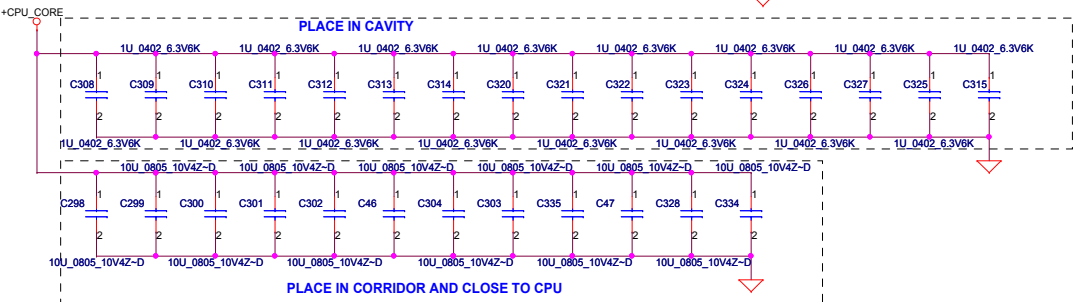
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USD

A2	VSS1	VSS162	N5
A4	VSS2	VSS161	N7
A8	VSS4	VSS160	N9
A15	VSS8	VSS159	N13
A18	VSS16	VSS158	N17
A19	VSS17	VSS157	P3
A20	VSS18	VSS156	P4
B1	VSS19	VSS155	P5
B2	VSS20	VSS154	P6
B5	VSS24	VSS153	P7
B8	VSS28	VSS152	P9
B13	VSS32	VSS151	P13
B20	VSS39	VSS150	P15
B21	VSS40	VSS149	P16
C8	VSS45	VSS148	P18
C17	VSS53	VSS147	P19
D1	VSS58	VSS146	R5
D5	VSS63	VSS145	R7
D8	VSS66	VSS144	R9
D14	VSS73	VSS143	R13
D18	VSS78	VSS142	R19
D21	VSS81	VSS141	R21
E3	VSS85	VSS140	T4
E6	VSS89	VSS139	T5
E7	VSS90	VSS138	T7
E8	VSS91	VSS137	T9
E15	VSS97	VSS136	T10
E16	VSS98	VSS135	T11
E19	VSS100	VSS134	T12
F4	VSS103	VSS133	T13
F5	VSS104	VSS132	T18
F6	VSS105	VSS131	T19
F7	VSS106	VSS130	U3
F12	VSS110	VSS129	U6
F18	VSS115	VSS128	U7
G1	VSS120	VSS127	U15
G4	VSS124	VSS126	U16
G7	VSS127	VSS125	U19
G9	VSS129	VSS124	V4
G13	VSS132	VSS123	V6
G21	VSS137	VSS122	V7
H2	VSS140	VSS121	V8
H4	VSS142	VSS120	V13
H7	VSS145	VSS119	V18
H9	VSS147	VSS118	V14
H13	VSS150	VSS117	V21
H16	VSS152	VSS116	W1
H18	VSS154	VSS115	W5
H19	VSS155	VSS114	W8
J5	VSS160	VSS113	W11
J7	VSS162	VSS112	W14
J9	VSS164	VSS111	W17
J13	VSS166	VSS110	W21
J17	VSS168	VSS109	W21
K1	VSS170	VSS108	Y1
K6	VSS175	VSS107	Y2
K7	VSS176	VSS106	Y20
K9	VSS178	VSS105	Y21
K13	VSS180	VSS104	AA2
K15	VSS182	VSS103	AA3
K21	VSS185	VSS102	AA4
L3	VSS188	VSS101	AA7
L4	VSS189	VSS100	AA10
L6	VSS191	VSS99	AA12
L7	VSS192	VSS98	AA15
L9	VSS194	VSS97	AA18
L13	VSS198	VSS96	AA19
L15	VSS200	VSS95	AA20
L18	VSS203		
L19	VSS204		
M1	VSS205		
M5	VSS206		
M7	VSS207		
M9	VSS208		
M13	VSS209		
M21	VSS210		
N4	VSS211		
VSS24			

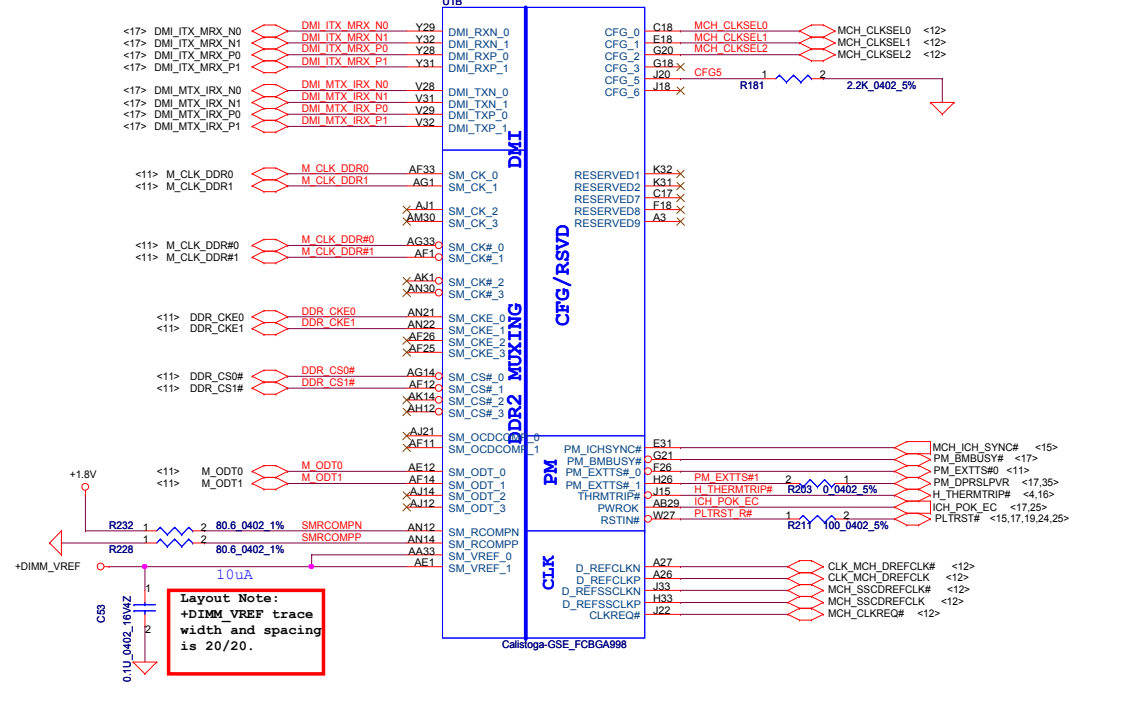
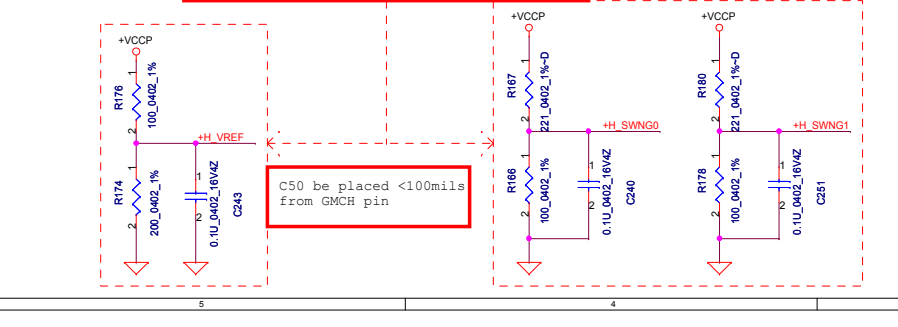
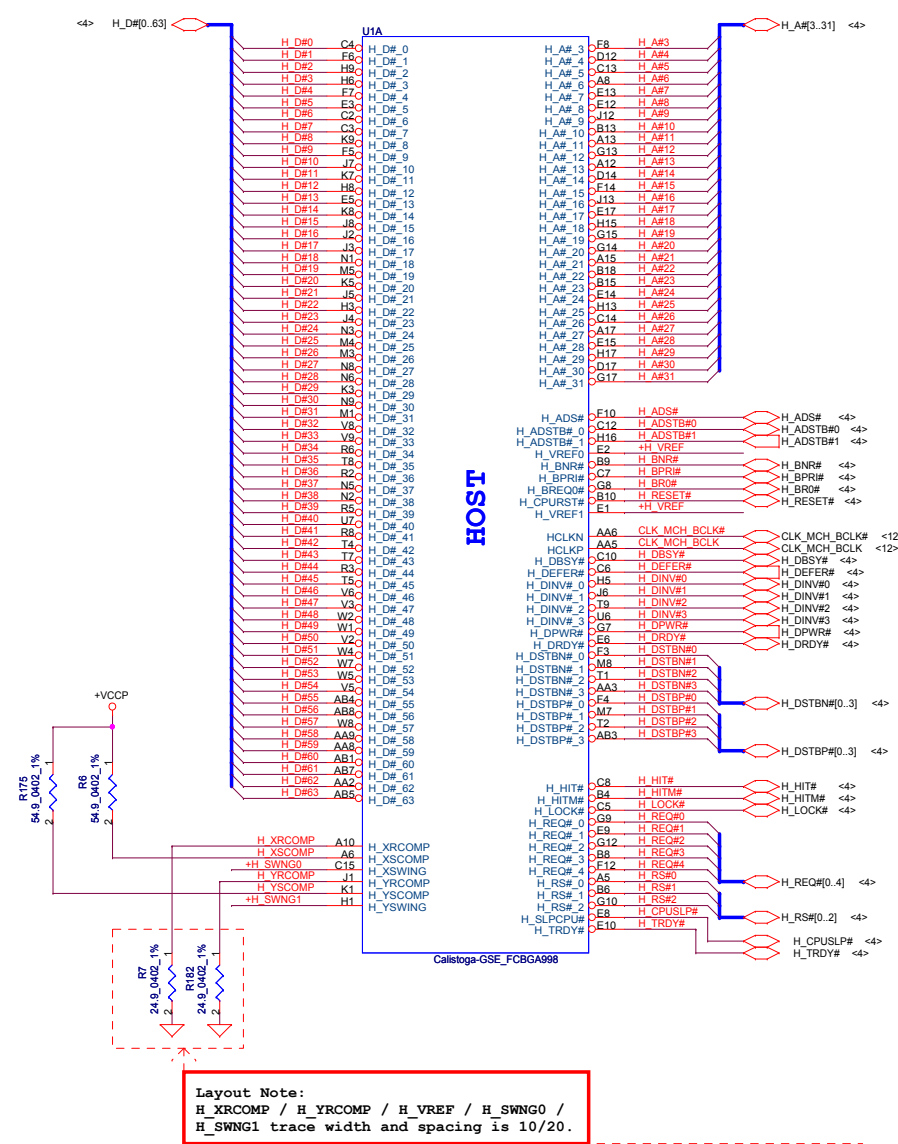


Length match within 25 mils
 The trace space 7 mils,
 Zo=27.4ohm



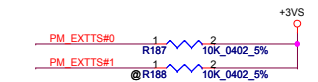
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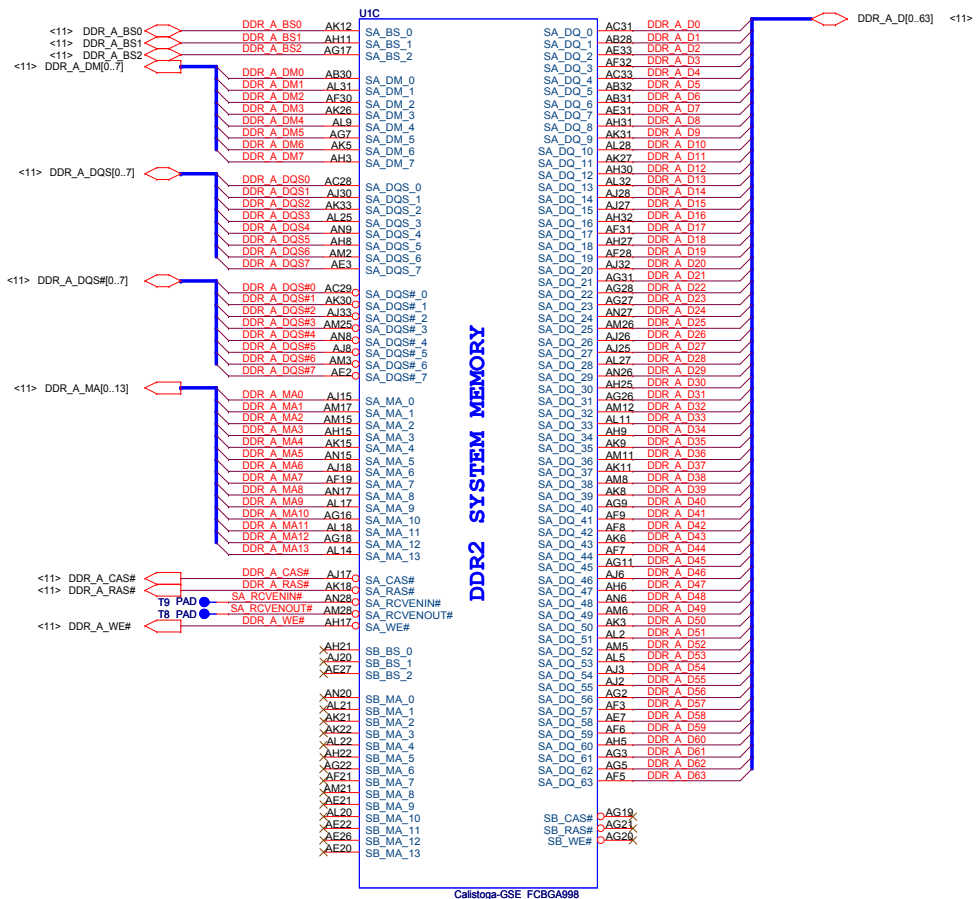


Strap Pin Table

CFG5	Low = DMI x 2 *
	High = DMI x 4

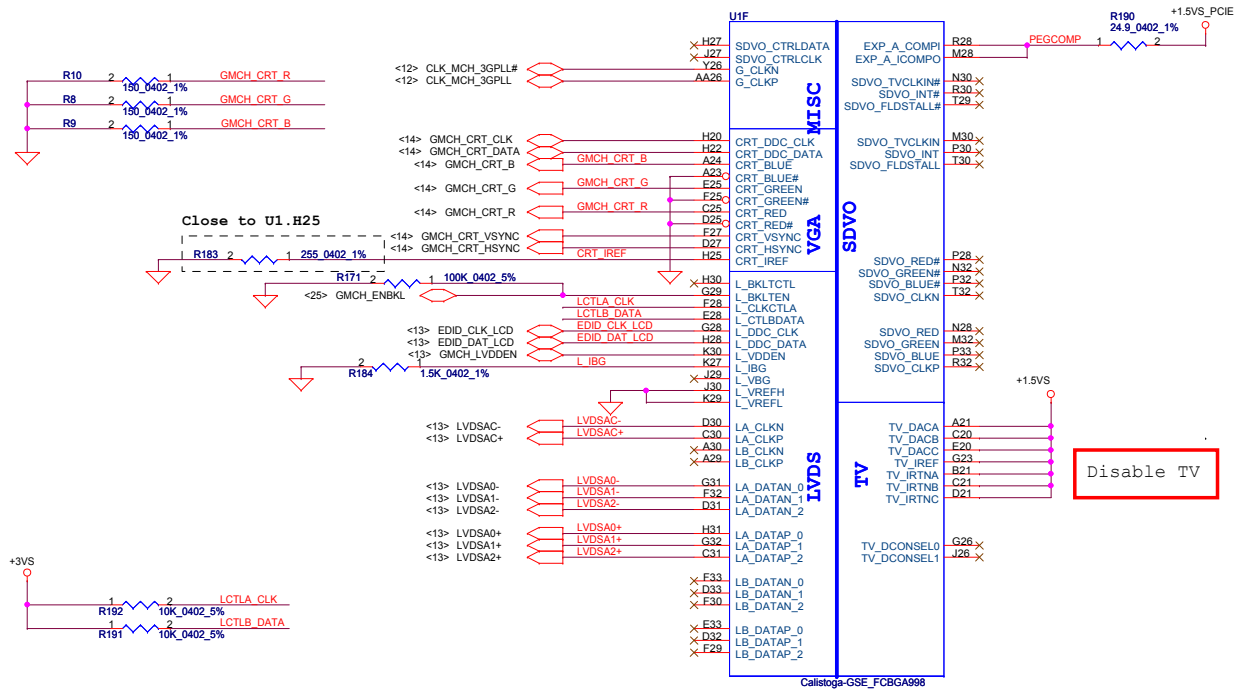


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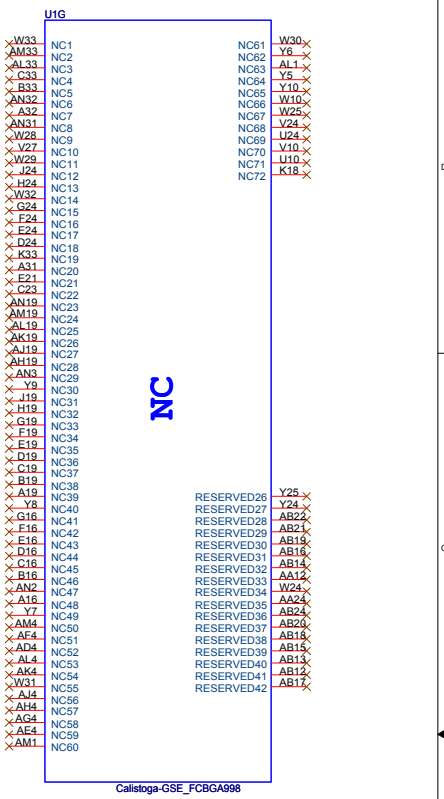
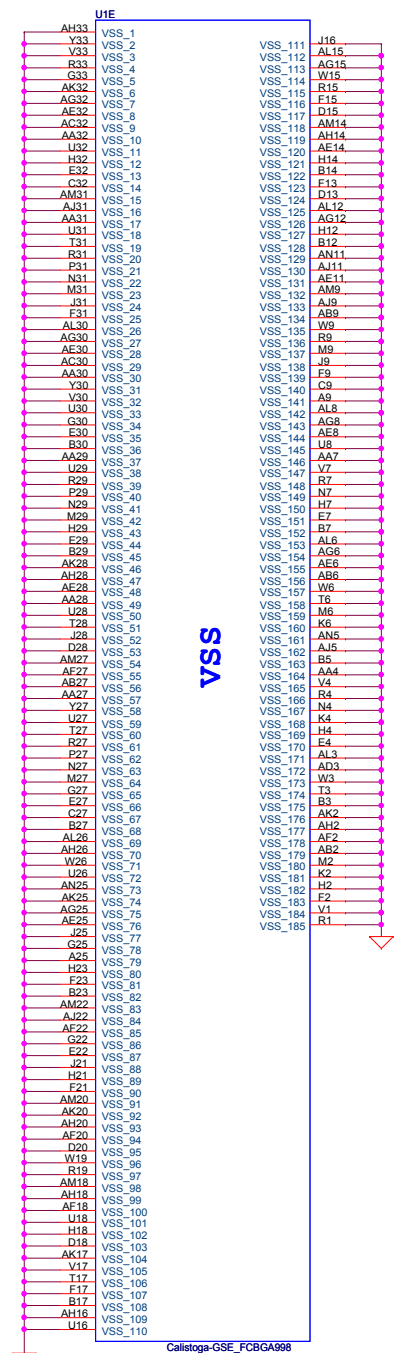
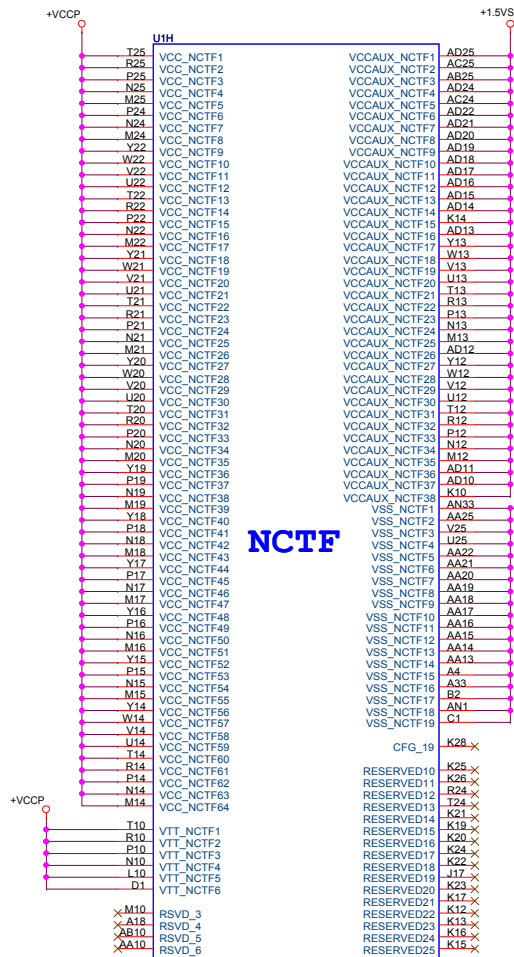


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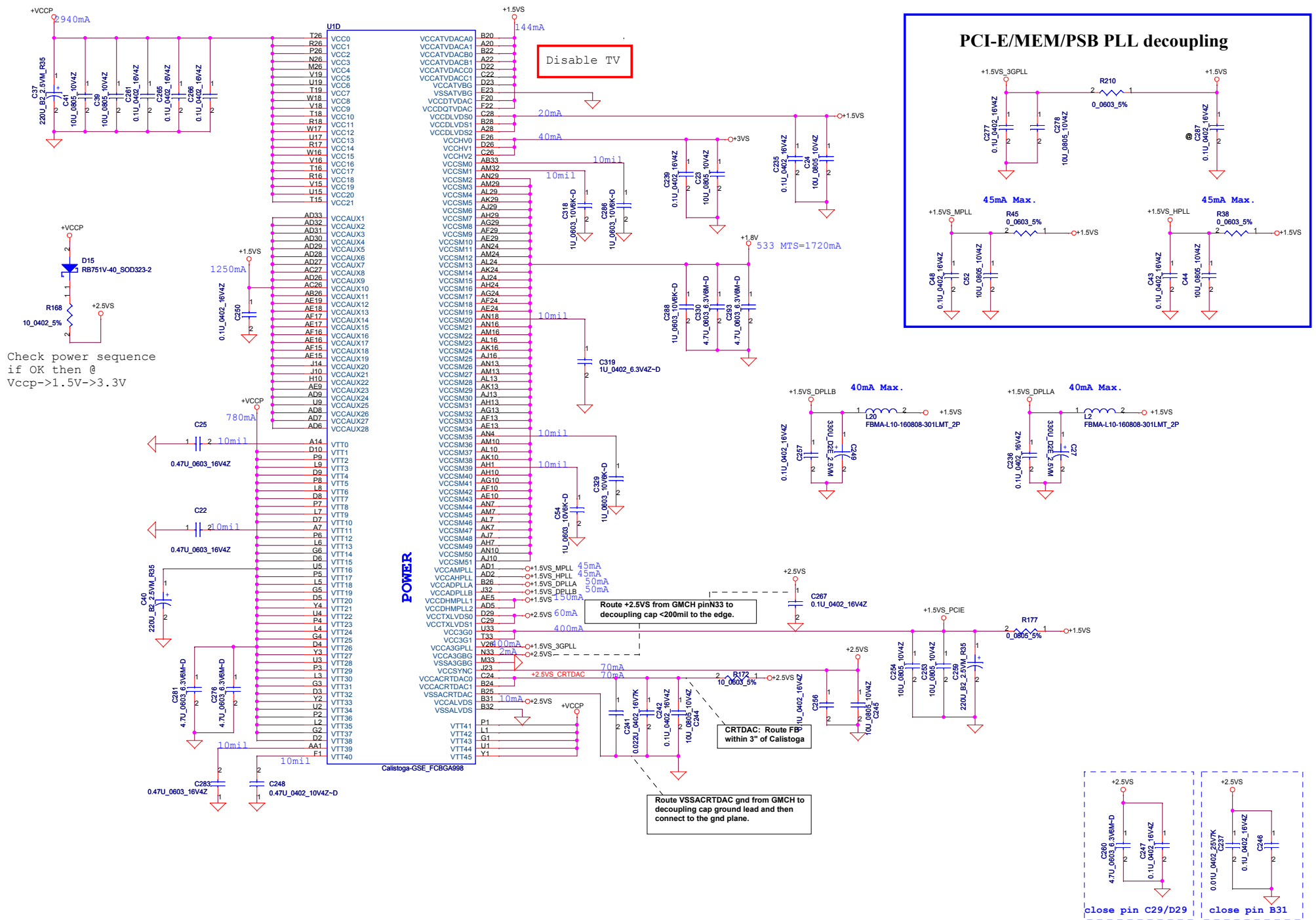
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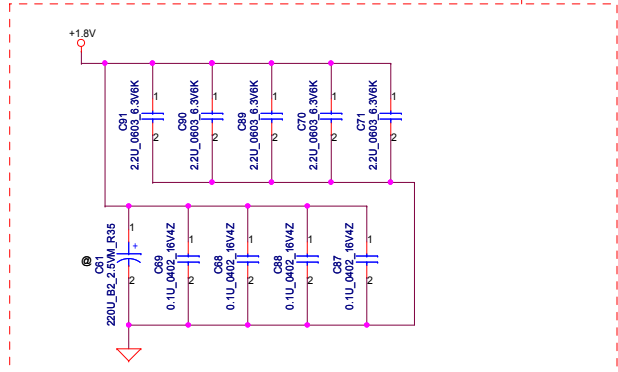
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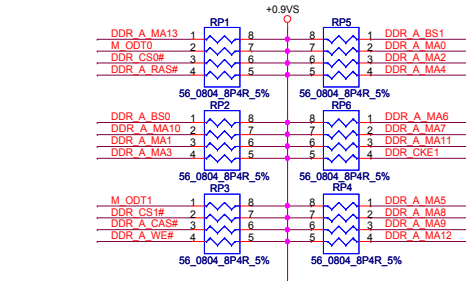
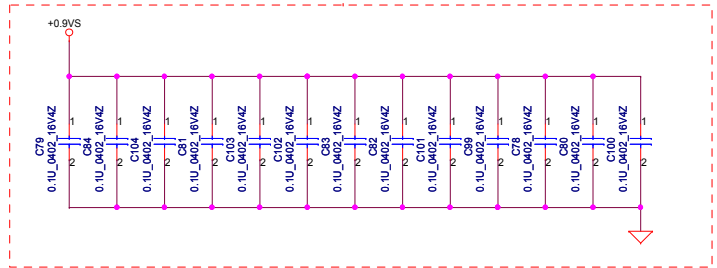
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- <7> DDR_A_DQS#[0..7]
- <7> DDR_A_D[0..63]
- <7> DDR_A_DM[0..7]
- <7> DDR_A_DQS#[0..7]
- <7> DDR_A_MA[0..13]

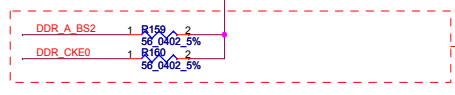
Layout Note:
Place near JDIM1



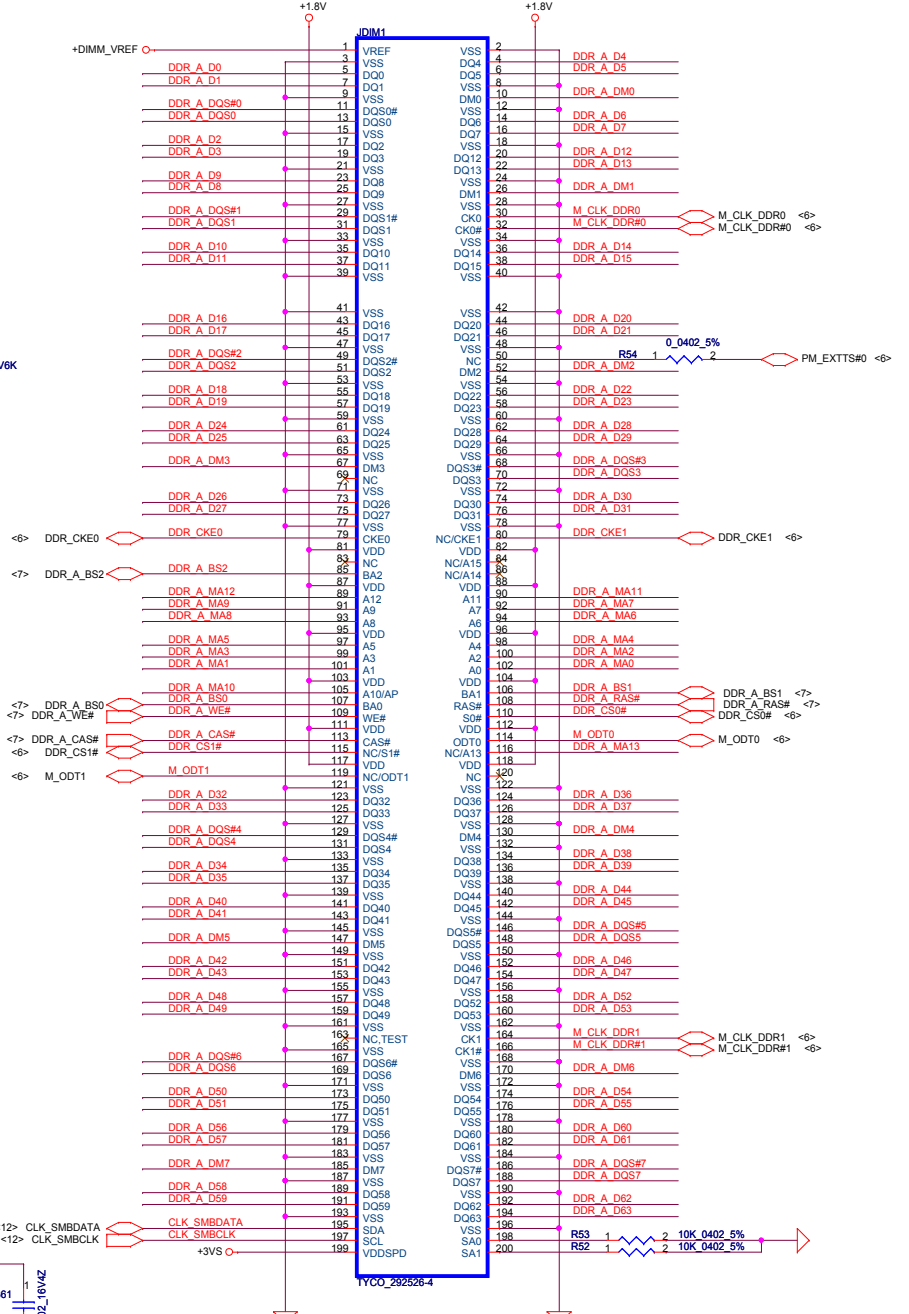
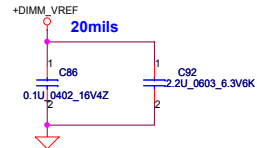
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely DIMMA, all trace length <750 mil



Layout Note:
Place these resistor closely DIMMA, all trace length Max=1.3"



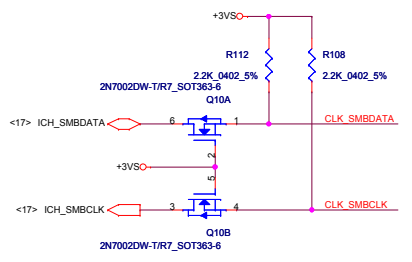
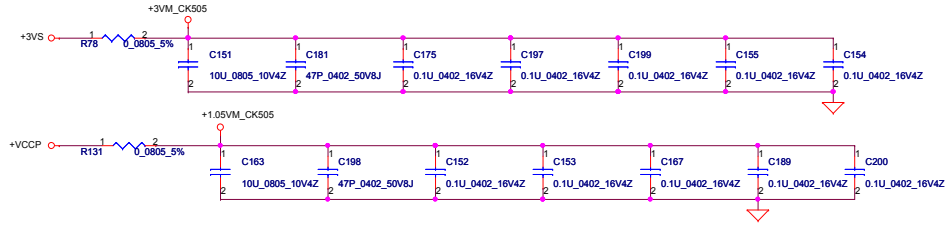
DIMMA

2/10: Change from 5.2mm to 4mm height CPN:SP07000CK00

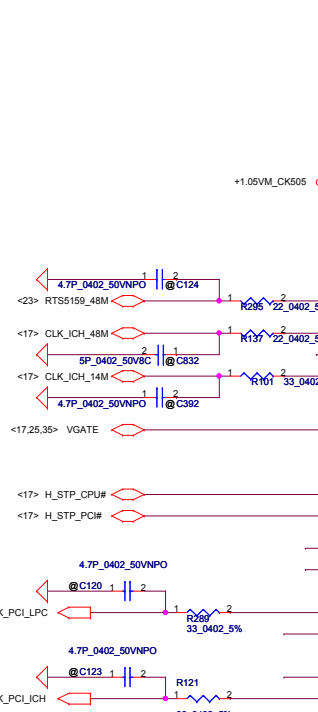
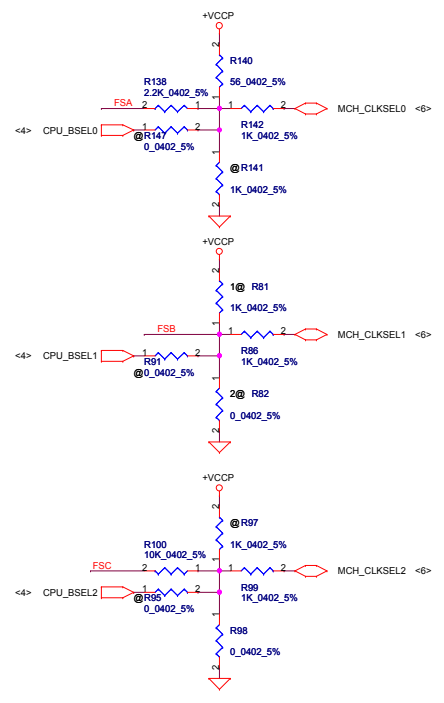
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Title			
DDRII-SODIMM			
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FSC	F5B	F5A	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
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Reserved								

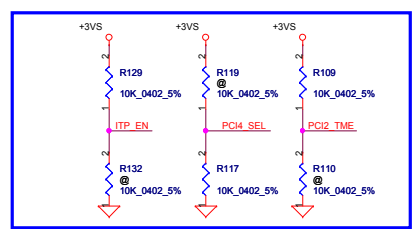


SA000020K00 (Silago : SLG8SP556VTR)
SA000020H10 (ICS : ICS9LPRS387AKLFT)



For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

For PCI2_TME: 0=Overclocking of CPU and SRC allowed
(ICS only) 1=Overclocking of CPU and SRC NOT allowed



Routing the trace at least 10mil



SRC PORT LIST

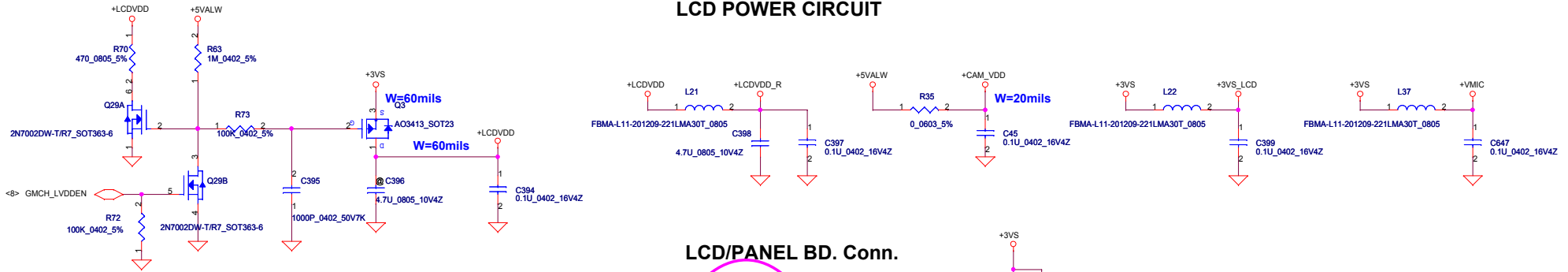
PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	PCIE SATA
SRC3	MCH_3GPLL
SRC4	
SRC6	PCIE_WLAN
SRC7	
SRC8	
SRC9	PCIE LAN
SRC10	PCIE ICH
SRC11	

REQ PORT LIST

PORT	DEVICE
REQ_3#	MCH_DREFCLK
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	
REQ_9#	PCIE LAN
REQ_10#	
REQ_11#	
REQ_A#	

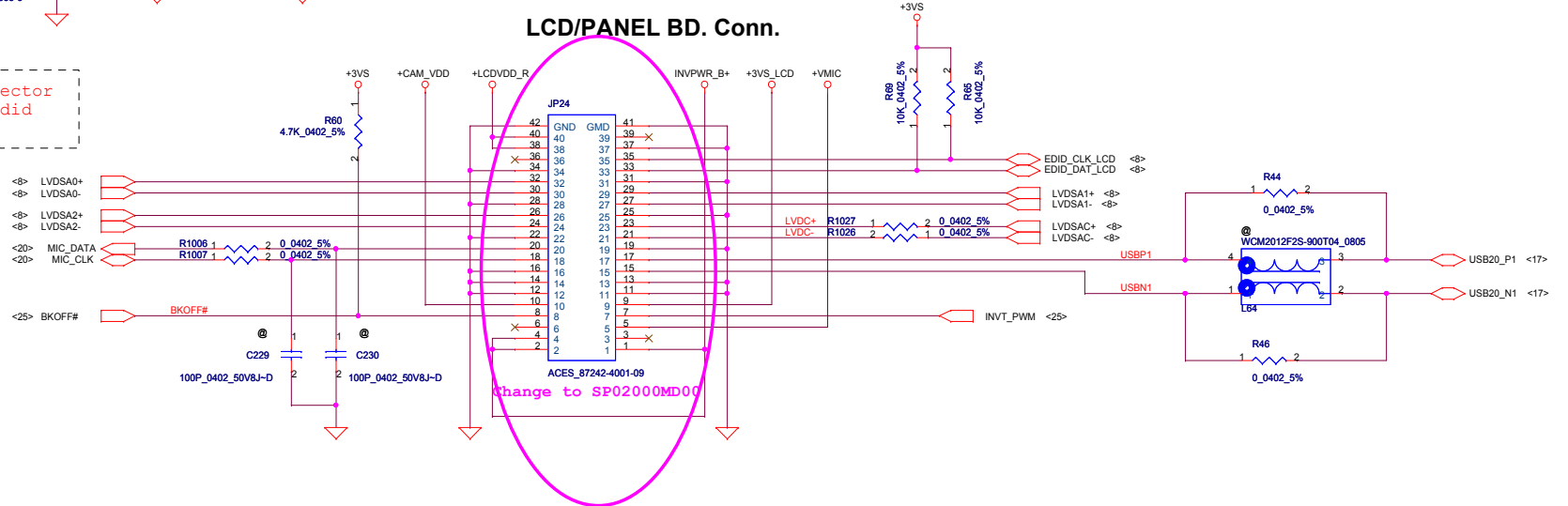
Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/10	Deciphered Date	2009/11/10	Clock Generator CK505	
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Size	Document Number	Date		Sheet	Rev
	LA-5091P	Wednesday, April 22, 2009		12	1.0
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LCD POWER CIRCUIT

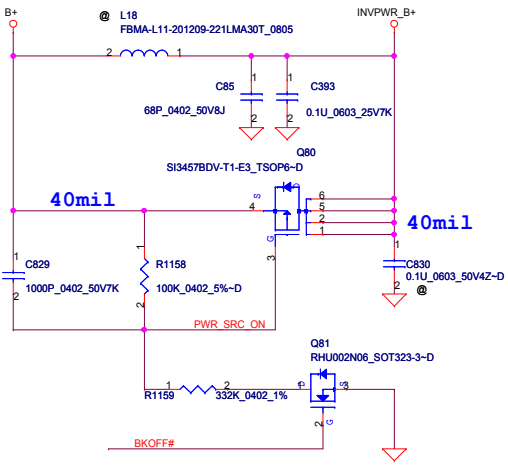


1/9: Reversed LVDS connector pinout, but LVDS cable did not need to change.

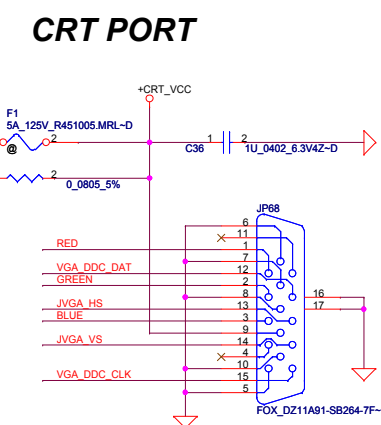
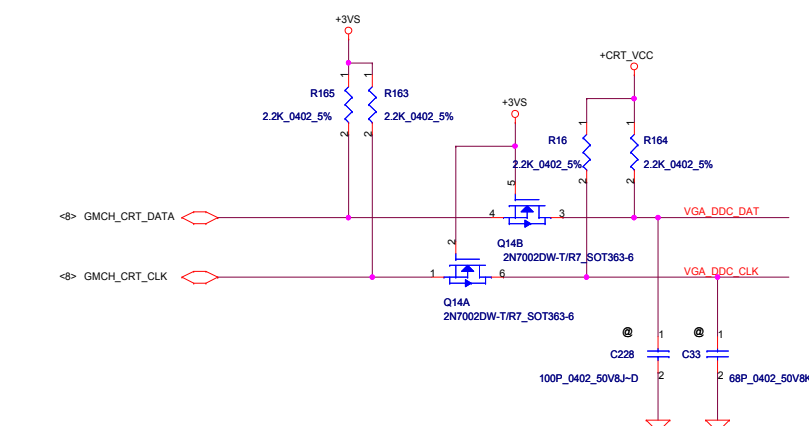
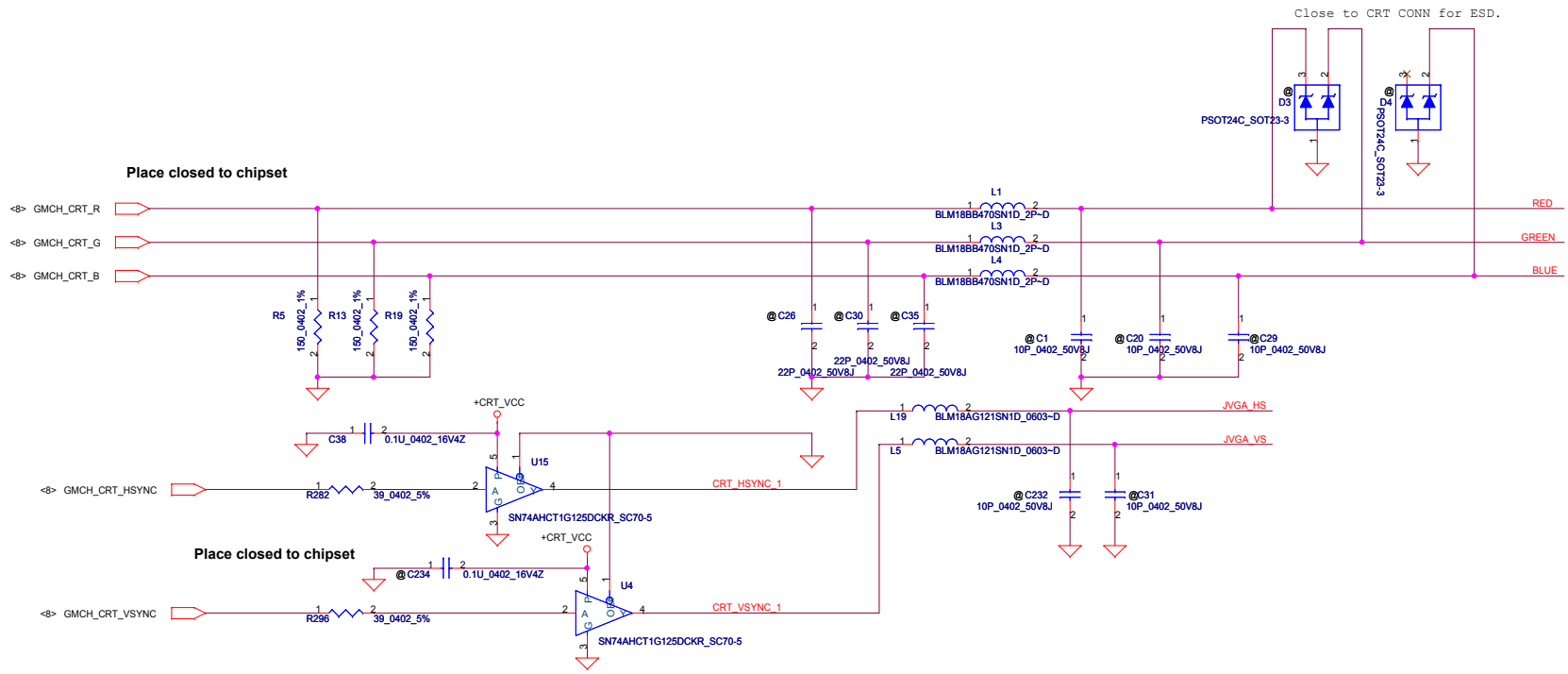
LCD/PANEL BD. Conn.



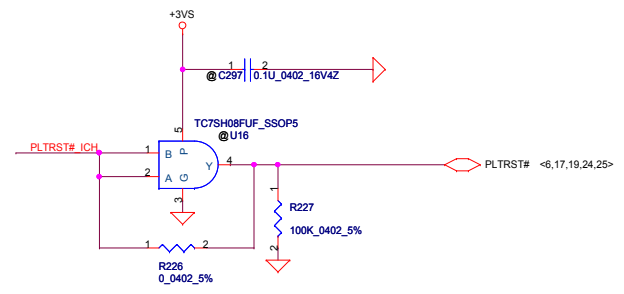
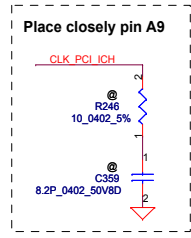
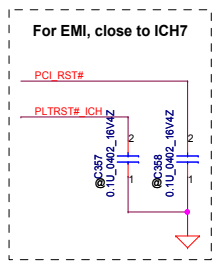
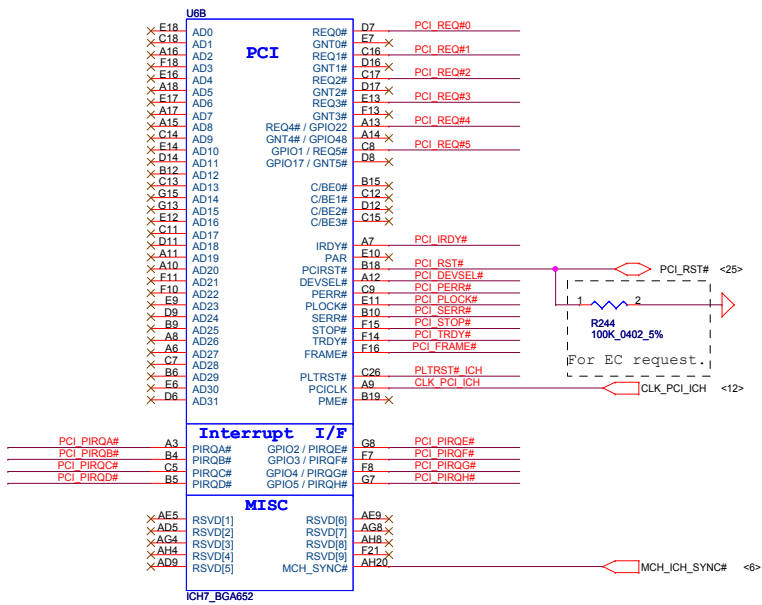
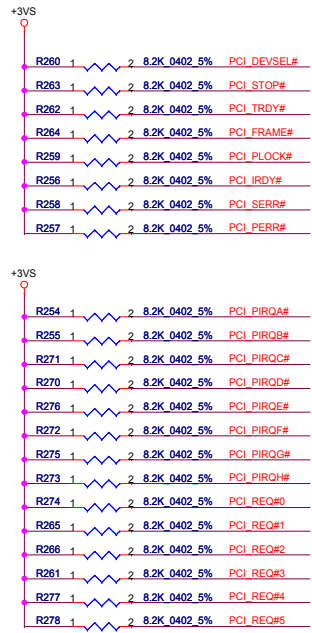
change to SP02000MD00



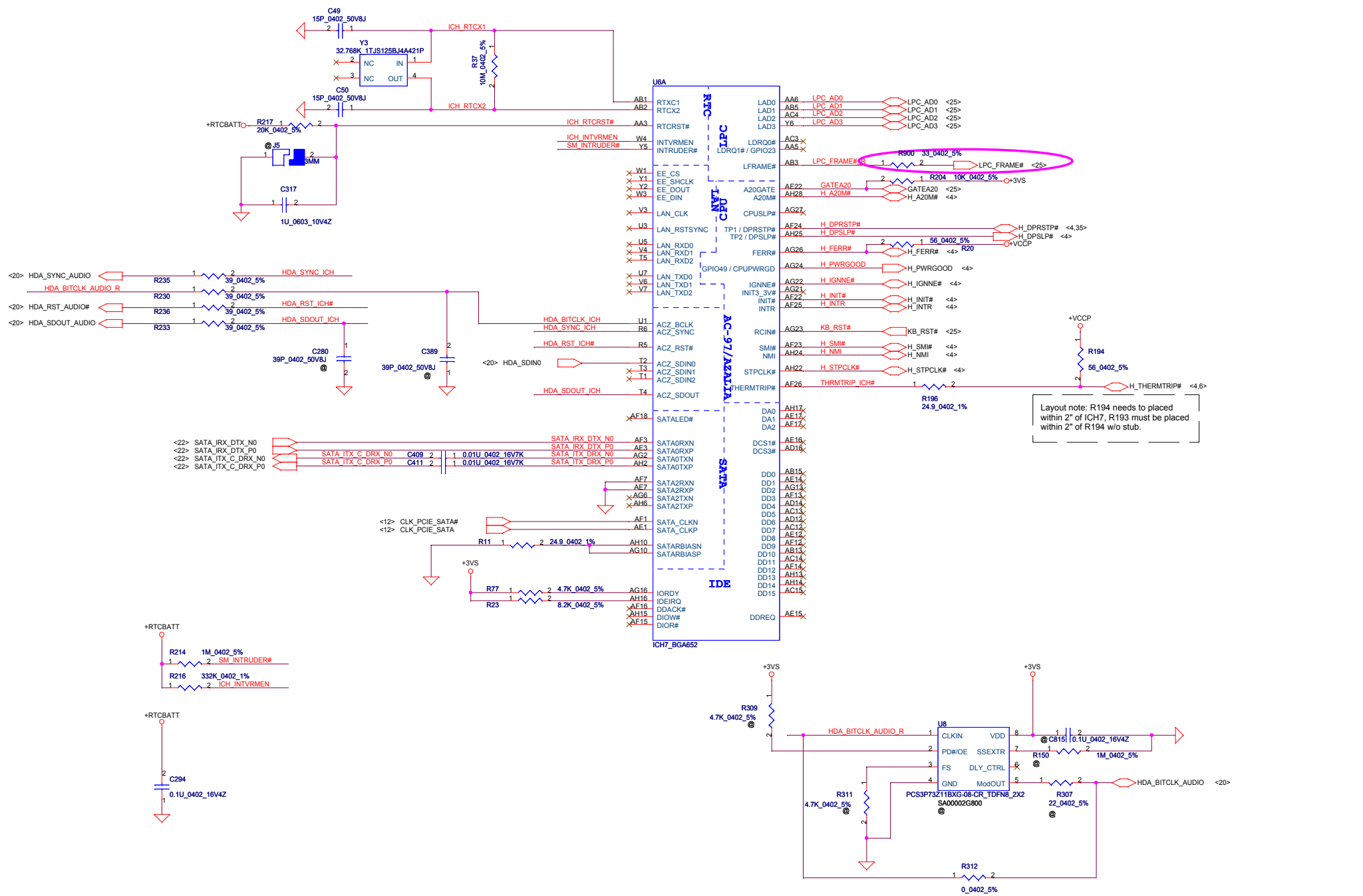
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/10	Deciphered Date	2009/11/10	Title	
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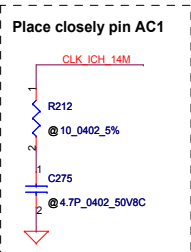
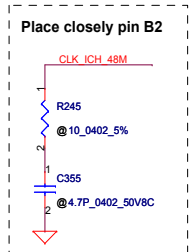
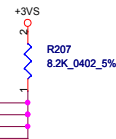
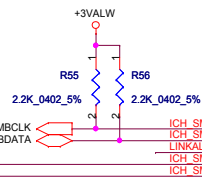
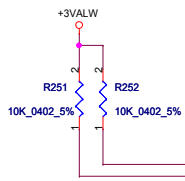
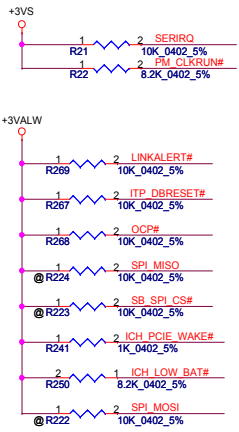
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/10	Deciphered Date	2009/11/10	Title	
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Size	Custom	Document Number	LA-5091P	Rev	1.0
Date:	Wednesday, April 22, 2009	Sheet	14	of	39



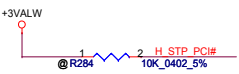
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Issued Date	2008/11/10	Deciphered Date	2009/11/10	Title		
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				Size	Document Number	Rev
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Security Classification		Compal Secret Data		Title		
Issued Date	2008/11/10	Deciphered Date	2009/11/10	ICH7M(2/4)-LAN/ATA/LPC/RTC		
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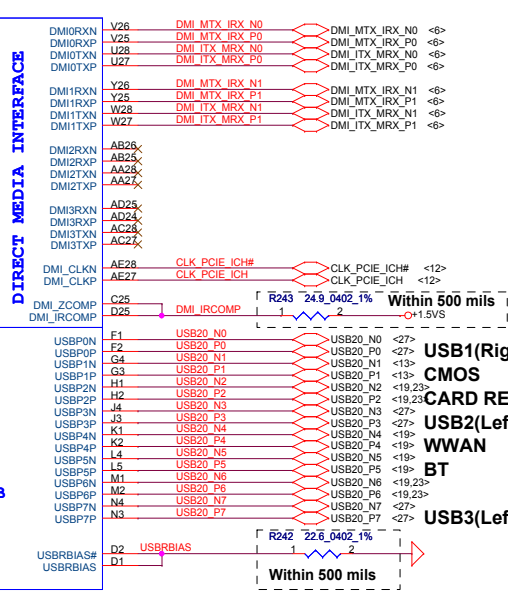
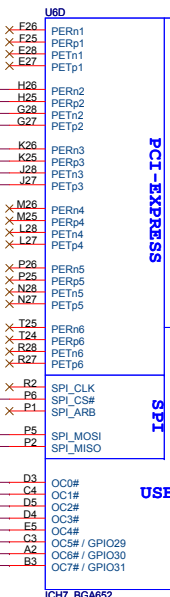
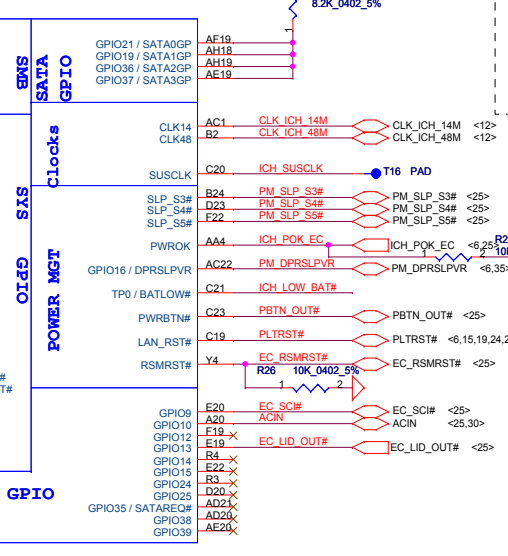
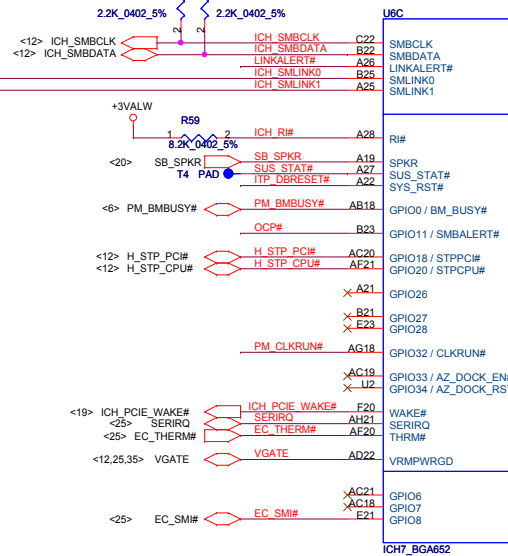
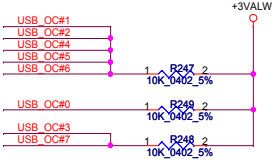
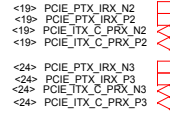


1/9: De-pop R284 for +3VS back drive issue.



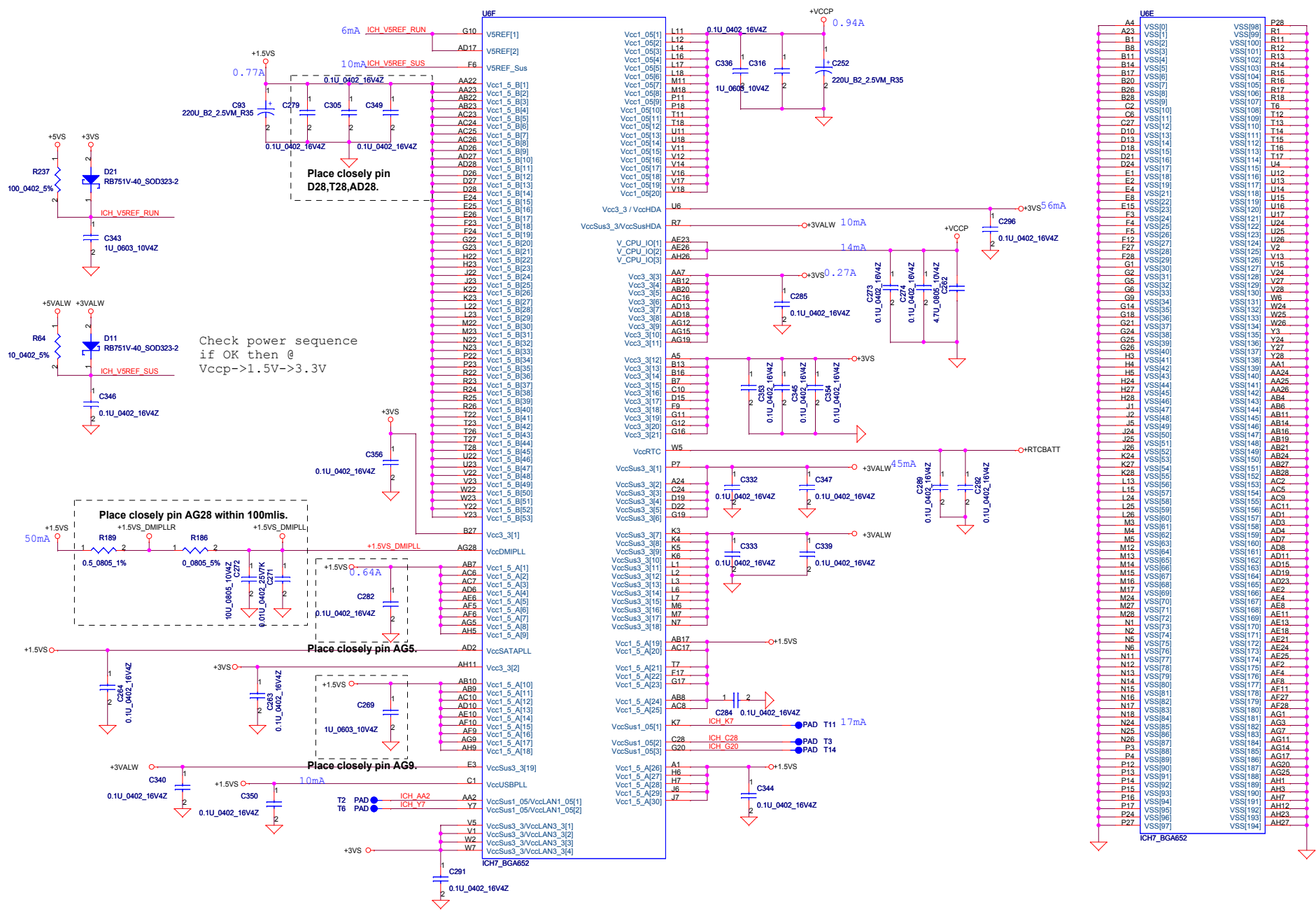
some intel ICH7M H_STP_PCI# has the below glitch that let Silego clk. gen enter iAMT mode when power on, but ICS clk. gen has no this issue now.

WLAN
LAN



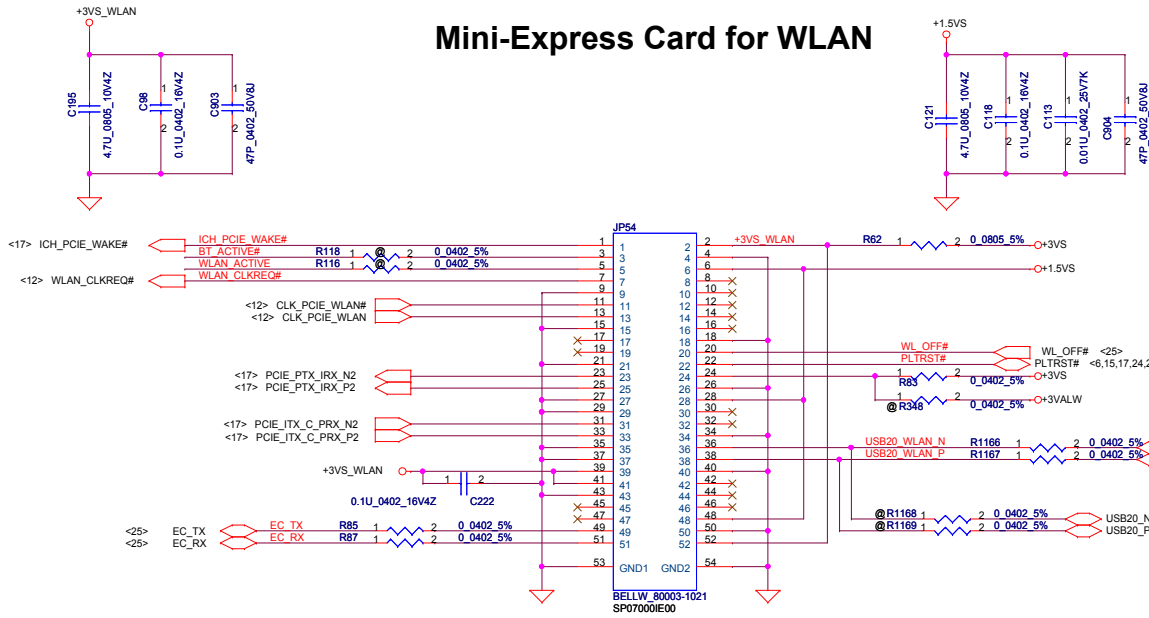
USB1(Right)
CMOS
CARD READER
USB2(Left)
WWAN
BT
USB3(Left)

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Size Custom	Document Number	LA-5091P		Rev	1.0
Date:	Wednesday, April 22, 2009	Sheet	17	of	39

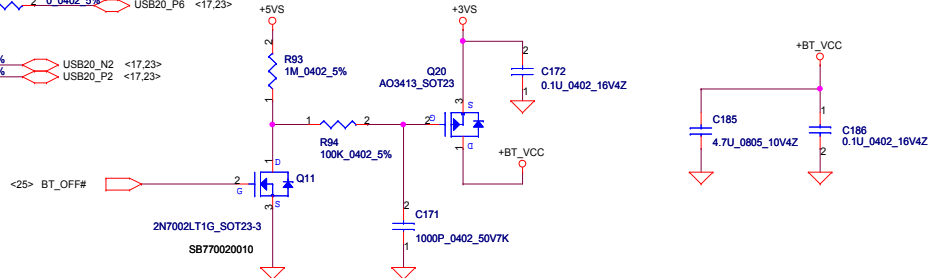


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Custom		LA-5091P		Rev	1.0
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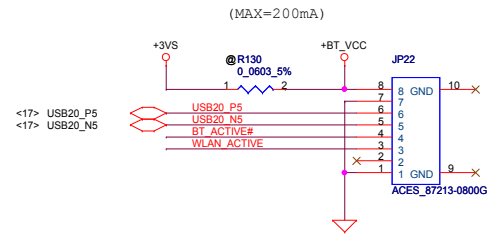
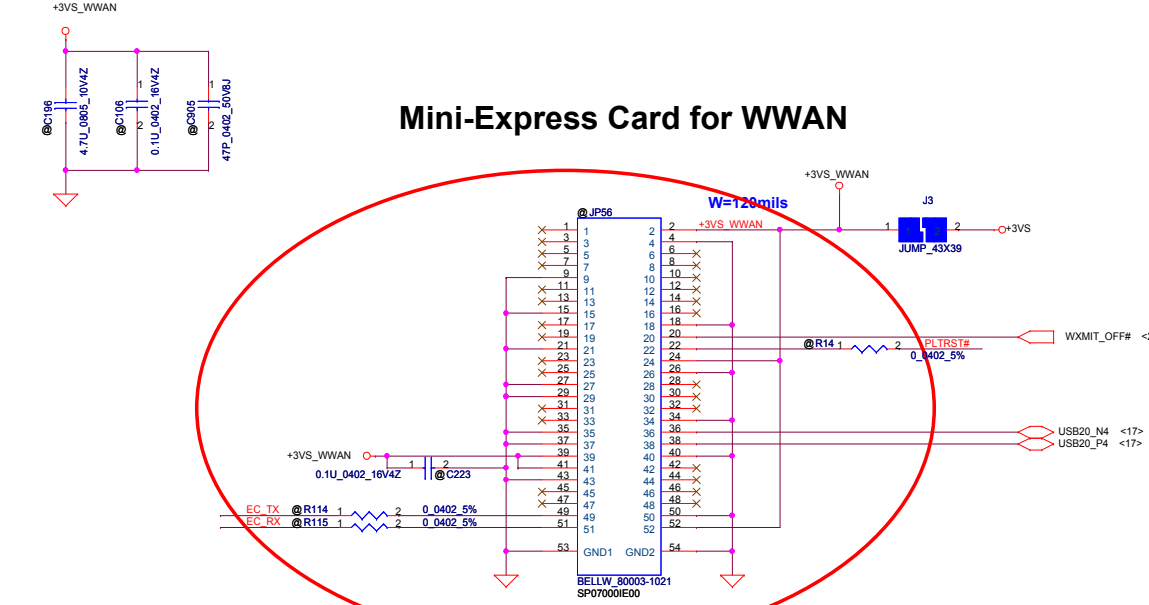
Mini-Express Card for WLAN



BlueTooth Interface

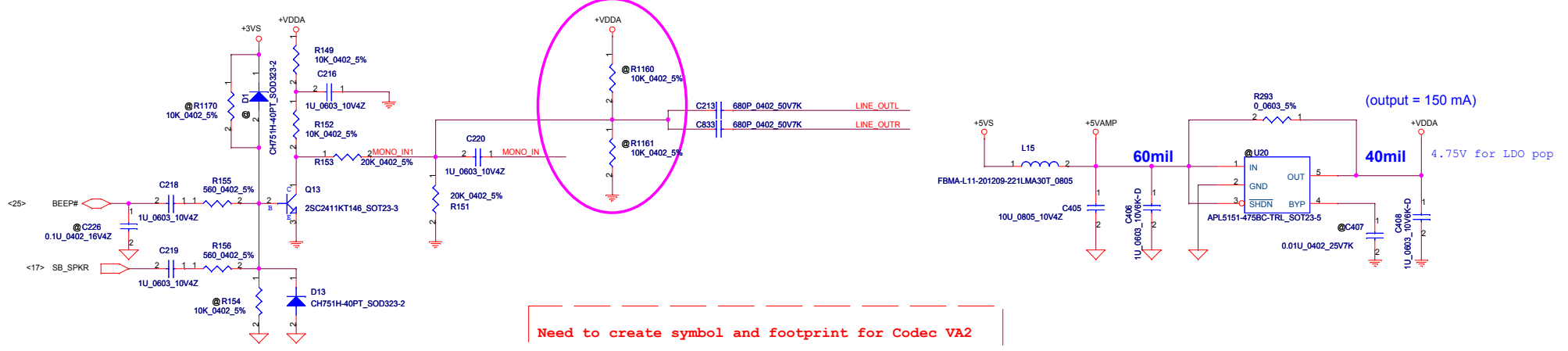


Mini-Express Card for WWAN

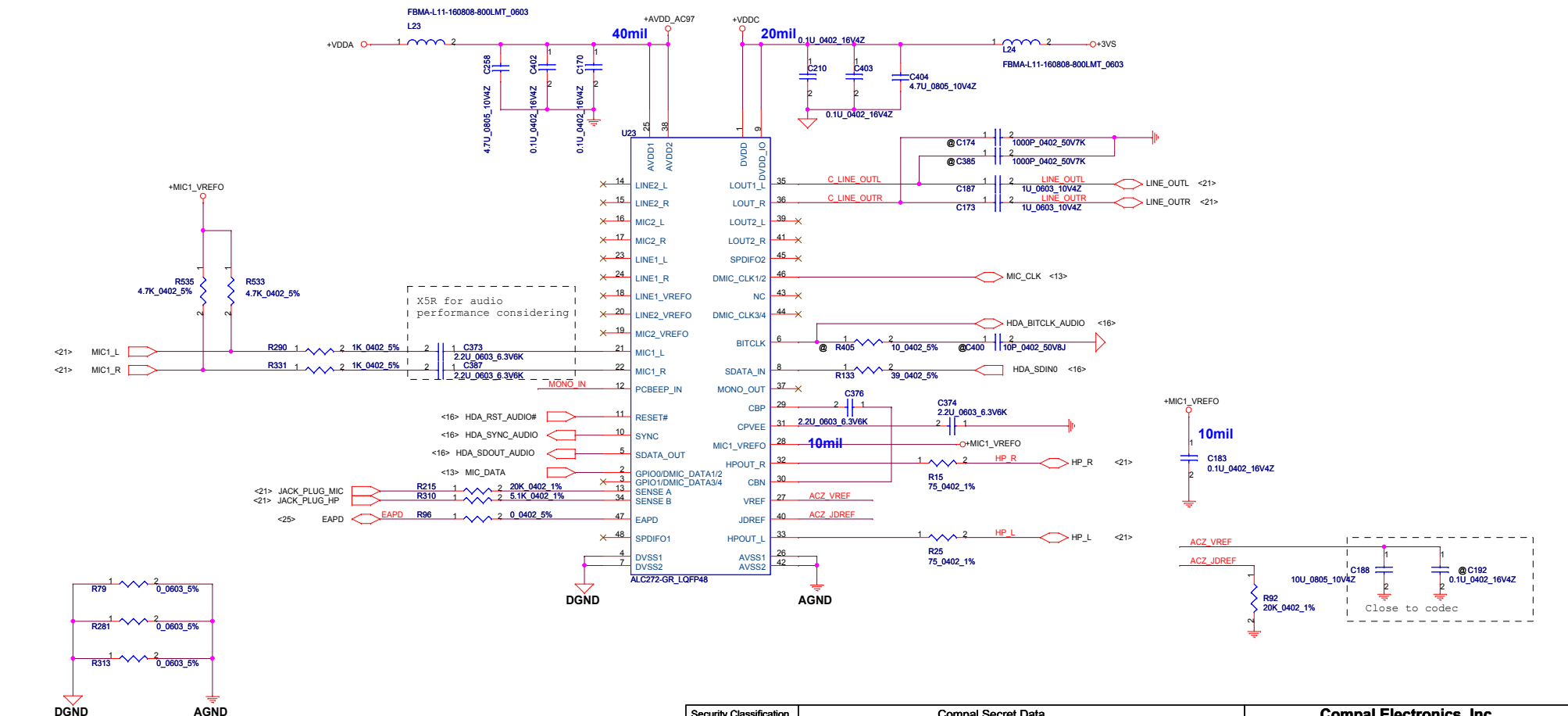


Tiger FW update for S3 issue.

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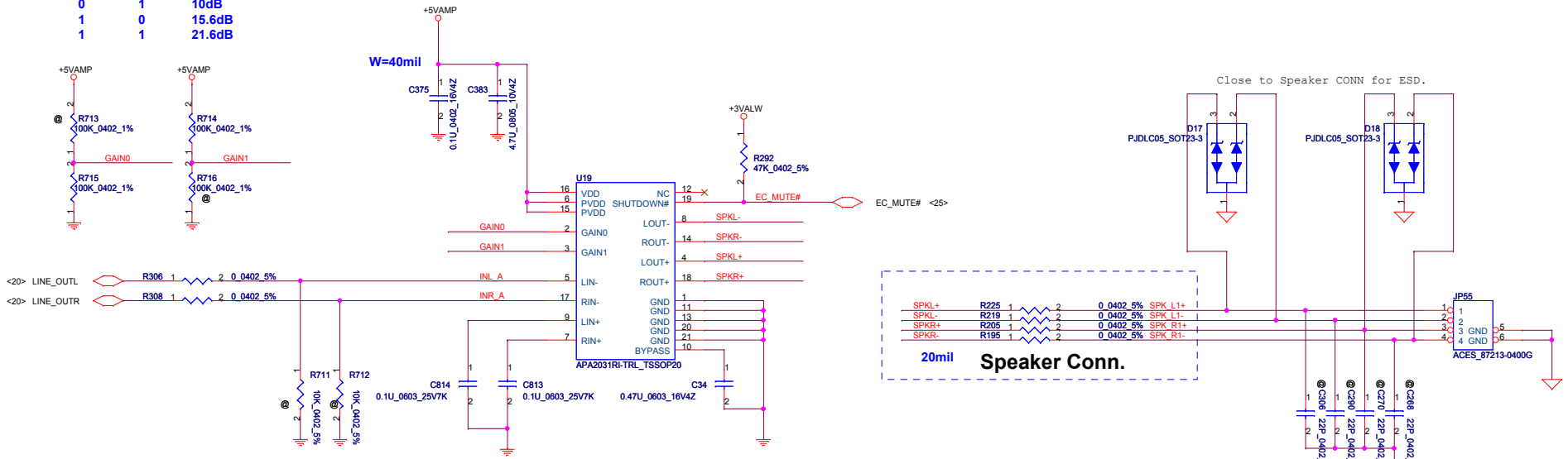
HD Audio Codec



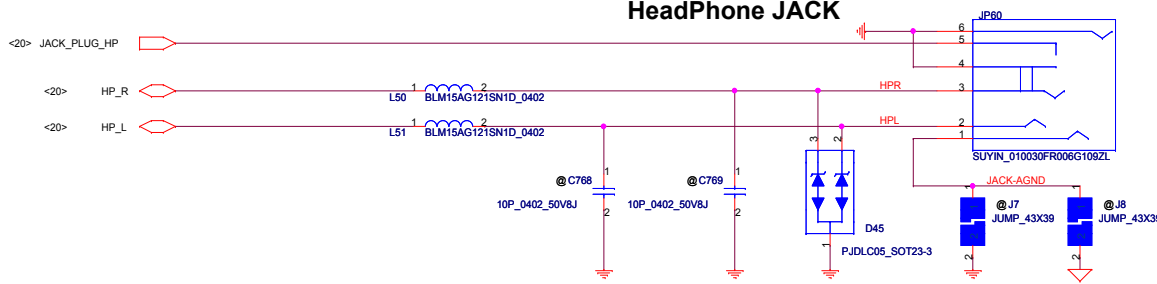
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/10	Deciphered Date	2009/11/10	ALC272-VB-GR Codec	
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APA2031A SPK Amplifier

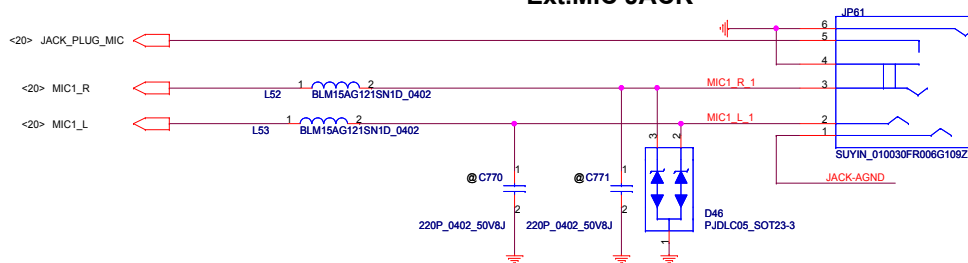
GAIN0	GAIN1	Gain
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



HeadPhone JACK

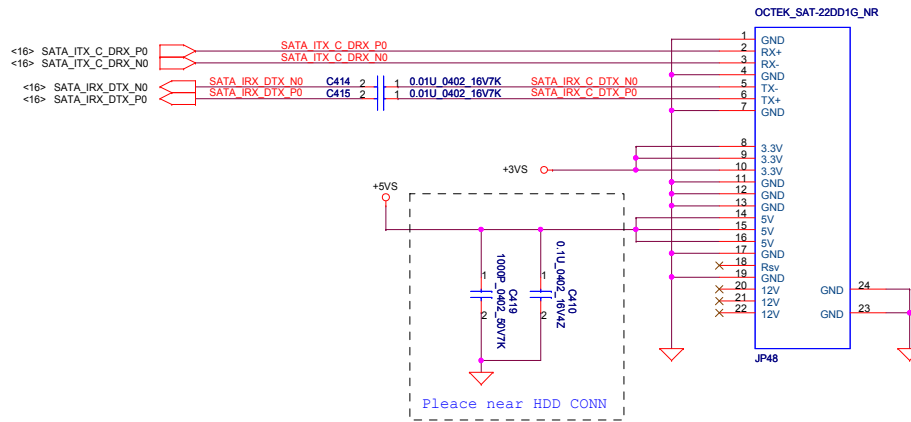


Ext.MIC JACK

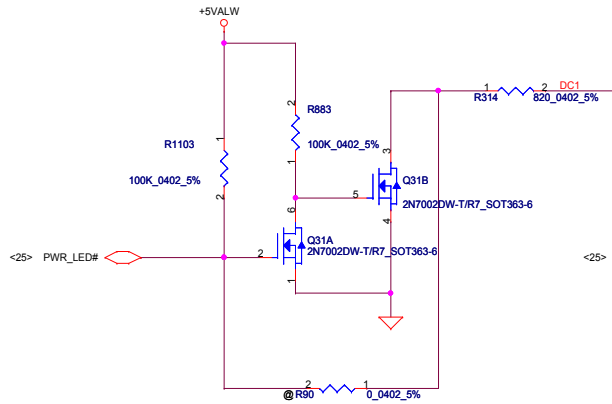


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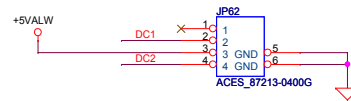
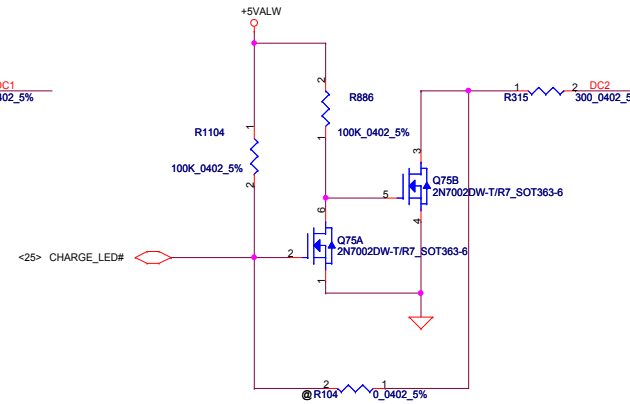
For HDD



POWER LED

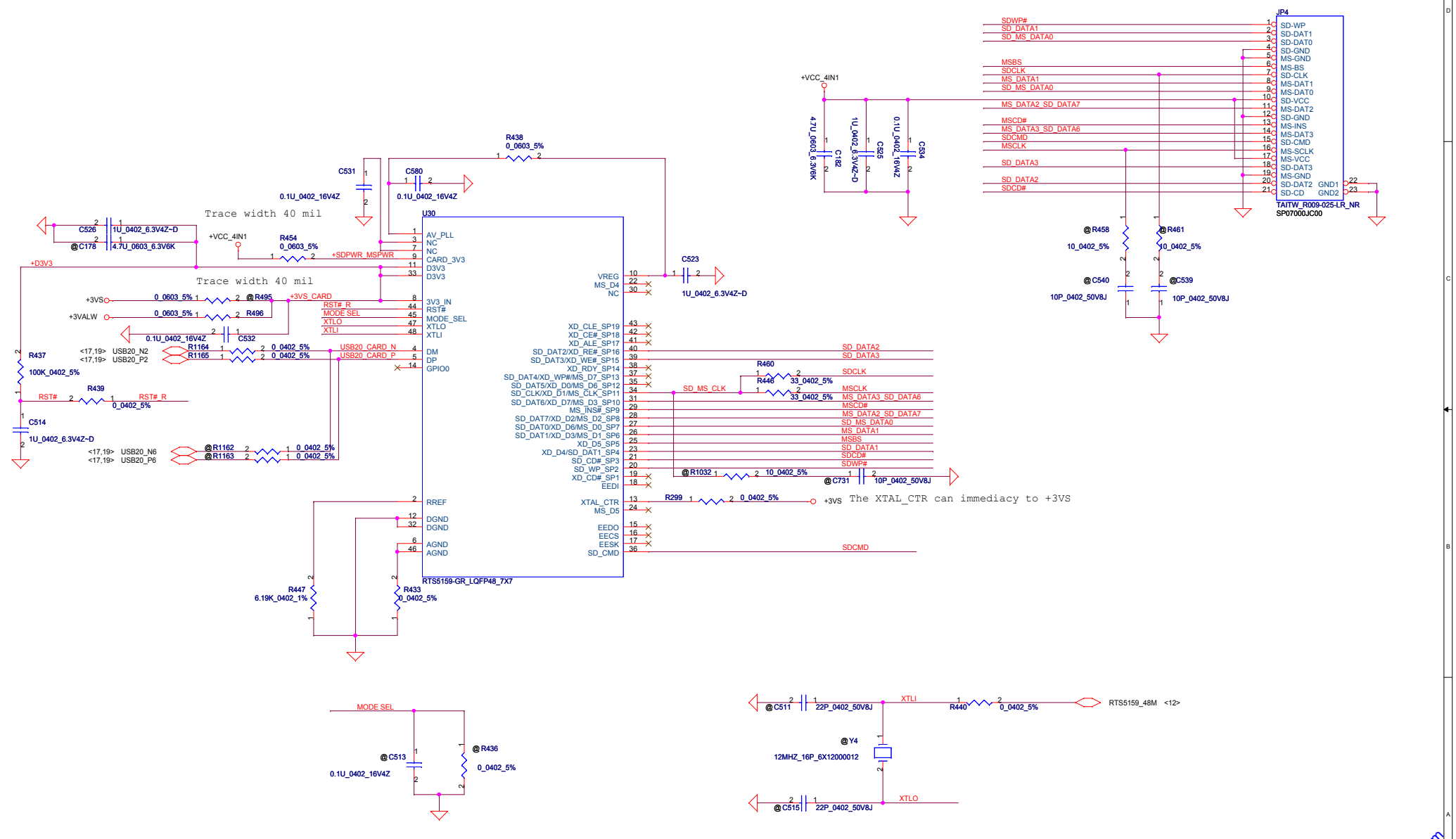


BATT CHARGE LED



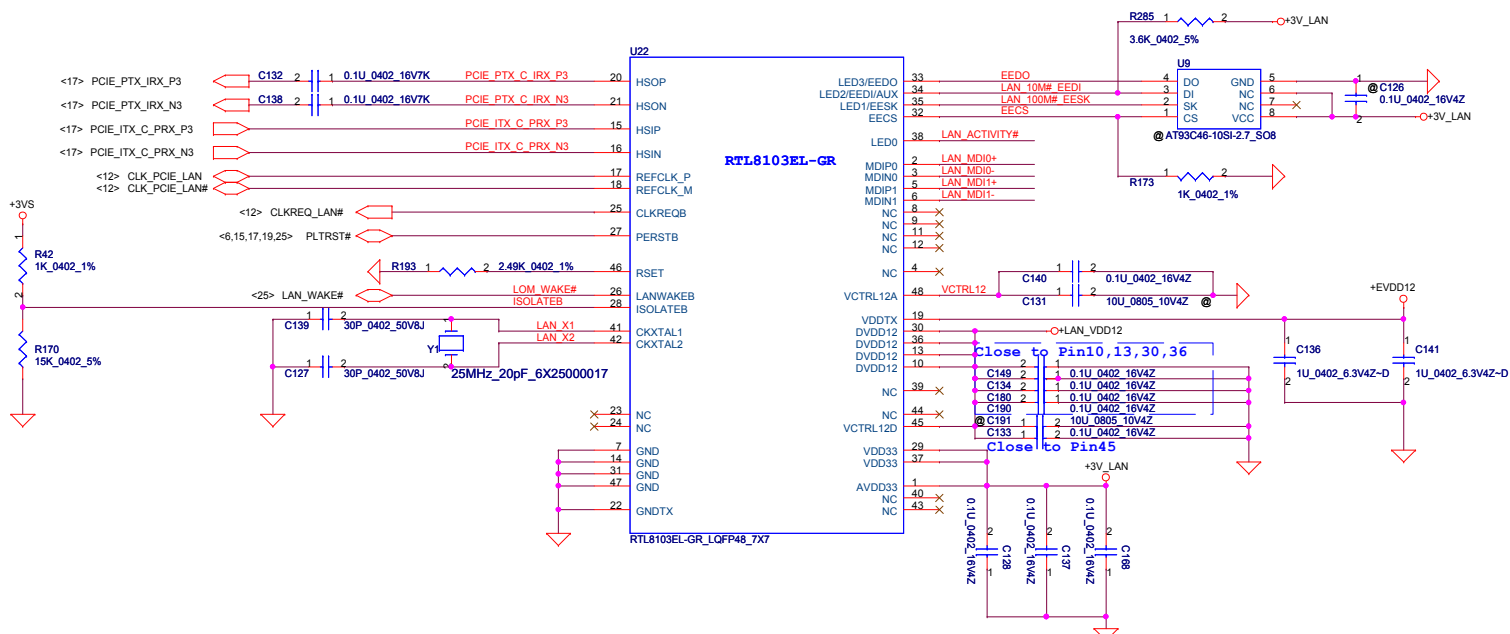
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/10	Deciphered Date	2009/11/10	Title HDD/LED	
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				Rev	1.0

4 in 1 Card Reader

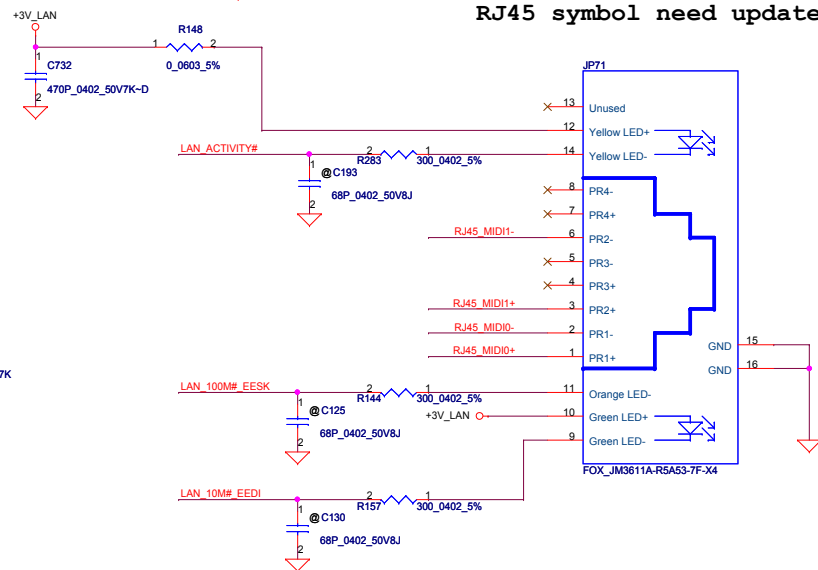
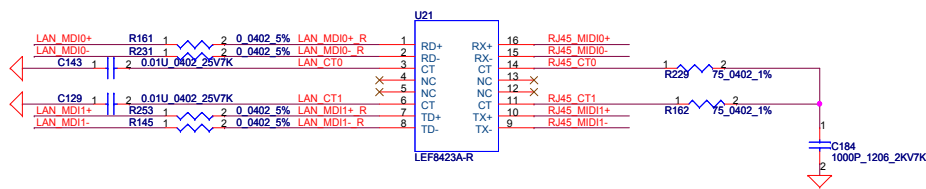


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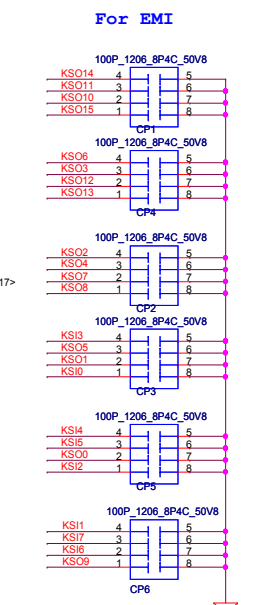
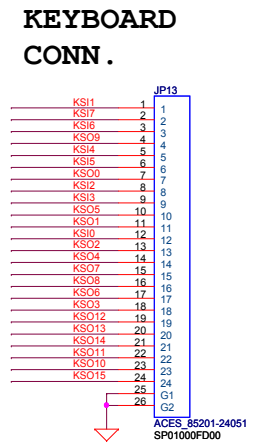
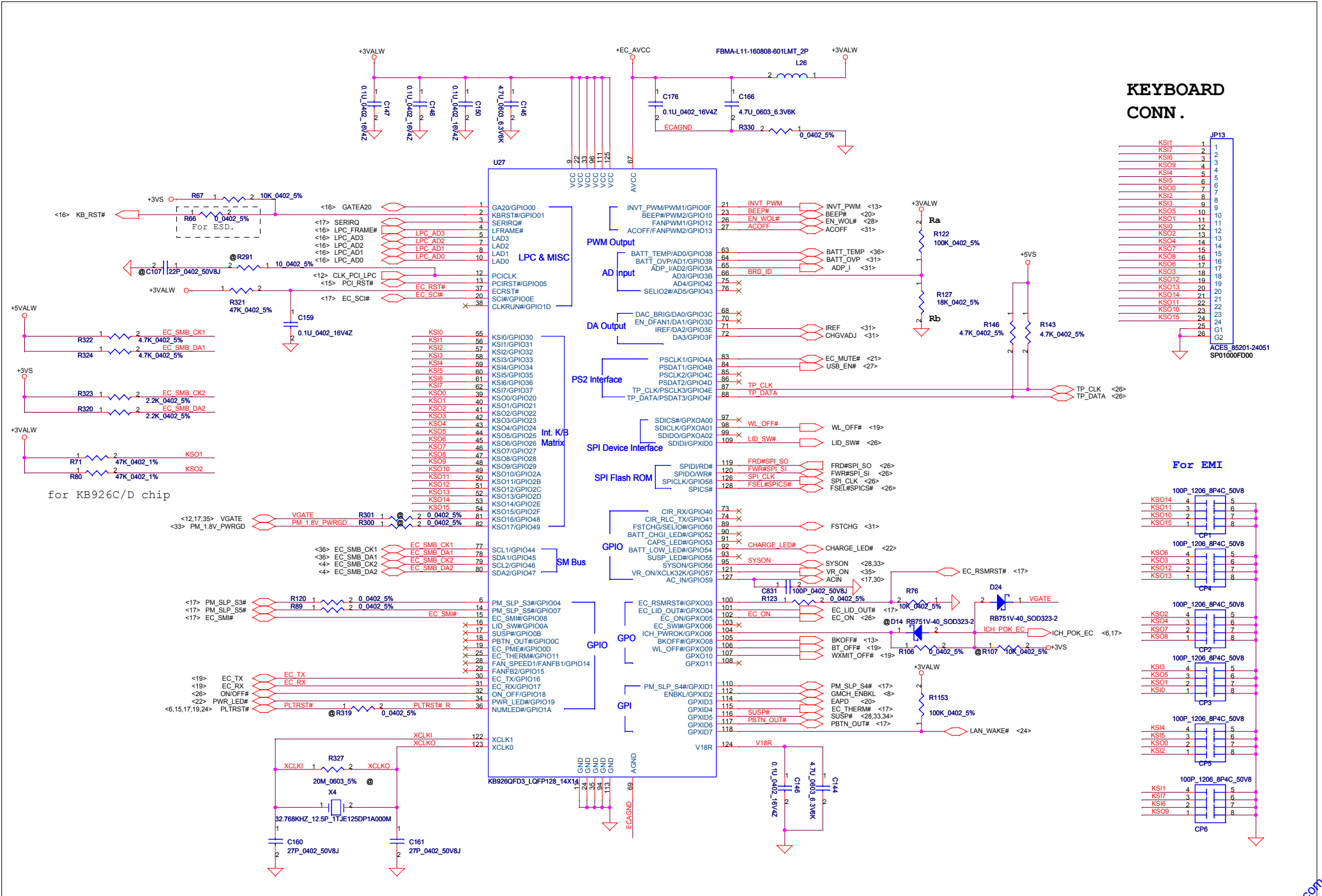
hexzain@hotmail.com



RJ45 symbol need update



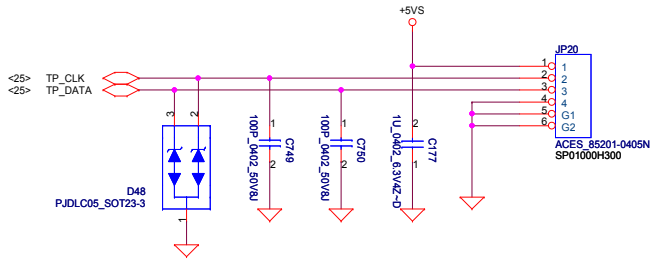
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				Customer	1.0
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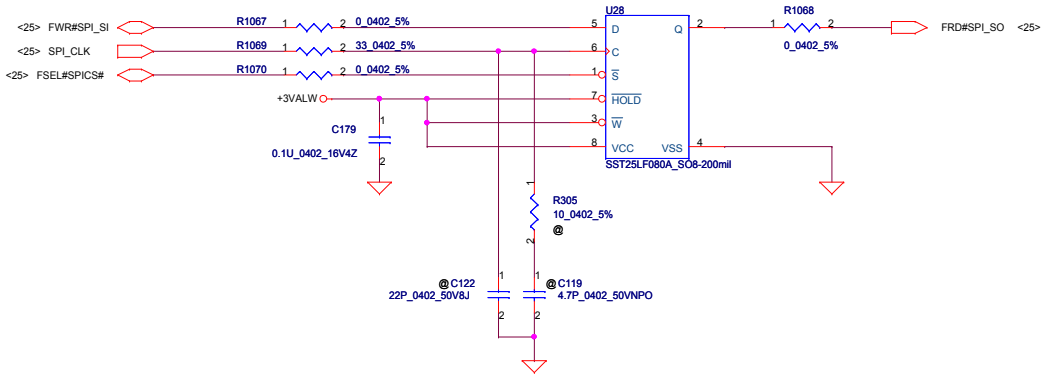
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Issued Date	2008/11/10	Deciphered Date	2009/11/10	Title	KB926
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Need to create symbol and footprint for MX SPI ROM

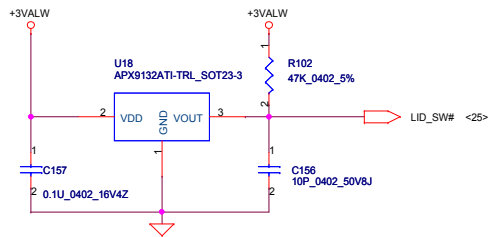
Touch/B Connector



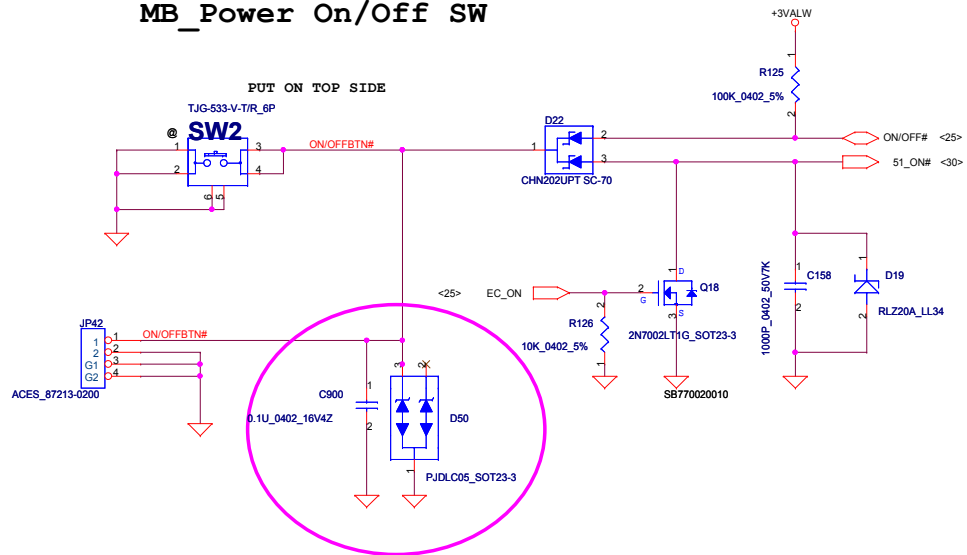
System SPI Flash ROM (8Mb)



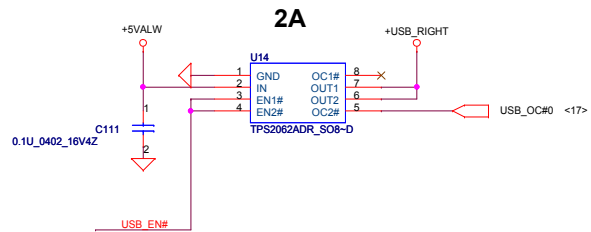
LID Switch



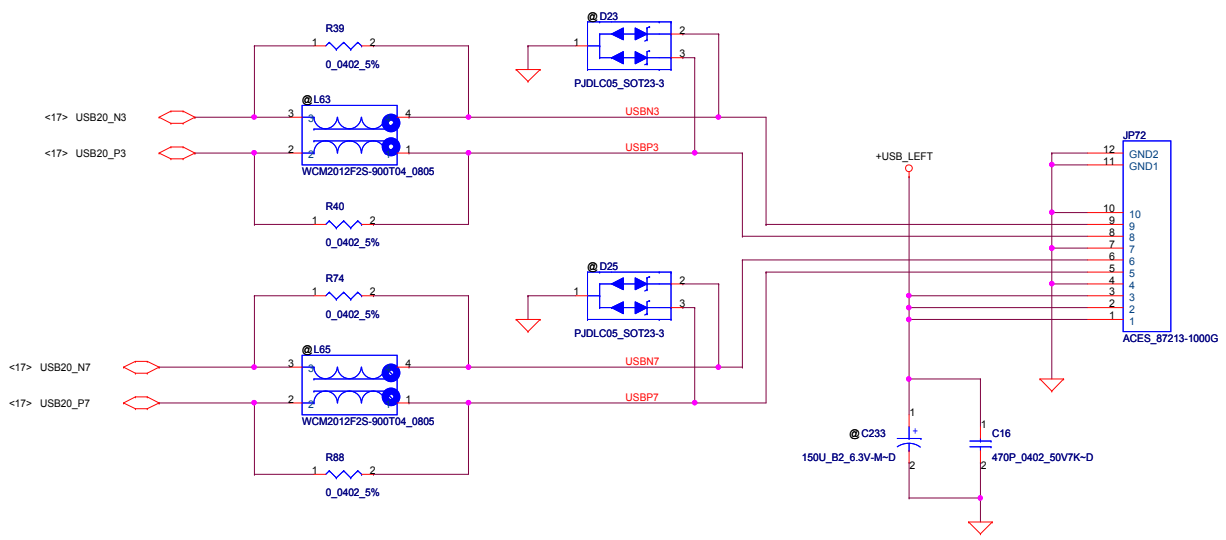
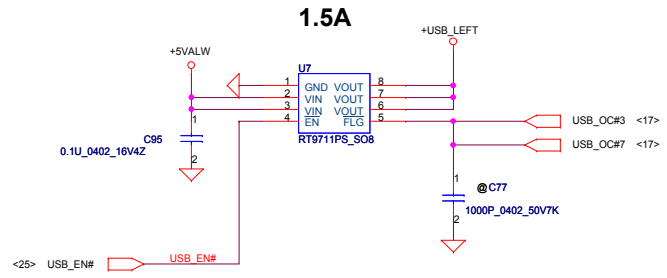
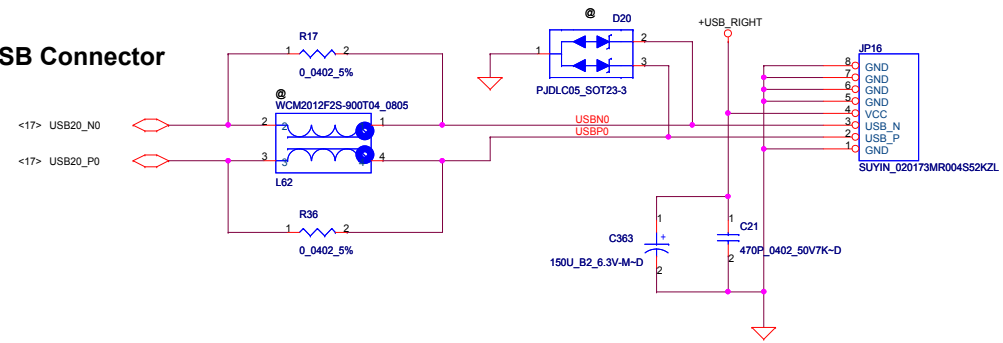
MB_Power On/Off SW



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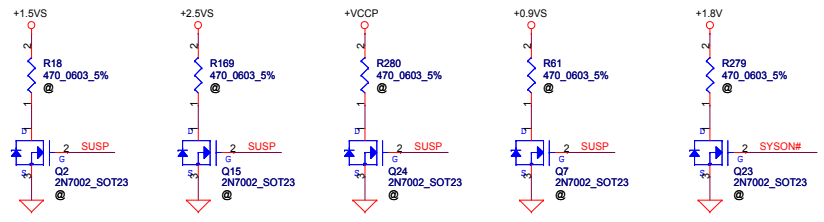
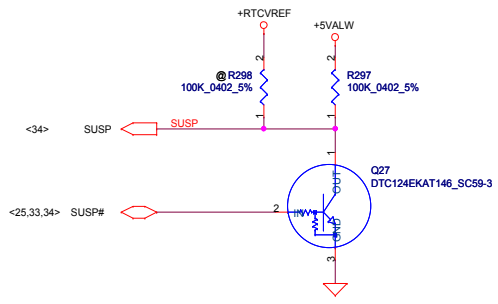
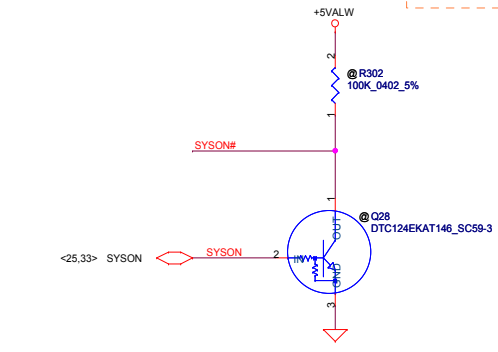
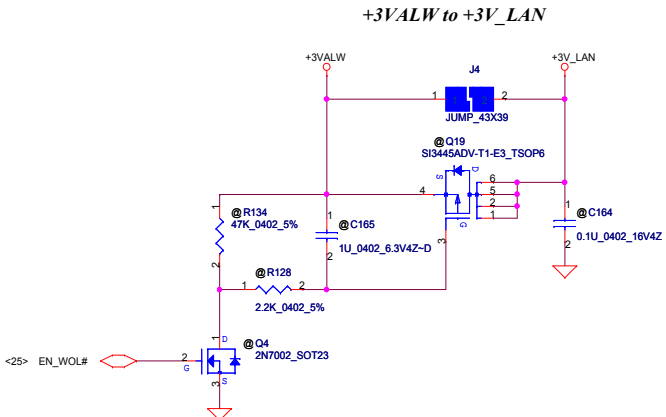
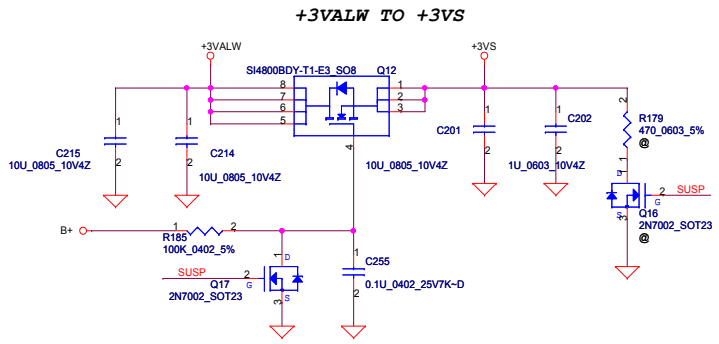
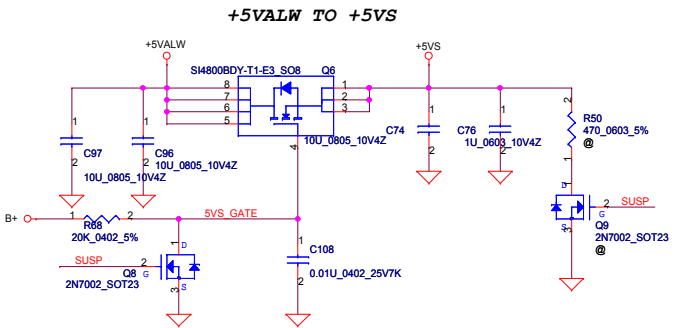


On Board USB Connector



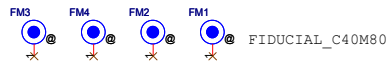
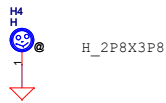
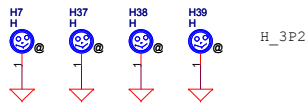
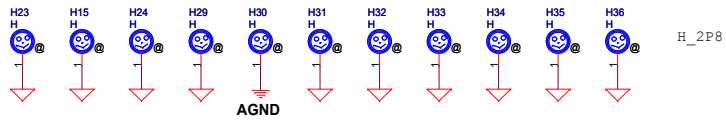
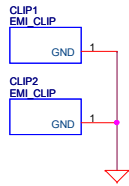
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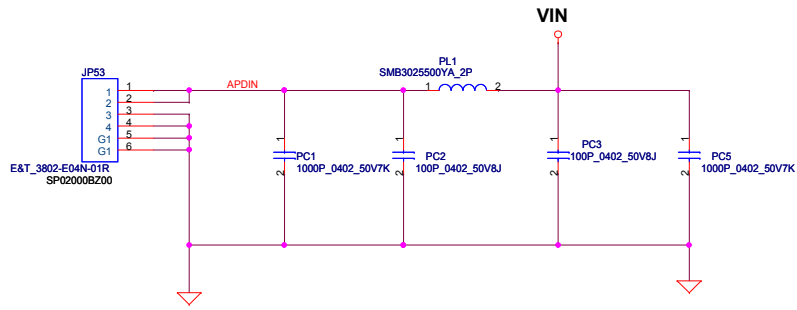
If the +1.8V discharge circuit is pop, R302, Q28 need pop.

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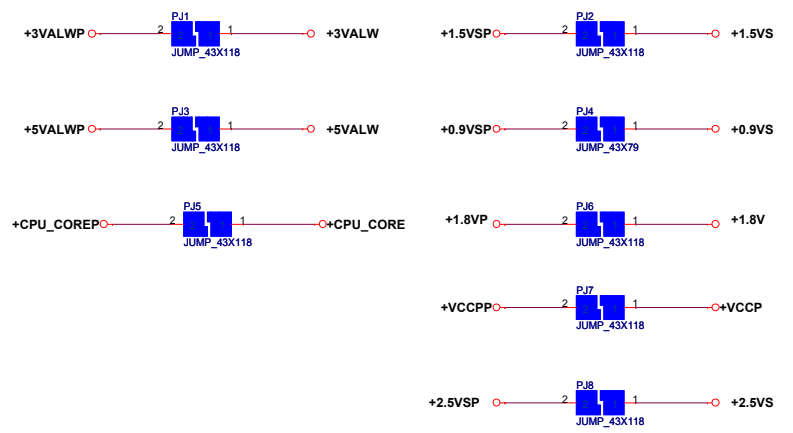
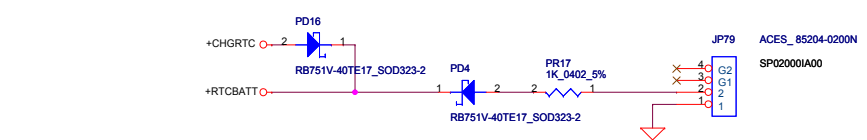
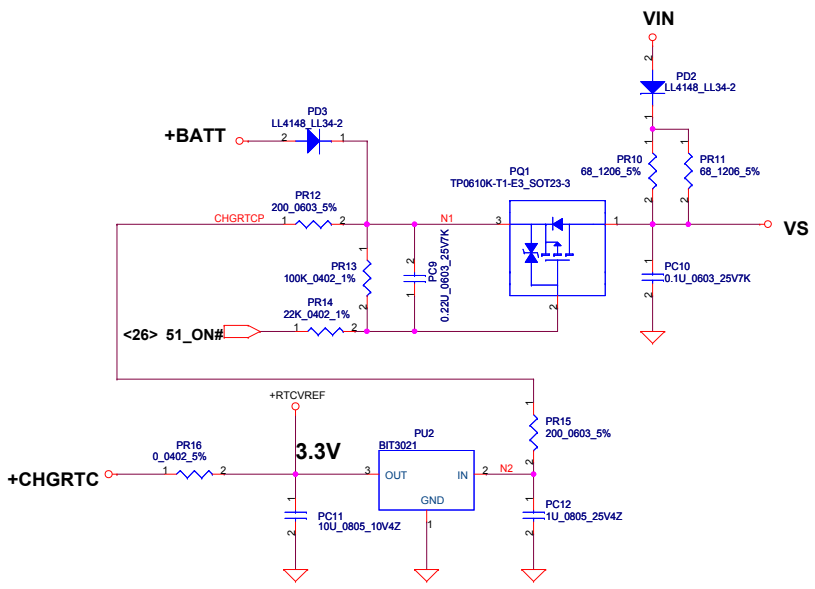
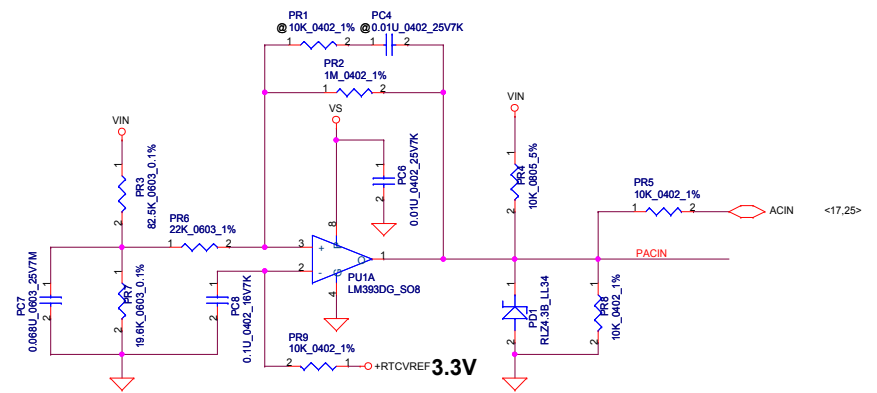


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lexaint@hotmail.com

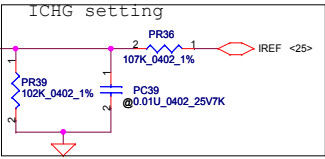
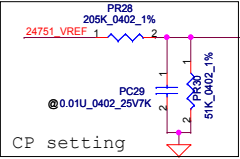
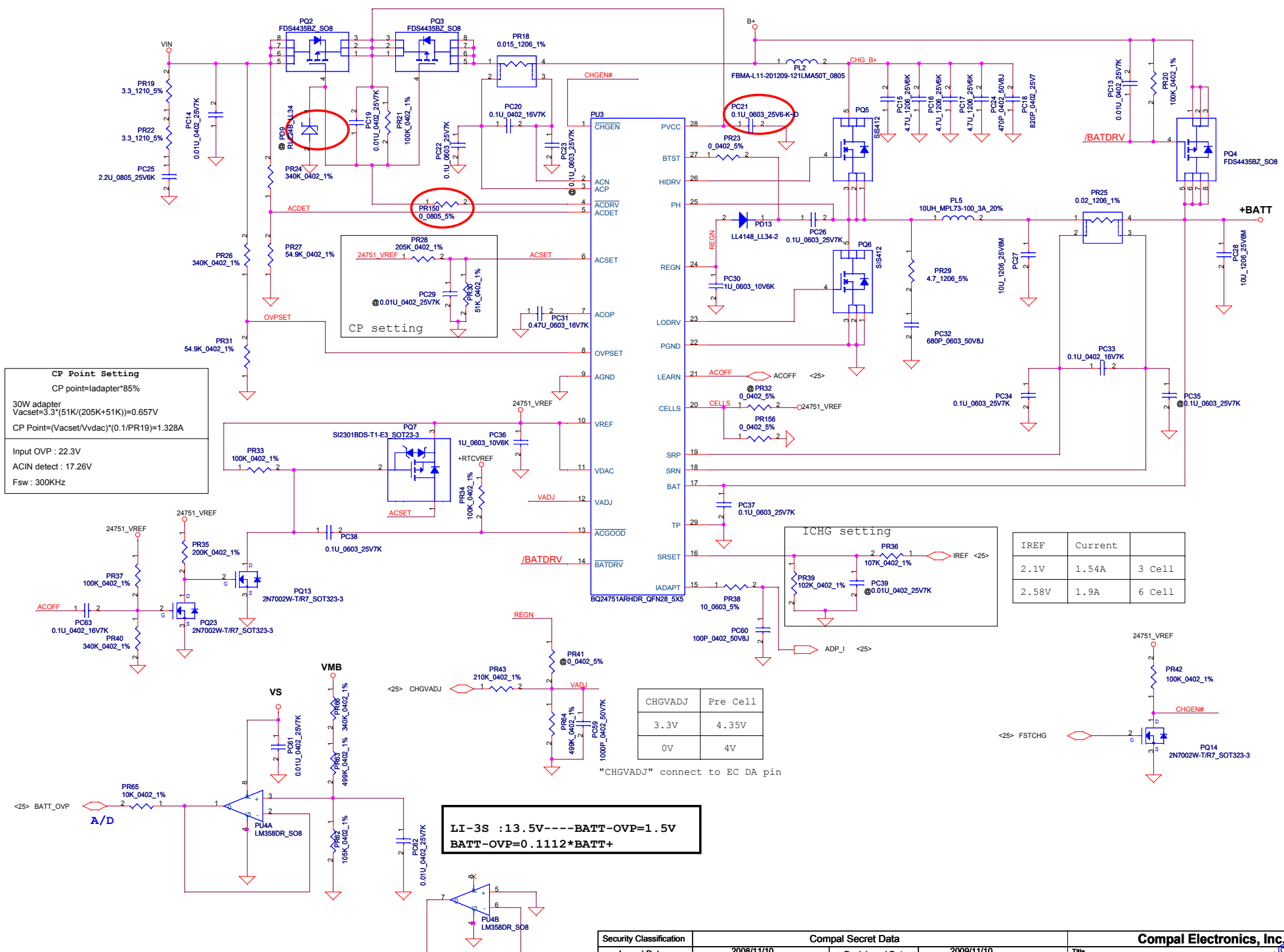


Vin Detector		
High	18.059	17.841 17.624
Low	17.418	17.210 16.998



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CP Point Setting
 CP point=ladapter*85%
 30W adapter
 Vacset=3.3*(51K/(205K+51K))=0.657V
 CP Point=(Vacset/Vvdac)*(0.1/PR19)=1.328A
 Input OVP : 22.3V
 ACIN detect : 17.26V
 Fsw : 300KHz

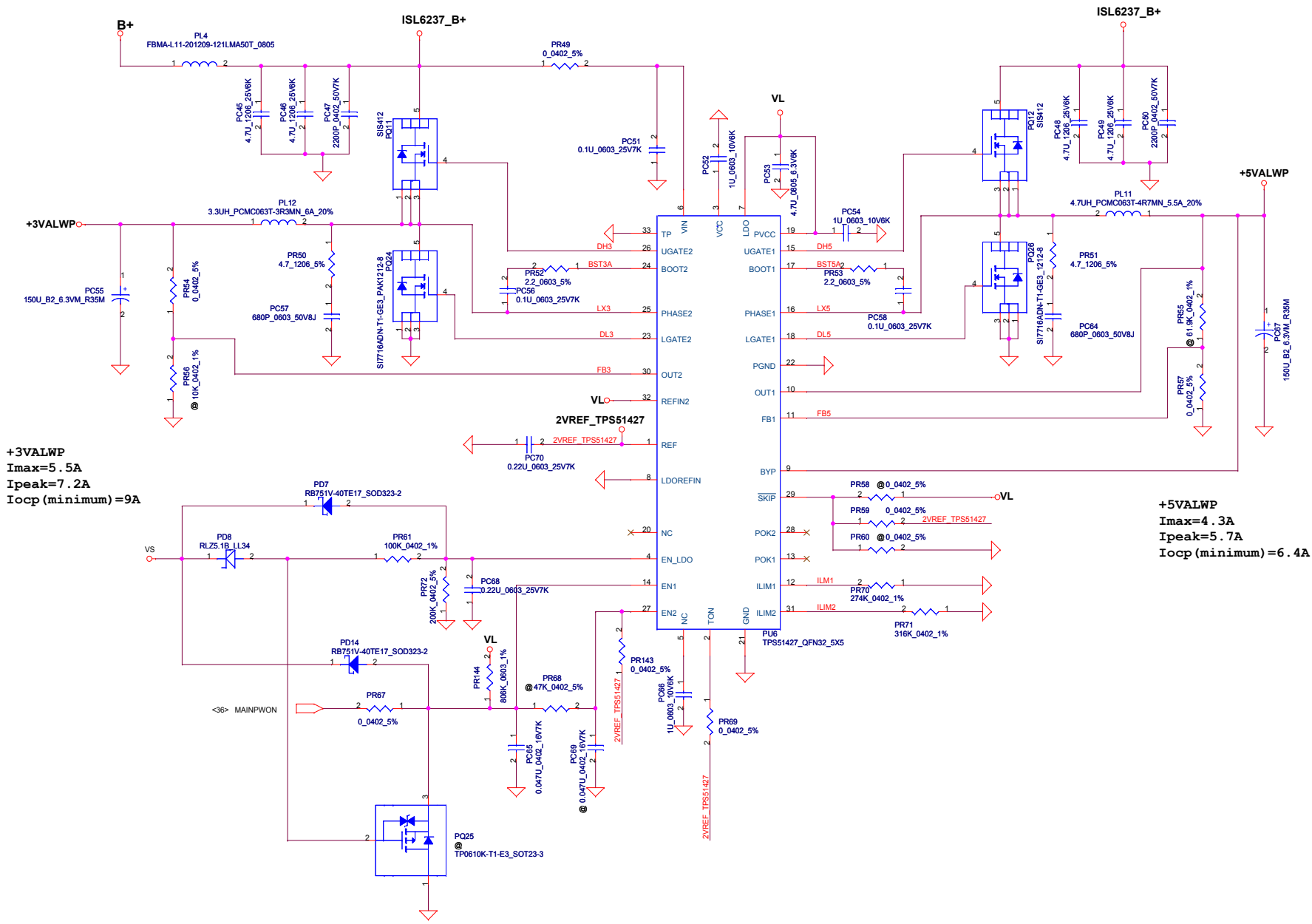


IREF	Current	
2.1V	1.54A	3 Cell
2.58V	1.9A	6 Cell

CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

LI-3S :13.5V---BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+

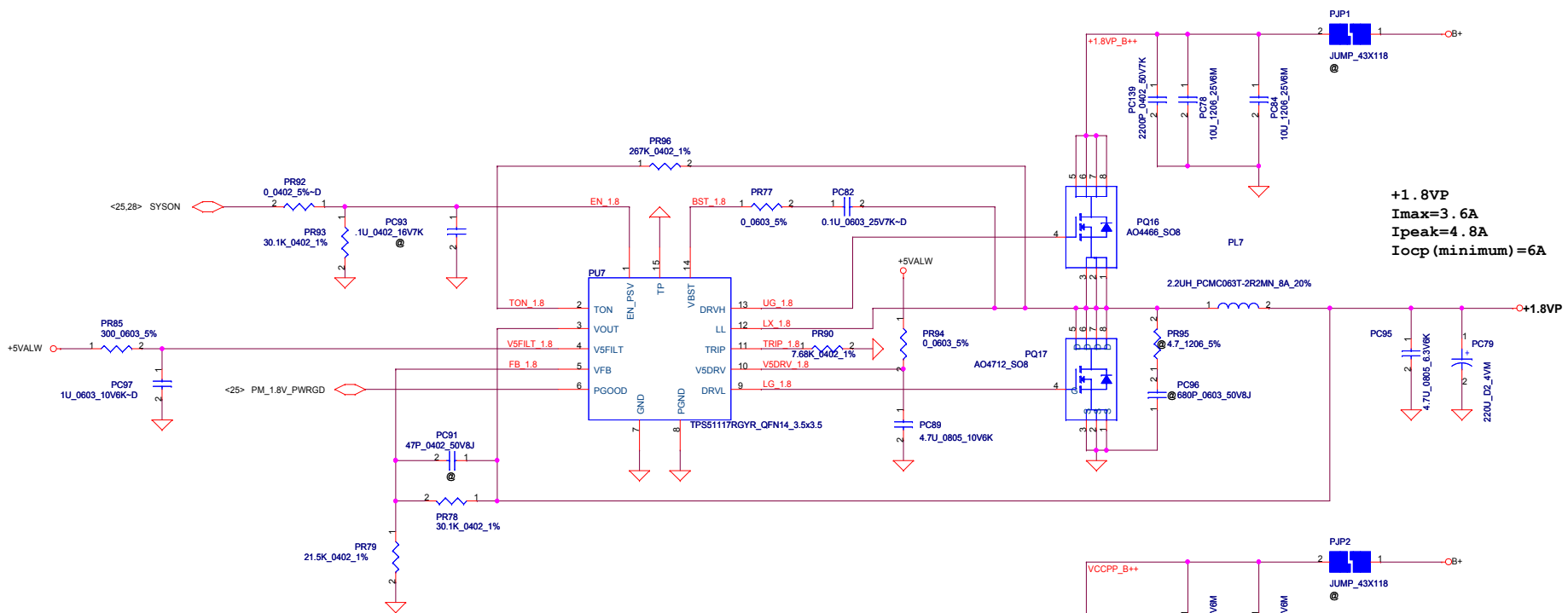
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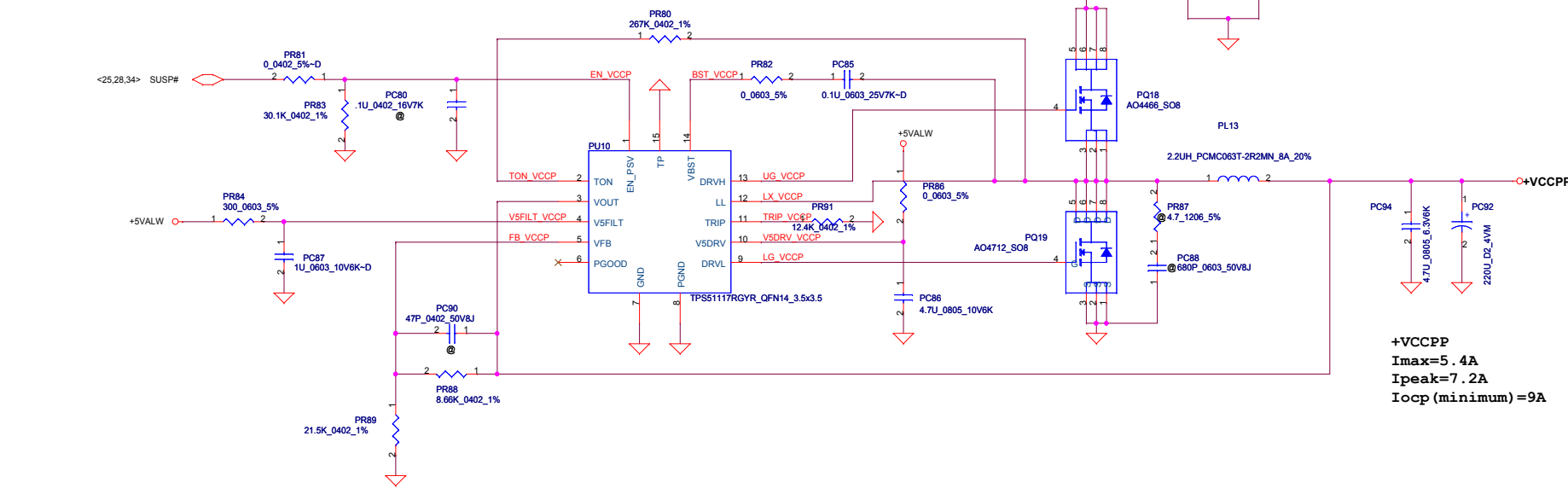
+3VALWP
 $I_{max} = 5.5A$
 $I_{peak} = 7.2A$
 $I_{ocp} (minimum) = 9A$

+5VALWP
 $I_{max} = 4.3A$
 $I_{peak} = 5.7A$
 $I_{ocp} (minimum) = 6.4A$

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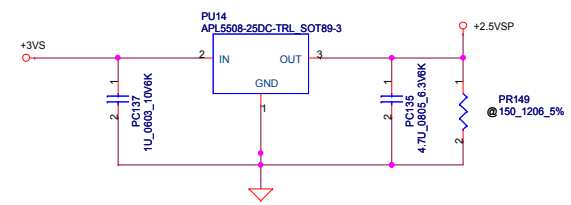
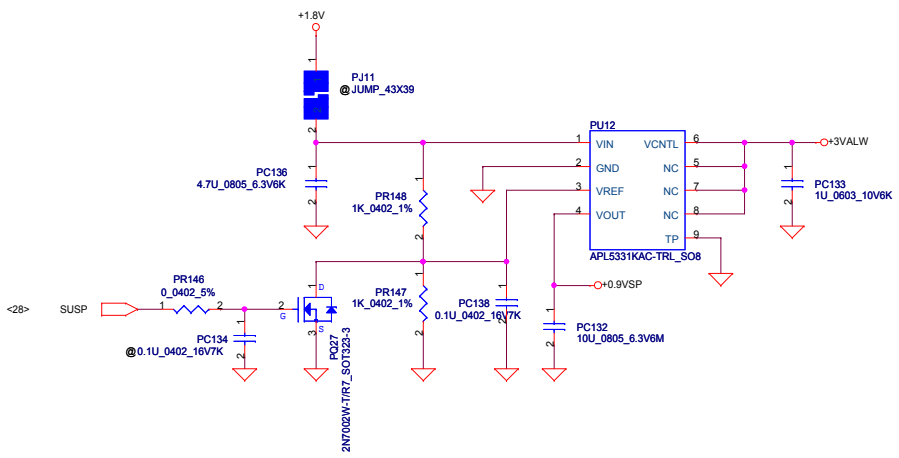
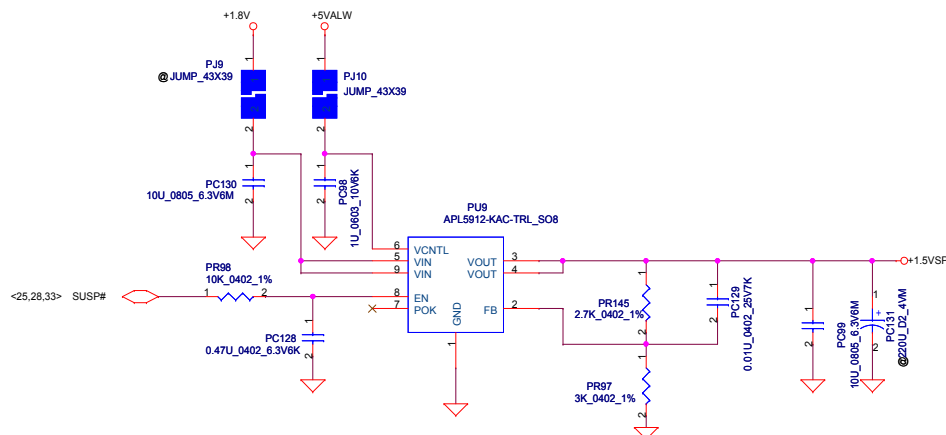


+1.8VP
Imax=3.6A
Ipeak=4.8A
Iocp (minimum)=6A

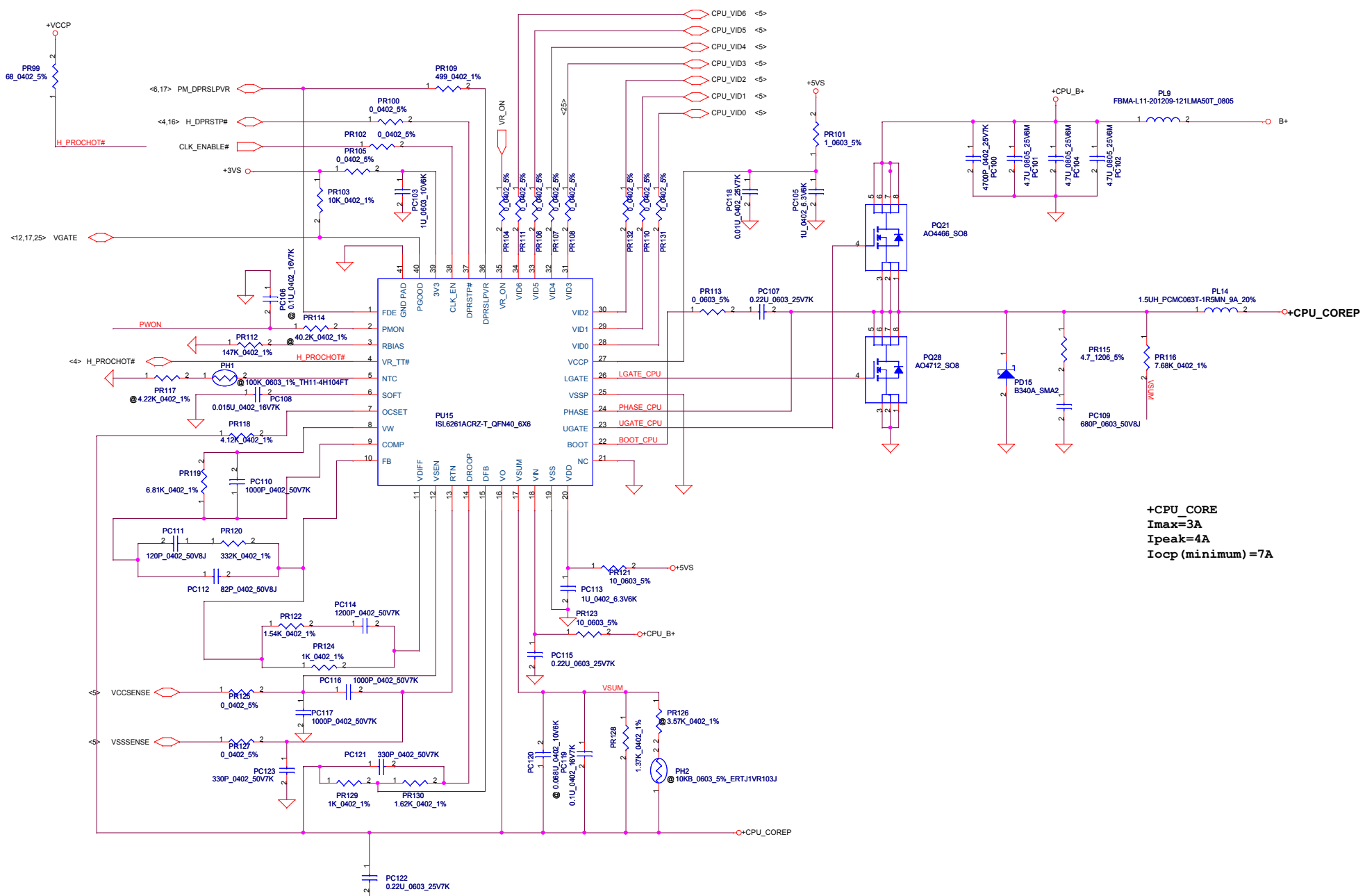


+VCCPP
Imax=5.4A
Ipeak=7.2A
Iocp (minimum)=9A

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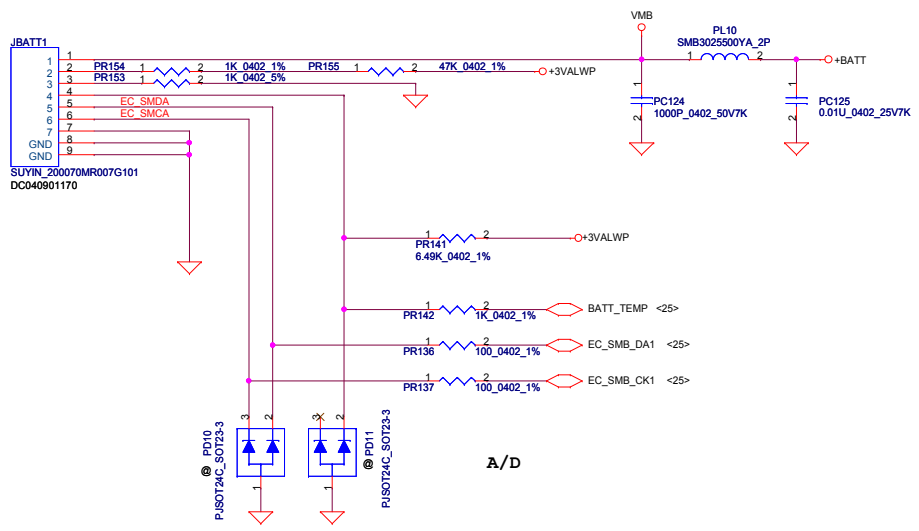


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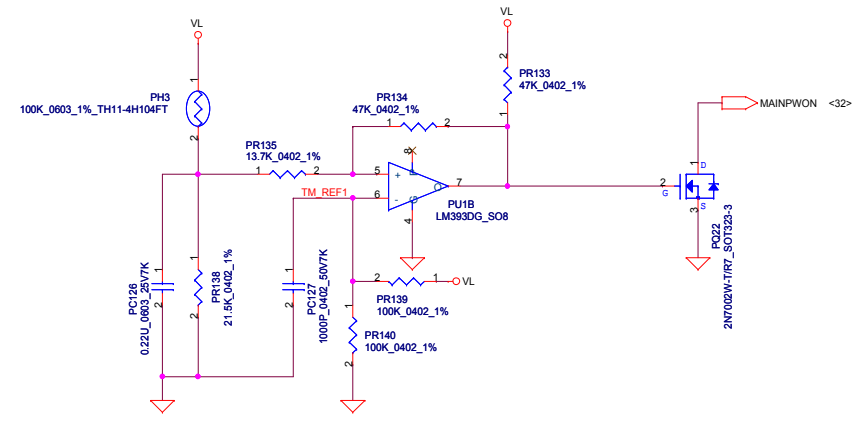


+CPU_CORE
I_{max}=3A
I_{peak}=4A
I_{ocp} (minimum) =7A

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PH3 under CPU botten side :
 CPU thermal protection at 85 degree C
 Recovery at 45 degree C



A/D

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Item	Date	Fixed Issue	Rev.	PG#	Modify List
1	2009/1/12	Circuit issue	0.2	13	Change JP24 pin definition
2	2009/1/12	System can't boot to S0	0.2	12	MCH_CLKREQ# connection move from U11.21 to U11.37
3	2009/1/12	Card reader remove crystal and use 48MHz from CLK generator	0.2	12 23	Pop R295, R137 change from 33 ohm to 22 ohm Pop R440, de-pop C511, C515, Y4
4	2009/1/12	WWAN function de-pop	0.2	19	De-pop C106, C196, C223, R75, R114, R115, JP56
5	2009/1/12	For S5 +3VS back drive issue	0.2	17	De-pop R284
6	2009/1/12	Material change	0.2	27	Change C233 and C363 to small package
7	2009/1/12	Codec can use 5V level for analog power	0.2	20	De-pop U20, C407 and pop R293
8	2009/1/12	LED circuit modify	0.2	22	1. JP62.11 as NC and JP62.3 connects to +5VALW. 2. Remove R294 and R576, and add serial resistors R314 and R315.
9	2009/1/13	Change material	0.2	21	Change Audio jack (JP60,JP61) to DC230005P00
10	2009/1/13	Change material	0.2	27	Change USB (JP16) connector to DC233004Q00
11	2009/1/13	Change material	0.2	26	Change SPI ROM (U28) to SA00000XT00
12	2009/1/14	Change material	0.2	14	Change Bead (L5,L19) to SM01003000L
13	2009/1/14	Swing is too big for SATA eye's diagram	0.2	16	Delete R12, and tied SATARBIASN & SATARBIASP together and connect to GND through a 24.9 ohm resistor
14	2009/1/15	For double place EMI solution	0.2	27	Delete R39,R40,R74,R88,L63,L65,D23,D25
15	2009/1/16	Board ID function	0.2	25	Pop R122, and change R127 to 8.2k
16	2009/1/17	Change pin out for LVDS connector	0.2	13	Swap INVT_PWM from JP24.3 to JP24.7
17	2009/1/17	Add control backlight function	0.2	13	Change Q80 to SB93457008L, pop Q80, C829, R1158, Q81,R1159, and de-pop L18
18	2009/1/17	Current leakage	0.2	28	De-pop R298, pop R297
19	2009/1/19	RGB EA fail	0.2	14	Change L1,L3,L4 to SM01000A00L
20	2009/1/19	Change material	0.2	24	Change JP71 to DC230901190
21	2009/1/20	add EMI solution	0.2	27	Add R39,R40,R74,R88,@D23,@D25,@L63,@L65
22	2009/1/20	For layout require	0.2	13	change R1006,R1007 to 0402 size
23	2009/1/20	For circuit design	0.2	13	change R1159 to 0402 size
24	2009/1/21	LAN LED reversed	0.2	24	Update JP71 symbol

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Item	Date	Fixed Issue	Rev.	PG#	Modify List
25	2009/1/21	Without beep when unplug RAM	0.2	20	Add C217,R1160,R1161,C213,C833
26	2009/1/21	Speaker pin out reversed	0.2	21	Modify JP55 pin definition
27	2009/1/21	Update SATA symbol	0.2	22	Modify JP48 pin name
28	2009/1/21	Remove WWAN signals	0.2	27	Change JP72 to 10 pin connector
29	2009/2/2	De-pop material	0.2	28	De-pop R302 and Q28
30	2009/2/6	Choose 48M function	0.2	23	Pop R299
31	2009/2/6	card reader INF installation issue	0.2	23	De-pop R436
32	2009/2/10	Fine tune LPC_FRAME# overshoot	0.3	16	Add R900
33	2009/2/18	Move cap to USB board	0.3	27	De-pop C233
34	2009/2/20	Solve "Zi Zi" noise	0.3	20	De-pop R1160,R1161 and remove C217
35	2009/2/20	Reserve for ESD	0.3	26	Add C900,D50 but de-pop
36	2009/2/27	Change CPU form N270 to N280	0.3	4,5,12	Change CPU P/N to N280 and de-pop R82 and pop R81 for FSB frequency to 667MHz
37	2009/2/27	To meet crystal requirement	0.3	25	Change C160 and C161 from 15pF to 27pF
38	2009/3/3	Modify board ID	1.0	25	Change R127 form 8.2k to 18k
39	2009/3/3	remove on board power switch	1.0	26	de-pop SW2
40	2009/3/4	WWAN concern	1.0	12	Add C903,C904,C905 and change C181,C198 from 0.1uF to 47pF
41	2009/3/10	USB modem issue	1.0	23	Reserve USB port 2 to WLAN and reserve USB port 6 to Card reader and add R1162,R1163,R1164,R1165,R1166,R1167,R1168,R1169
42	2009/3/10	For derating concern	1.0	19	Delete R75 and add J3
43	2009/3/11	Modify H4 and H23	1.0	29	Change H4 from H_3P0X4P0 to H_2P8X3P8 and H23 from H_3P0 to H_2P8.
44	2009/3/11	For beep noise	1.0	20	Add D1 and R1170
45	2009/3/31	change X1 part	1.0	10,25	Change C260,C276,C281,C330 to SE107475M0L, change C831 to SE071101J80

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	RTC Battery Pin define	RTC Battery can not work	0.1		JP79 connection pin1 exchange pin2	1/13	B
2		Battery connect placement from TOP to Bottom	0.1		JABTT1 footprint change to SUYIN_200070MR007G101ZR_7P-T	1/13	B
3		COST	0.1		PQ5,PQ6,PQ11,PQ12 P/N change from SB00000AU00 to SB00000IA00 PQ16,PQ18 P/N change from SB00000920L to SB00000CG00 PQ17,PQ19 P/N change from SB000004T8L to SB00000AJ00	1/14	B
4		Modify load line setting	0.1		PR116 change from 11.68K to 7.68K PR128 change from 1.82K to 1.37K	1/14	B
5		Modify charger current setting	0.1		PR36 change from 174K to 107K	1/14	B
6		COST	0.1		PU5 P/N change from SA00002D200 to SA00002V40L PU2 P/N change from SA009200010 to SA00002E200 PC24 P/N change from SE071471J80 to SE074471K80	1/17	B
7		For EMI	0.1		Add PC139 2200PF	1/17	B
8		Battery cell setting	0.1		Add PR156 0 Unpop PR32 0	1/17	B
9		Modify P/N for unify	0.2		PR81, PR92 P/N change from SD02800008L to SD028000080 PR142, PR154 P/N change from SD03410018L to SD034100180 PR138 P/N change from SD034215280 to SD03421528L PR133, PR134 P/N change from SD034470280 to SD03447028L PC105, PC113 P/N change from SE000000K80 to SE000000K8L PC82, PC85 P/N change from SE042104K8L to SE042104K80 PC11 P/N change from SE053106Z80 to SE053106Z8L PC87, PC97 P/N change from SE080105K8L to SE080105K80	2/18	C
10		Change P/N for Lead Free	0.3		PR128 P/N change from SD034137100 to SD03413718L PR3 P/N change from SD027825200 to SD027825280	3/18	X build
11		Change drive IC voltage input resistor for suqence	0.3		PR84 change from 0 to 300 PR85 change from 0 to 300	3/18	X build
12		Change P/N for approve	0.3		PU5 P/N change from SA00002V40L to SA00002V400	3/19	X build
13		Protect Charger IC burn out for Adapter Inrush Current	0.3		Add NonPop PD9 SC4LZ24B0T1 S ZEN DIO RLZ24B (LL-34) Add PR150 SD00200008L S RES 1/8W 0 +5% 0805	3/27	X build
14	Enter windows hang	Reduce CPU Switch phase ring for High speed trace	0.3		Pop PR115 S RES 1/4W 4.7 +-5% 1206 Pop PC109 S CER CAP 680P 50V J NPO 0603	4/17	X build

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