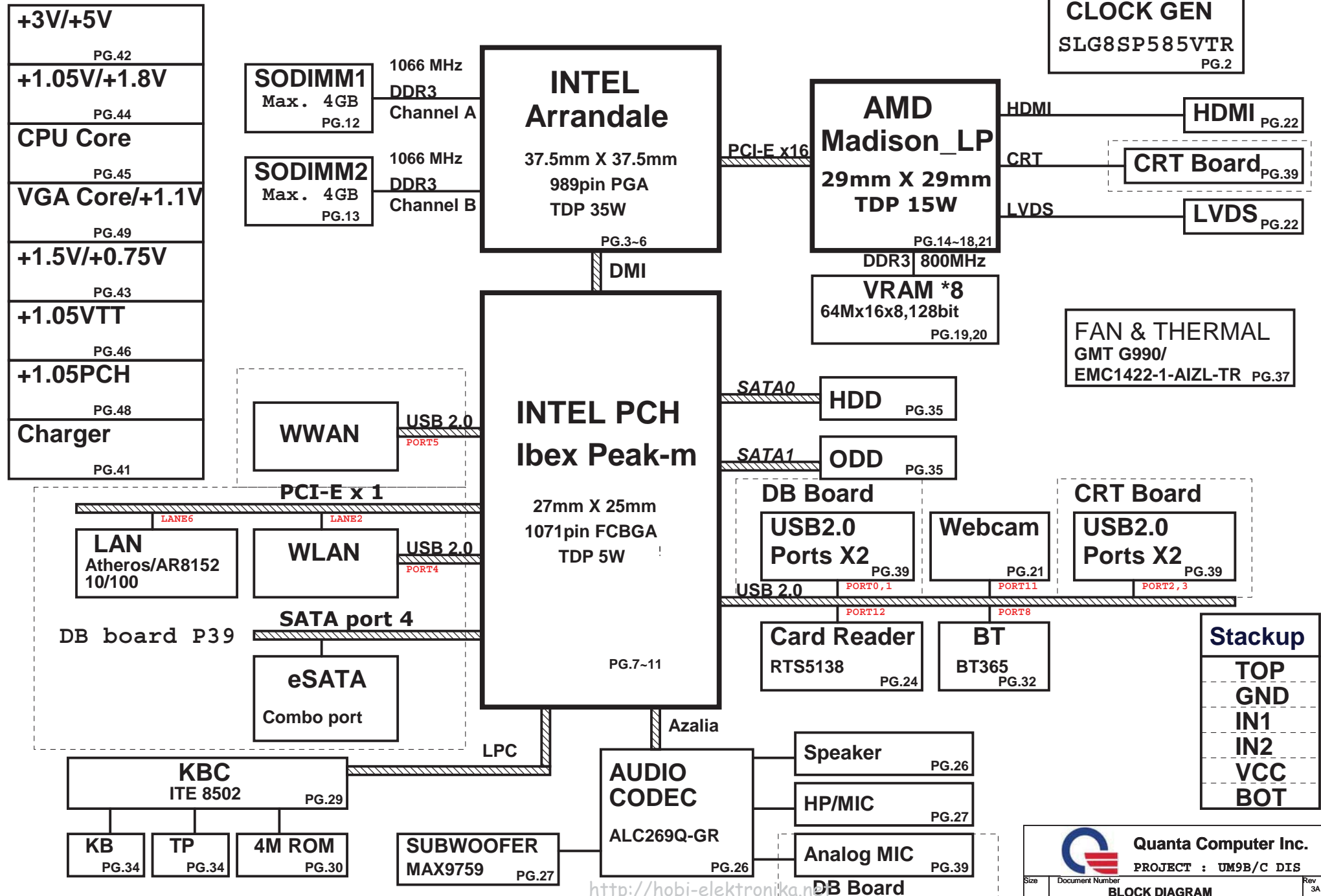


UM9B/C DISCRETE SYSTEM DIAGRAM

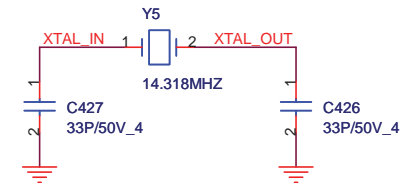
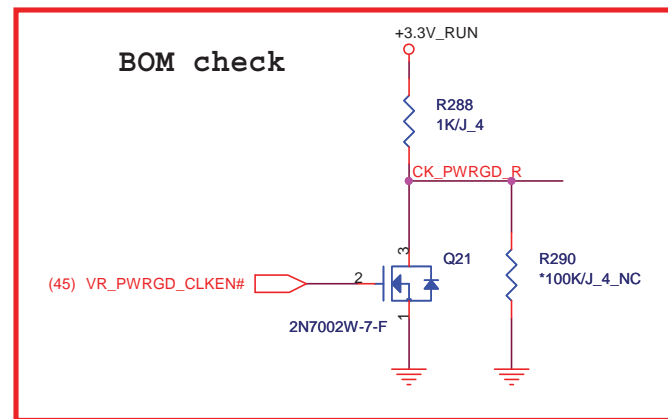
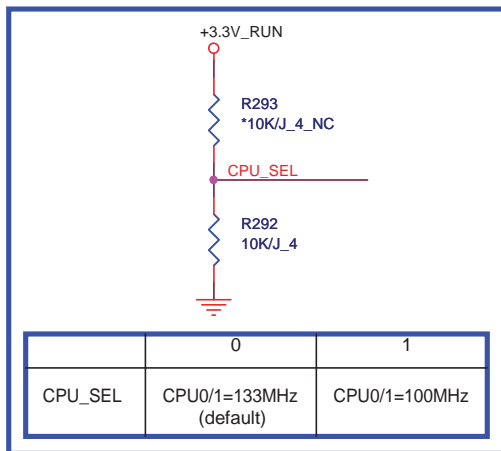
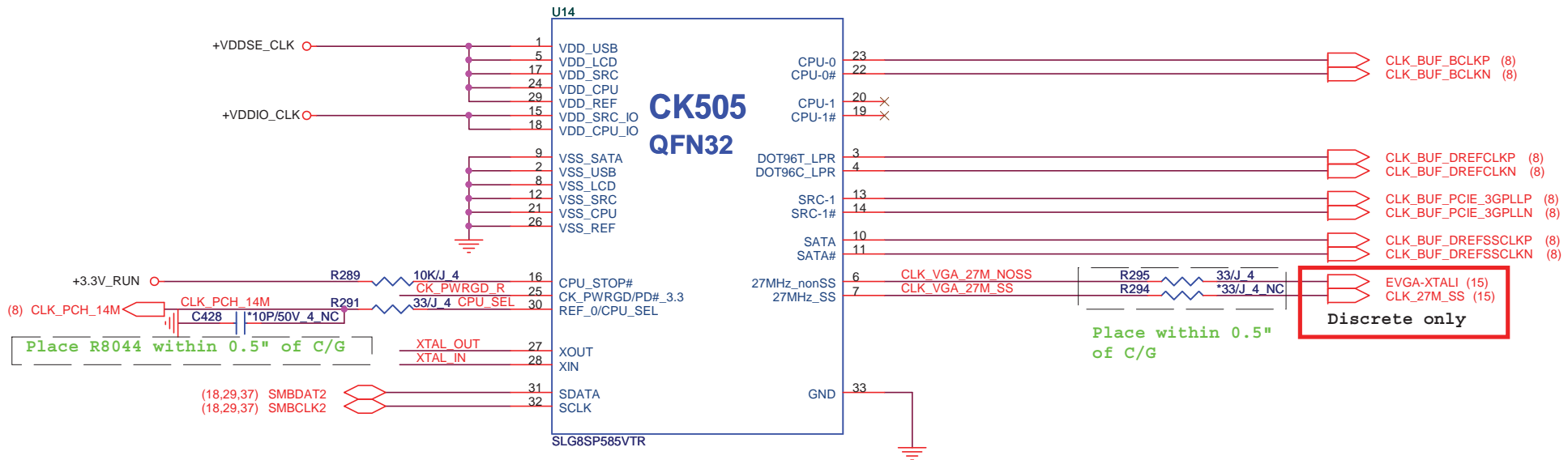
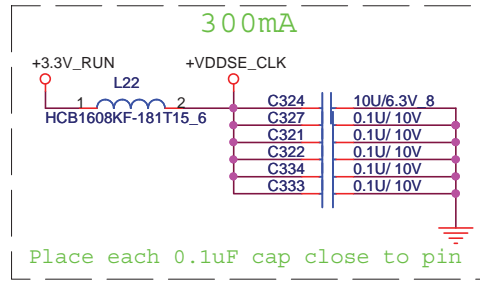
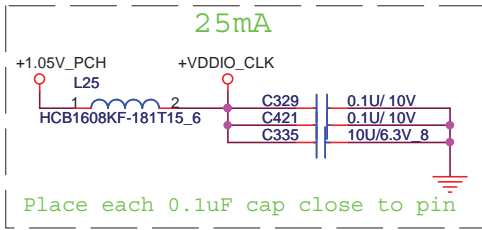


<http://hobi-elektronika.net>

Quanta Computer Inc.
 PROJECT : UM9B/C DIS
BLOCK DIAGRAM

Size	Document Number	Rev
		3A
Date:	Wednesday, January 27, 2010	Sheet 1 of 51

PDC (Power Cap quantities follow UM3)

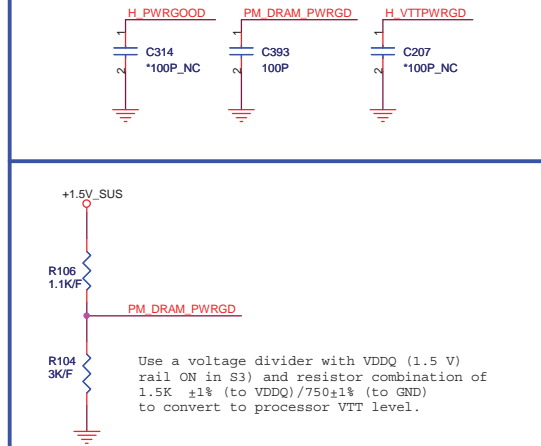
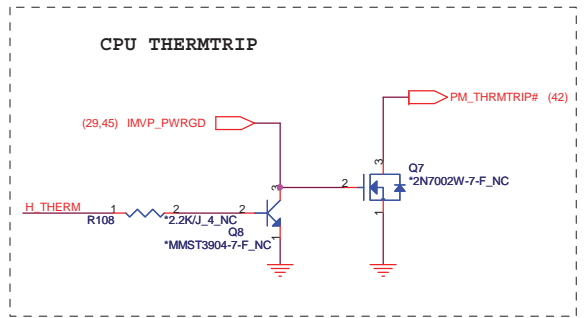
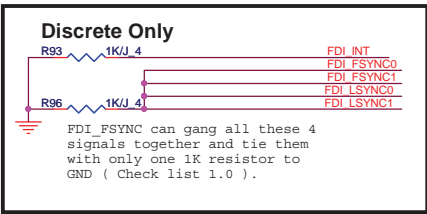
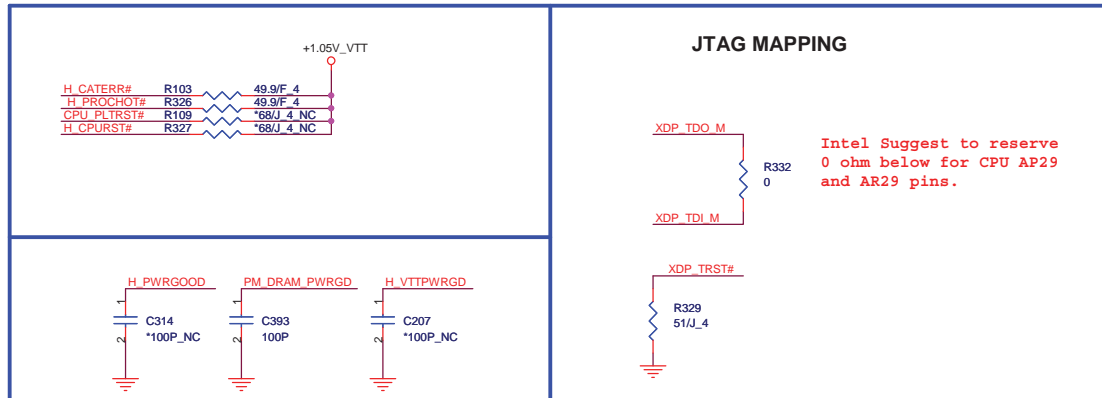
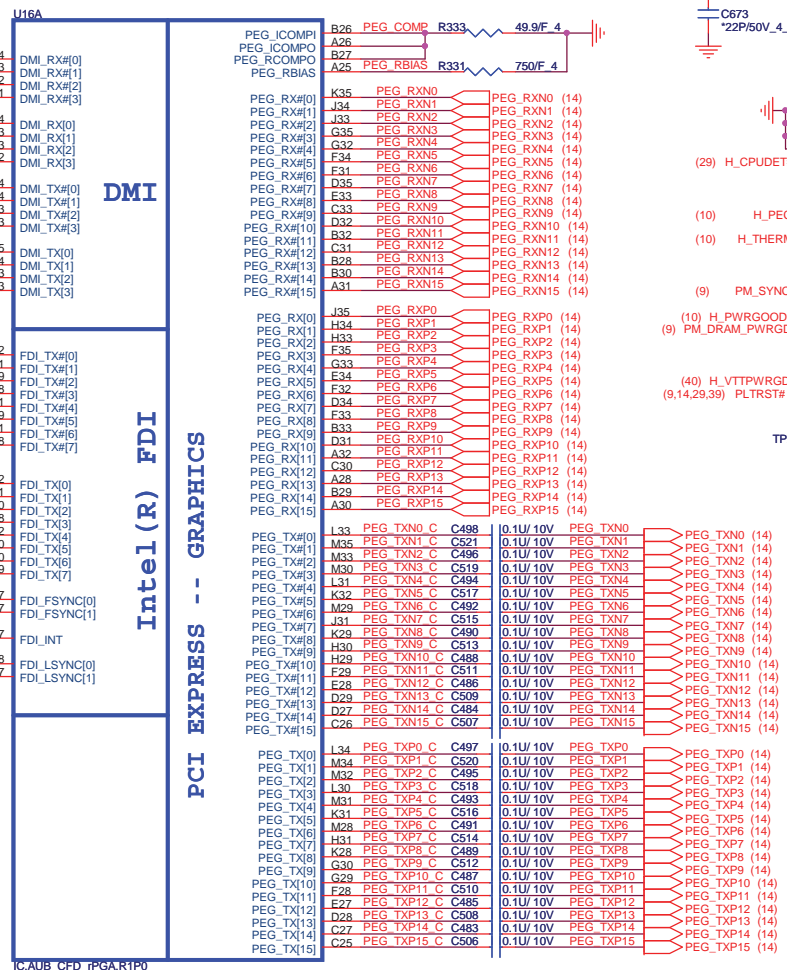


Quanta Computer Inc.
PROJECT : UM9B/C DIS

Size	Document Number	Rev
	Clock Gen(9LRS3197)/HOLES	3A
Date:	Monday, February 01, 2010	Sheet 2 of 51

	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

DPLL_REF_SSCLK: Embedded Display Port PLL Differential Clock In. If no eDP, do we need implement these R?

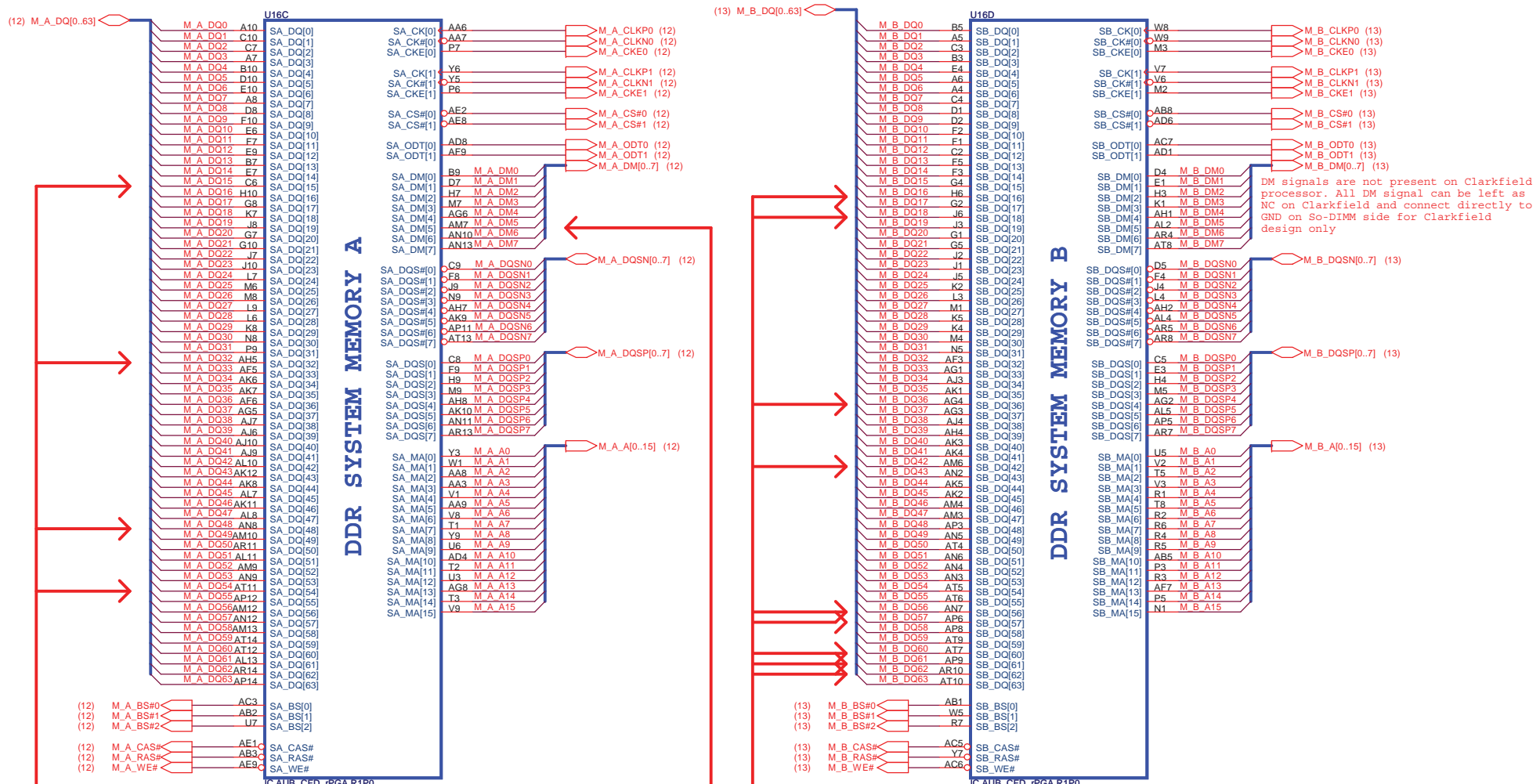


Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

Quanta Computer Inc.
PROJECT : UM9B/C DIS

Size	Document Number	Rev
	PROCESSOR 1/4(HOST&PEX)	3A
Date:	Monday, February 01, 2010	Sheet 3 of 51

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

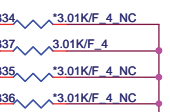
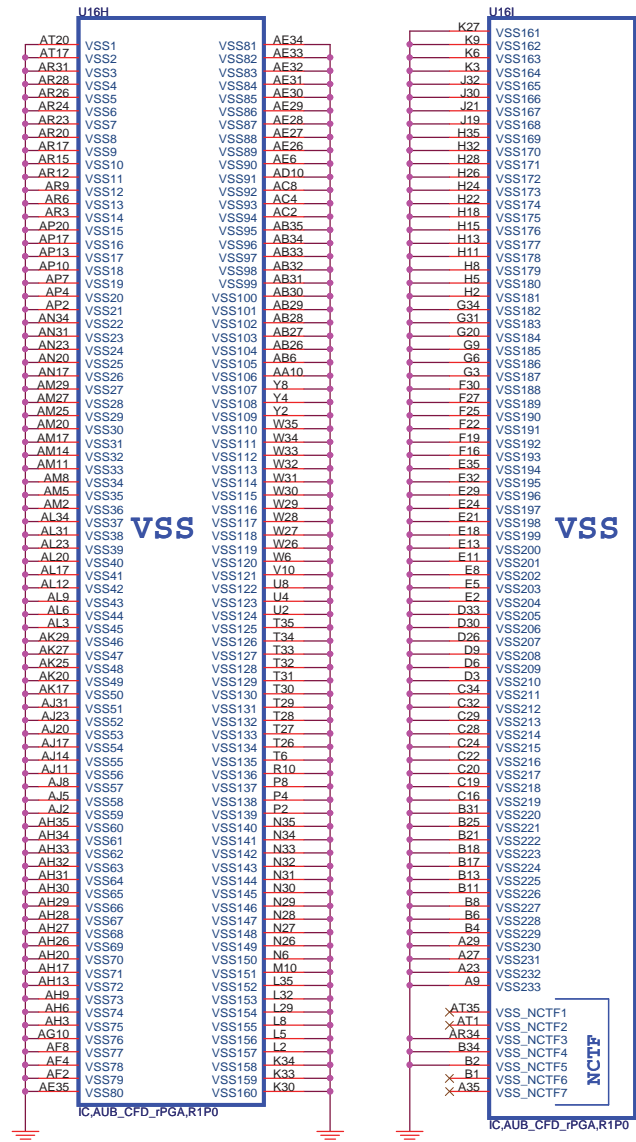
Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

Quanta Computer Inc.
PROJECT : UM9B/C DIS

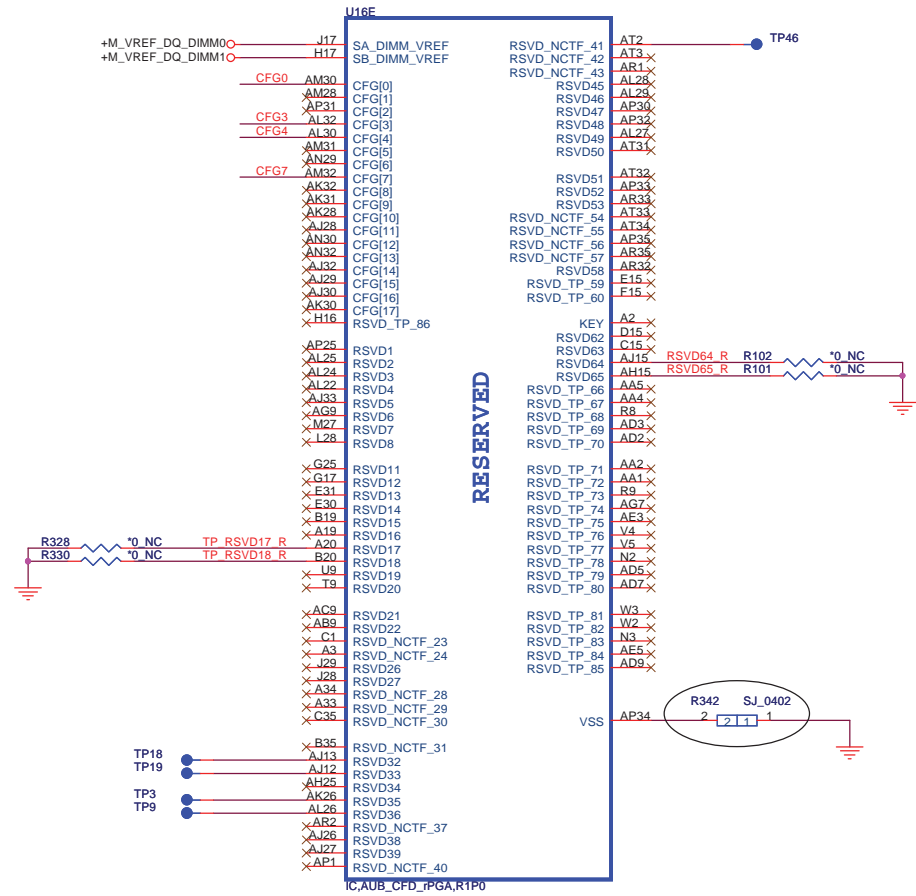
Size	Document Number	Rev
	PROCESSOR 2/4(DDR)	3A
Date:	Monday, February 01, 2010	Sheet 4 of 51

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1



For Discrete only

CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG

Quanta Computer Inc.
 PROJECT : UM9B/C DIS

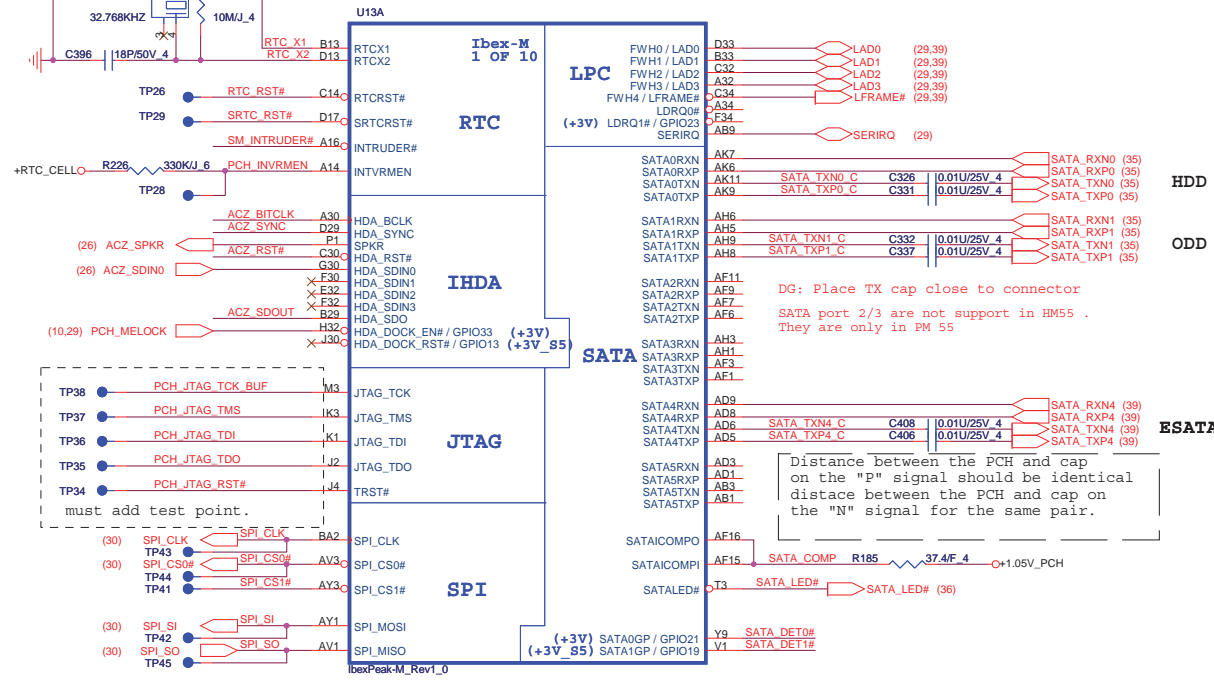
Size | Document Number | Rev
 | | | 3A

PROCESSOR 4/4 (GND)

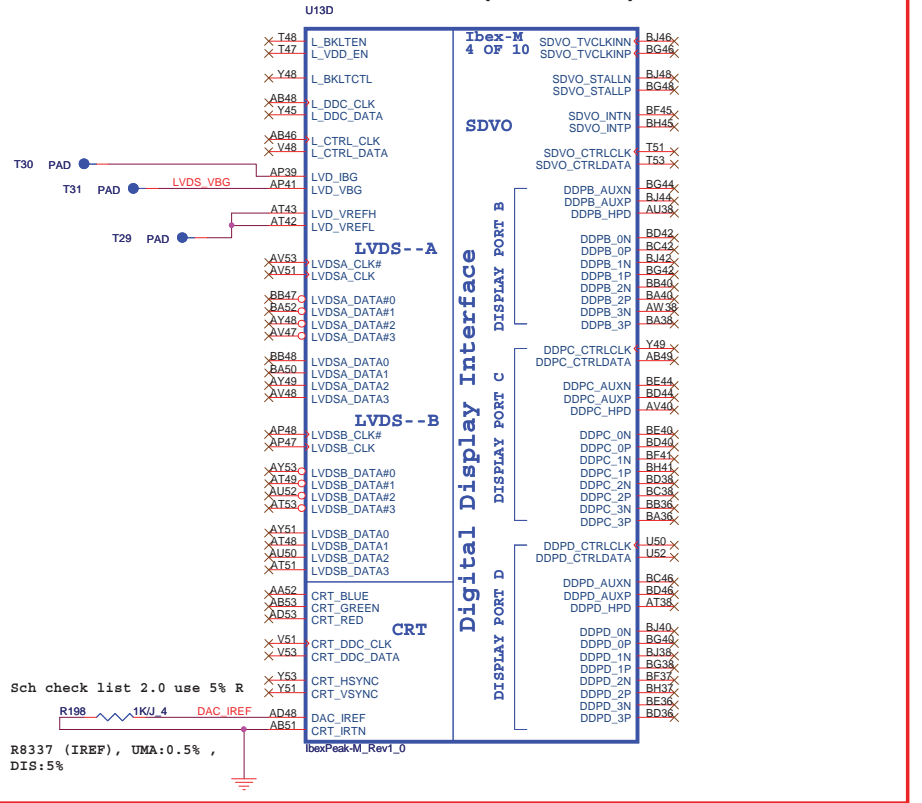
Date: Wednesday, January 27, 2010 | Sheet 6 of 51

The Clarkfield processor's PCI Express 2.0 jitter specifications may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

IBEX PEAK-M (HDA,JTAG,SATA)



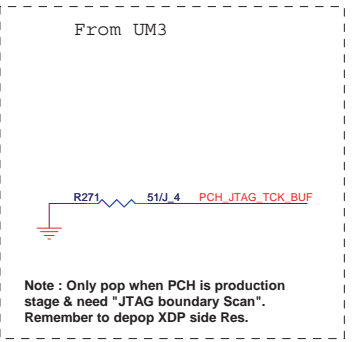
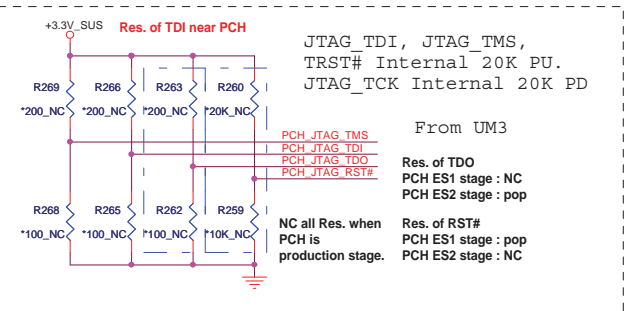
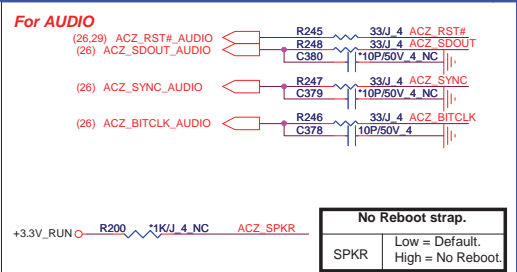
UMA CRT, LVDS&HDMI signals IBEX PEAK-M (LVDS,DDI)



1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

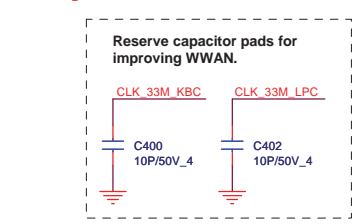
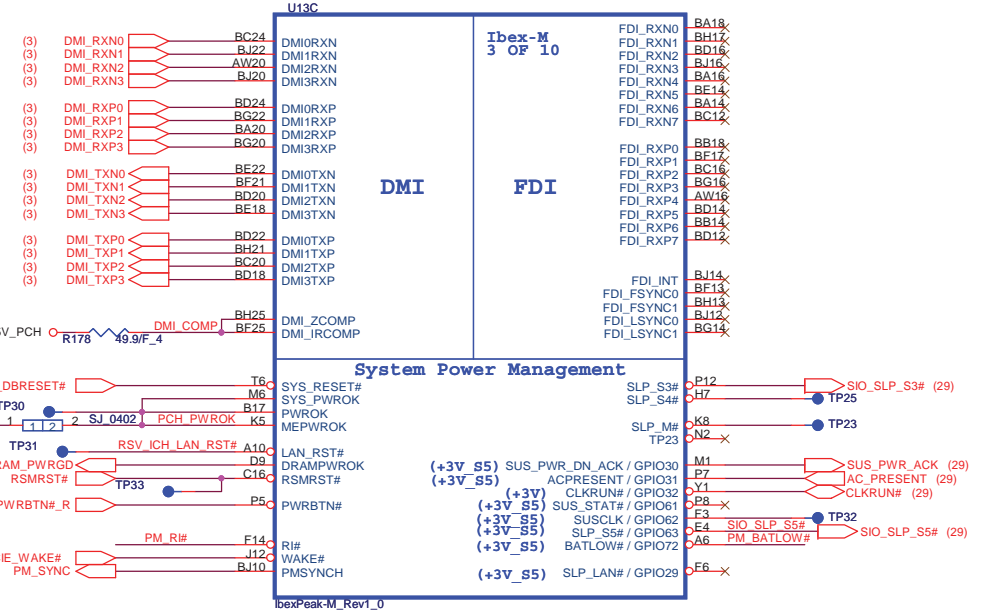
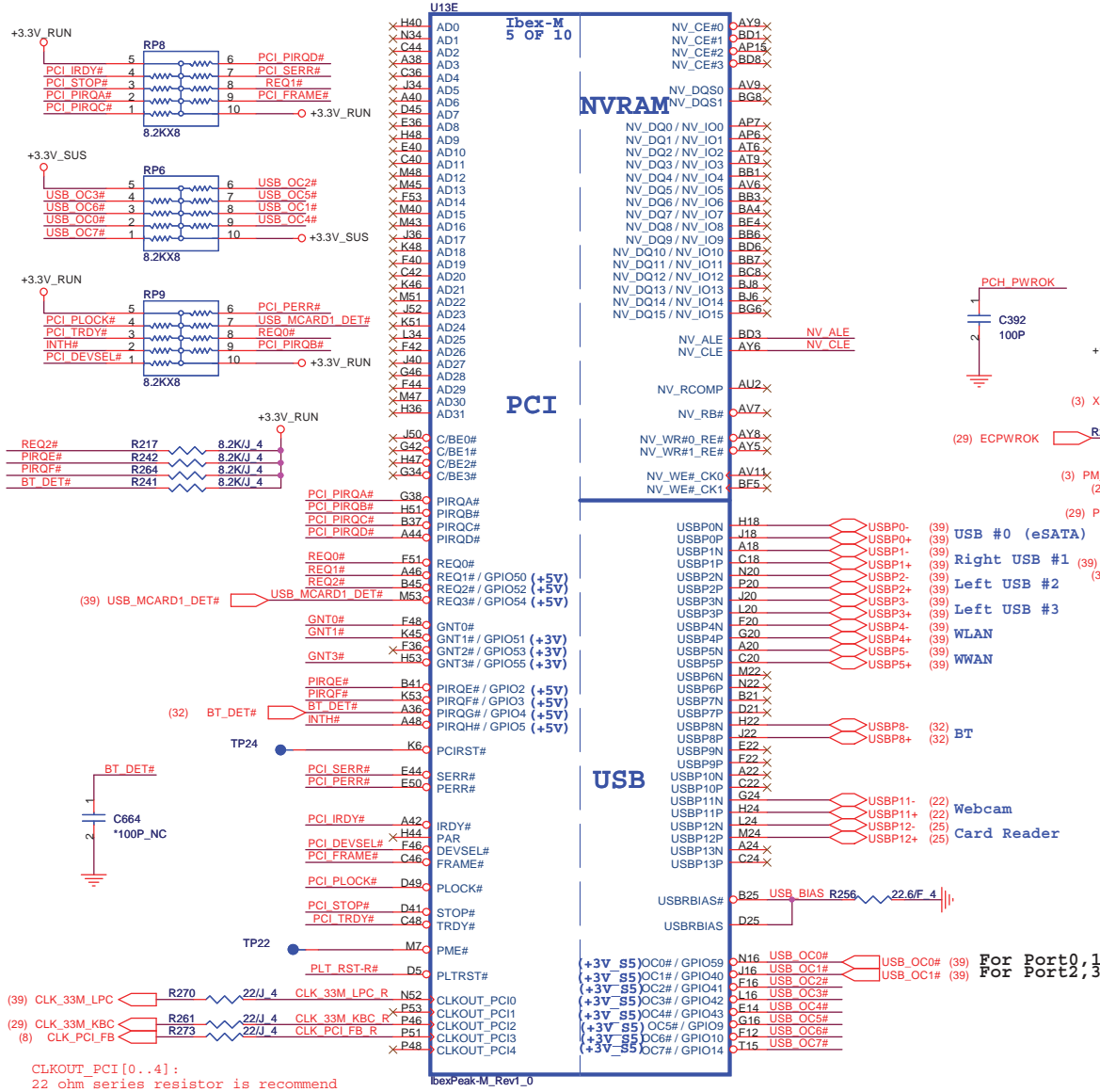
ITPM ENABLE/DISABLE
From UM3

TPM Function	
Enable	Mount
Disable	NC (Default)



IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)

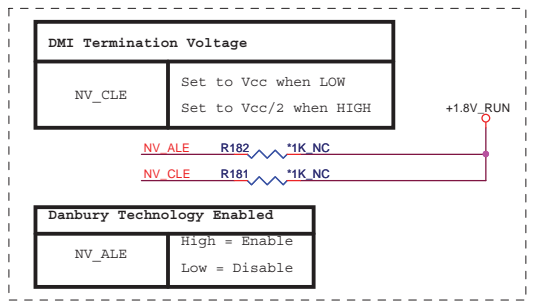
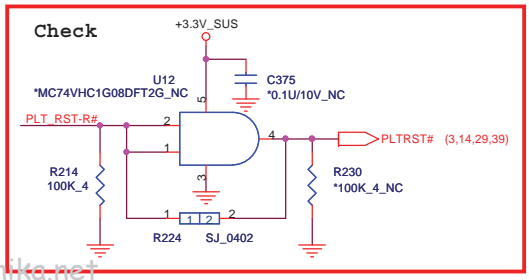
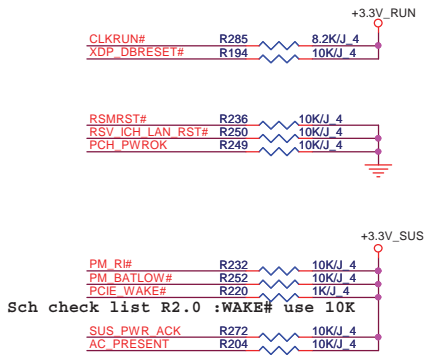


Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

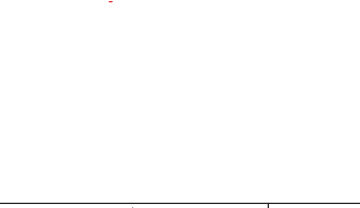
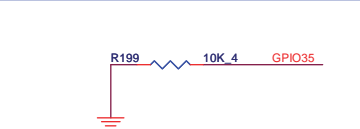
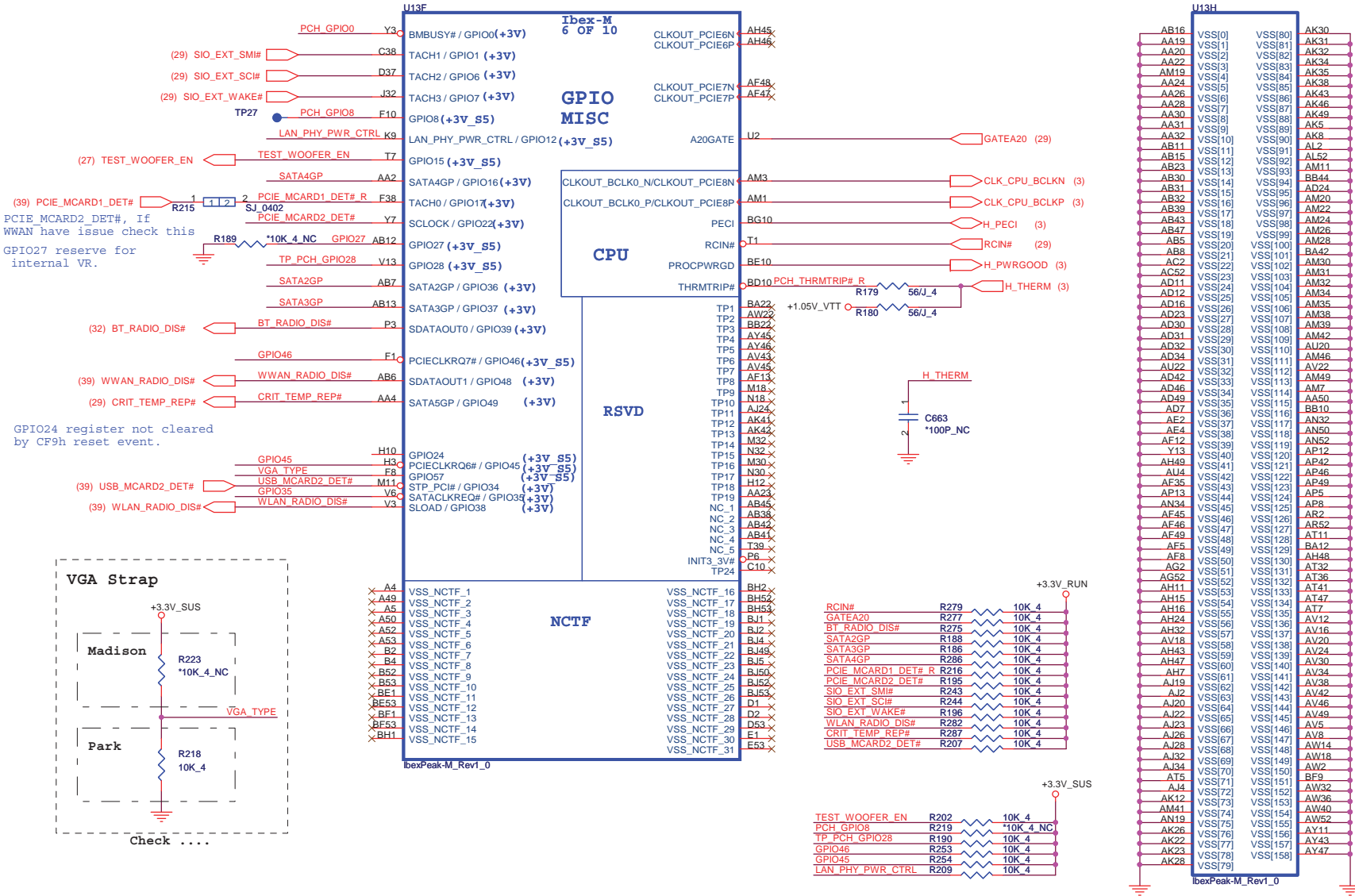
A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 swap override/Top-Block Swap Override enabled	High = Default
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled	High = Default



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)



GPIO[7,6,1,17], PCIECLKRQ6#/GPIO45, GPIO28 Internal 20K PU

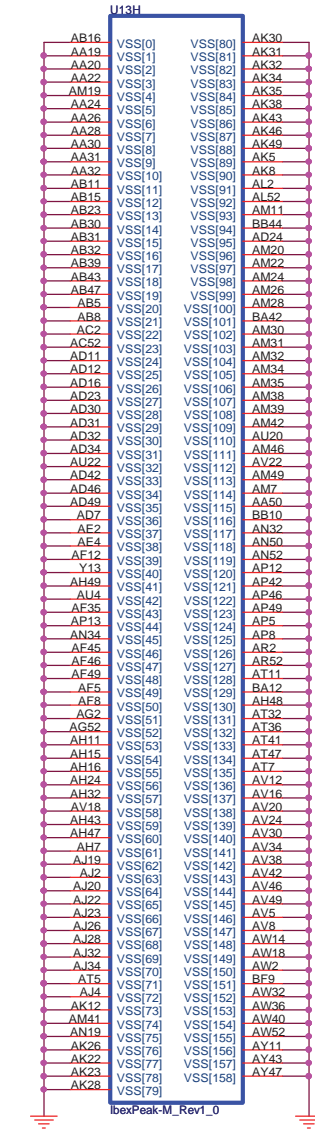
- BH2 10K 4
- BH52 10K 4
- BH53 10K 4
- BH1 10K 4
- B12 10K 4
- B14 10K 4
- B19 10K 4
- B2 10K 4
- B4 10K 4
- B52 10K 4
- B53 10K 4
- BE1 10K 4
- BE53 10K 4
- BE1 10K 4
- BE53 10K 4
- E1 10K 4
- E53 10K 4

- R279 10K 4
- R277 10K 4
- R275 10K 4
- R188 10K 4
- R186 10K 4
- R296 10K 4
- R195 10K 4
- R243 10K 4
- R244 10K 4
- R196 10K 4
- R282 10K 4
- R287 10K 4
- R207 10K 4

- R202 10K 4
- R219 10K_4_NC
- R190 10K 4
- R253 10K 4
- R254 10K 4
- R209 10K 4



Wwan_Radio_Dis# 1-X High = Strong (Default)



EMBUSY#: (Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

EMBUSY#: If not used, require a weak pull-up (8.2- 10k to 10k) to Vcc3.3. CRB (V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

Flash Descriptor Security Override

GPIO33	Low = Enabled High = Disabled
--------	----------------------------------

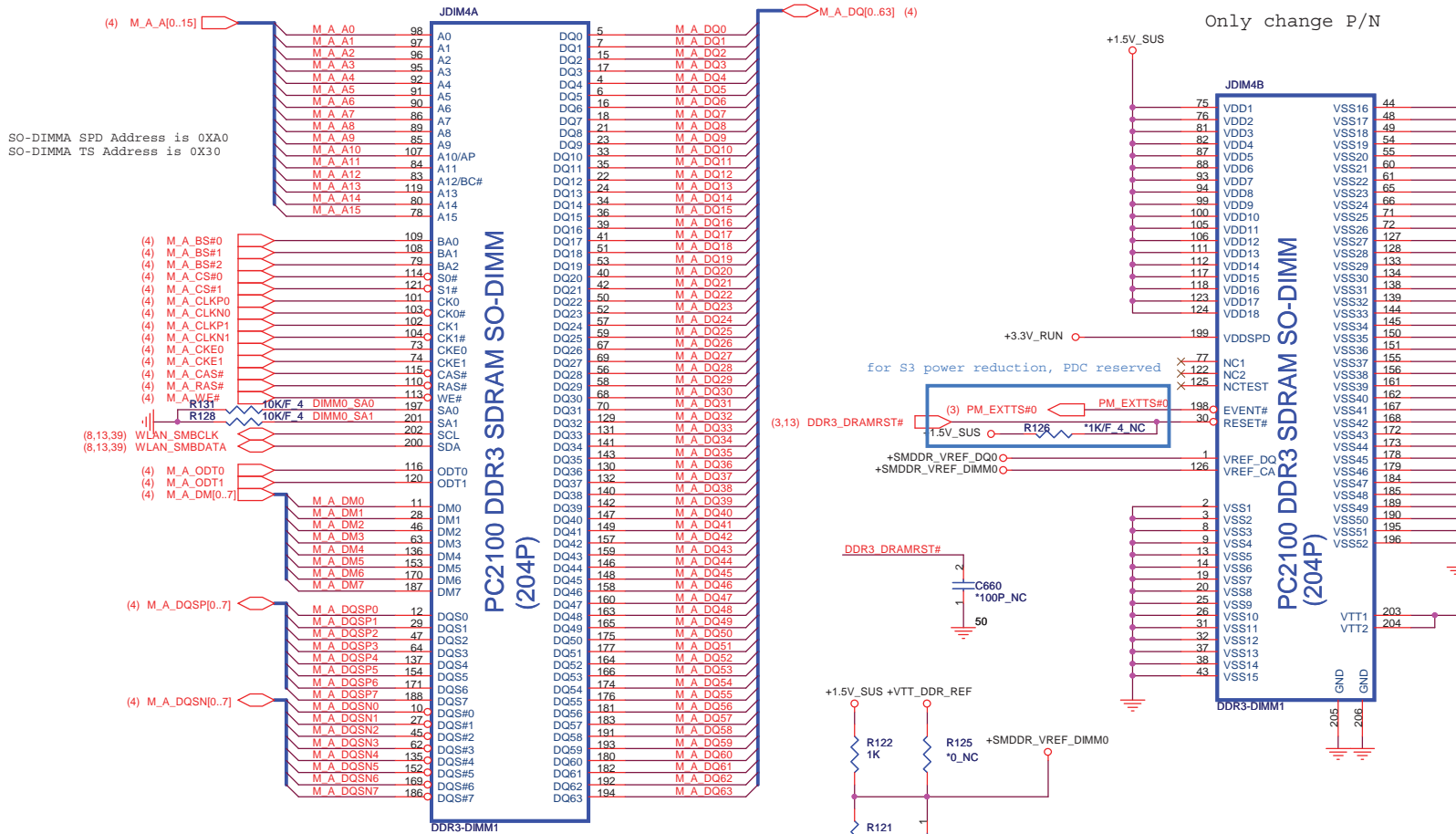
(7,29) PCH_MELOCK

(Internal 20K/F pull high to +3.3V_RUN)

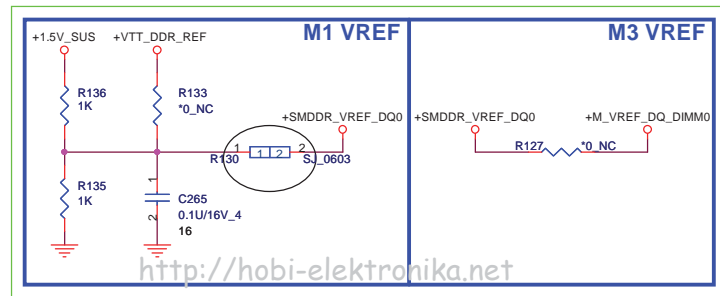
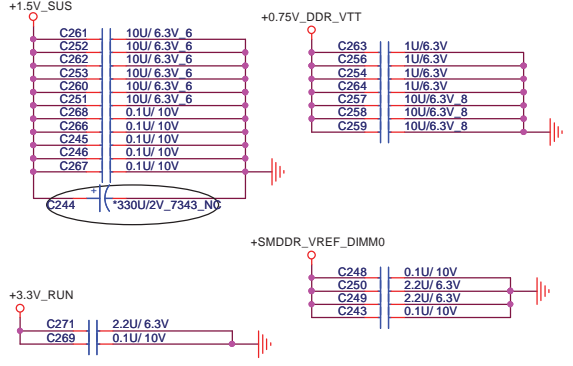
Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

Only change P/N

Only change P/N



Place these Caps near So-Dimm0.
 Some Projects replace 10UF 0805 by 4.7UF 0603
 It can cost down 30%



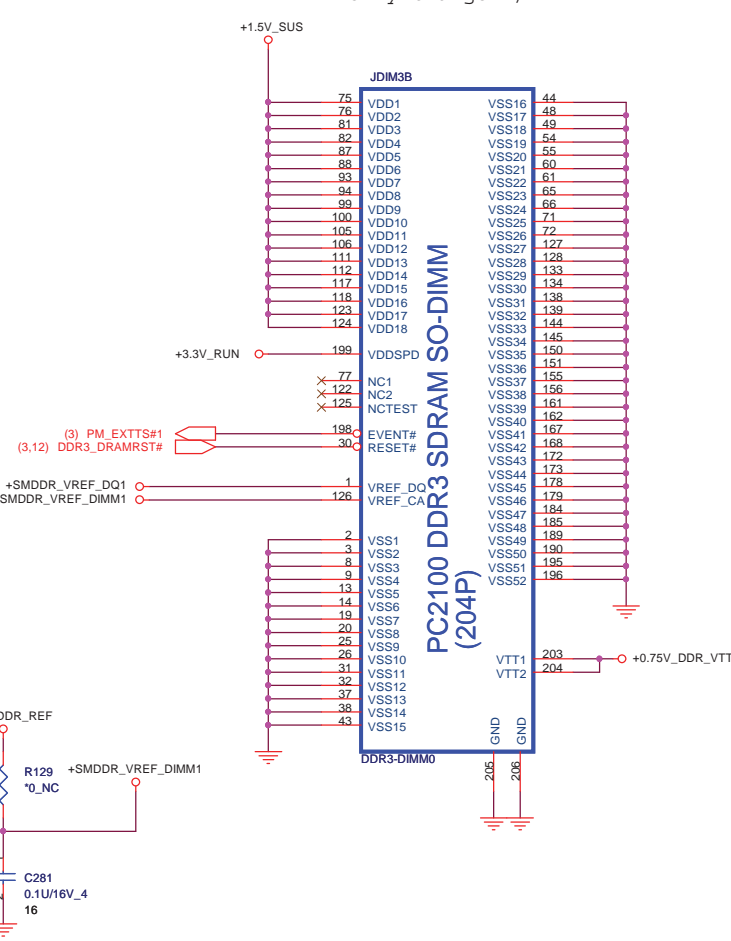
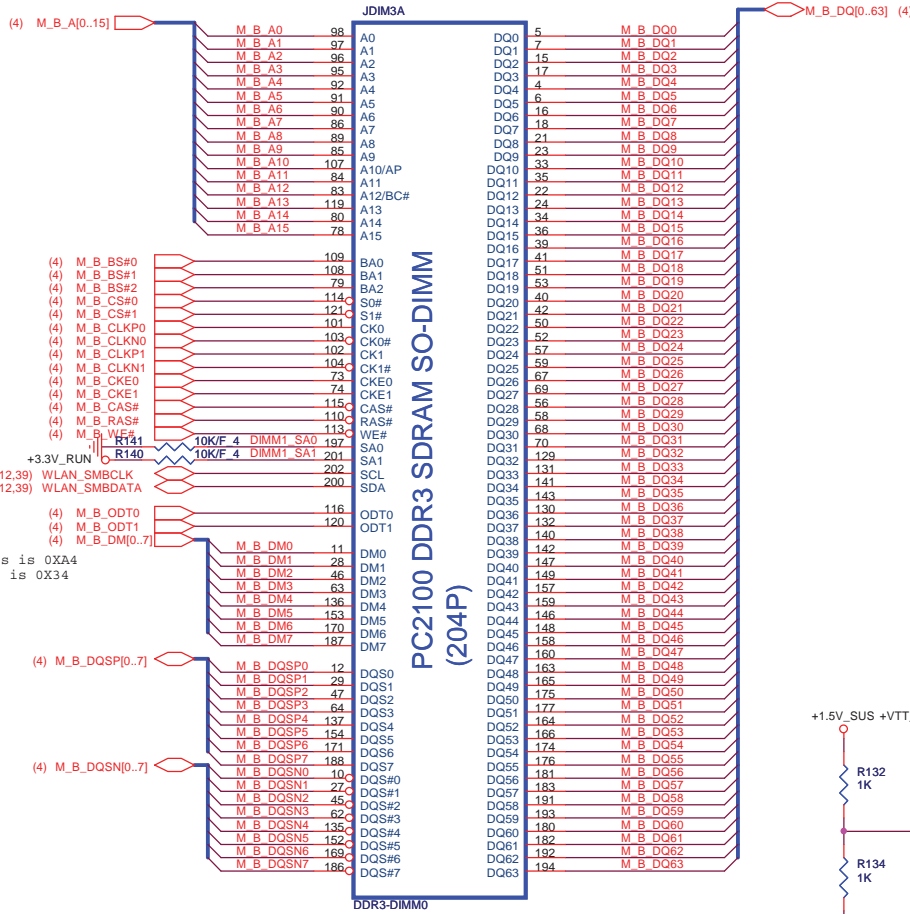
Quantities and M1/M3 follow UM3
 Locations follow PDC

Quanta Computer Inc.
 PROJECT : UM9B/C DIS

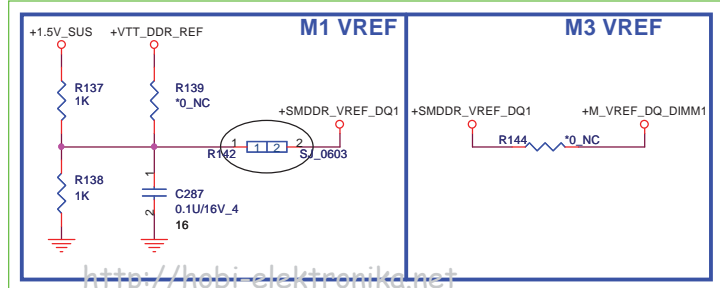
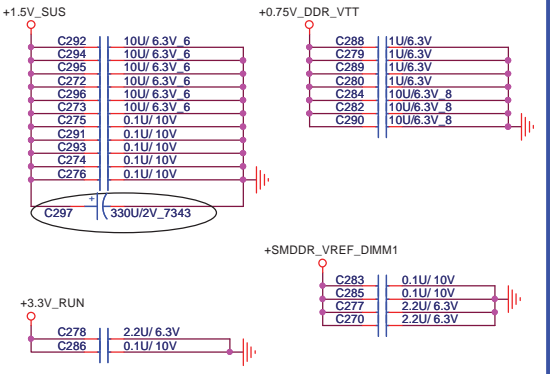
Size	Document Number	Rev
	DDR3 DIMM-0	3A
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Only change P/N

Only change P/N



Place these Caps near So-Dimm1.
 Some Projects replace 10UF 0805 by 4.7UF 0603
 It can cost down 30%



Quantities and M1/M3 follow UM3
 Locations follow PDC

Quanta Computer Inc.
 PROJECT : UM9B/C DIS

Size	Document Number	Rev
	DDR3 DIMM-1	3A
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U19A

PCI EXPRESS INTERFACE

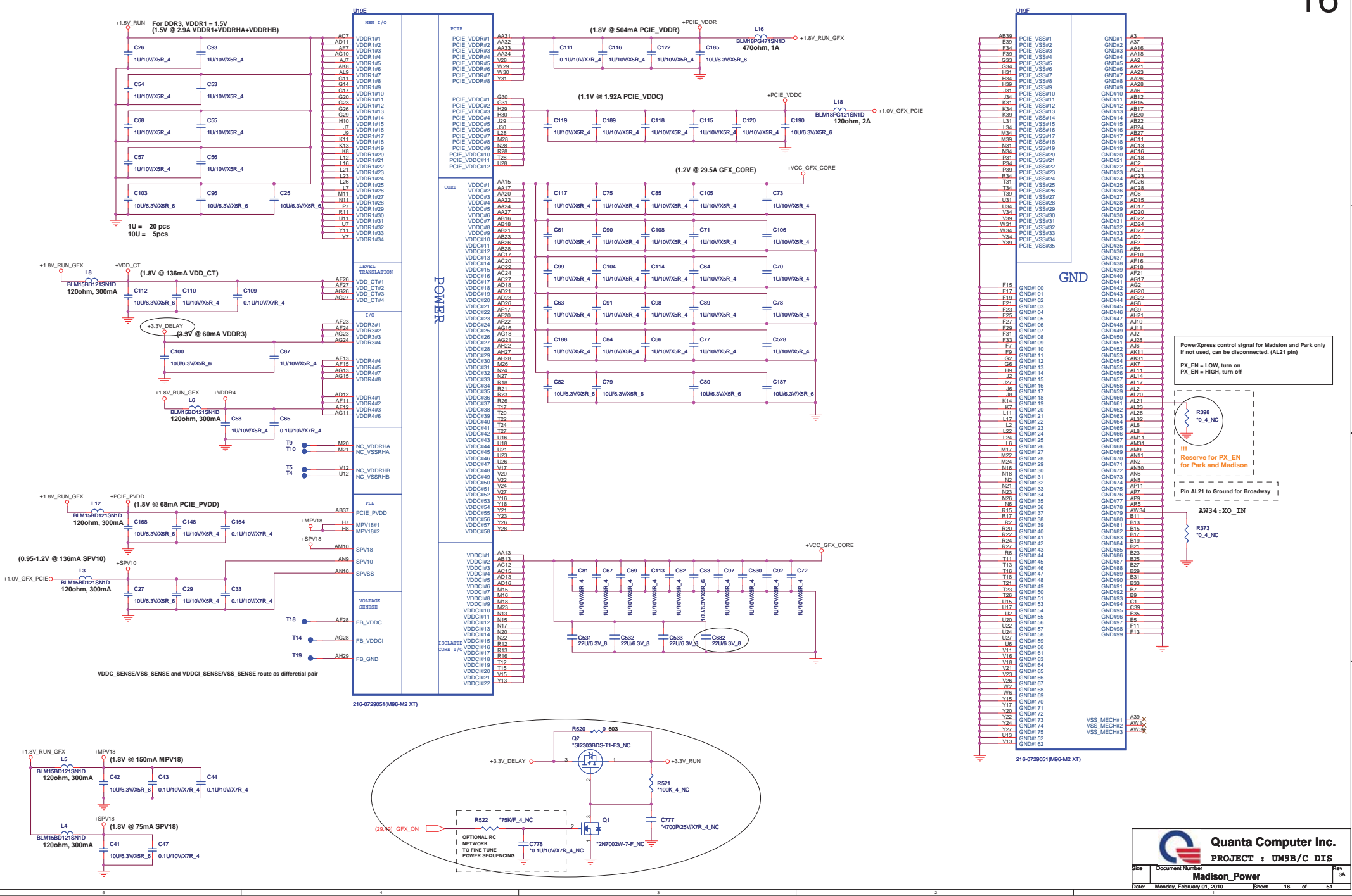


216-0729051(M96-M2 XT)

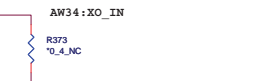
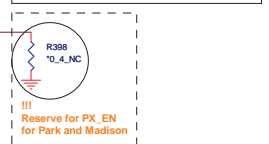
Quanta Computer Inc.
PROJECT : UM9B/C DIS

Size Document Number Rev 3A
Madison PCIE I/F

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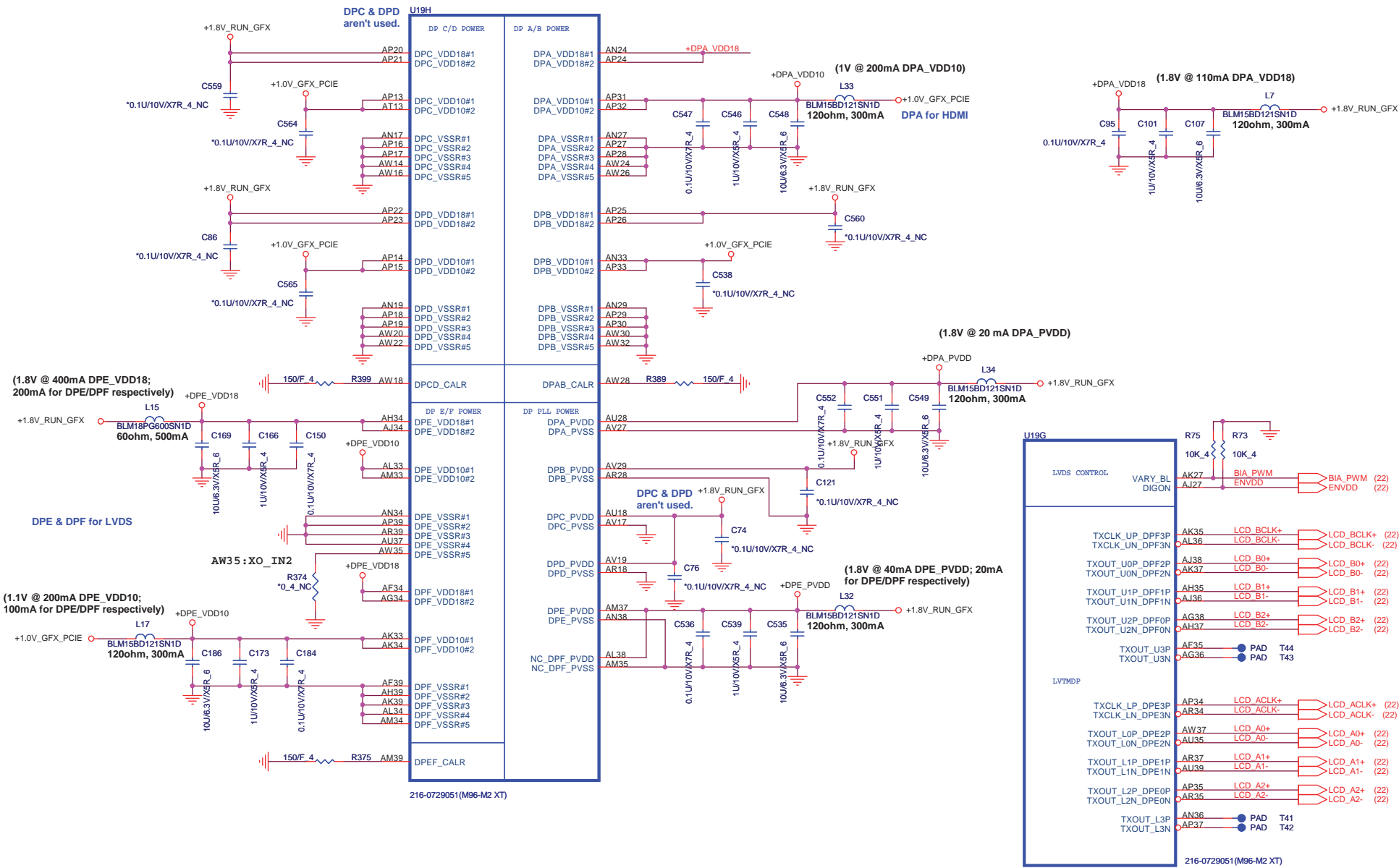
PowerXpress control signal for Madison and Park only
 If not used, can be disconnected. (AL21 pin)
 PX_EN = LOW, turn on
 PX_EN = HIGH, turn off

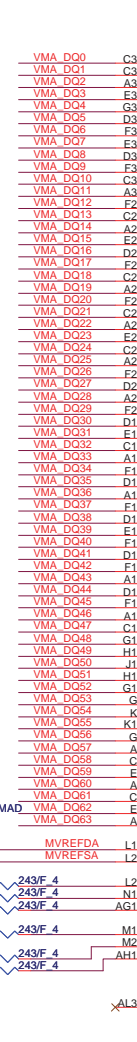
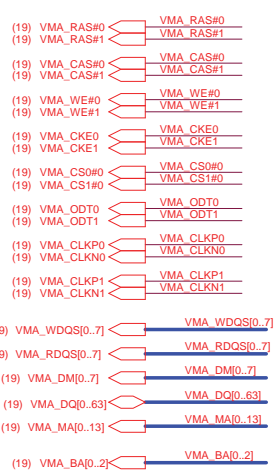


Quanta Computer Inc.
PROJECT : UM9B/C DIS

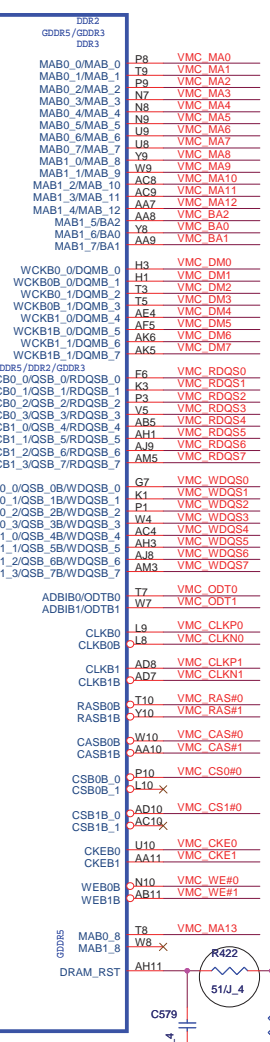
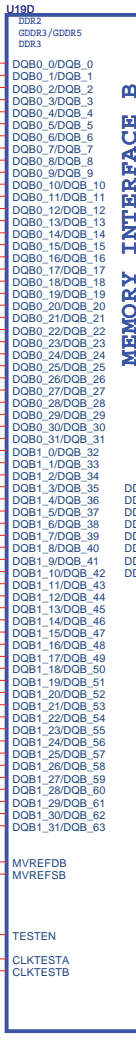
Size: Document Number: Rev: 3A
 Date: Monday, February 01, 2010 Sheet: 16 of 51

!!!
 For M96/92, DPx_VDD10 = 1.1V
 For M97 DPx_VDD10 = 1.0V

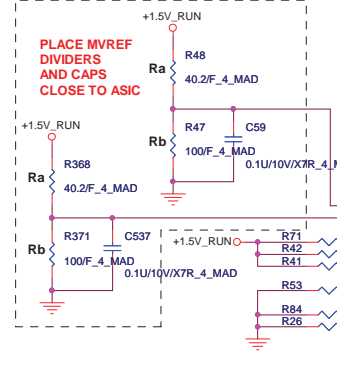




MEMORY INTERFACE A

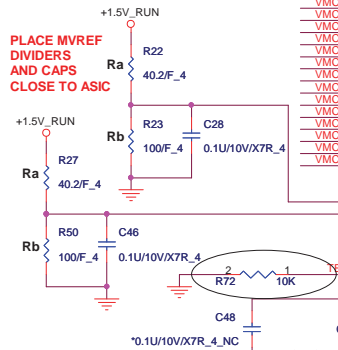
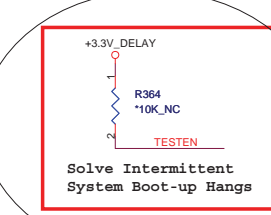


MEMORY INTERFACE B



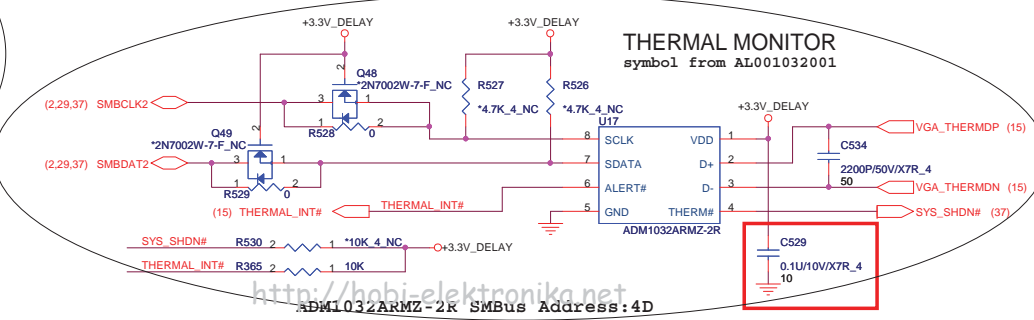
Solve Intermittent System Boot-up Hangs

VGA	ENG	MP
R386	V	
R390	V	
R363	V	
R364	V	
R72		V

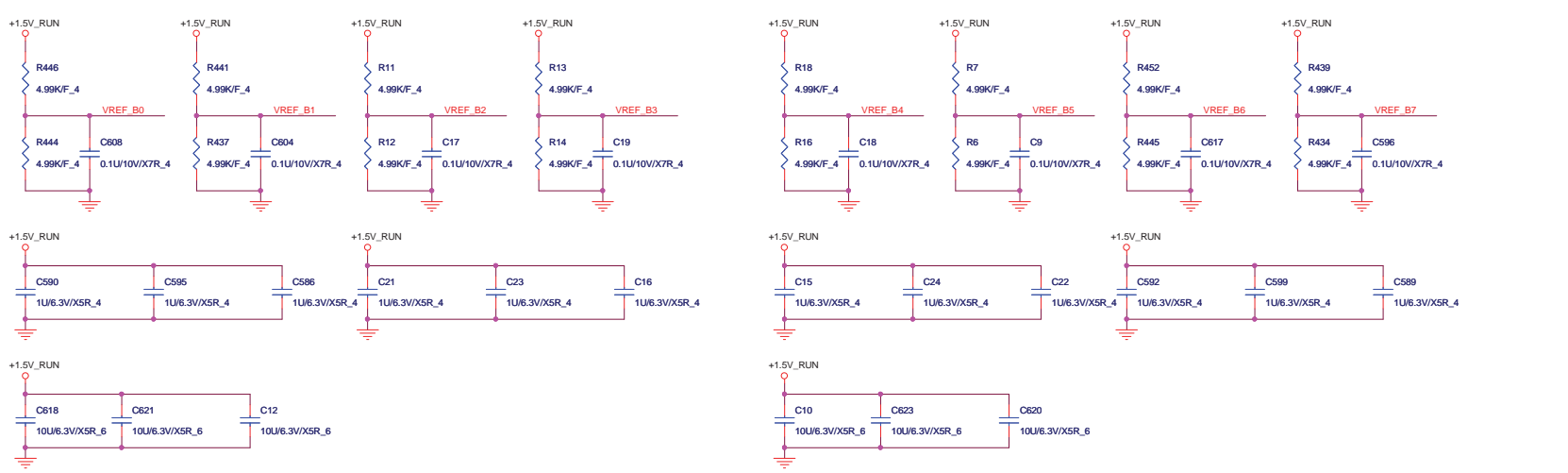
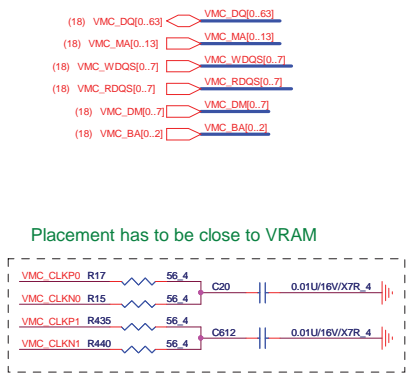
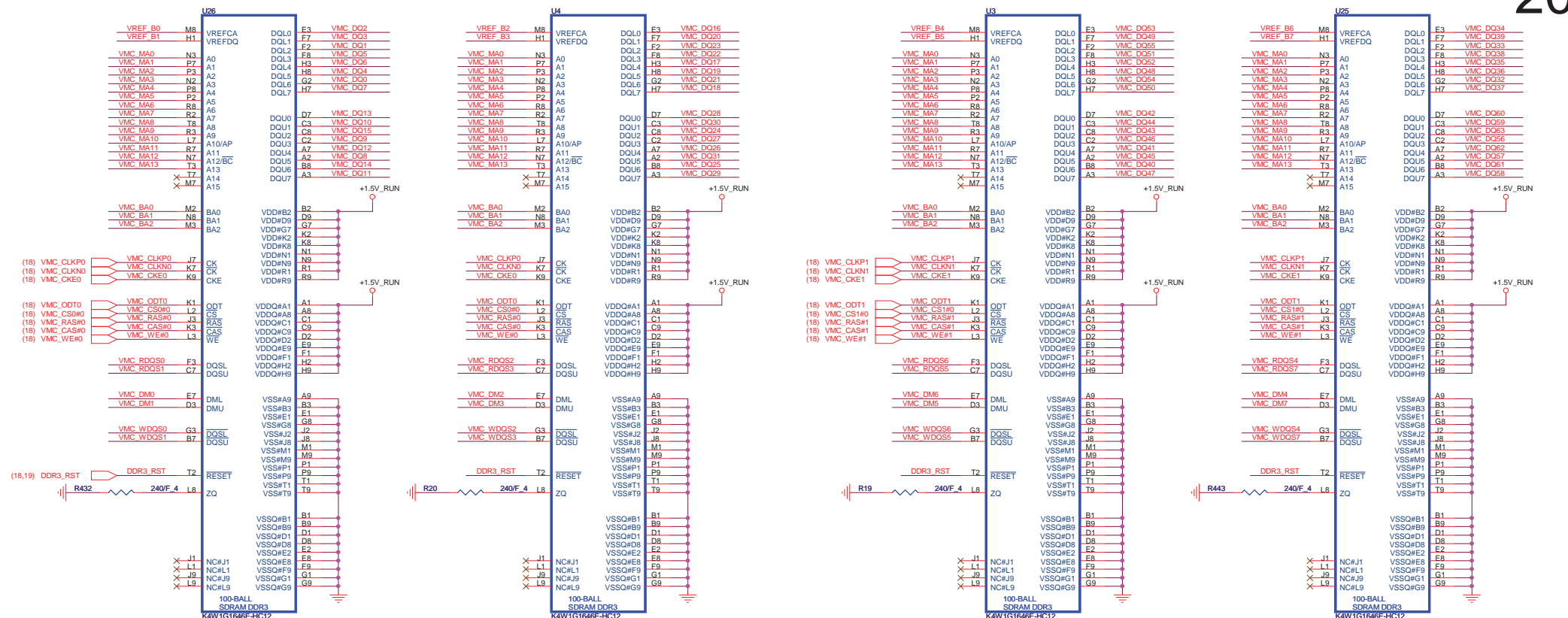


DDR3/GDDR3 Memory Stuff Option

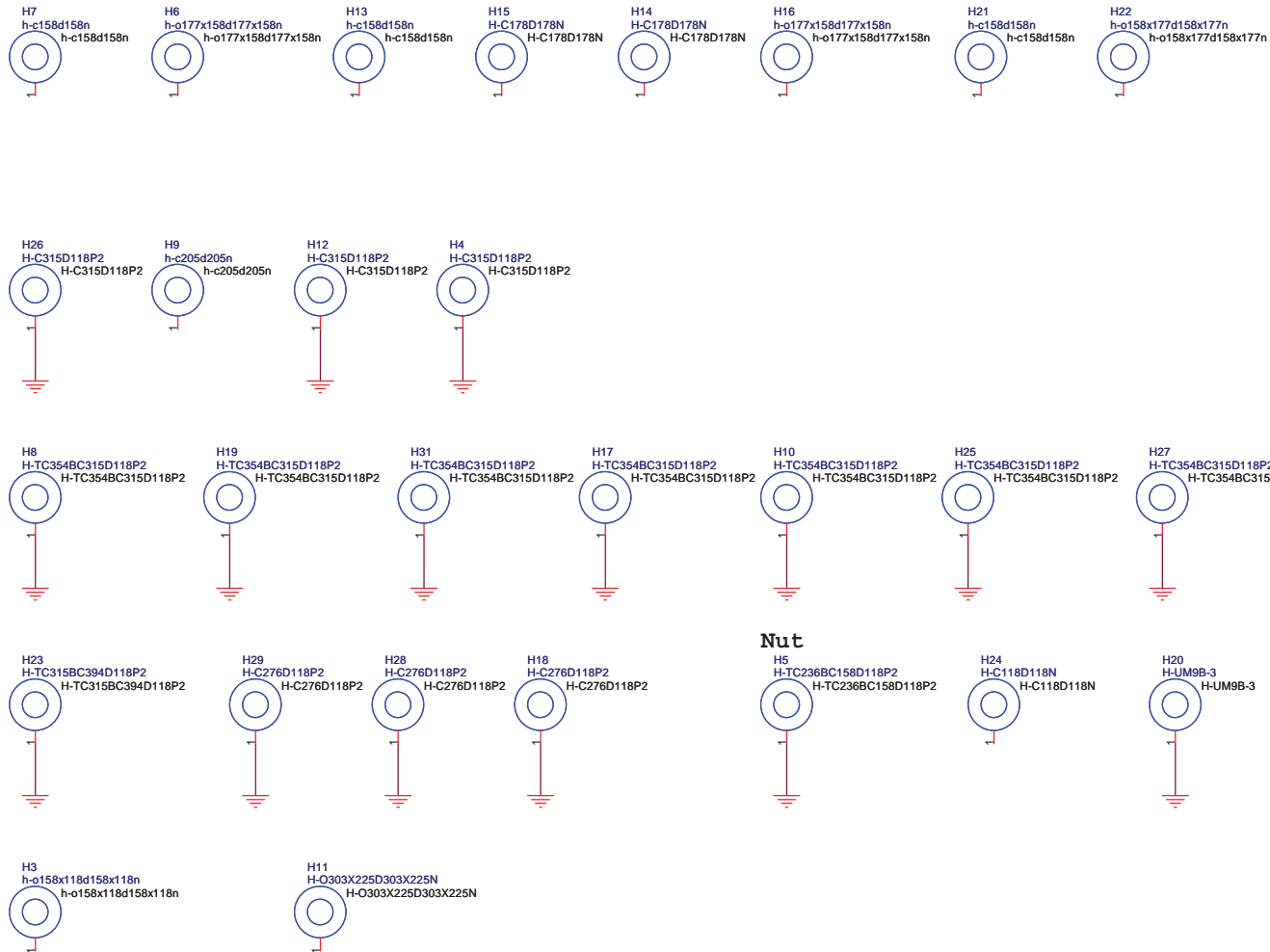
MVDDQ	GDDR3	DDR3
	1.5V/1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

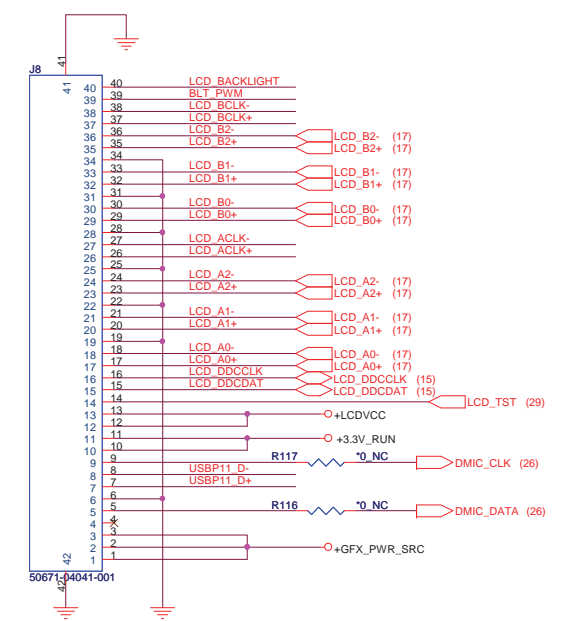
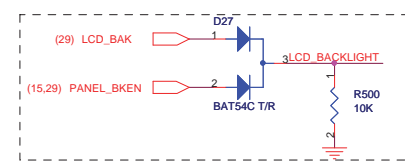
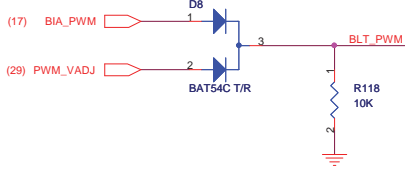
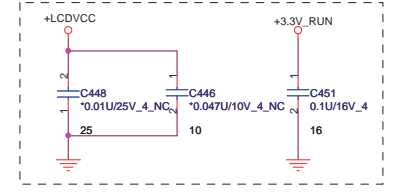
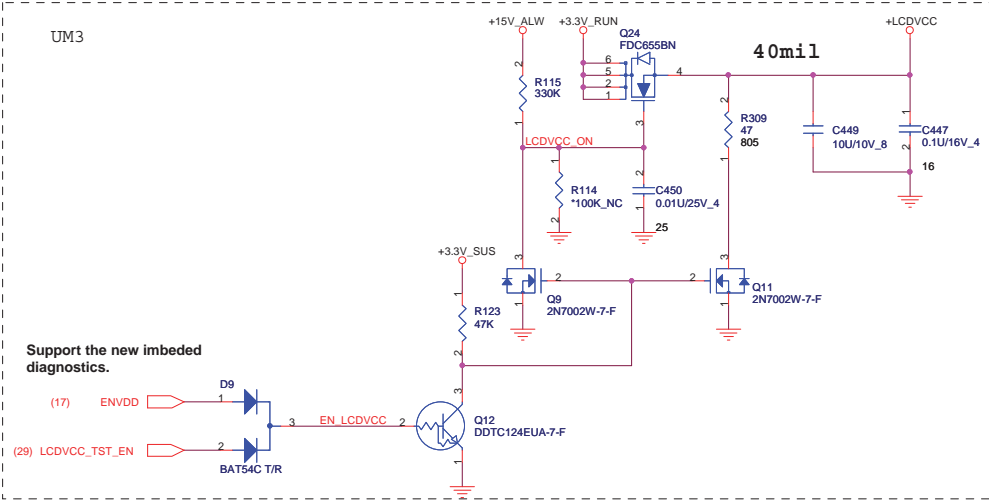


Quanta Computer Inc.
PROJECT : UM9B/C DIS
Madison MEMORY/THERM
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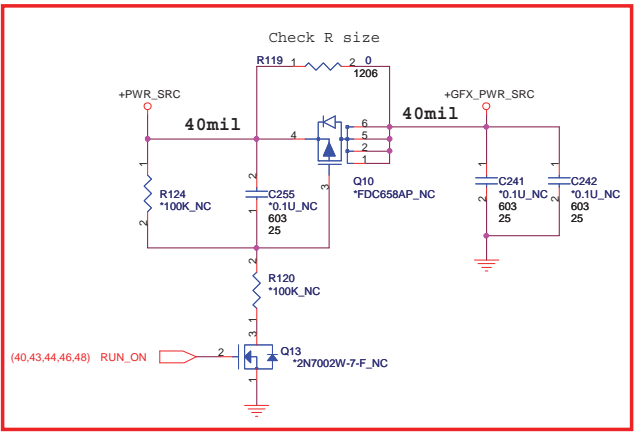


Follow 9/9 mail, check GND.



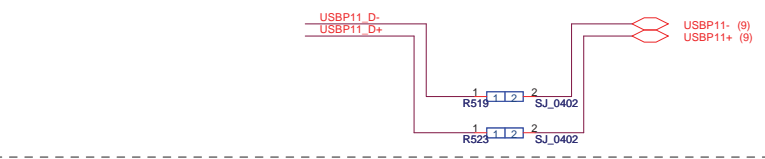
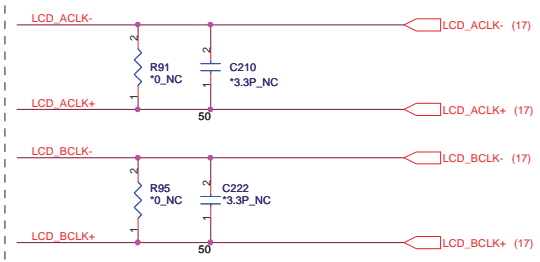


Support the new imbedded diagnostics.

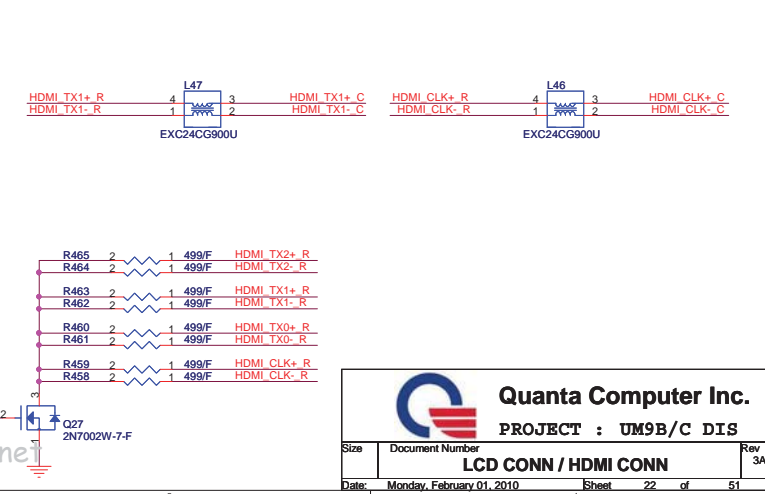
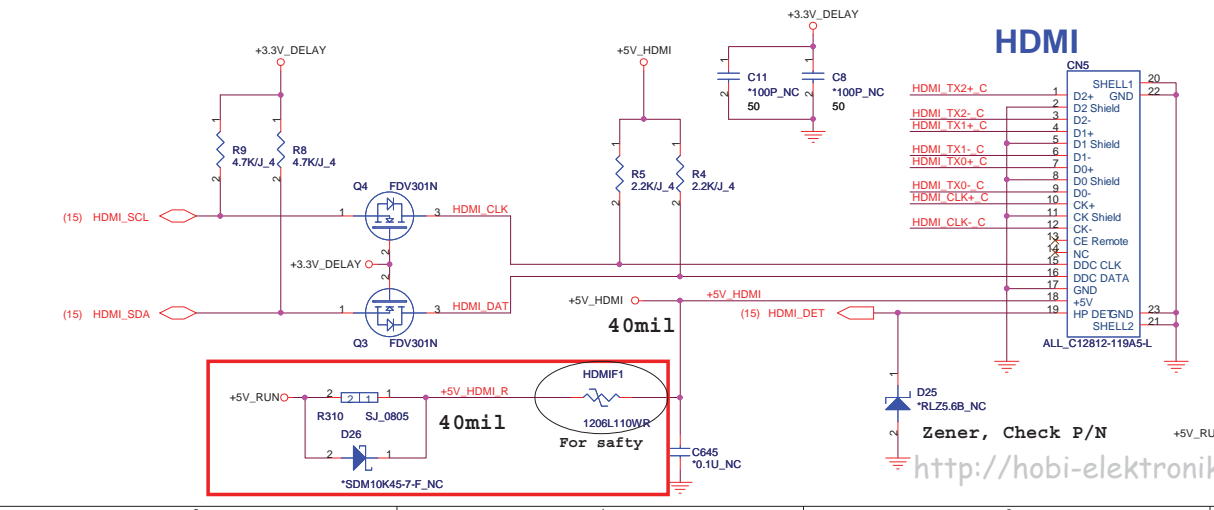
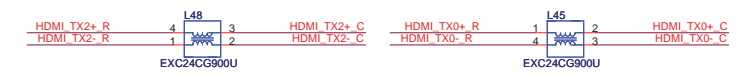


Shunt capacitors on LVDS for improving WWAN.

LCD B0-	C224	1	2	*3.3P	NC	50	LCD B0+
LCD B1-	C223	1	2	*3.3P	NC	50	LCD B1+
LCD B2-	C211	1	2	*3.3P	NC	50	LCD B2+
LCD A0-	C220	1	2	*3.3P	NC	50	LCD A0+
LCD A1-	C209	1	2	*3.3P	NC	50	LCD A1+
LCD A2-	C221	1	2	*3.3P	NC	50	LCD A2+



(15) HDMI_TX2+ R	C633	0.1u/10V_X7R	4	HDMI TX2+ R
(15) HDMI_TX2- R	C632	0.1u/10V_X7R	4	HDMI TX2- R
(15) HDMI_TX1+ R	C631	0.1u/10V_X7R	4	HDMI TX1+ R
(15) HDMI_TX1- R	C630	0.1u/10V_X7R	4	HDMI TX1- R
(15) HDMI_TX0+ R	C628	0.1u/10V_X7R	4	HDMI TX0+ R
(15) HDMI_TX0- R	C629	0.1u/10V_X7R	4	HDMI TX0- R
(15) HDMI_CLK+ R	C625	0.1u/10V_X7R	4	HDMI CLK+ R
(15) HDMI_CLK- R	C624	0.1u/10V_X7R	4	HDMI CLK- R




Quanta Computer Inc.
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LCD CONN / HDMI CONN
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UM3


This page to CRT board

<http://hobi-elektronika.net>

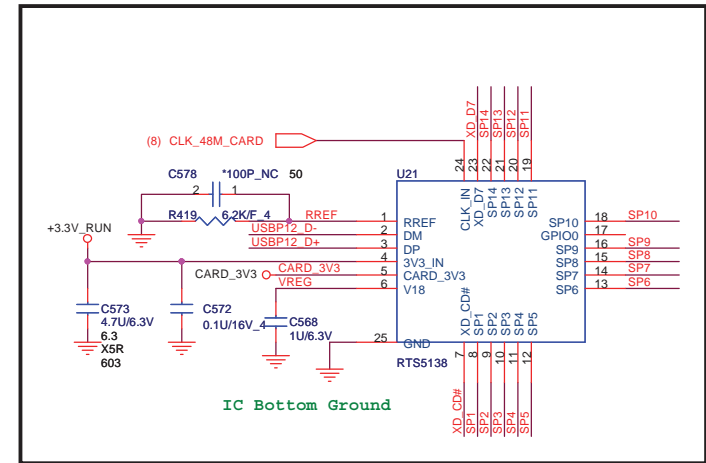
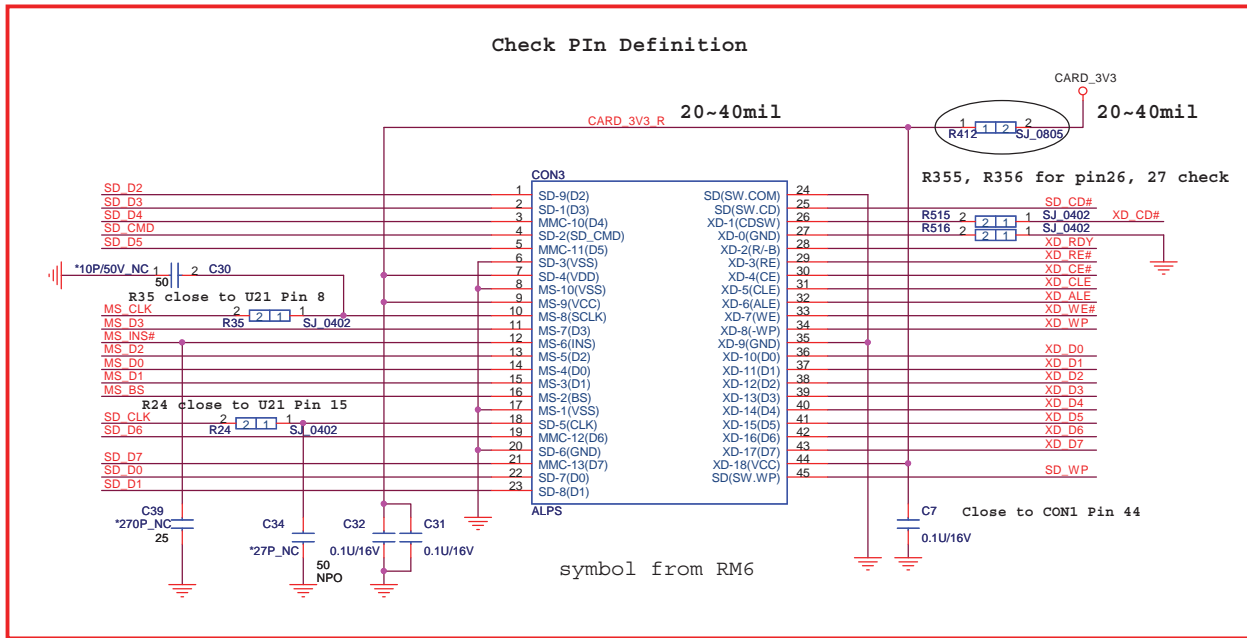
		Quanta Computer Inc.
		PROJECT : UM9B/C DIS
Size	Document Number	Rev
	CRT CONN	3A
Date:	Wednesday, January 27, 2010	Sheet 23 of 51

To CRT BOARD

<http://hobi-elektronika.net>

		Quanta Computer Inc.
		PROJECT : UM9B/C DIS
Size	Document Number	Rev
	DB CONN/Left USB	3A
Date:	Wednesday, January 27, 2010	Sheet 24 of 51

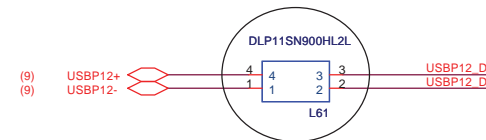
Check PIn Definition

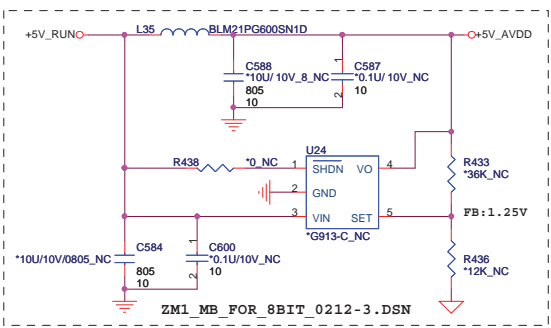


RTS5138 - QFN24

SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#	SD D1	MS INS#
SP3	XD CE#	SD D0	MS D3
SP4	XD CLE	SD D7	MS D7
SP5	XD ALE	SD D7	MS D3
SP6	XD WE#	SD CD#	
SP7	XD WP	SD D6	MS D6
SP8	XD D0	SD CLK	MS D2
SP9	XD D1	SD D5	MS D0
SP10	XD D2	SD CMD	
SP11	XD D3	SD D4	MS D4
SP12	XD D4	SD D3	MS D1
SP13	XD D5	SD D2	MS D5
SP14	XD D6	MS BS	

Share Pin





UM3, symbol from PDC

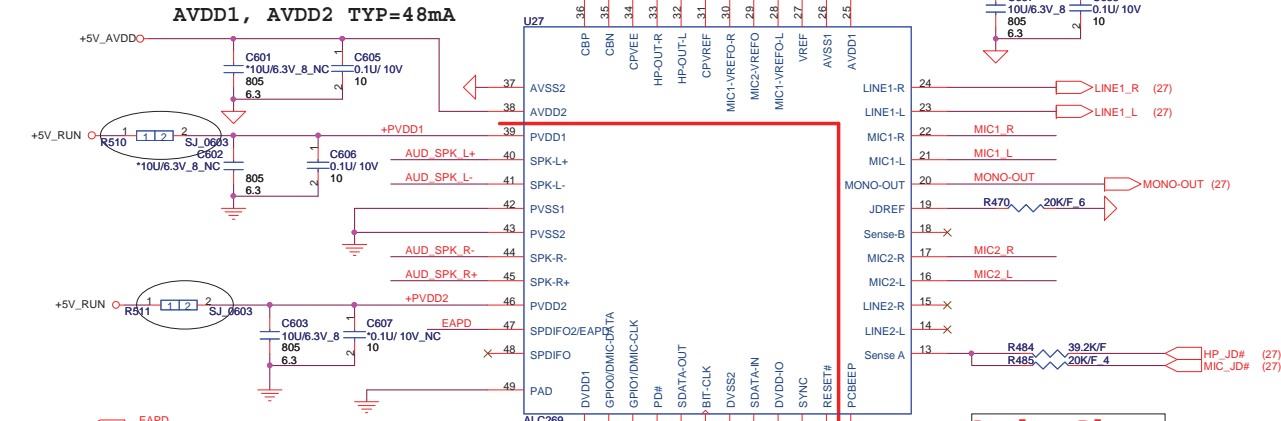
*NOTE: ALC269_VB type add the LDO circuit in IC

PIN NAME	R457	R455	R456	C636	CODEC IC
28 MIC1_VREF0-L			POP	NC	ALC269
31 CPVREF	POP	NC			VA

VA type: PIN28 作為MIC之偏壓
PIN31接A-GND

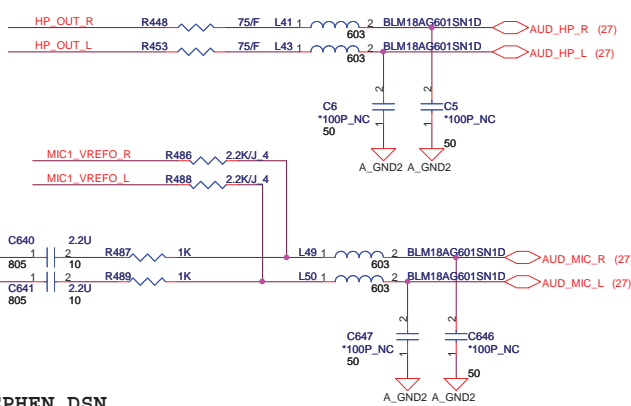
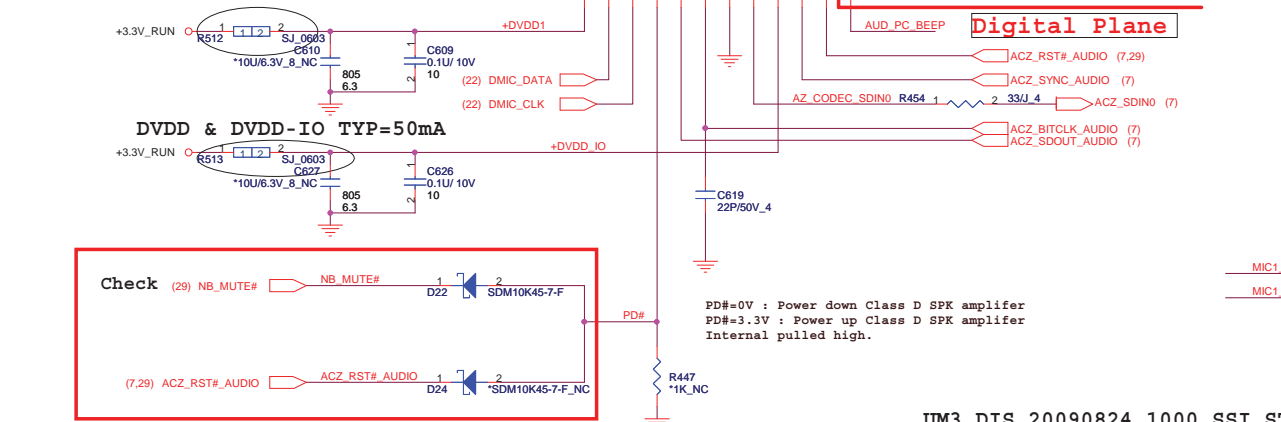
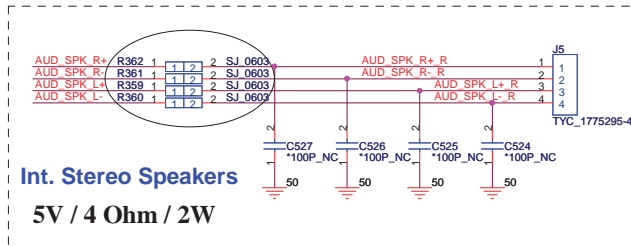
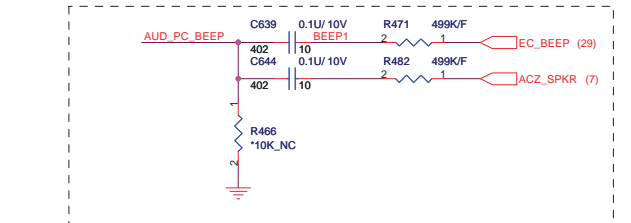
PIN NAME	R457	R455	R456	C636	CODEC IC
28 MIC1_VREF0-L			NC	POP	ALC269
31 CPVREF	NC	POP			VB

VB type: PIN31 作為MIC之偏壓
PIN28接CAP作為內部LDO
output 輸出濾波用

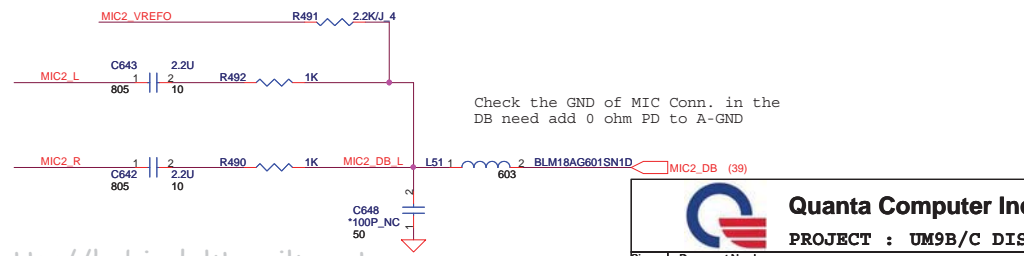
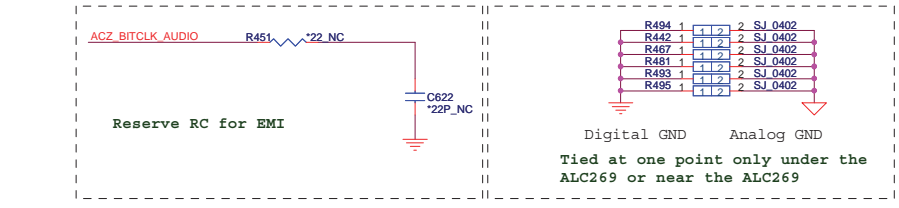


Analog Plane

Digital Plane



UM3_DIS_20090824_1000_SSI_STEPHEN.DSN



Check the GND of MIC Conn. in the DB need add 0 ohm PD to A-GND

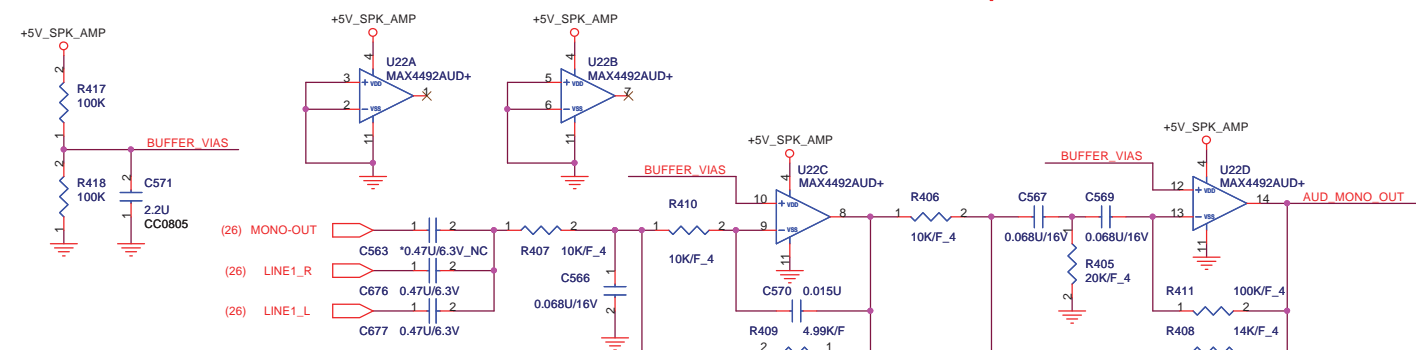
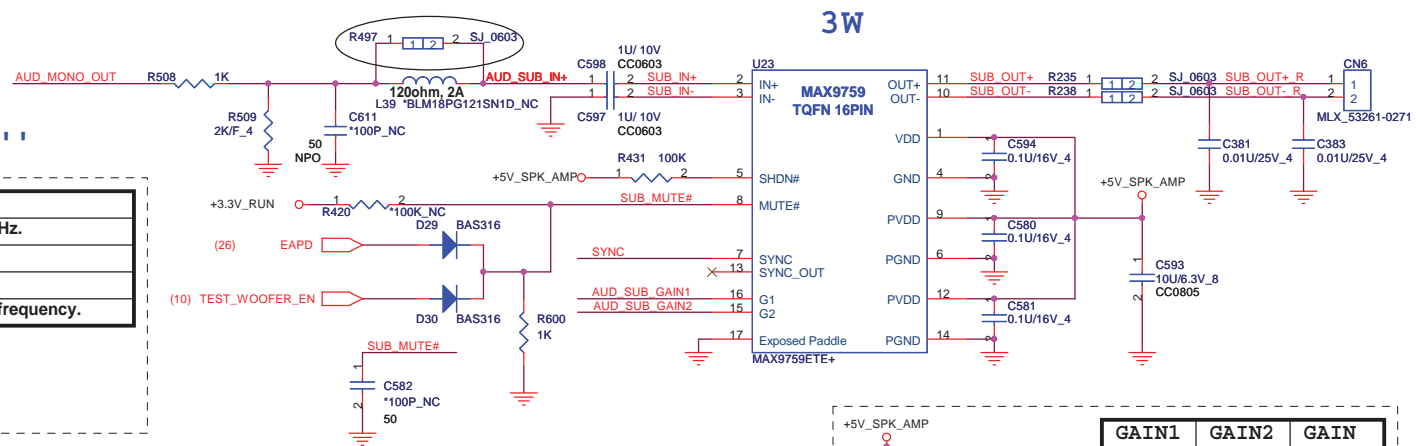
<http://hobi-elektronika.net>

Quanta Computer Inc.
PROJECT : UM9B/C DIS

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	Azelia CODEC(ALC269)	3A
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INTERNAL SUBWOOFER AMP Only for 17''

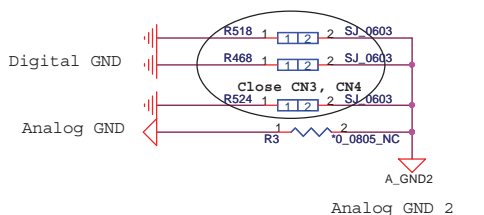
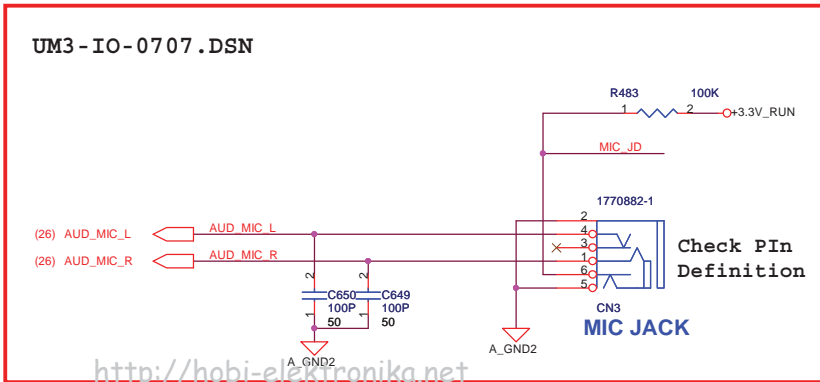
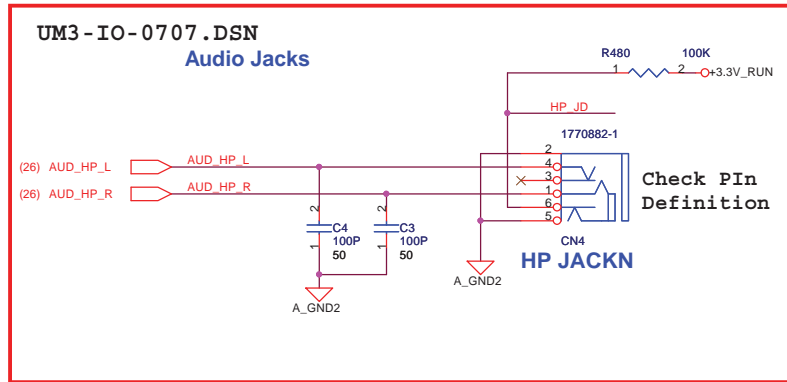
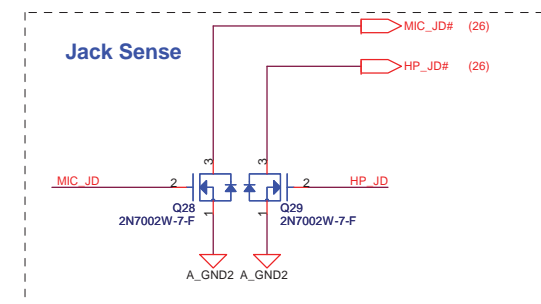
SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.



GAIN1	GAIN2	GAIN
0	0	24dB
1	0	18dB
0	1	12dB
1	1	6dB


FB_60ohm+-25%_100MHz
_3A_0.05ohm DC
 Layout Note:
 Place close to pin 8.

NB_MUTE#	TEST_WOOFER_EN	AUD_SPK_PD#	SUB_MUTE#
0	0	L (Disable SPK)	L (Disable Woofer)
0	1	L (Disable SPK)	H (Test Woofer)
1	0	H (Test SPK)	L (Disable Woofer)
1	1	H (Test SPK)	H (Test Woofer)





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		Quanta Computer Inc.
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(34) KSO[0..17]
(34) KSI[0..7]

ITE8502E LQFP-128L

- KSO17 57 KSO17/GPC5
- KSO16 56 KSO16/GPC3
- KSO15 55 KSO15
- KSO14 54 KSO14
- KSO13 53 KSO13
- KSO12 52 KSO12/SLCT
- KSO11 51 KSO11/ERR
- KSO10 49 KSO10/PE
- KSO9 48 KSO9/BUSY
- KSO8 44 KSO8/ACK
- KSO7 43 KSO7/PD7
- KSO6 42 KSO6/PD6
- KSO5 41 KSO5/PD5
- KSO4 40 KSO4/PD4
- KSO3 39 KSO3/PD3
- KSO2 38 KSO2/PD2
- KSO1 37 KSO1/PD1
- KSO0 36 KSO0/PD0
- KS17 65 KS17
- KS16 64 KS16
- KS15 63 KS15
- KS14 62 KS14
- KS13 61 KS13/SLIN
- KS12 60 KS12/INT
- KS11 59 KS11/AFD
- KS10 58 KS10/STB

KEYBOARD

ADC/DAC

PWM

LPC

IR/UART

SMBUS

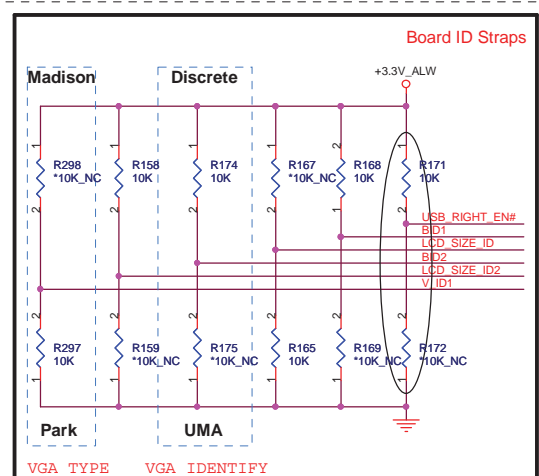
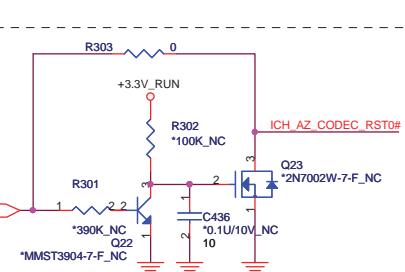
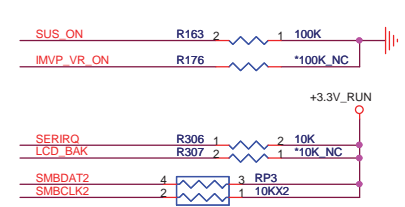
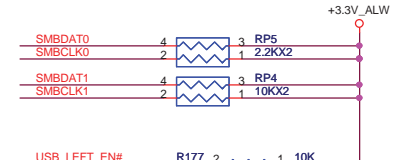
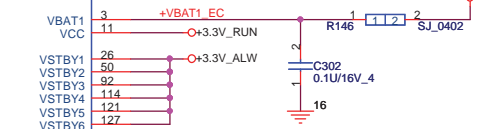
PS/2

GPIO

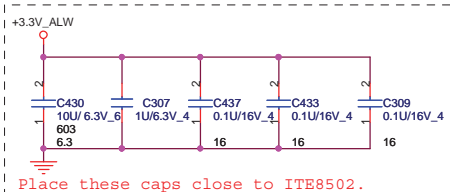
LPC/FWH FLASH

RGPC

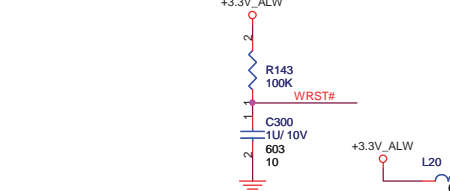
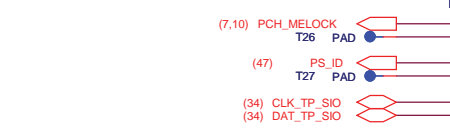
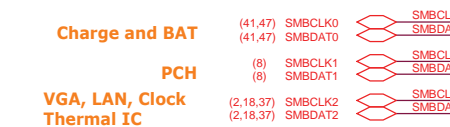
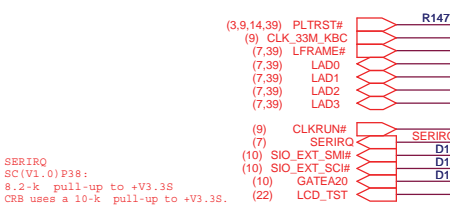
GPIO



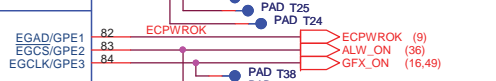
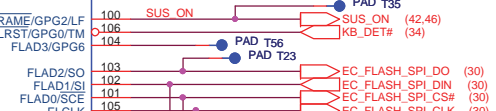
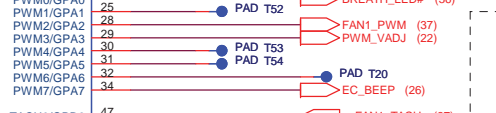
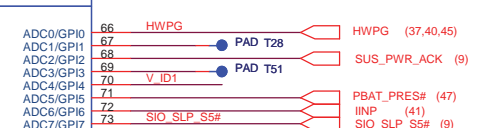
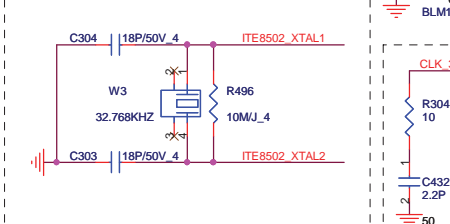
BID1	BID0	UM9(UMA)	UM9C(Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	QT (A00)	QT (A00)
0	0	(A01)	(A01)



Place these caps close to ITE8502.



32KHz Clock.(Layout close to EC)



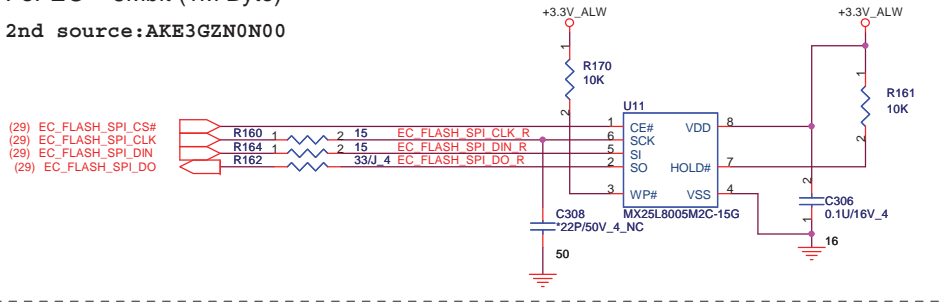
ITE8502E
lqfp128-16x16-4

Quanta Computer Inc.
PROJECT : UM9B/C DIS

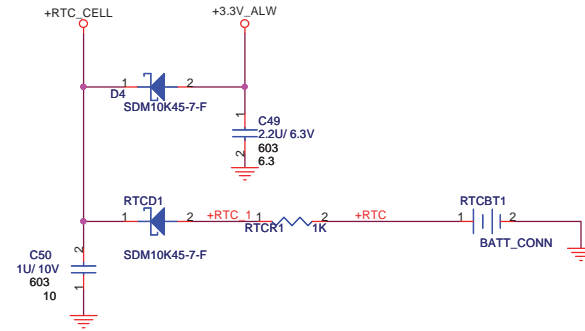
Size: Document Number: **SIO ITE8502** Rev: 3A
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For EC 8Mbit (1M Byte)

2nd source:AKE3GZN0N00



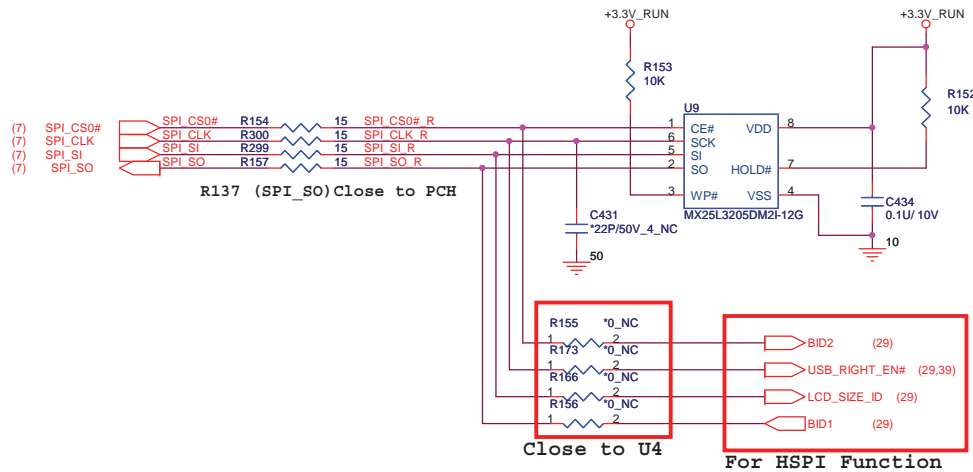
RTC BATTERY



For PCH

32Mbit (4M Byte)

2nd source:AKE39ZP0N00



UM3

WWAN To DB

<http://hobi-elektronika.net>

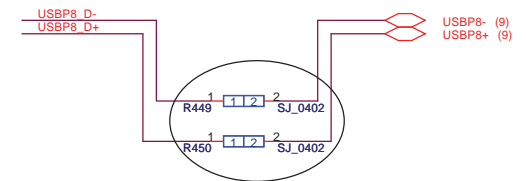
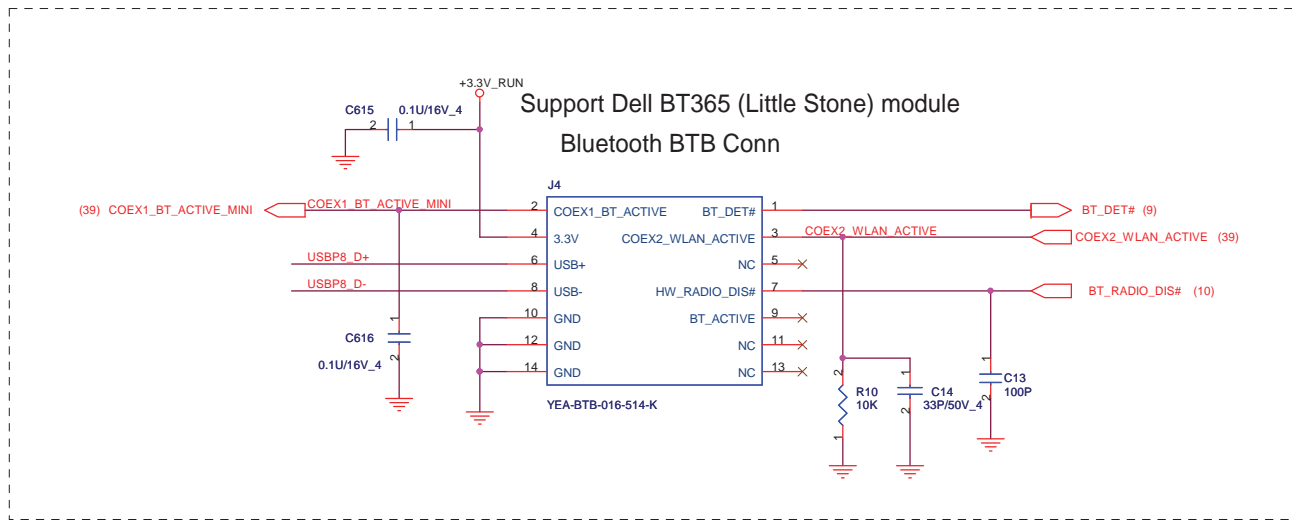


Quanta Computer Inc.

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	MINI-Card WWAN	3A
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WLAN To DB



eSATA and USB To DB

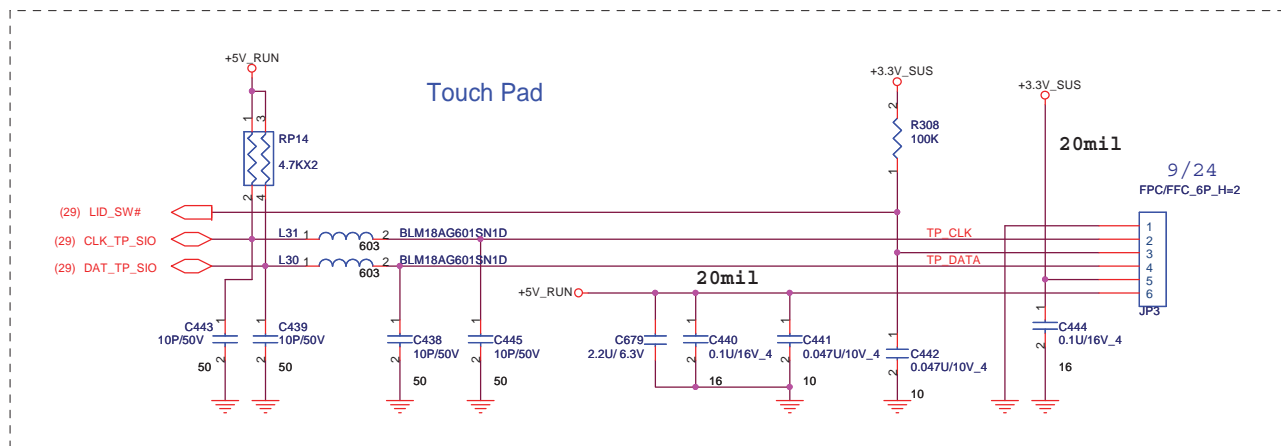
<http://hobi-elektronika.net>



Quanta Computer Inc.

PROJECT : UM9B/C DIS

Size	Document Number	Rev
	eSATA & Right USB	3A
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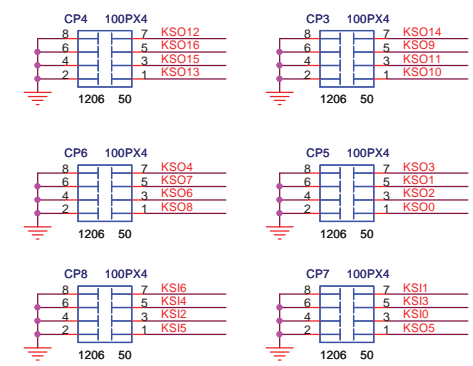
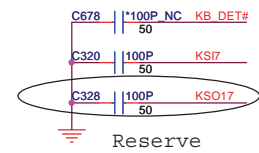
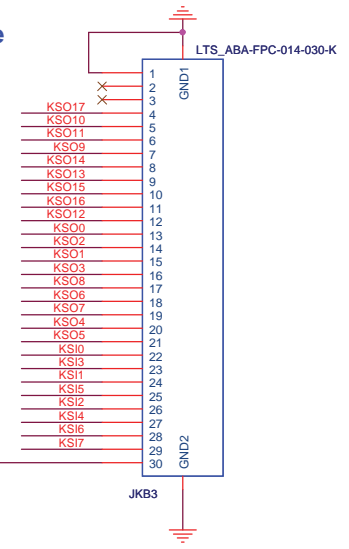


UM3 KEYBOARD CONNECTOR

Top side

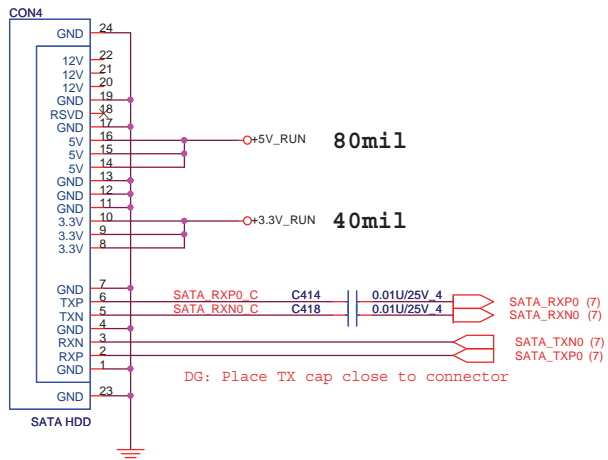
- (29) KSO[0..17]
- (29) KSI[0..7]

Check KB detect function
UM9 no KSO17

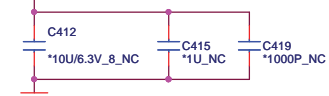


100P CAPS CLOSE TO JKB3

SATA Connector.



+3.3V_RUN Place caps close to connector.



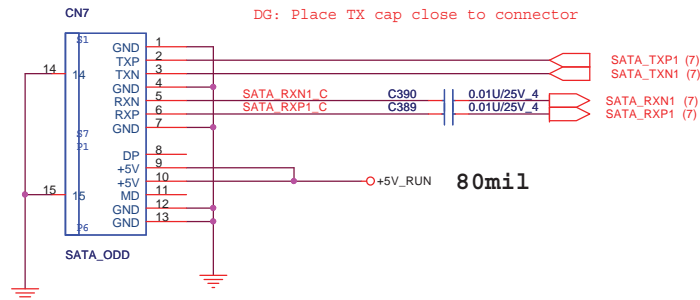
Place caps close to connector.

+5V_RUN

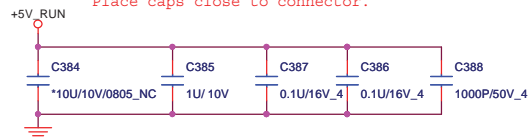


UM3

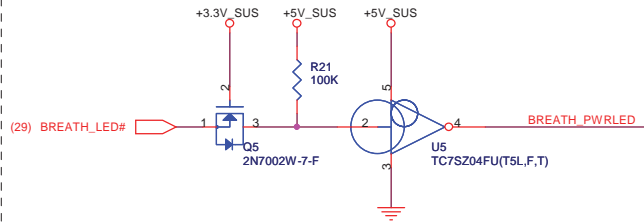
ODD Connector



Place caps close to connector.

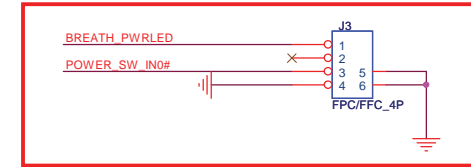


Power

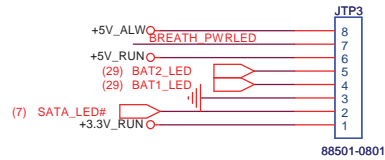


UM3

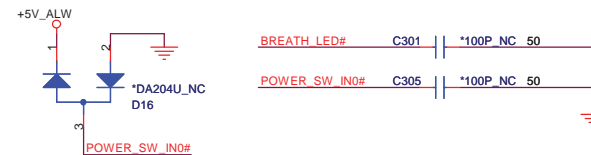
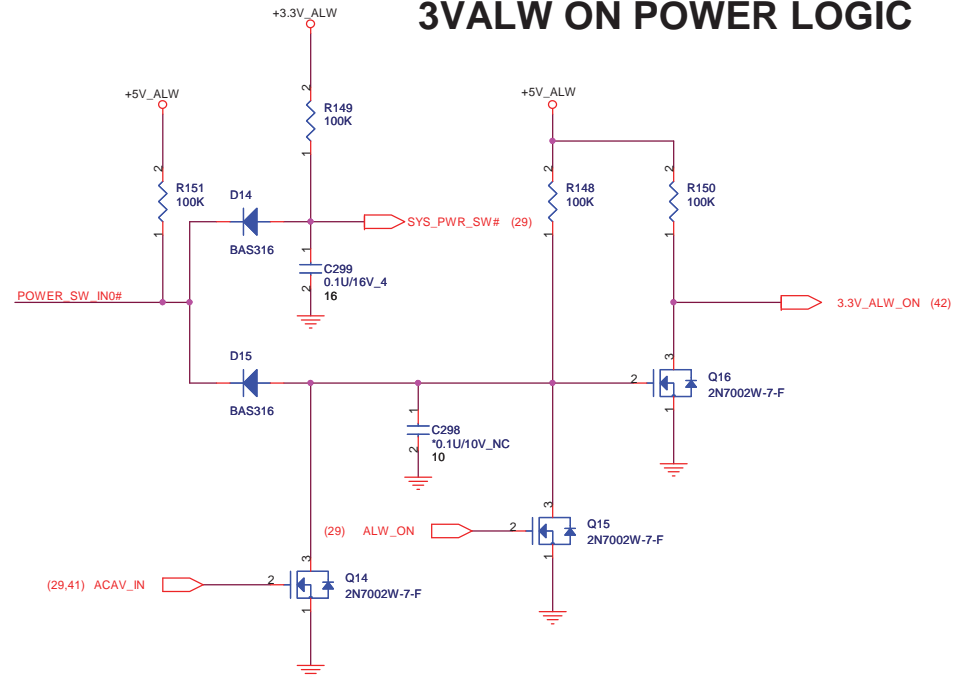
Power button Cable




Check Connector P/N and footprint

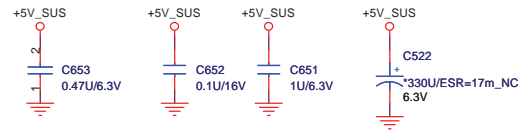
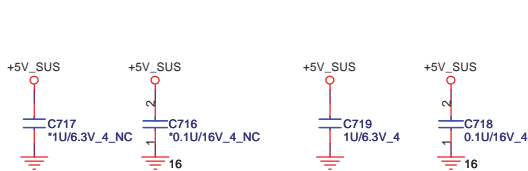
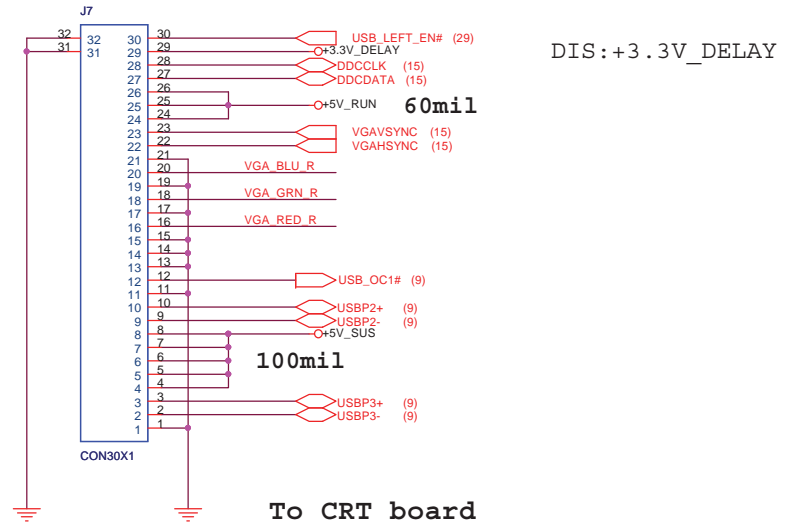
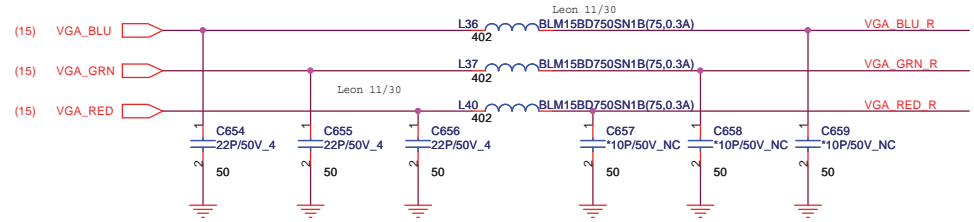
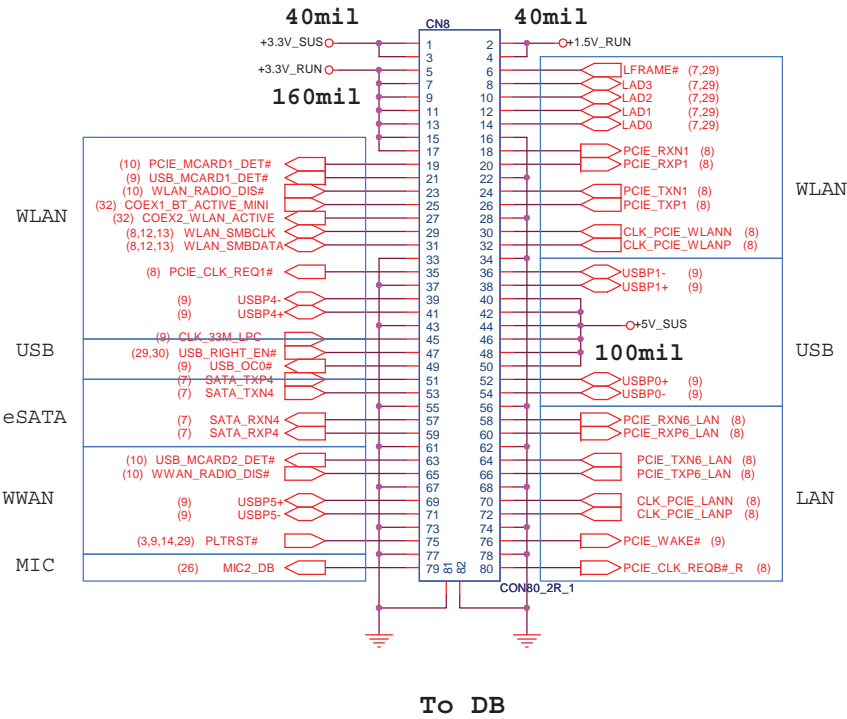


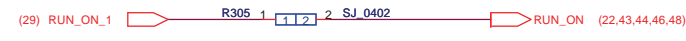
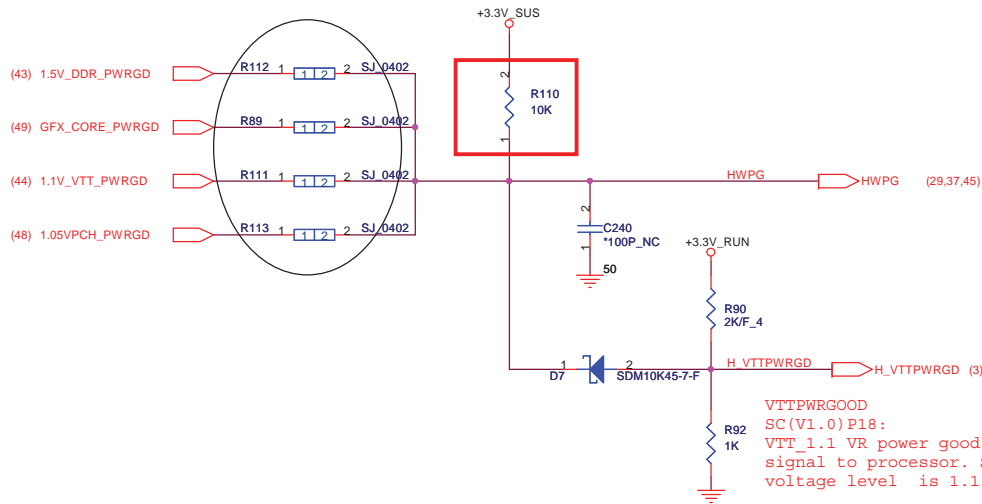
3VALW ON POWER LOGIC



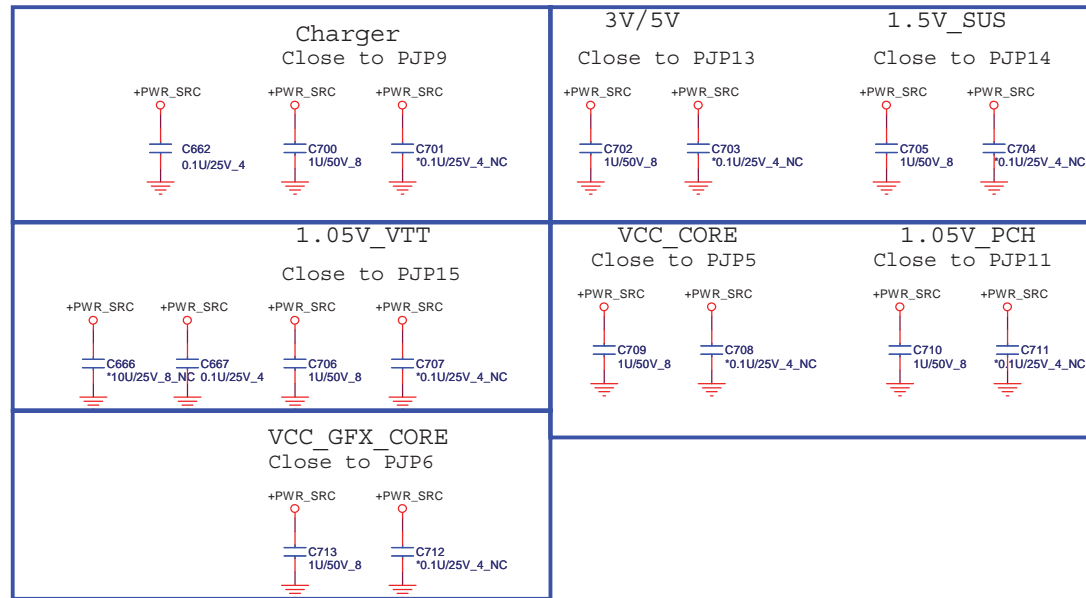
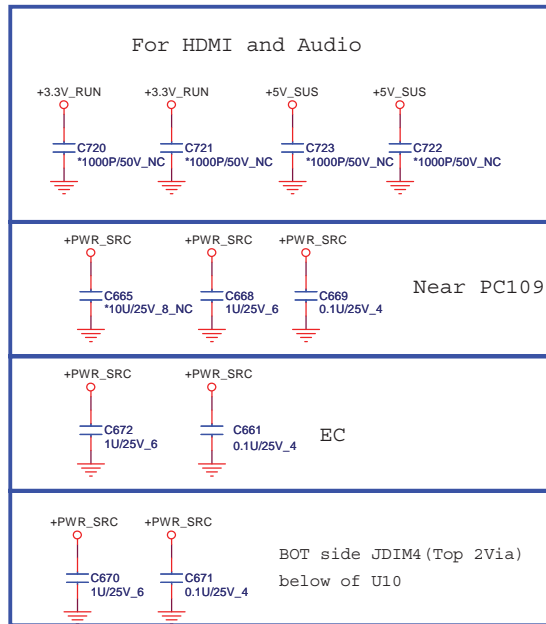
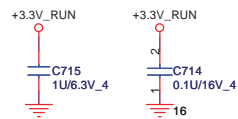
LAN To DB

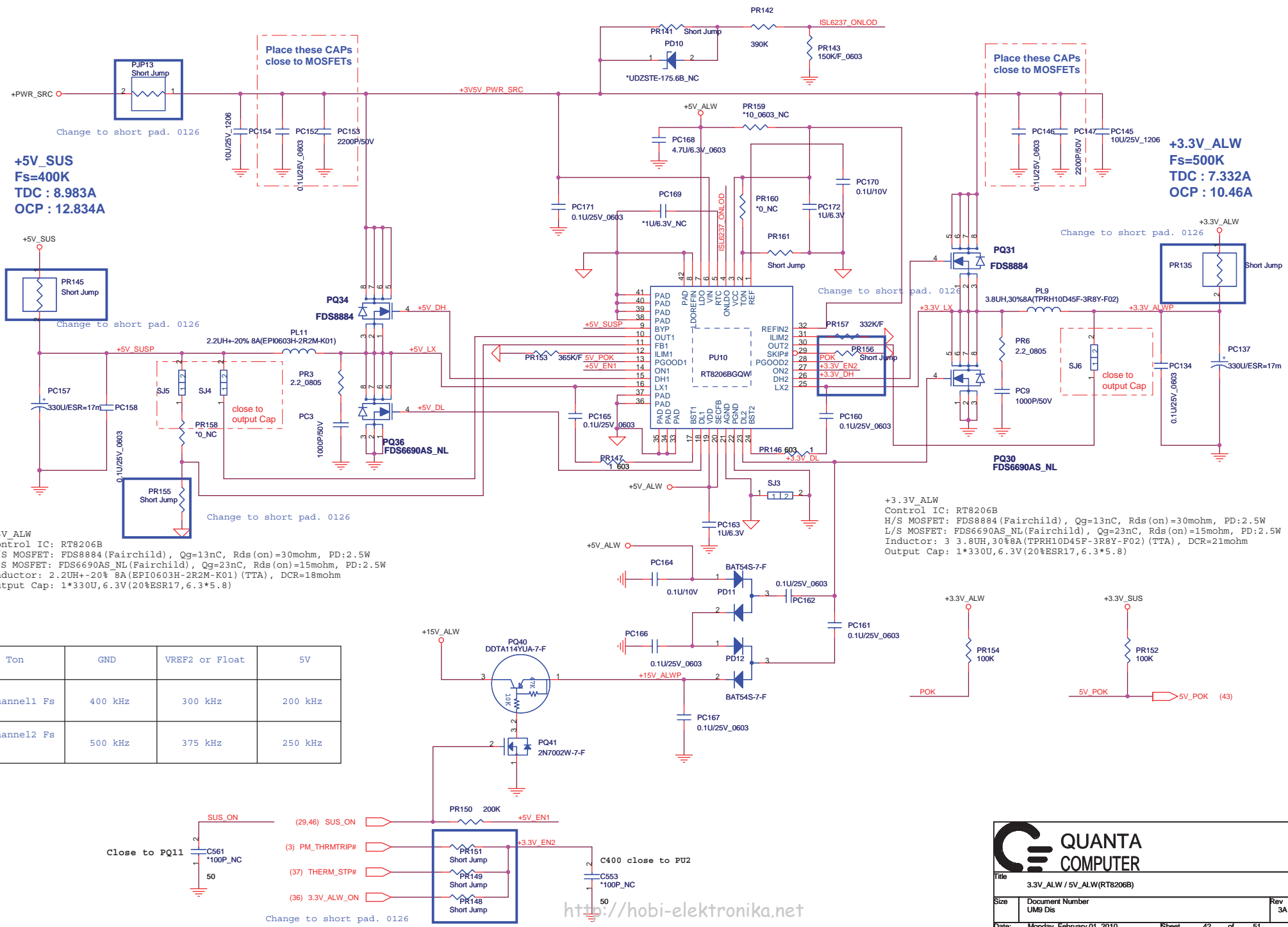
		Quanta Computer Inc.
		PROJECT : UM9B/C DIS
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	LAN(AR8152/RJ-45)	3A
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VTT_PWRGOOD
 SC(V1.0)P18:
 VTT_1.1 VR power good
 signal to processor. Signal
 voltage level is 1.1 V.





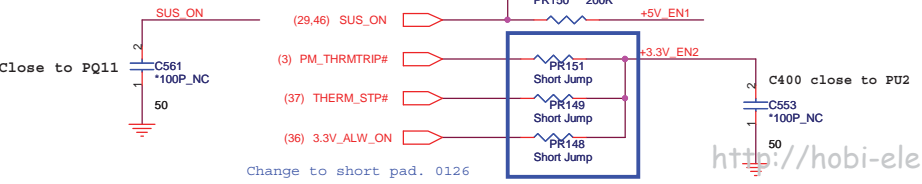
+5V_SUS
 Fs=400K
 TDC : 8.983A
 OCP : 12.834A

+3.3V_ALW
 Fs=500K
 TDC : 7.332A
 OCP : 10.46A

+5V_ALW
 Control IC: RT8206B
 H/S MOSFET: FDS8884 (Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
 L/S MOSFET: FDS6690AS NL (Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
 Inductor: 2.2UH+20% 8A (EPI0603H-2R2M-K01) (TTA), DCR=18mohm
 Output Cap: 1*330U, 6.3V (20%ESR17, 6.3*5.8)

+3.3V_ALW
 Control IC: RT8206B
 H/S MOSFET: FDS8884 (Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
 L/S MOSFET: FDS6690AS NL (Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
 Inductor: 3.8UH, 30%8A (TPRH10D45F-3R8Y-F02) (TTA), DCR=21mohm
 Output Cap: 1*330U, 6.3V (20%ESR17, 6.3*5.8)

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz

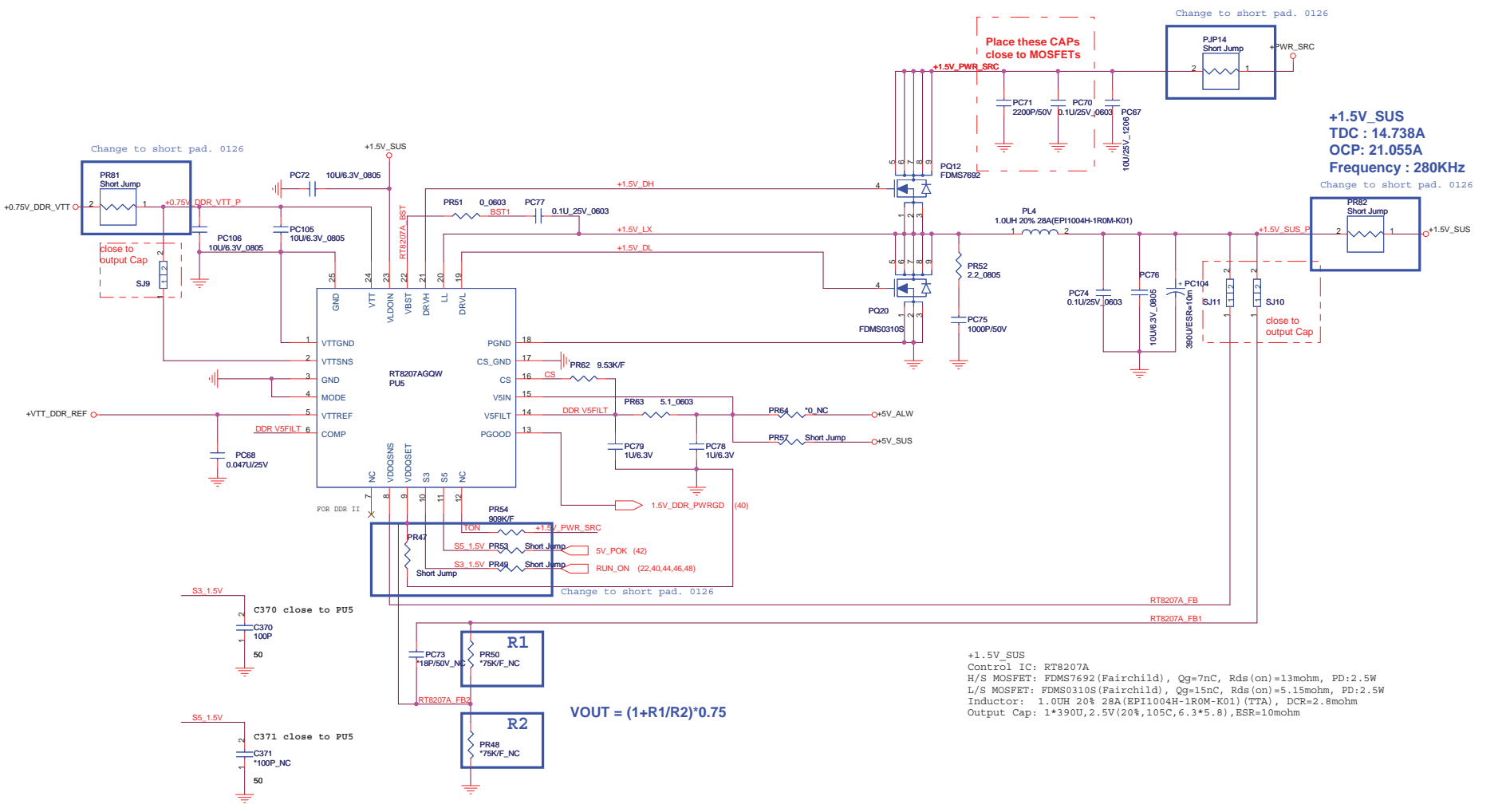


QUANTA COMPUTER

Title: 3.3V_ALW / 5V_ALW (RT8206B)

Size	Document Number	Rev
	UMG Dis	3A

Date: Monday, February 01, 2010 Sheet 42 of 51



+1.5V_SUS
 TDC : 14.738A
 OCP : 21.055A
 Frequency : 280KHz

+1.5V_SUS
 Control IC: RT8207A
 H/S MOSFET: FDMS7692 (Fairchild), Qg=7nC, Rds(on)=13mohm, PD:2.5W
 L/S MOSFET: FDMS0310S (Fairchild), Qg=15nC, Rds(on)=5.15mohm, PD:2.5W
 Inductor: 1.0UH 20% 28A (EPI1004H-1R0M-K01) (TTA), DCR=2.8mohm
 Output Cap: 1*390U, 2.5V (20%, 105C, 6.3*5.8), ESR=10mohm

$$V_{OUT} = (1 + R1/R2) * 0.75$$

VDDQ and VTT discharge control

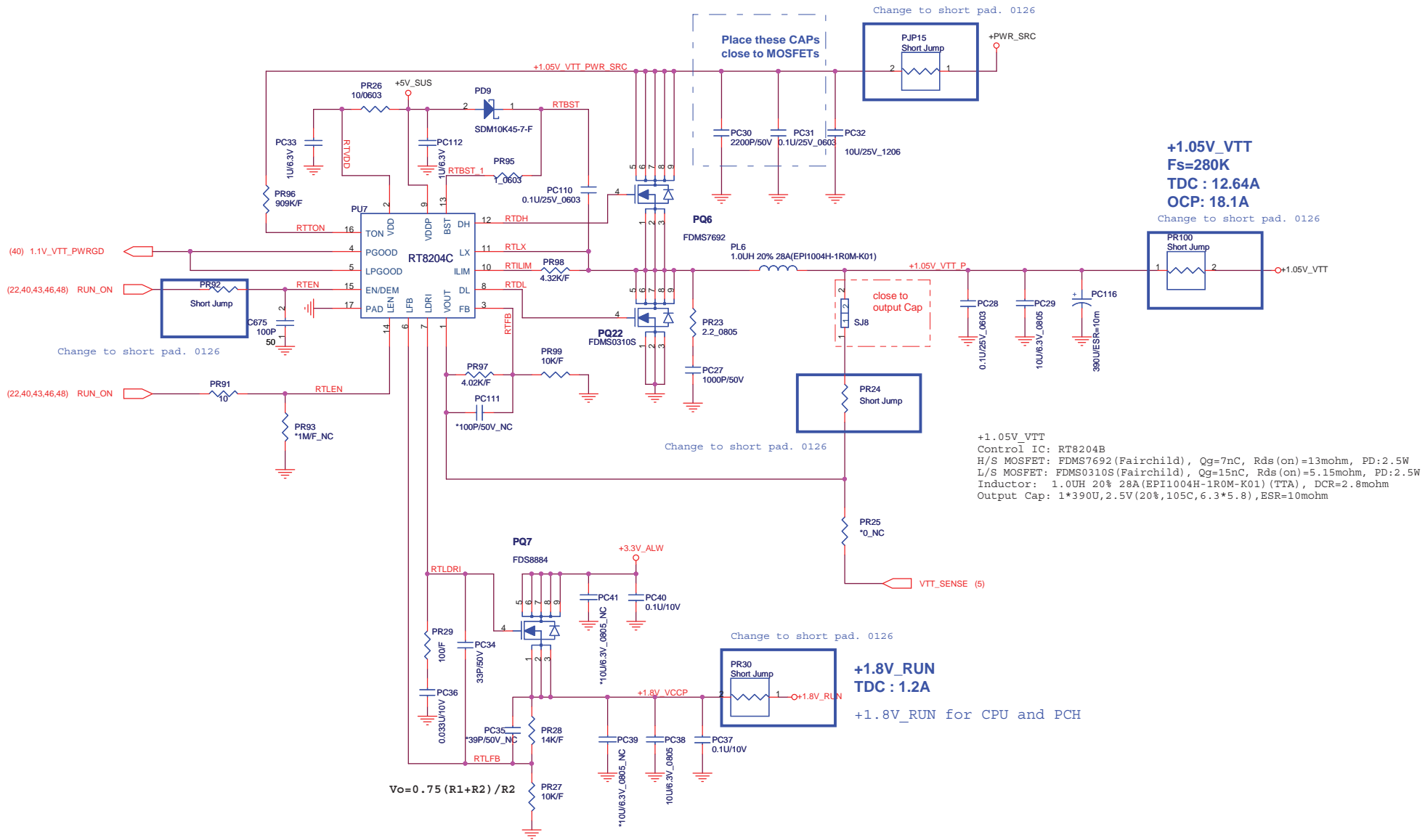
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

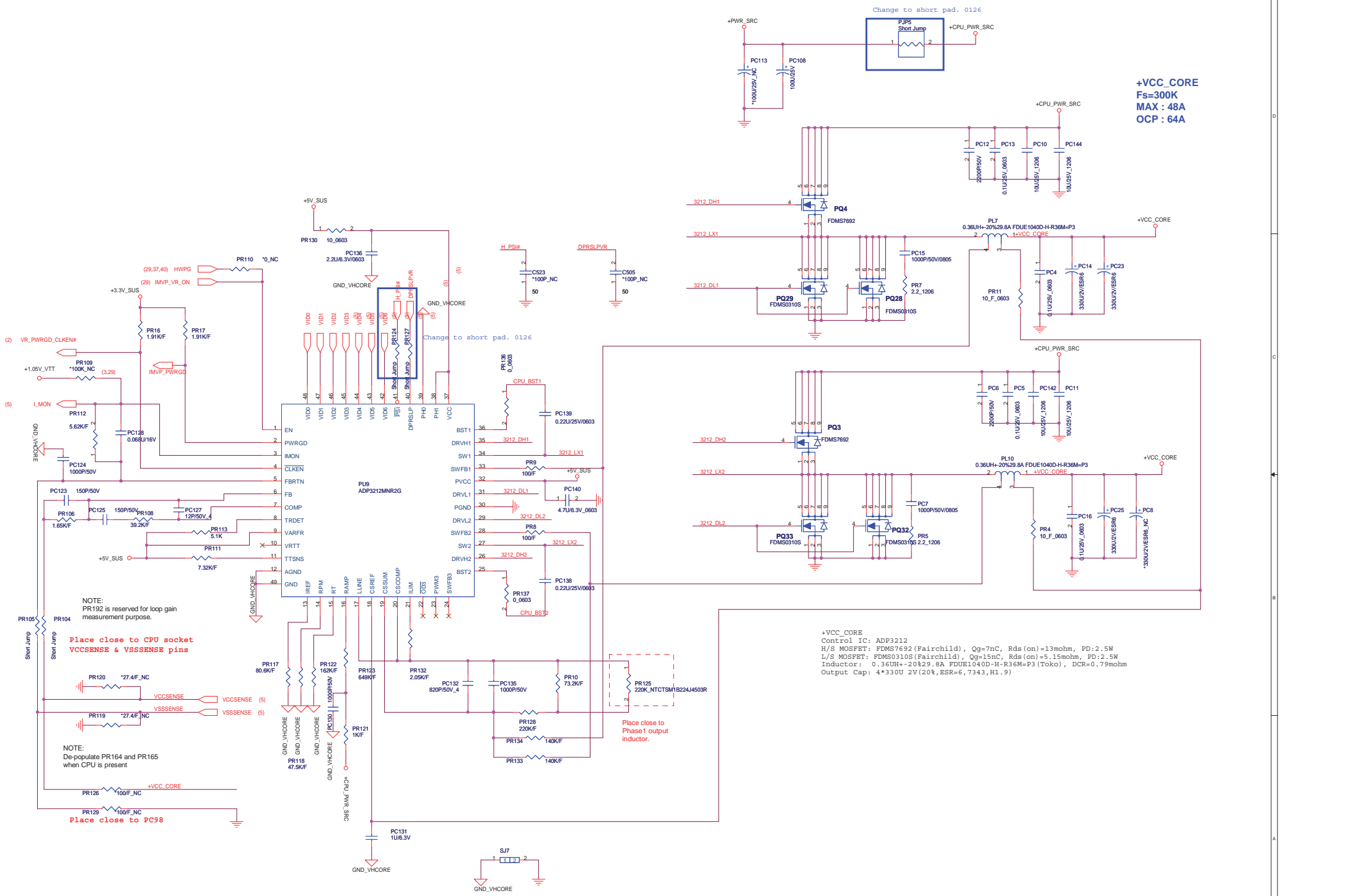
VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQNS/2	DDR3
V5IN	1.8V	VDDQNS/2	DDR2
FB Resistors	Adjusting	VDDQNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)



Title		
+1.05V_VTT(RT8204C)		
Size	Document Number	Rev
	UMG Dis	3A
Date:	Monday, February 01, 2010	Sheet 44 of 51



+VCC_CORE
Fs=300K
MAX : 48A
OCF : 64A

NOTE:
 PR192 is reserved for loop gain measurement purpose.

Place close to CPU socket
VCCSENSE & VSSSENSE pins

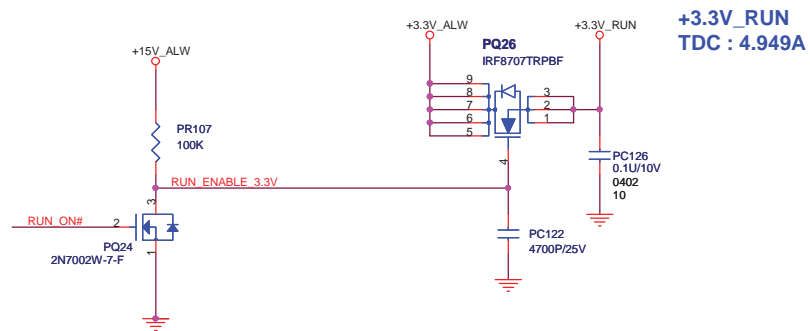
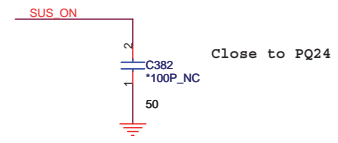
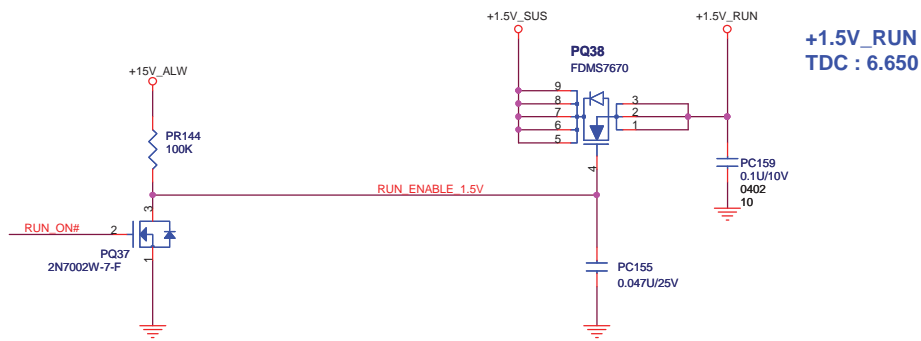
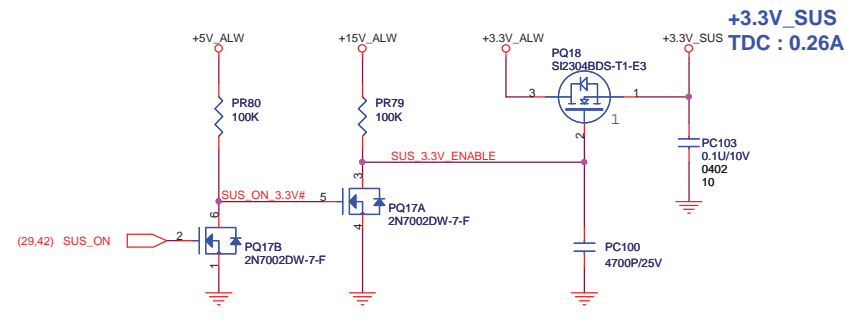
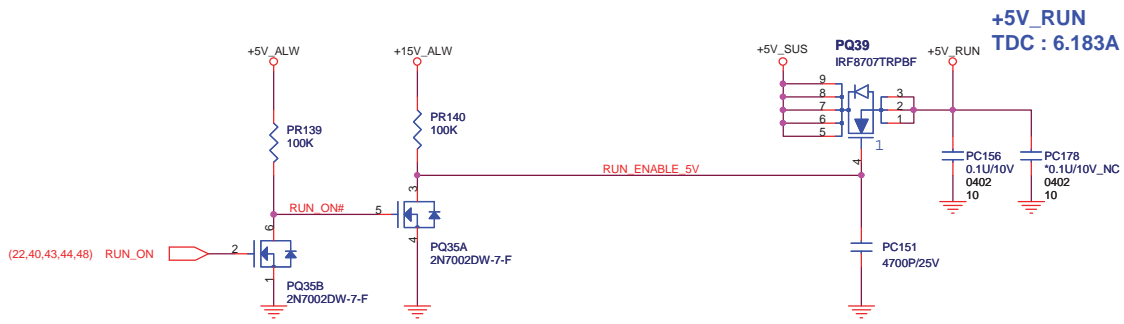
NOTE:
 De-populate PR164 and PR165
 when CPU is present

Place close to PC98

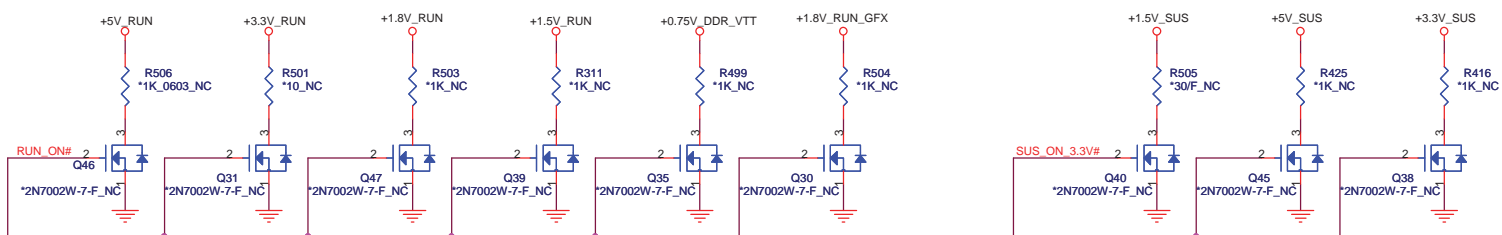
Place close to
 Phase1 output
 inductor.

+VCC_CORE
 Control IC: ADP3212
 H/S MOSFET: FDMS7692 (Fairchild), Qg=7nC, Rds(on)=13mohm, PD:2.5W
 L/S MOSFET: FDMS0310S (Fairchild), Qg=15nC, Rds(on)=5.15mohm, PD:2.5W
 Inductor: 0.36uH+20%±29.8A FDUE1040D-H-R36M-P3 (Tokko), DCR=0.79mohm
 Output Cap: 4*330U 2V(20%,ESR=6,7343,H1.9)

Title		CPU core (ADP3212MNR2G)	
Size	Document Number	Rev	
UMB Dts		3A	
Date:	Monday, February 01, 2010	Sheet	45 of 51



Reserve discharge path



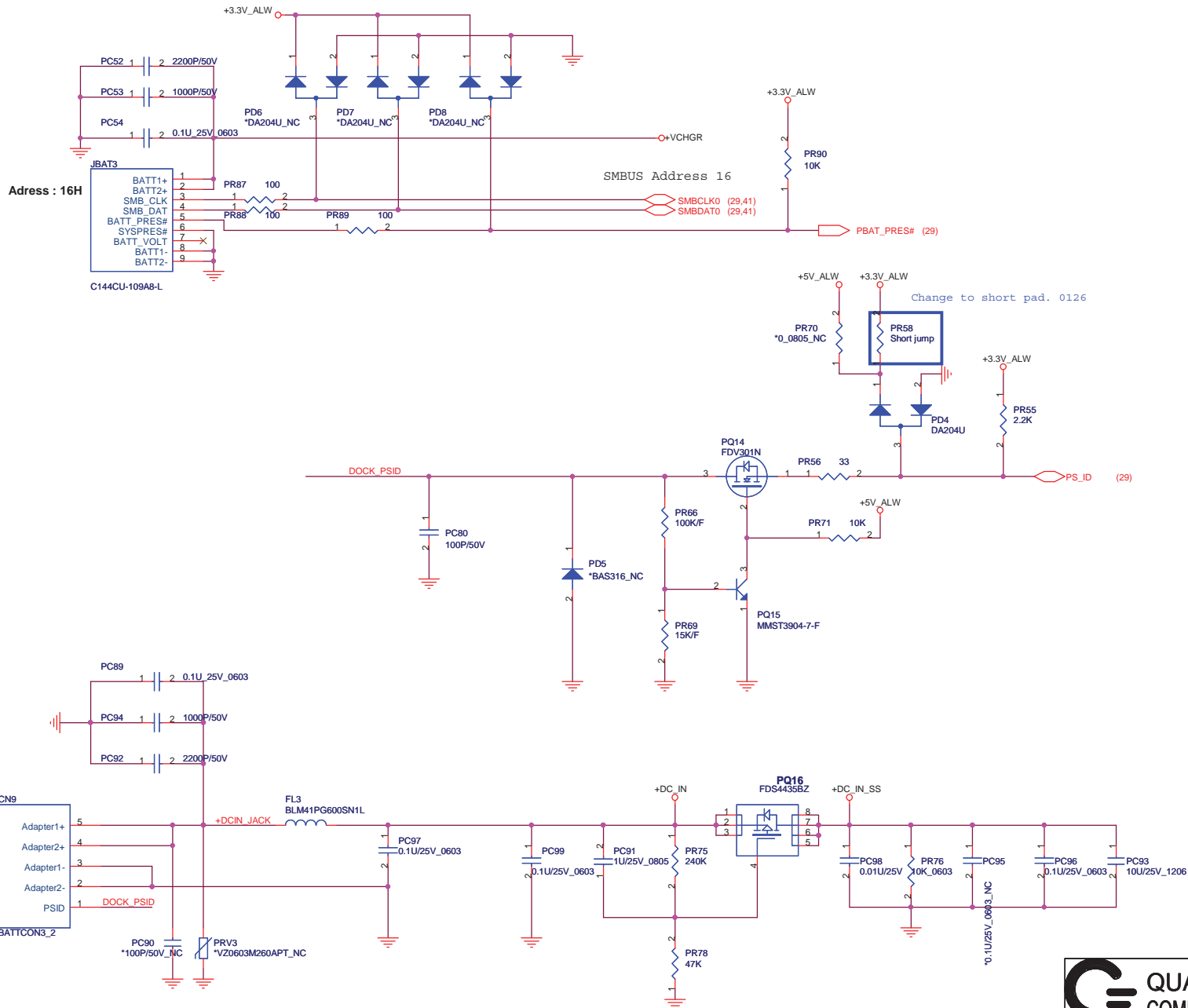
<http://hobi-elektronika.net>

**QUANTA
COMPUTER**

Title: RUN / SUS POWER SW

Size	Document Number UMG Dis	Rev 3A
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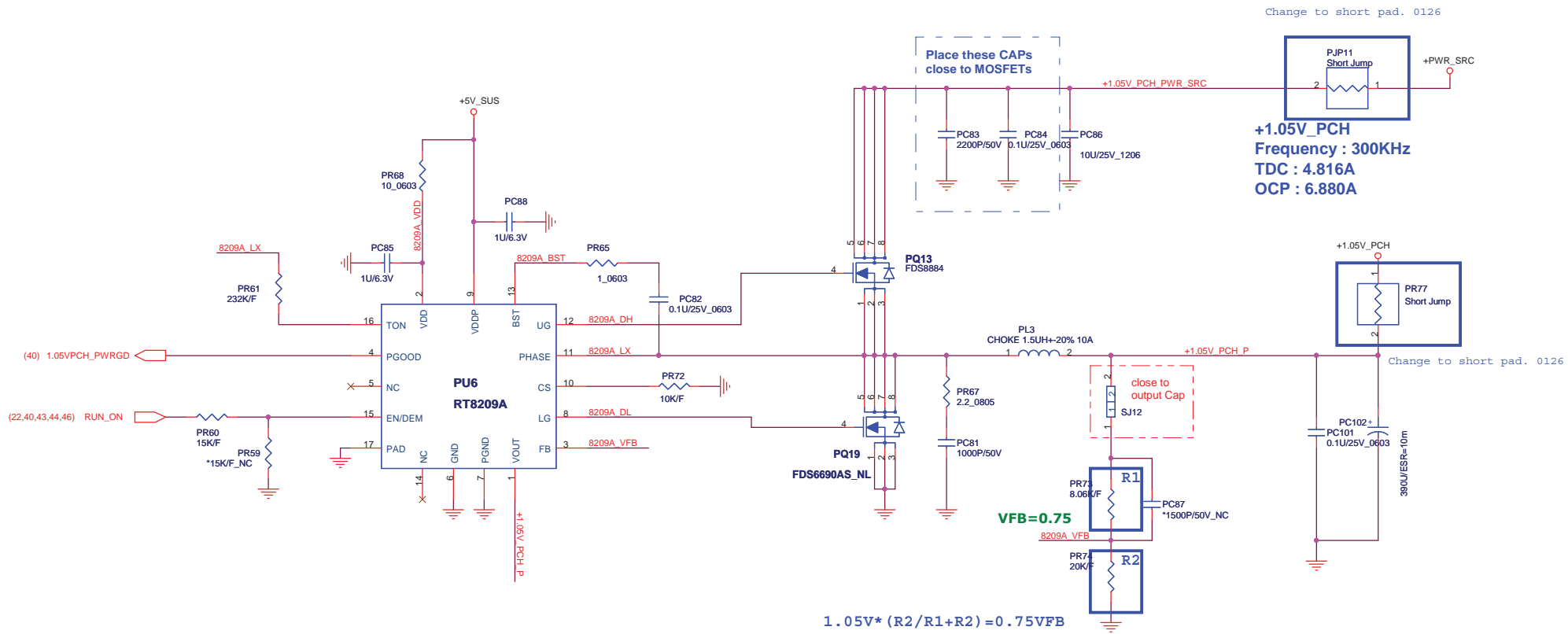


Address : 16H

Change to short pad. 0126

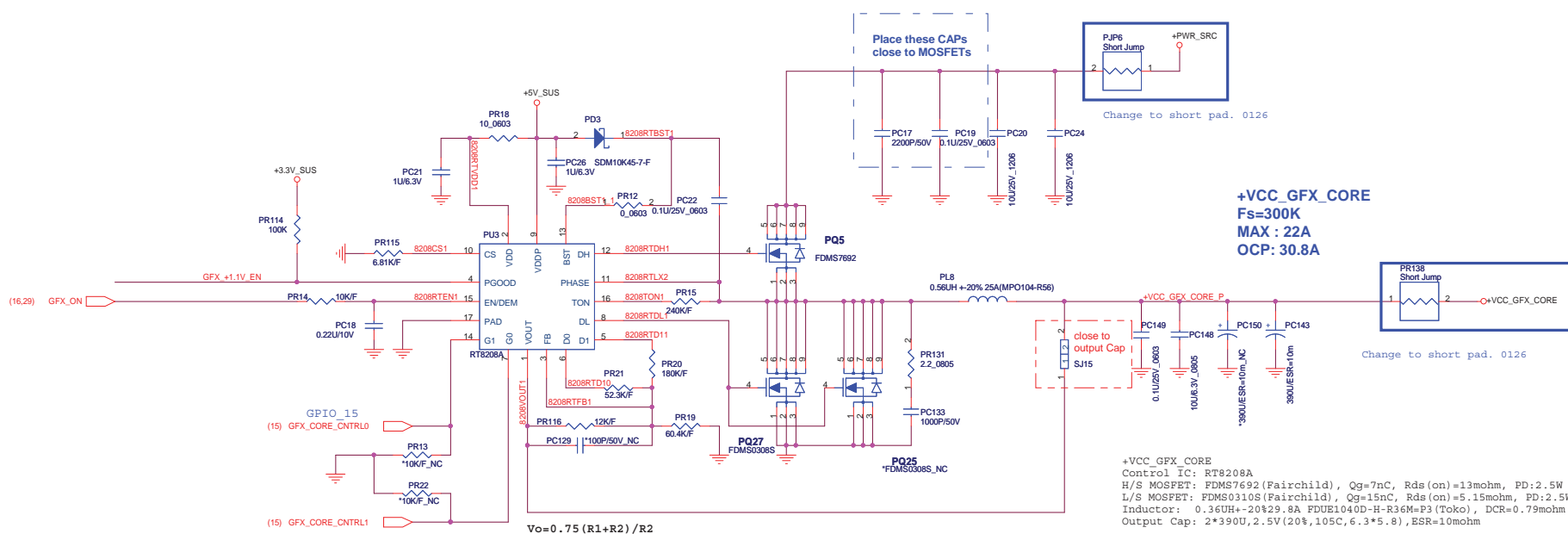


Title DCIN, BATT CONNECTOR		
Size	Document Number UM9 Dis	Rev 3A
Date:	Monday, February 01, 2010	Sheet 47 of 51



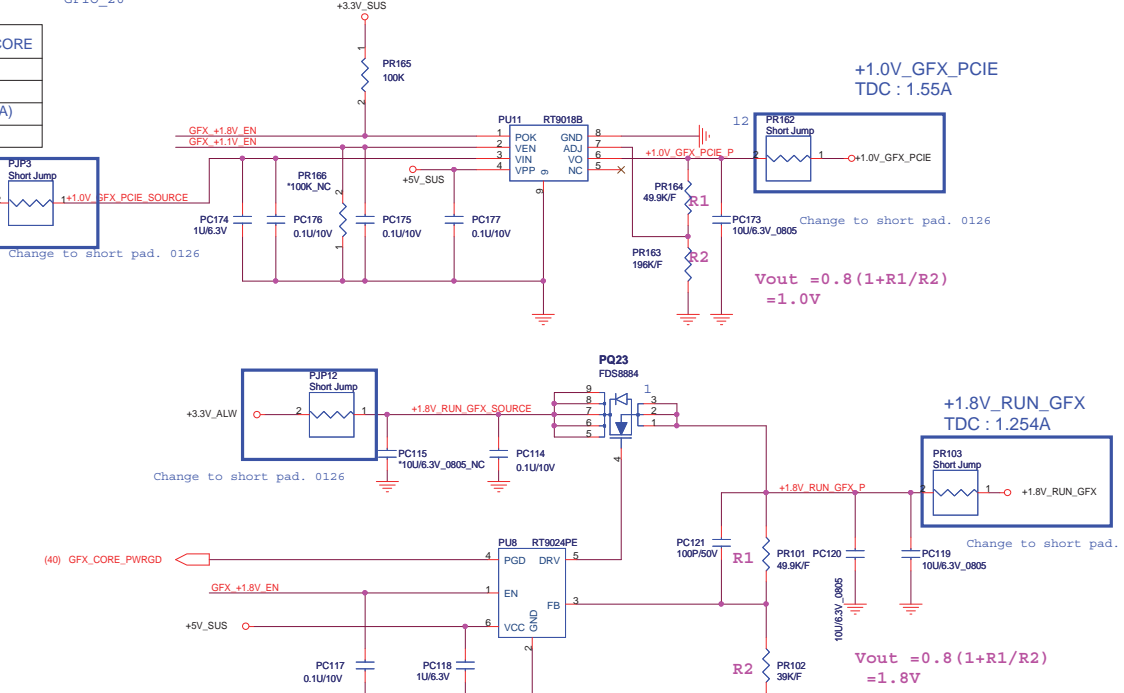
+1.05V_PCH
Control IC: RT8209A
H/S MOSFET: FDS8884 (Fairchild), Qg=13nC, Rds(on)=30mohm, PD=2.5W
L/S MOSFET: FDS6690AS_NL (Fairchild), Qg=23nC, Rds(on)=15mohm, PD=2.5W
Inductor: 1.5uH+-20% 9A (10D40F-1R5M) (TTA), DCR=10.5mohm
Output Cap: 1*390u, 2.5V (20%, 105C, 6.3*5.8), ESR=10mohm

Title		
+1.05V_PCH(RT8209A)		
Size	Document Number	Rev
	UMG Dis	3A
Date:	Monday, February 01, 2010	Sheet 48 of 51

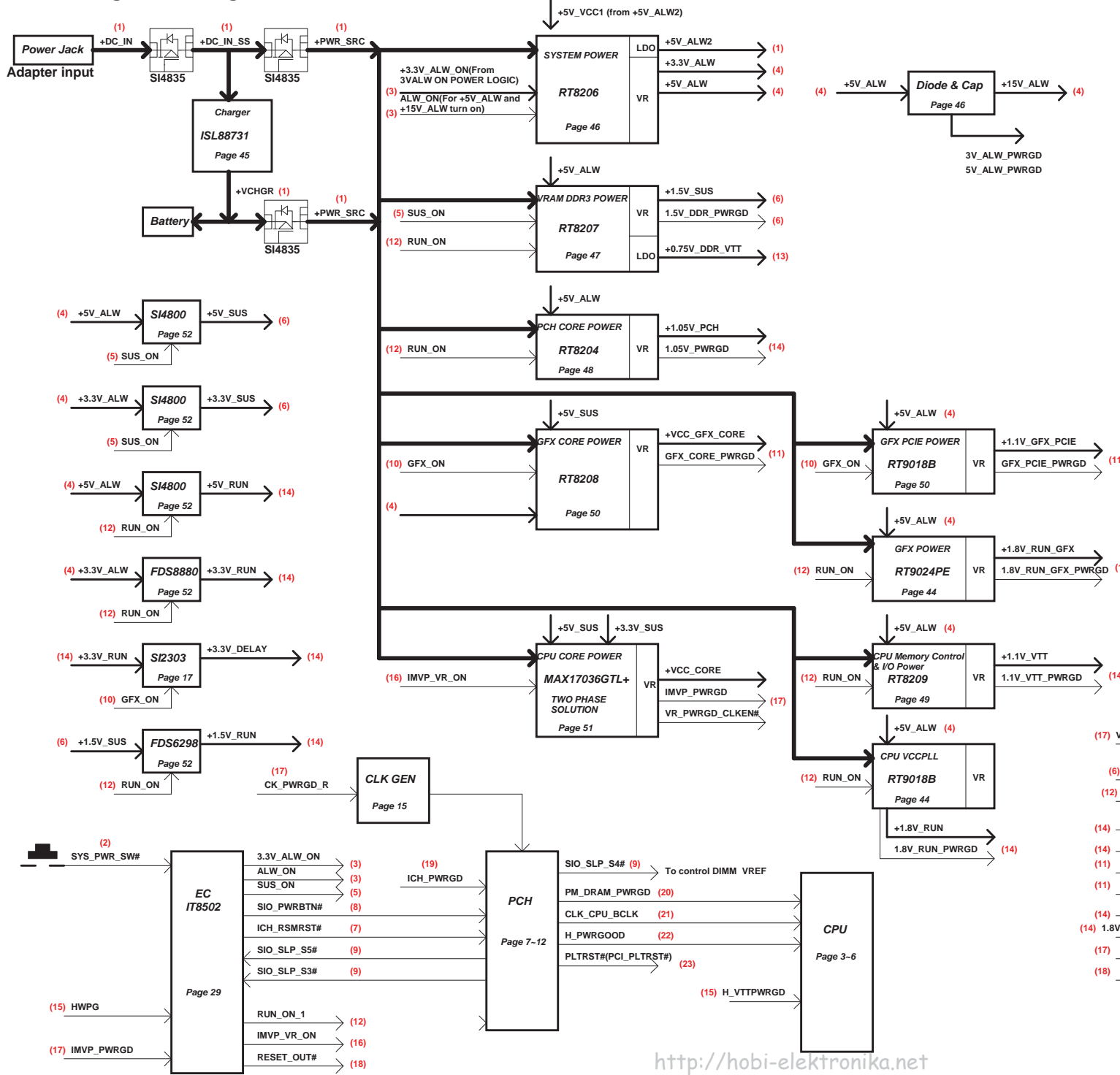


For Park-XT:

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
LOW	HIGH	1.07V(N/A)
HIGH	HIGH	1.12V

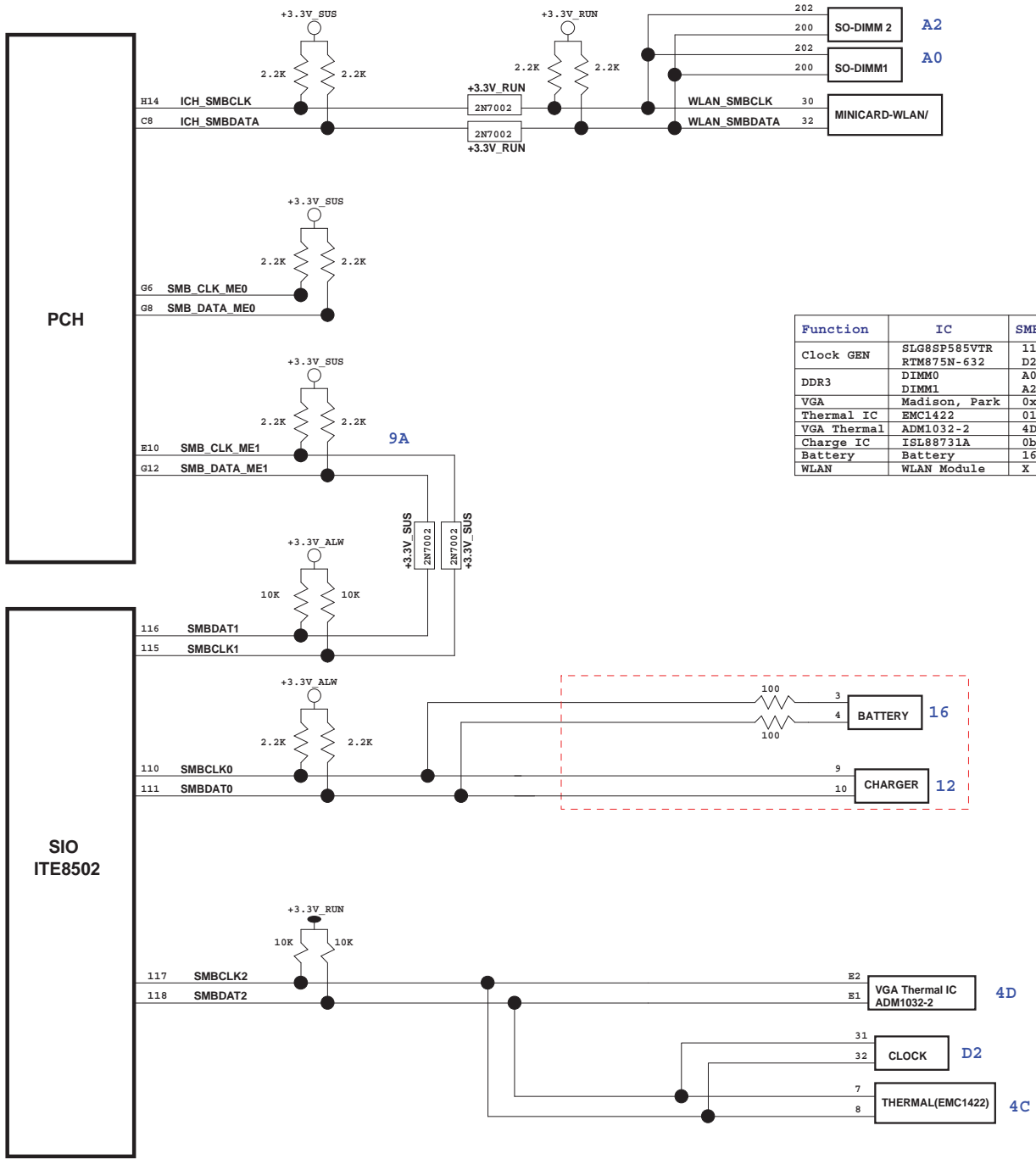


Power Design Block Diagram 2009/08/24



- (1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC, +5V_ALW2,
- (2) SYS_PWR_SW#
- (3) 3.3V_ALW_ON, ALW_ON
- (4) +3.3V_ALW, +5V_ALW, +15V_ALW
- (5) SUS_ON
- (6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
- (7) ICH_RSMRST#
- (8) SIO_PWRBTN#
- (9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
- (10) GFX_ON
- (11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
- (12) RUN_ON_1(RUN_ON)
- (13) +0.75V_DDR_VTT
- (14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
- (16) IMVP_VR_ON
- (17) +VCC_CORE, IMVP_PWRGD
- (18) RESET_OUT#
- (19) ICH_PWRGD
- (20) PM_DRAM_PWRGD
- (21) CLK_CPU_BCLK(PCH to CPU)
- (22) H_PWRGOOD
- (23) PLTRST#(PCI_PLTRST#)

<http://hobi-elektronika.net>



Function	IC	SMBus Address
Clock GEN	SLG8SP585VTR RTM875N-632	11010010 (D2h) D2h
DDR3	DIMM0 DIMM1	A0 A2
VGA	Madison, Park	0x41
Thermal IC	EMC1422	0100 1100b (4Ch)
VGA Thermal	ADM1032-2	4D
Charge IC	ISL88731A	0b0001001 (0x12)
Battery IC	Battery	16h
WLAN	WLAN Module	X