

FX5 SAPPORO-INTEGRATED

REV : A00

POWER

SYSTEM RESET CIRCUIT PG 39

RUN POWER SW PG 46

BATT CHARGER PG 40

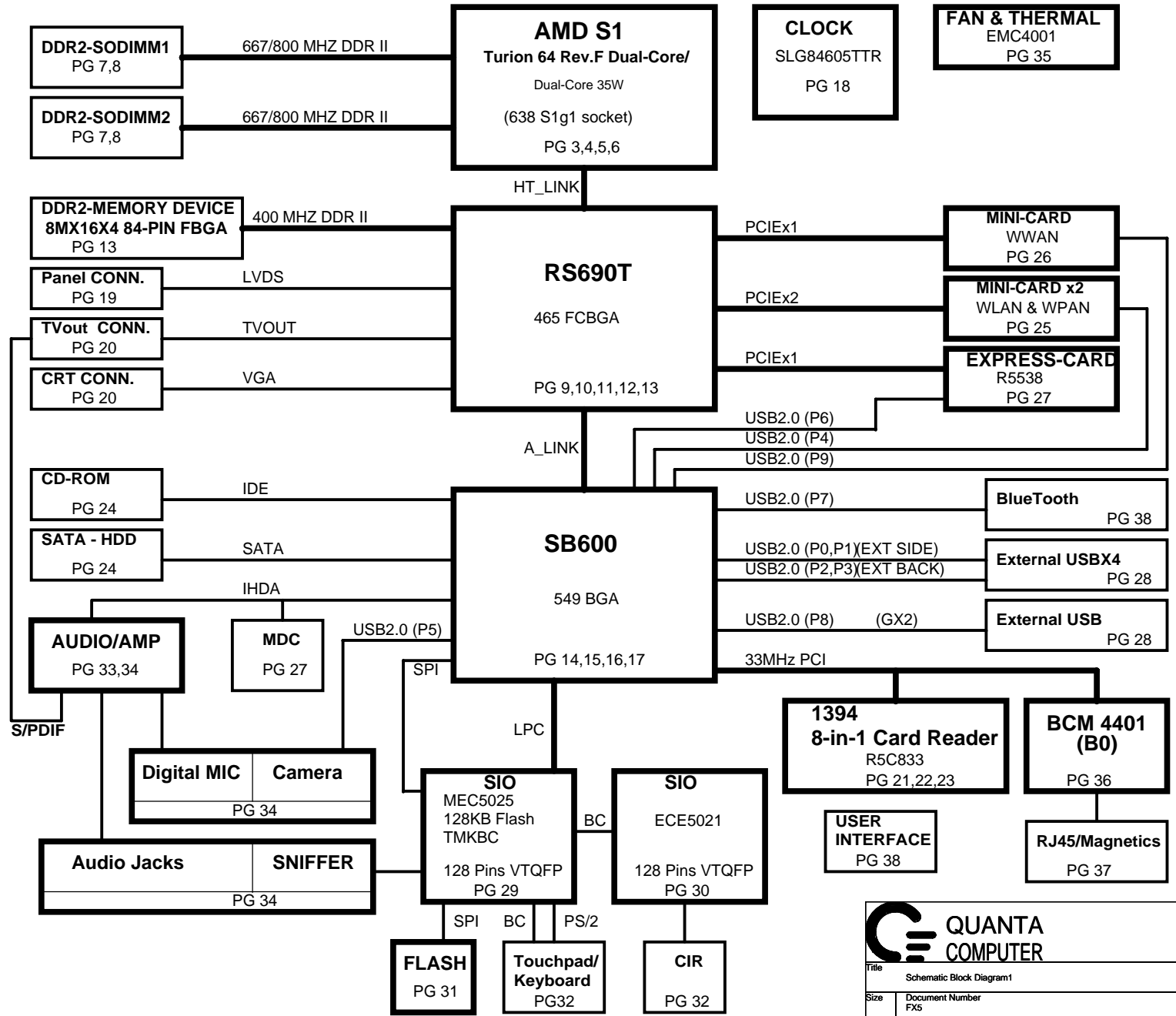
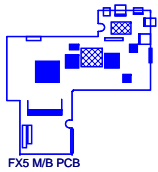
AC/BATT CONNECTOR PG 41

CPU VR PG 44

DC/DC +3.3V_SUS/+5V_SUS/+15V_SUS PG 45

REGULATOR VCC_NB & +1.2V_ALW_SUS PG 42

REGULATOR +1.8V_SUS/+0.9V_DDR_VTT/+1.5V_RUN PG 43



Title		
Schematic Block Diagram1		
Size	Document Number	Rev
FX5		1A
Date:	Friday, May 04, 2007	Sheet 1 of 61



PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax and VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

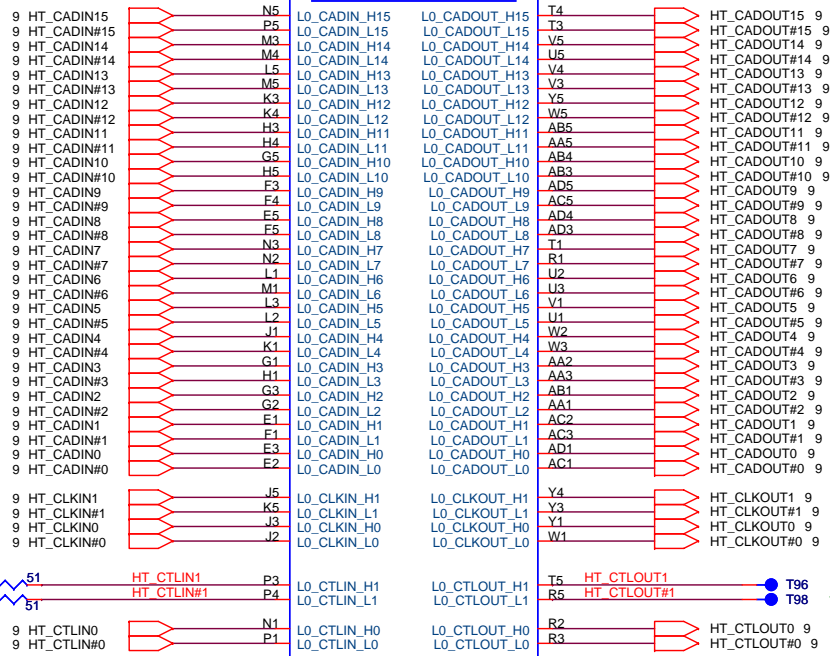
LAYOUT: Place bypass cap on topside of board



NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

+1.2V_RUN

U18A



Place R167 and R166 less than 100mils from CPU

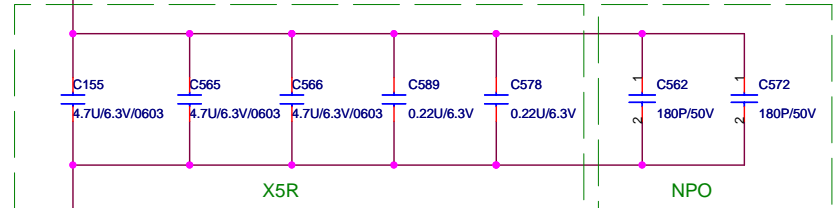
+1.2V_RUN



Place T96 and T98 less than 100mils from CPU



+1.2V_RUN



Athlon 64 S1 Processor Socket



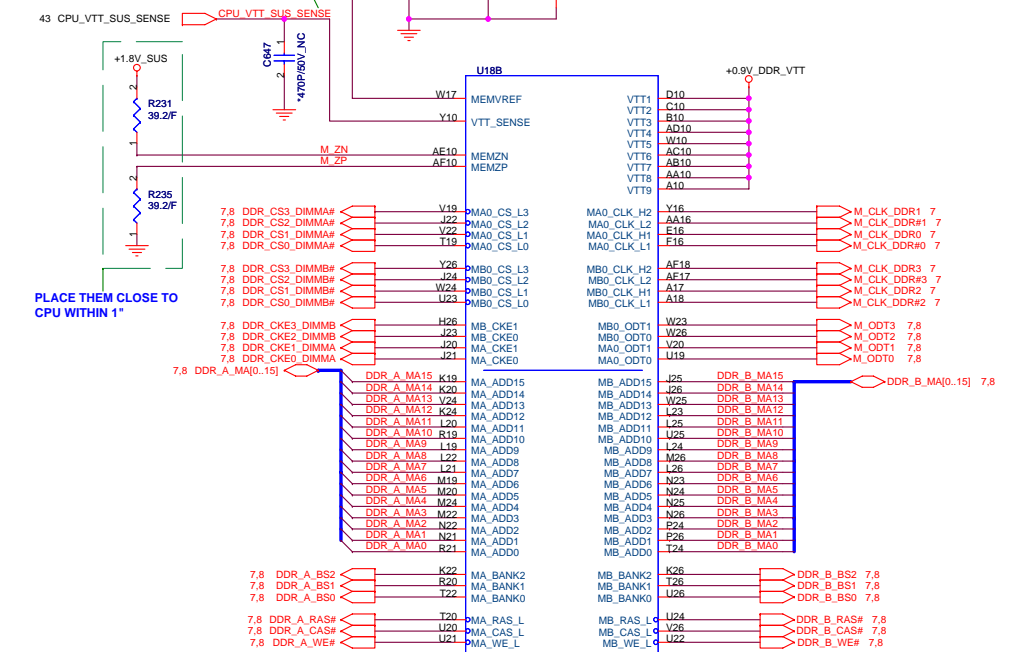
Title		
ATHLON64 HT I/F		
Size	Document Number	Rev
	FX5	1A
Date:	Friday, May 04, 2007	Sheet 3 of 61



VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

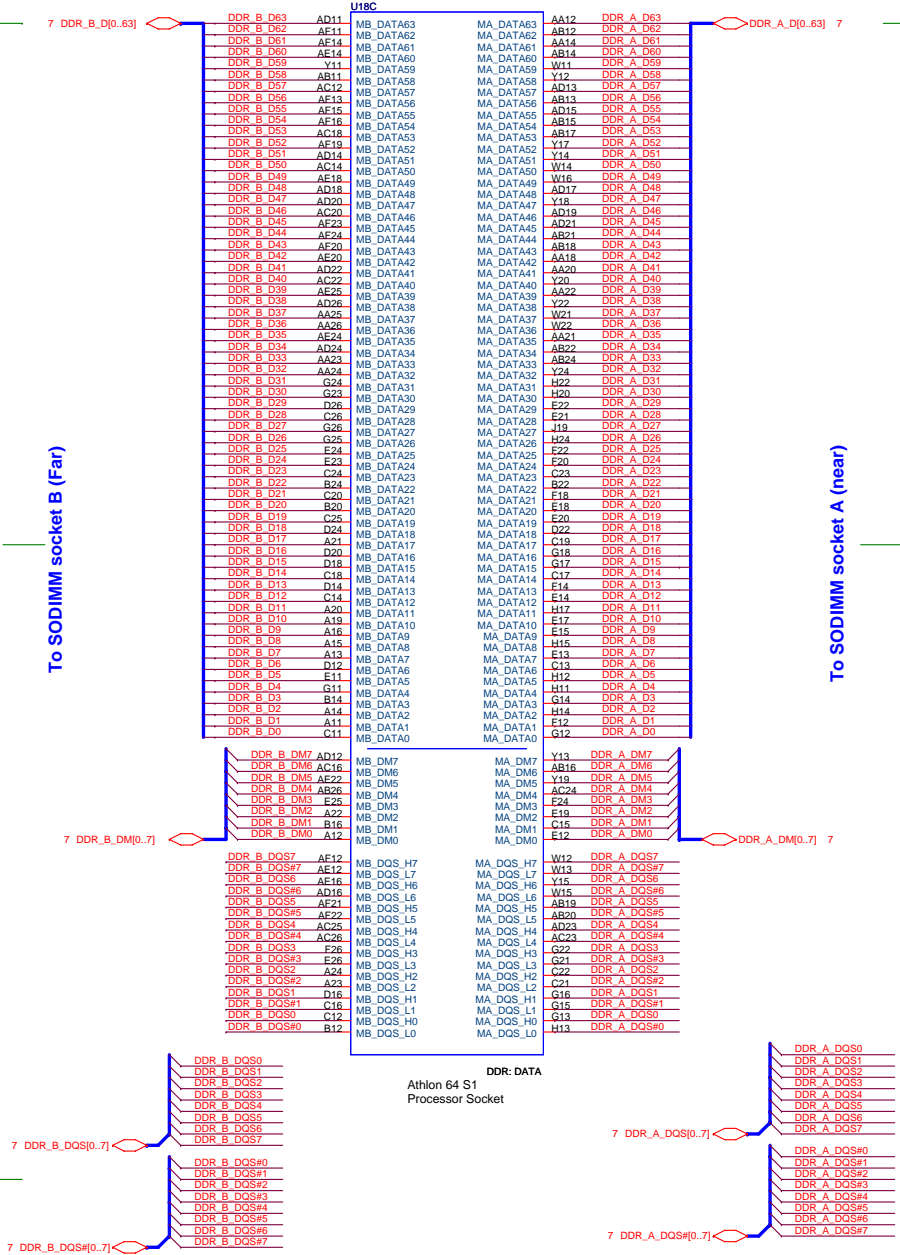
Place Capacitors for +0.9V_CPU_M_VREF_SUS < 1" from the RS690T. +0.9V_CPU_M_VREF_SUS trace length < 6", trace width > 15mils and 20mils spacing from any adjacent signals in X, Y, Z directions.

CPU_VTT_SUS_SENSE should be routed as 10mils and 10mils spacing from any adjacent signals in X, Y, Z directions.



PLACE THEM CLOSE TO CPU WITHIN 1"

Processor DDR2 Memory Interface



DDR II: CMD/CTRL/CLK
Athlon 64 S1
Processor Socket

DDR: DATA
Athlon 64 S1
Processor Socket

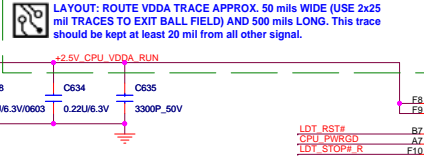


ATHLON Control and Debug

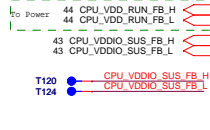
The AMD SI feature has errata, and will not be implemented.



Check ferrite bead with an approximate impedance of 35, a maximum DC resistance of 40 m, and a current rating of at least 500 mA.



Place R168 and R165 < 1.5'. Route CPU_HTRREF1/0 with 5 mils trace width and 10 mils spacing from other signals in X, Y, Z directions



CPU_DBRDY
CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI

T125 CPU_TEST25_H_BYPASSCLK_H
T118 CPU_TEST25_L_BYPASSCLK_L
T125 CPU_TEST19_PLLTEST0
T133 CPU_TEST18_PLLTEST1

T112 CPU_TEST17_BP3
T125 CPU_TEST16_BP2
T108 CPU_TEST15_BP1
T117 CPU_TEST12_SCANSHIFTENB

T33 CPU_TEST07_ANALOG_T
T87 H_THERMDC
T95 H_THERMDA
T103 CPU_TEST2_DRAIN0

T142 CPU_RSVD_M00_CLK3_P
T134 CPU_RSVD_M00_CLK0_P
T132 CPU_RSVD_M00_CLK0_N

T70 CPU_RSVD_M00_CLK3_P
T89 CPU_RSVD_M00_CLK3_N
T144 CPU_RSVD_M00_CLK0_P
T147 CPU_RSVD_M00_CLK0_N

T142 CPU_RSVD_M00_CLK3_P
T89 CPU_RSVD_M00_CLK3_N
T144 CPU_RSVD_M00_CLK0_P
T147 CPU_RSVD_M00_CLK0_N

T70 CPU_RSVD_M00_CLK3_P
T89 CPU_RSVD_M00_CLK3_N
T144 CPU_RSVD_M00_CLK0_P
T147 CPU_RSVD_M00_CLK0_N

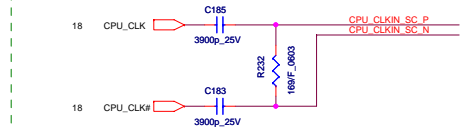
T70 CPU_RSVD_M00_CLK3_P
T89 CPU_RSVD_M00_CLK3_N
T144 CPU_RSVD_M00_CLK0_P
T147 CPU_RSVD_M00_CLK0_N

T70 CPU_RSVD_M00_CLK3_P
T89 CPU_RSVD_M00_CLK3_N
T144 CPU_RSVD_M00_CLK0_P
T147 CPU_RSVD_M00_CLK0_N

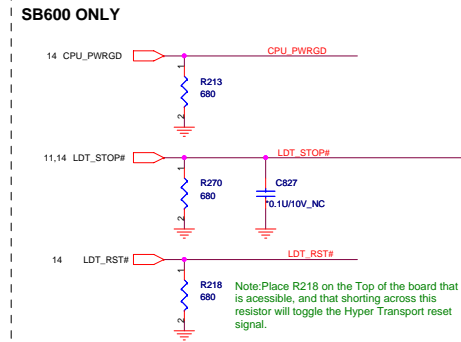
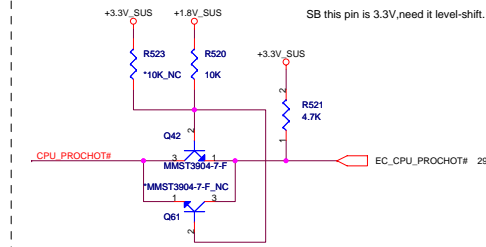
T70 CPU_RSVD_M00_CLK3_P
T89 CPU_RSVD_M00_CLK3_N
T144 CPU_RSVD_M00_CLK0_P
T147 CPU_RSVD_M00_CLK0_N

T70 CPU_RSVD_M00_CLK3_P
T89 CPU_RSVD_M00_CLK3_N
T144 CPU_RSVD_M00_CLK0_P
T147 CPU_RSVD_M00_CLK0_N

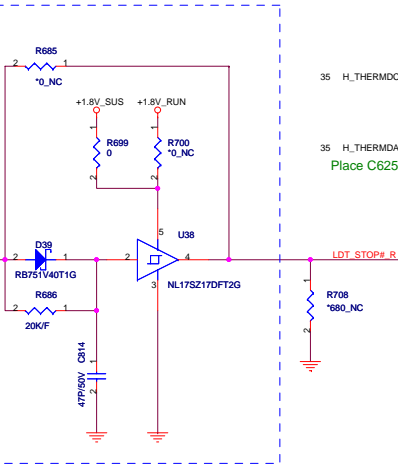
T70 CPU_RSVD_M00_CLK3_P
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T147 CPU_RSVD_M00_CLK0_N



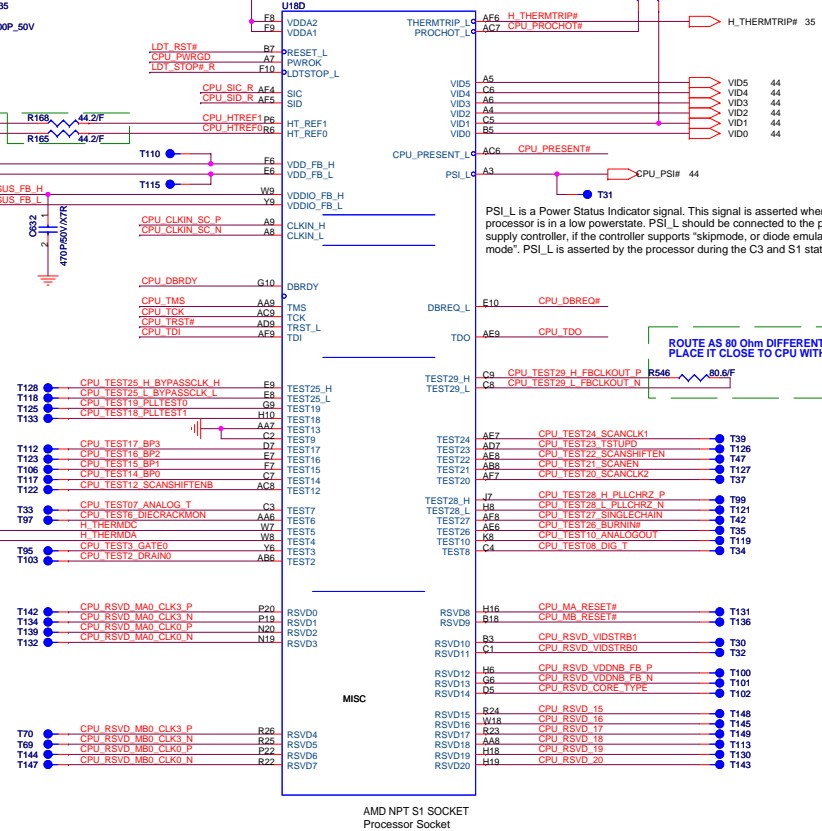
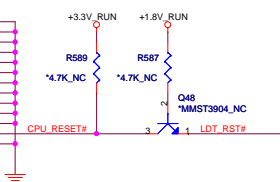
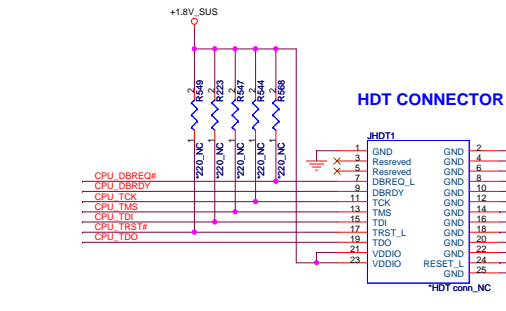
1. Keep trace to resistor less than 600 mils from cpu and trace to cap less than 1250 mils
2. CPUCLK and CPUCLK# mismatch < 35 mils.



Note: Place R218 on the Top of the board that is accessible, and that shorting across this resistor will toggle the Hyper Transport reset signal.



Place C625 < 100 mils from CPU.

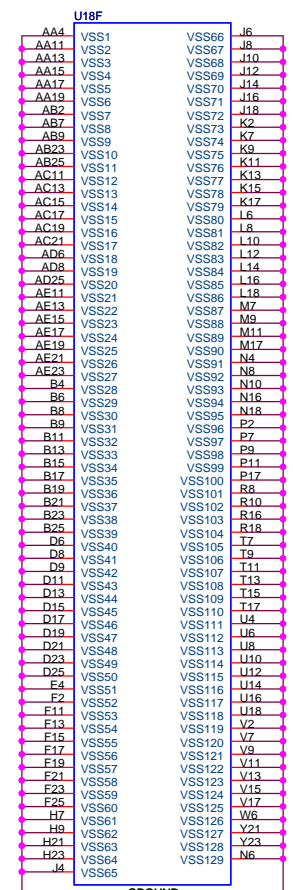
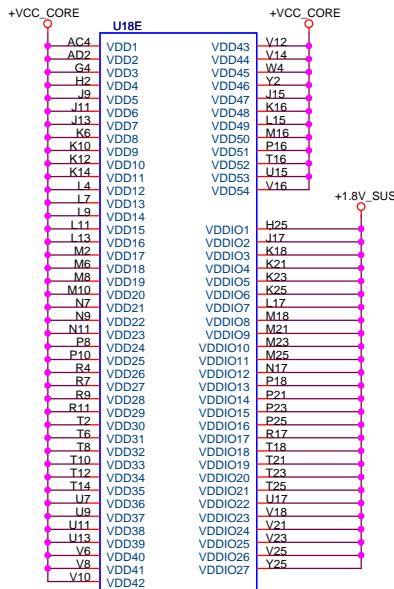


CPU_TEST27_SINGLECHAIN R216 *300_NC
CPU_TEST16_BURNIN# R206 *300_NC
CPU_PRESENT# R516 *10F
CPU_TEST25_H_BYPASSCLK_H R566 *510F

CPU_TEST21_SCANEN R541 *300
CPU_TEST20_SCANCLK2 R209 *300_NC
CPU_TEST14_SCANCLK1 R212 *300_NC
CPU_TEST22_SCANSHIFTEN R221 *300_NC
CPU_TEST12_SCANSHIFTENB R536 *300_NC
CPU_TEST15_BP1 R530 *300_NC
CPU_TEST14_BP0 R540 *300_NC

CPU_TEST25_L_BYPASSCLK_L R535 *510F
CPU_TEST19_PLLTEST10 R542 *300
CPU_TEST18_PLLTEST11 R575 *300

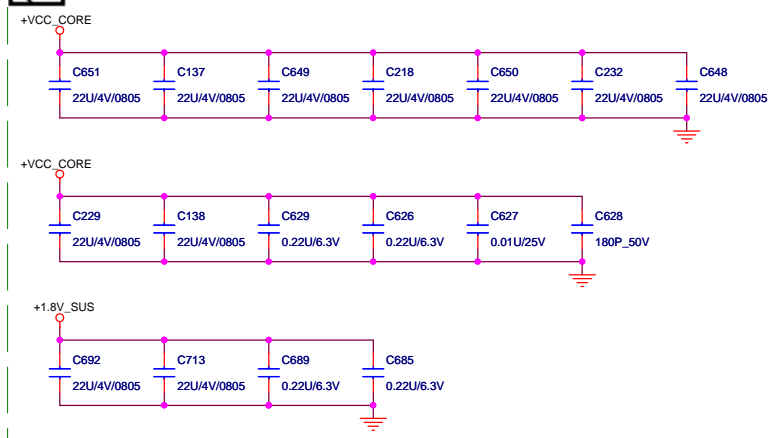




Athlon 64 S1 Processor Socket

Athlon 64 S1g1 uPGA638 Top View

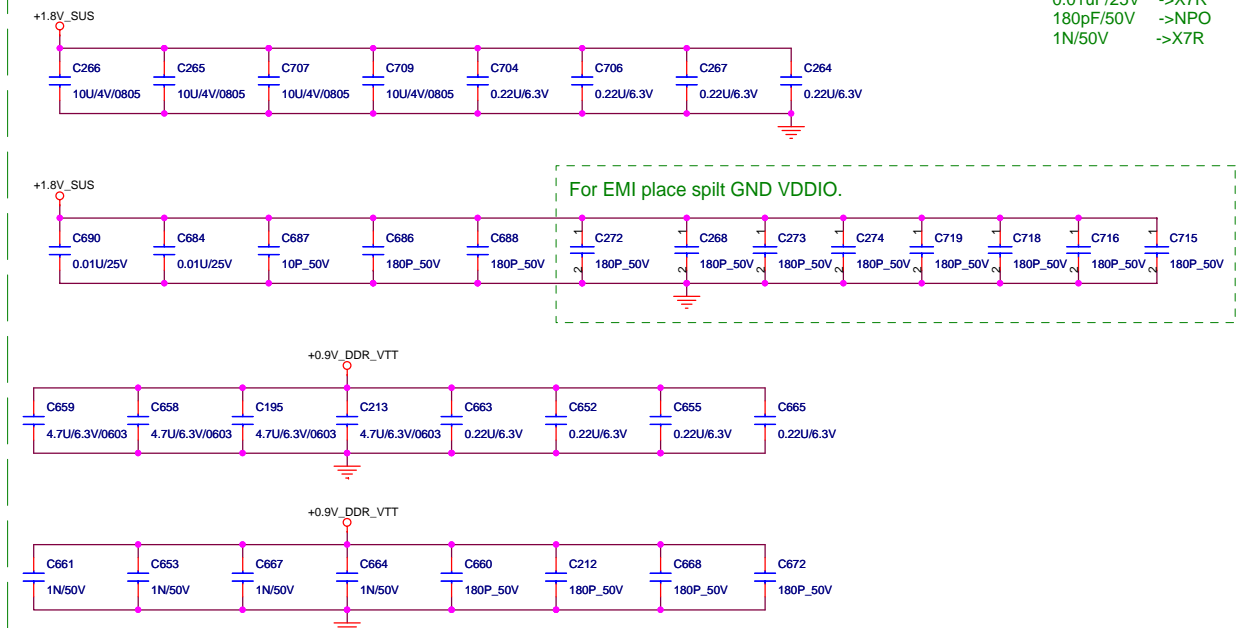
BOTTOMSIDE DECOUPLING



22uF/4V/0805->X6S
 0.22uF/6.3V ->X5R
 0.01uF/25V ->X7R
 180pF/50V ->NPO

DECOUPLING BETWEEN PROCESSOR AND DIMMs

PLACE CLOSE TO PROCESSOR AS POSSIBLE



10u/4V/0805->X6S
 4.7u/6.3V/0603->X5R
 0.22uF/6.3V ->X5R
 0.01uF/25V ->X7R
 180pF/50V ->NPO
 1N/50V ->X7R

PROCESSOR POWER AND GROUND

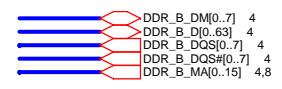
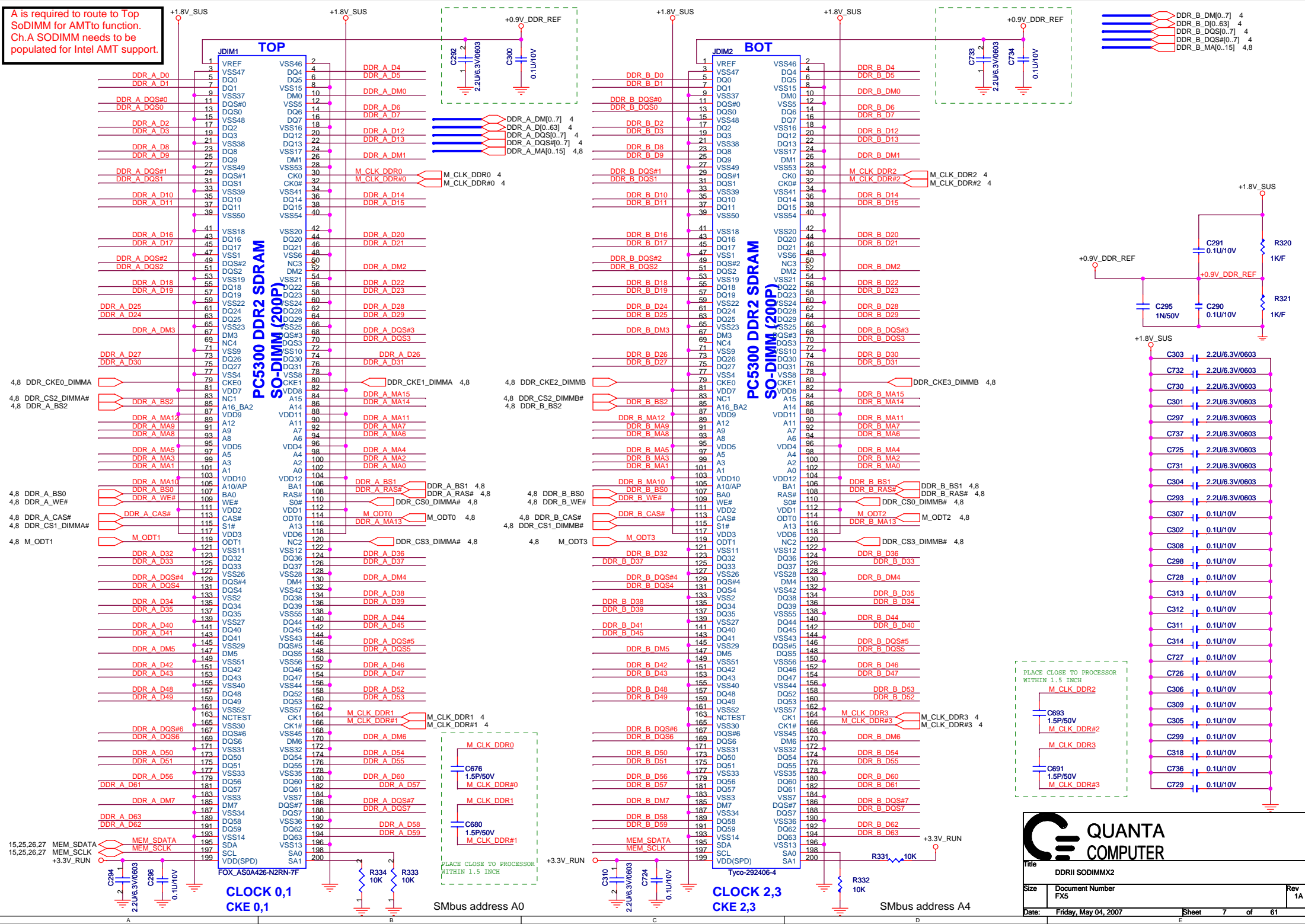
QUANTA COMPUTER

Title: ATHLON64 PWR & GND

Size: Document Number FX5 Rev 1A

Date: Friday, May 04, 2007 Sheet 6 of 61

A is required to route to Top SoDIMM for AMT to function. Ch.A SODIMM needs to be populated for Intel AMT support.



PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

M_CLK_DDR2
C693 1.5P/50V
M_CLK_DDR#2

M_CLK_DDR3
C691 1.5P/50V
M_CLK_DDR#3

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

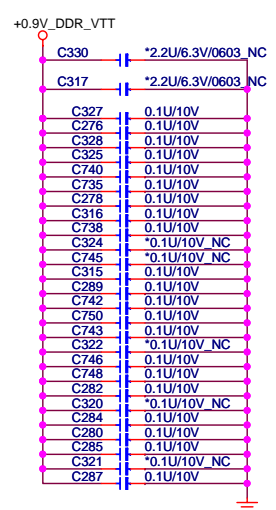
M_CLK_DDR0
C676 1.5P/50V
M_CLK_DDR#0

M_CLK_DDR1
C680 1.5P/50V
M_CLK_DDR#1

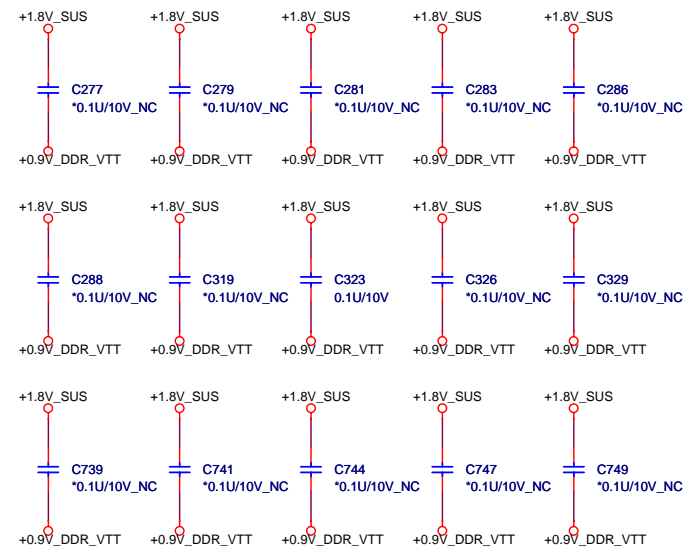
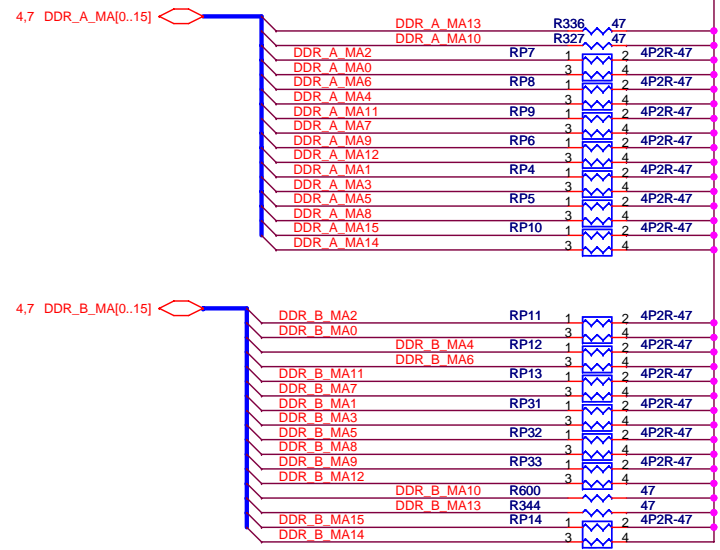
QUANTA COMPUTER

Title: DDR1 SODIMM2

Size	Document Number FX5	Rev 1A
Date: Friday, May 04, 2007	Sheet 7 of 61	



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT

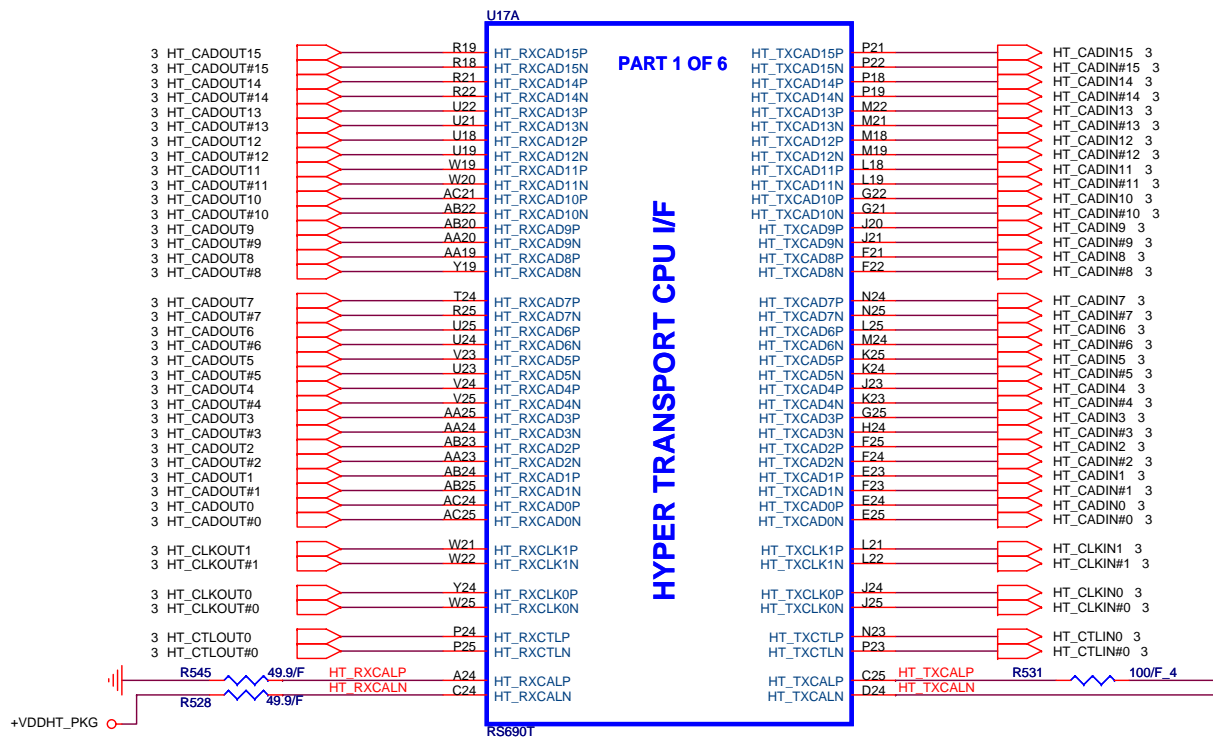


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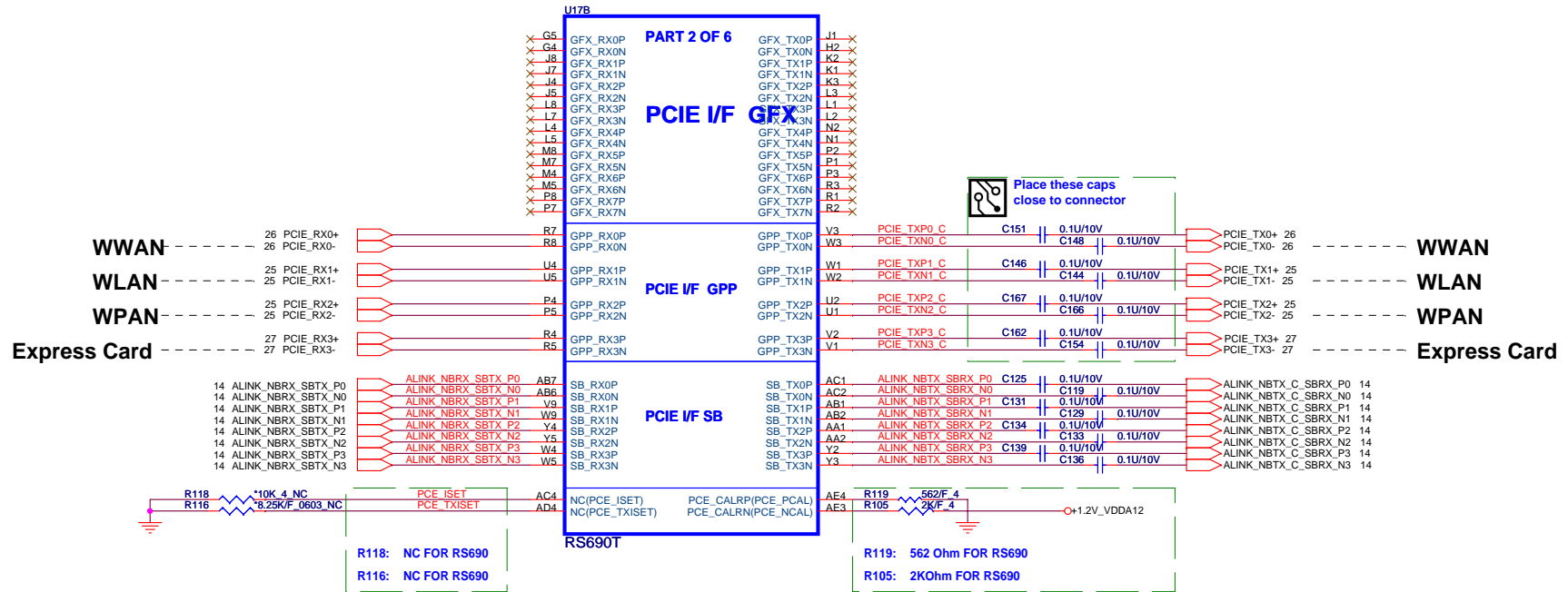
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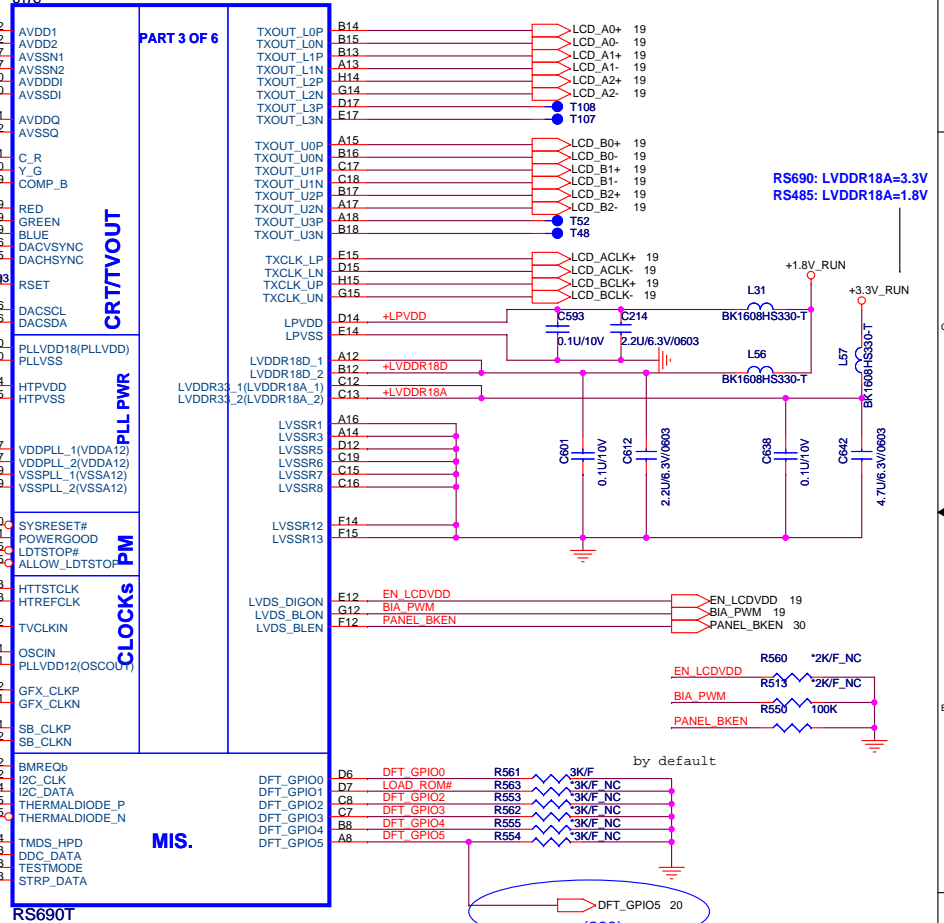
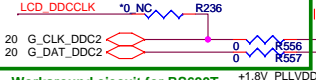
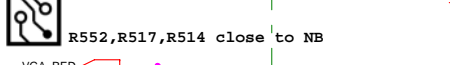
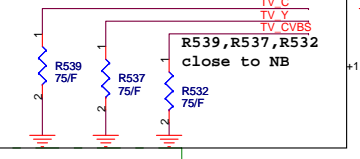
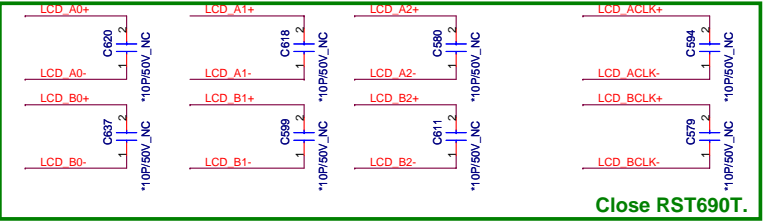
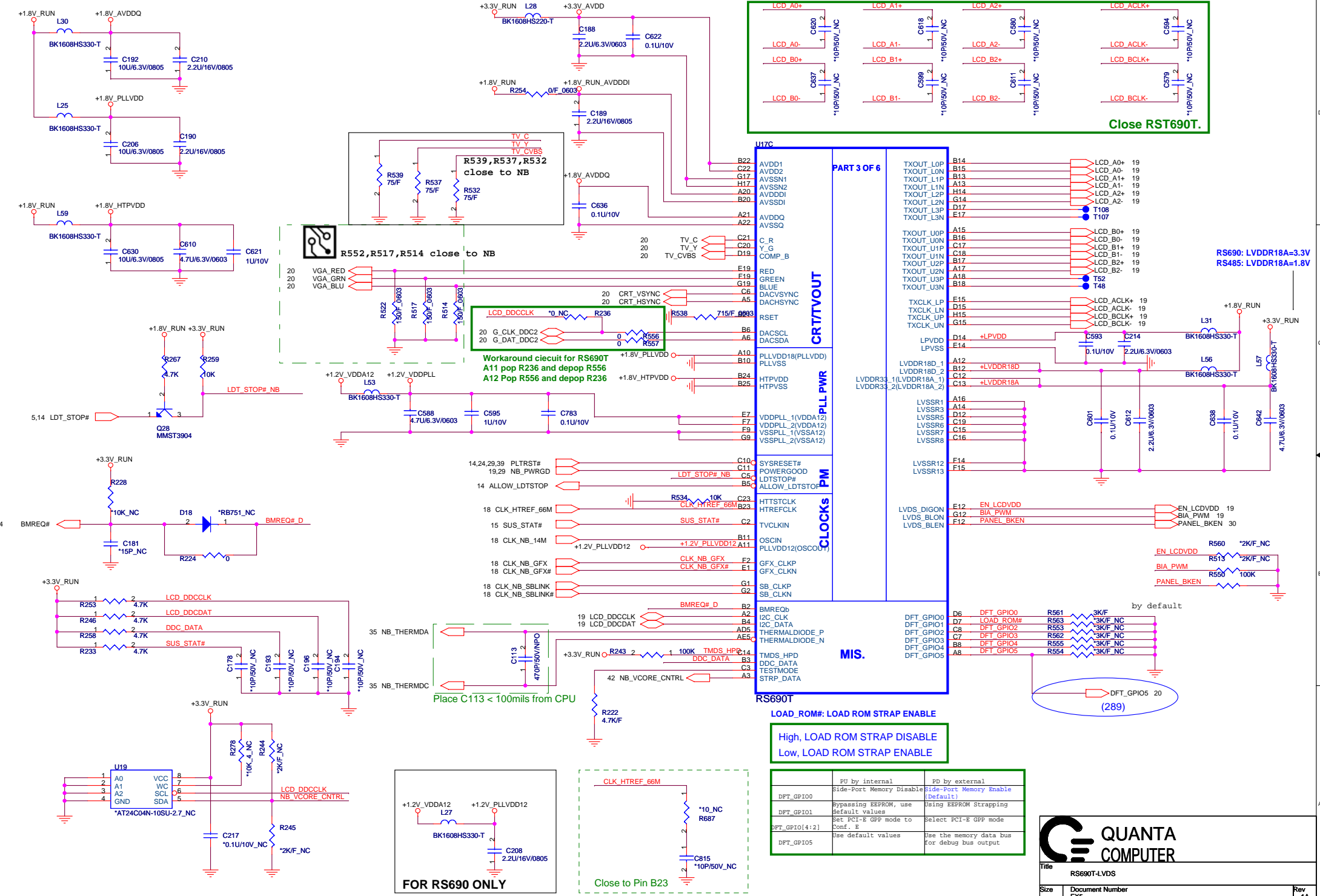
Size	Document Number FX5	Rev 1A
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Date: Friday, May 04, 2007 Sheet 8 of 61



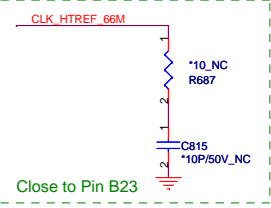
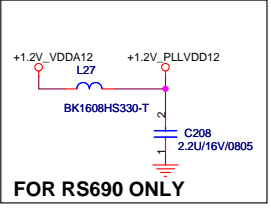
Title		RS690T-HT LINK0 I/F
Size	Document Number	Rev
	FX5	1A
Date:	Friday, May 04, 2007	Sheet 9 of 61

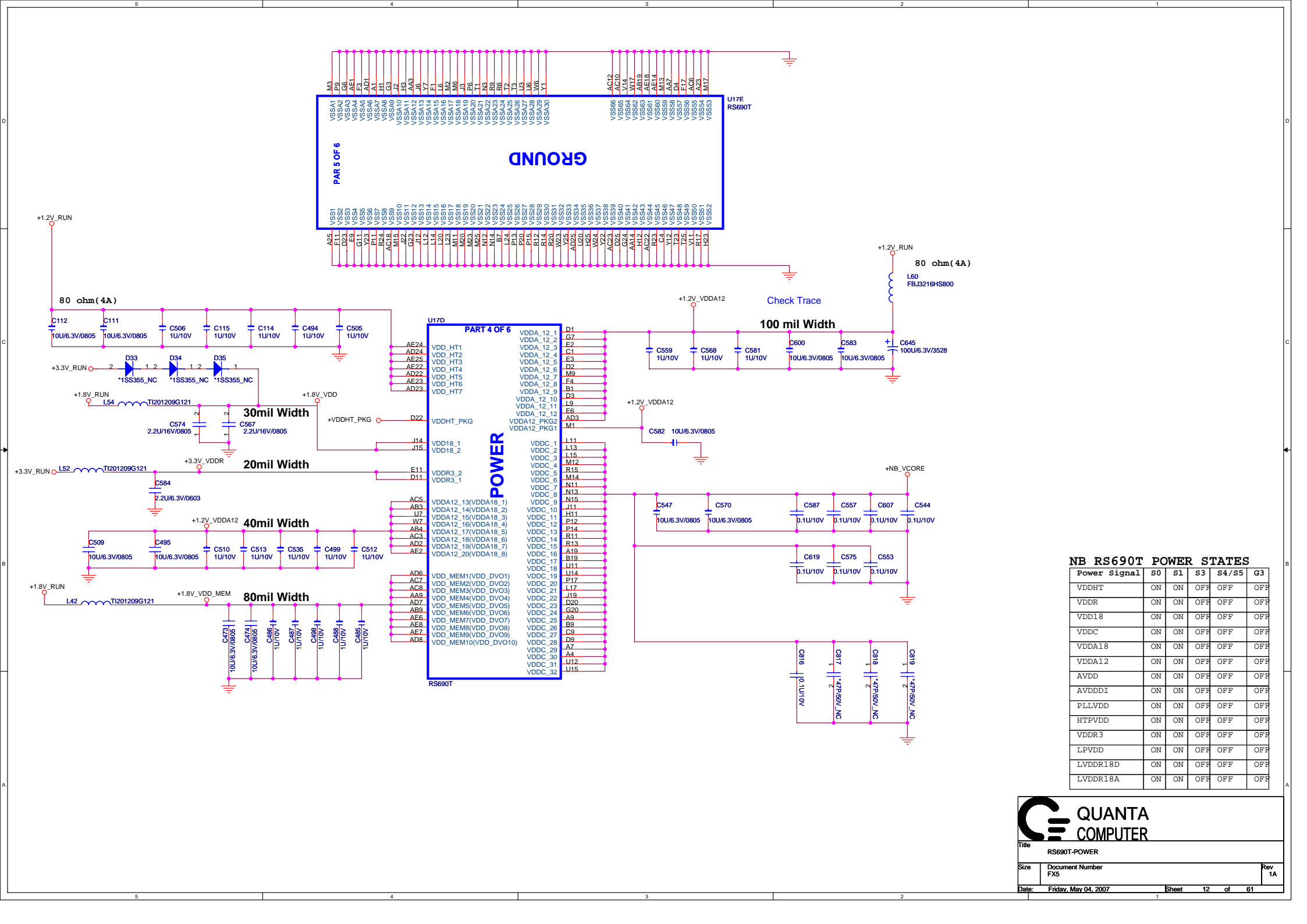




LOAD_ROM#: LOAD ROM STRAP ENABLE
 High, LOAD ROM STRAP DISABLE
 Low, LOAD ROM STRAP ENABLE

	PU by internal	PD by external
DFT_GPIO0	Side-Port Memory Disable	Side-Port Memory Enable (Default)
DFT_GPIO1	Bypassing EEPROM, use Default values	Using EEPROM Strapping
DFT_GPIO(4:2)	Set PCI-E GPP mode to Conf. E	Select PCI-E GPP mode
DFT_GPIO5	Use default values	Use the memory data bus for debug bus output





NB RS690T POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

QUANTA COMPUTER

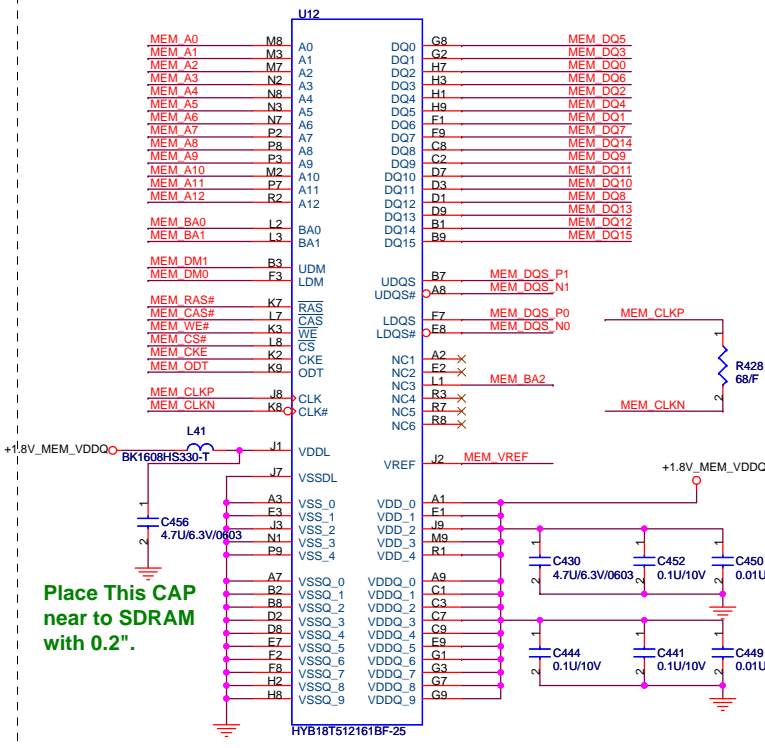
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Size: Document Number FX5

Date: Friday, May 04, 2007

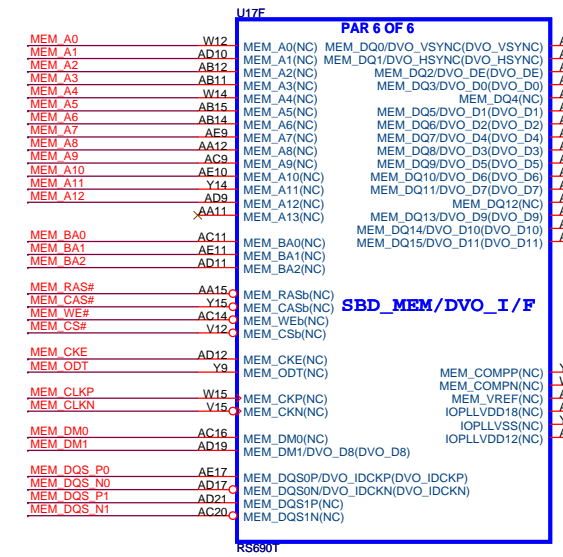
Sheet 12 of 61

Rev 1A

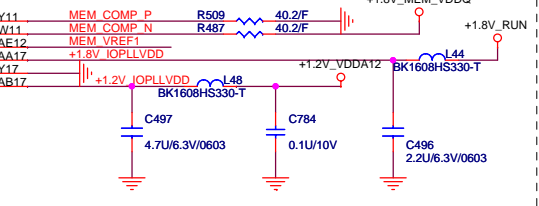


Place This CAP near to SDRAM with 0.2".

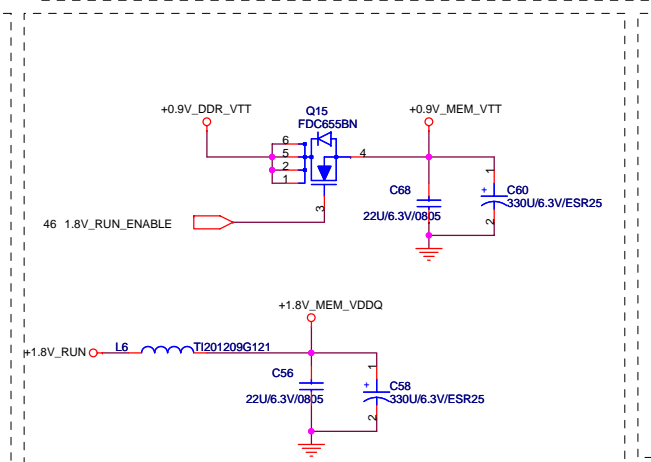
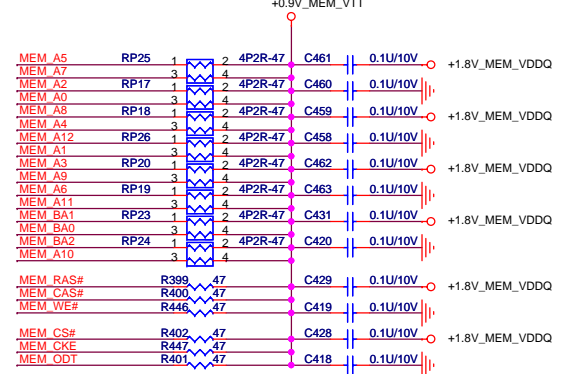
Place Those CAP near to SDRAM with 0.2".
512-Mbit DDR2 8Mbit*16*4bank



MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other signals in X,Y,Z directions



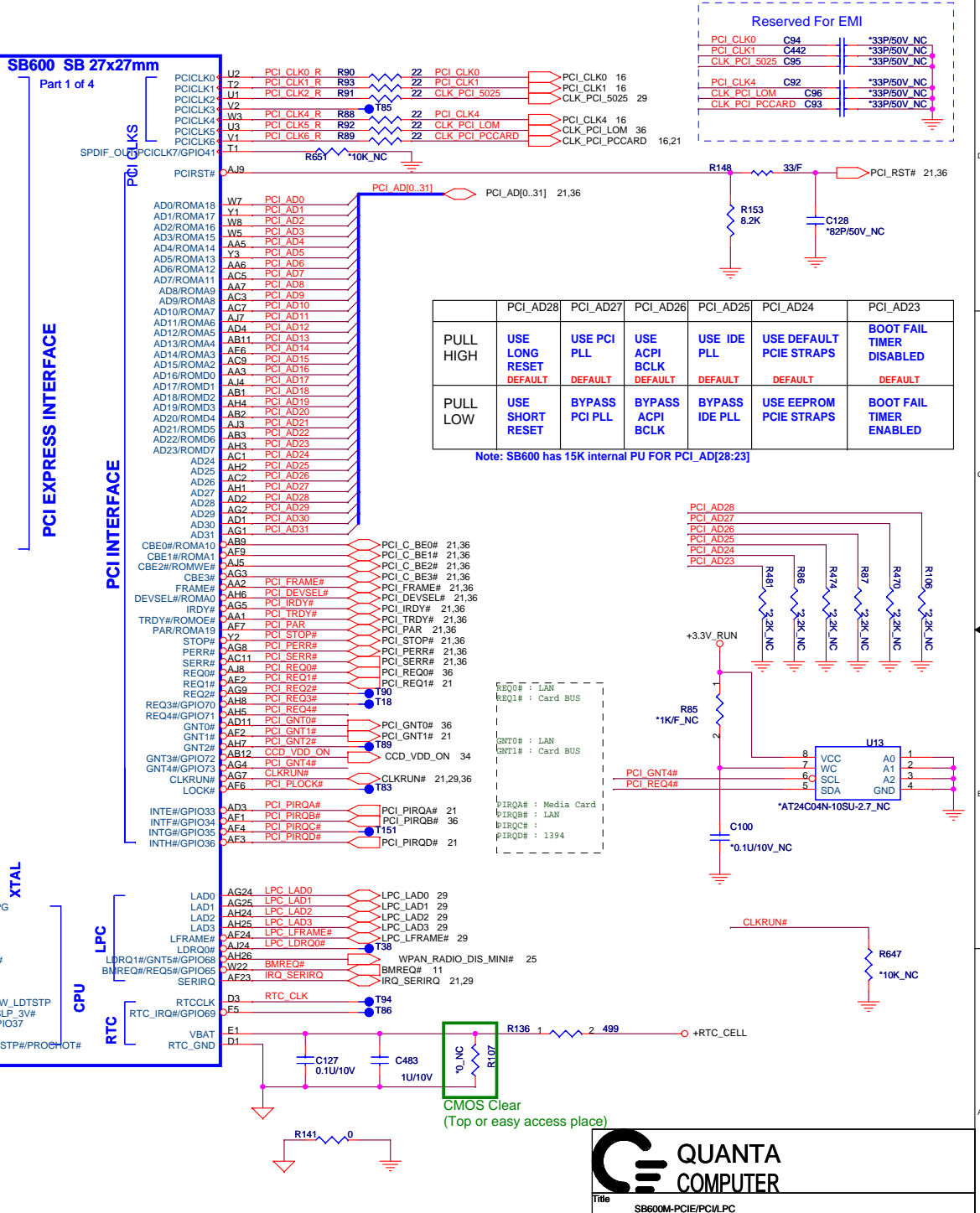
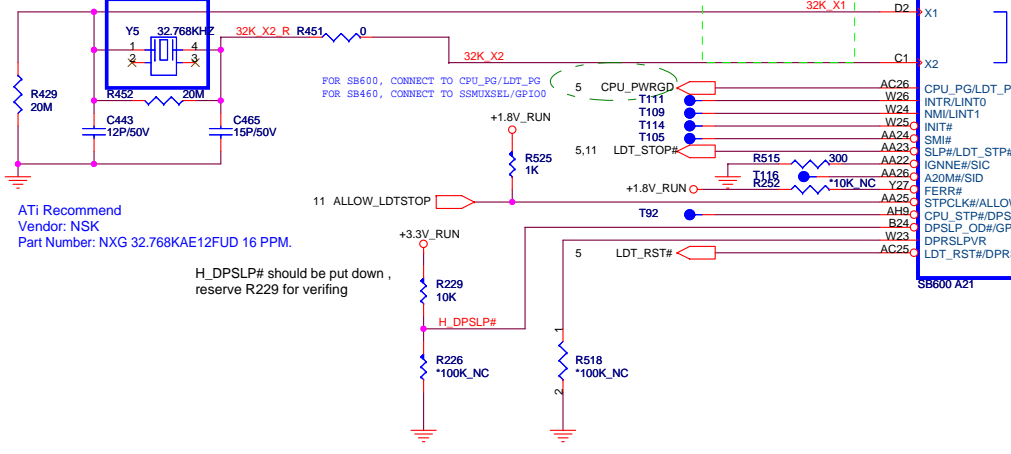
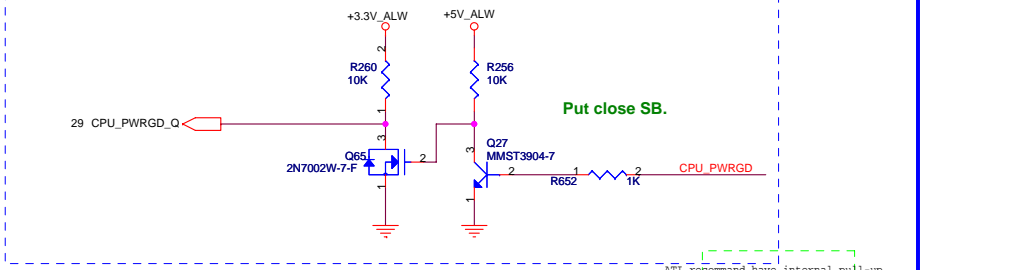
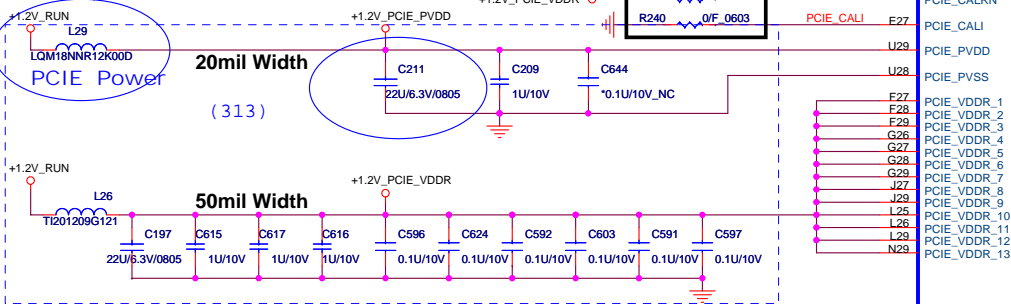
At least 200mils wide and locate after DDR2 SDRAM



Local Frame Buffer(64MB) DDRII Power



SB CALIBRATION RESISTOR VALUE		
BALL	SB600	SB460
CALRP	562 OHM 1%	150 OHM 1%
CALRN	2.05K 1%	150 OHM 1%
CALI	0 ohm	4.12K 1%



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOT FAIL TIMER DISABLED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLED

Note: SB600 has 15K internal PU FOR PCI_AD[28:23]

QUANTA COMPUTER

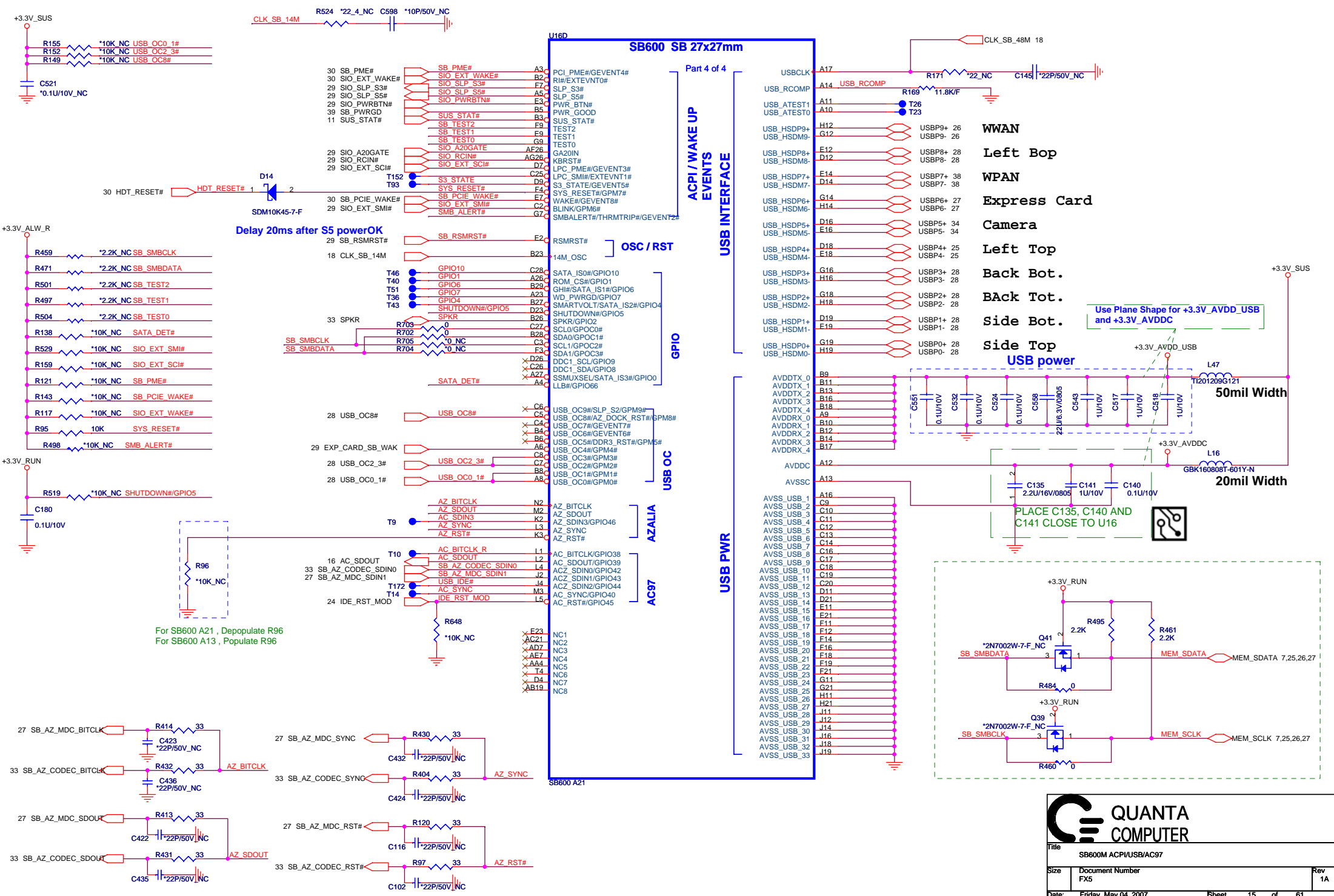
Title: SB600M-PCIE/PCI/LPC

Size: Document Number FX5

Date: Friday, May 04, 2007

Sheet 14 of 61

Rev 1A




For SB600 A21 , Depopulate R96
For SB600 A13 , Populate R96

Use Plane Shape for +3.3V_AVDD_USB
and +3.3V_AVDDC

50mil Width

20mil Width

PLACE C135, C140 AND
C141 CLOSE TO U16



**QUANTA
COMPUTER**

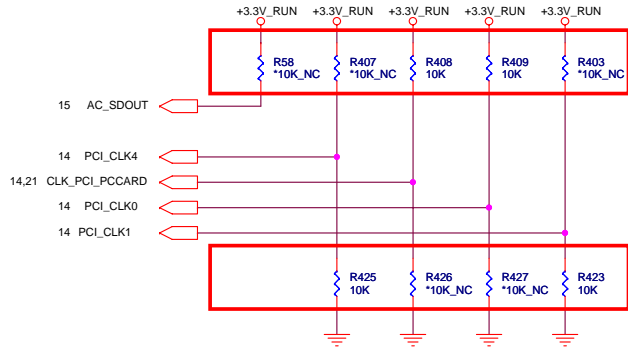
Title: SB600M ACPI/USB/AC97

Size	Document Number	Rev
	FX5	1A

Date: Friday, May 04, 2007 Sheet 15 of 61

15K internal PU for RTC_CLK
 ,External PU/PD is not required.
 SB600 has 15K internal PD for AC_SDOU1

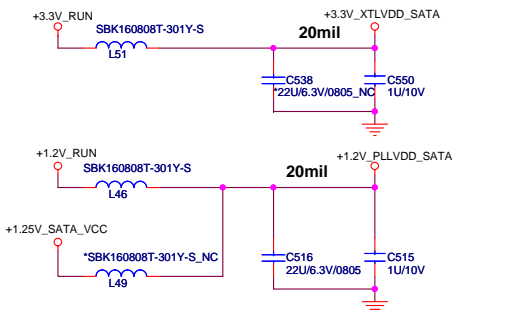
REQUIRED STRAPS



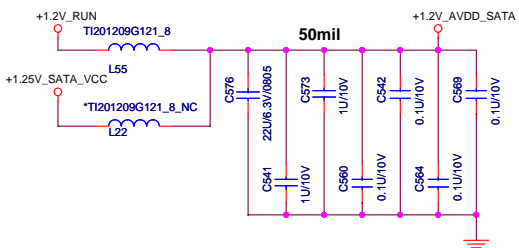
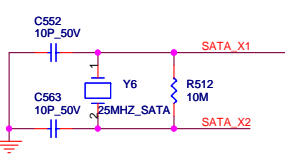
CLK_PCI_PCCARD

CLK_PCI_PCCARD					
	AC_SDOU	RTC_CLK	PCI_CLK4	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8 H, H = PCI ROM H, L = SPI ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	L, H = LPC ROM L, L = FWH ROM	DEFAULT

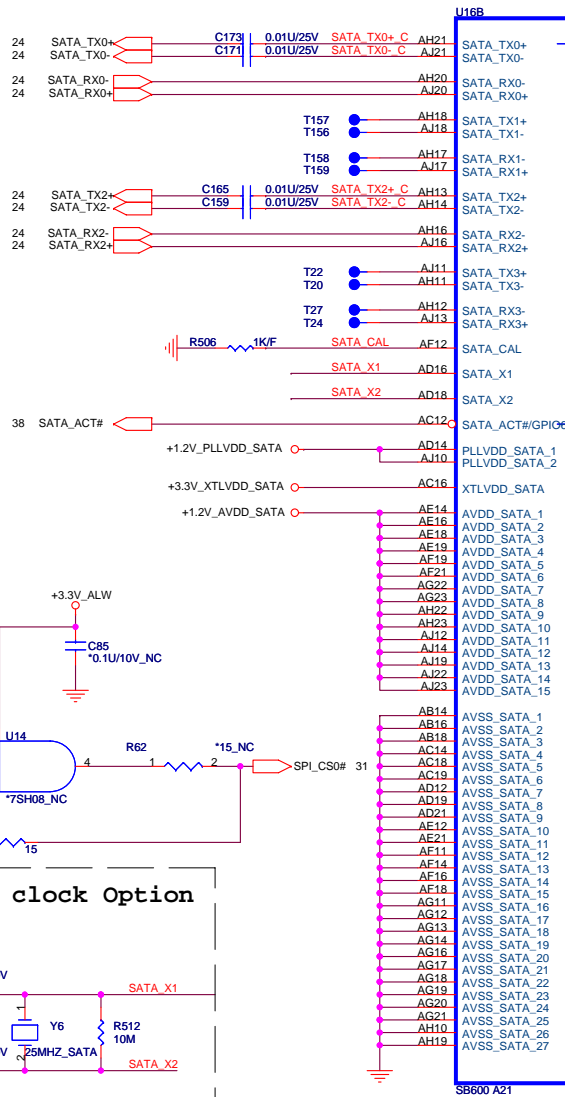
SATA Power



SATA clock Option



For SATA issue where the interface is being dropped down to PIO mode when SATA is used in an IDE configuration. Will fix for this issue implemented in A21.



SERIAL ATA

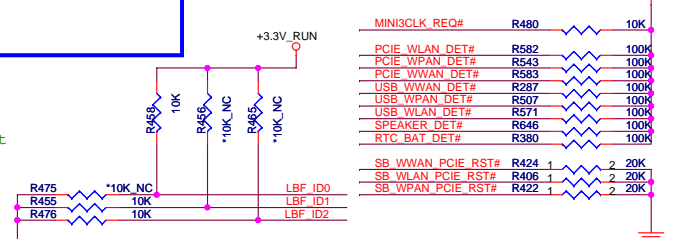
SERIAL ATA POWER

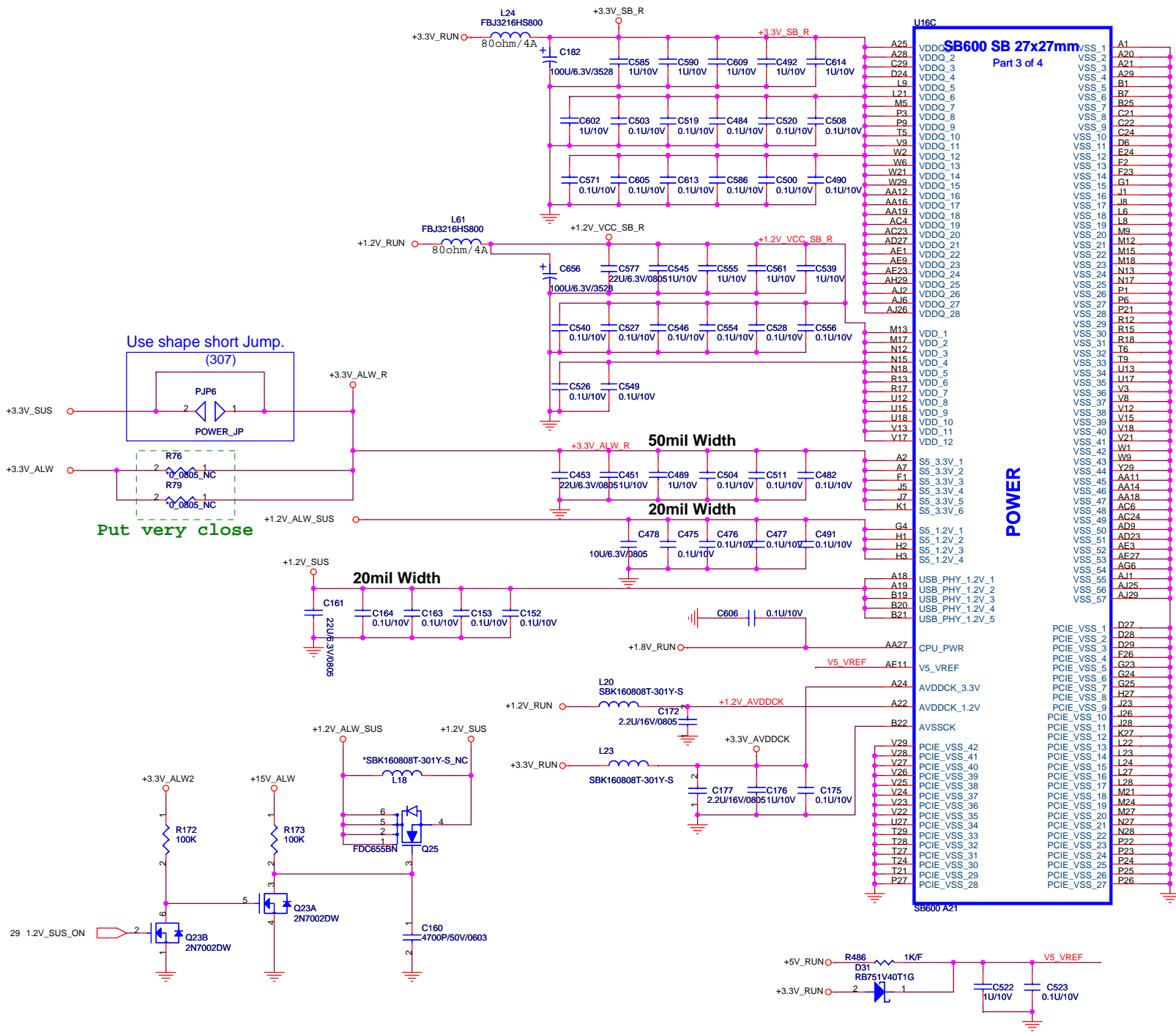
SPI ROM

HW MONITOR

Local Frame Buffer Strapping List

	LBF_ID2	LBF_ID1	LBF_ID0
Hyanix	0 R476	0 R455	0 R475
Qimonda	0 R476	0 R455	1 R458
Samsung	0 R476	1 R456	0 R475

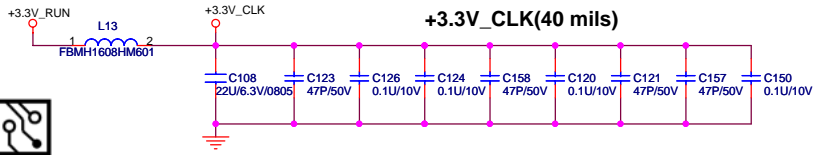




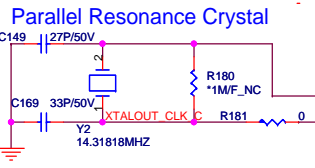
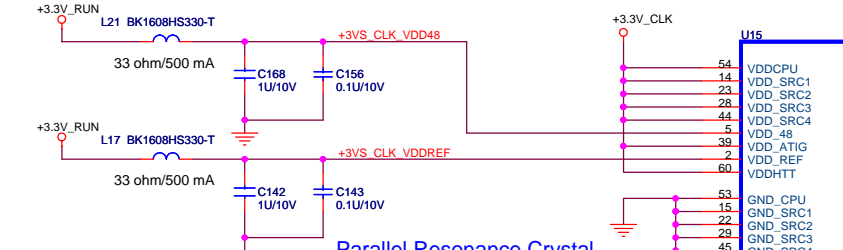
QUANTA COMPUTER

File: SB600M STRAPS

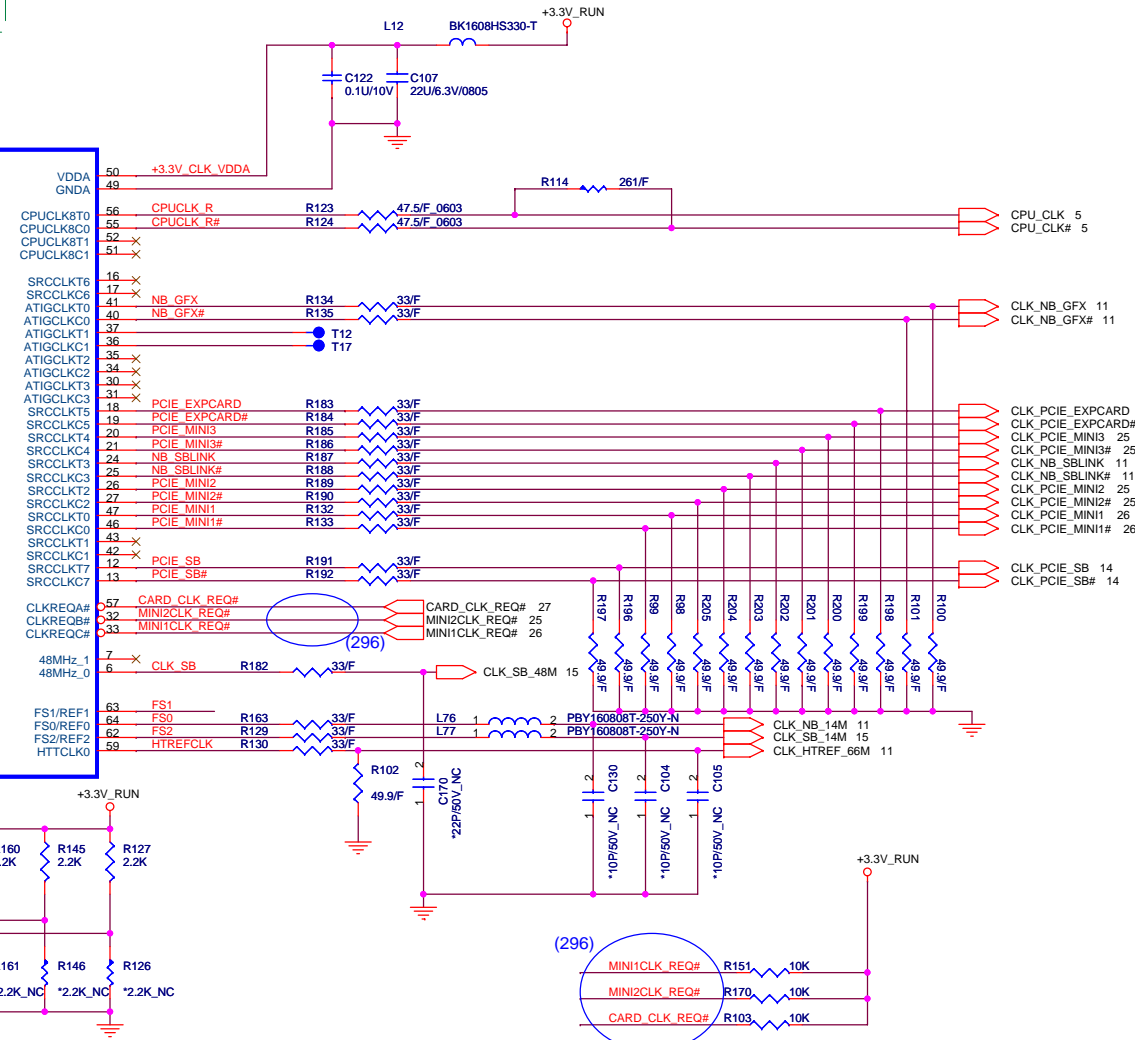
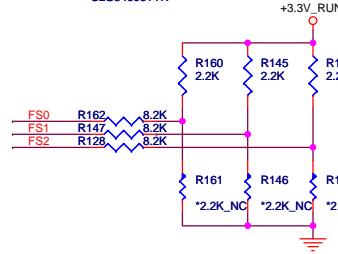
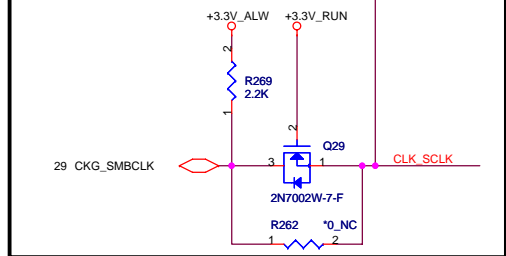
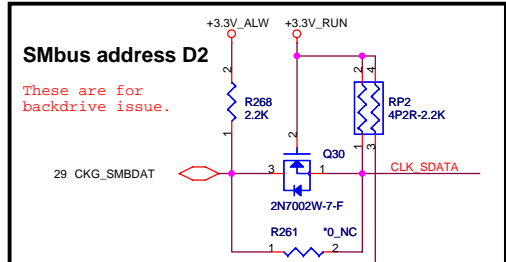
Size	Document Number FX5	Rev 1A
Date:	Friday, May 04, 2007	Sheet 17 of 61



- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U15
- 2- PUT DECOUPLING CAPS CLOSE TO Clock Gen. POWER PIN



$I_{oh} = 5 * I_{ref}$
 (2.32mA)
 $V_{oh} = 0.71V @ 60\ ohm$
 Place R131 less than 100mils from Clock Gen.



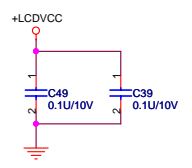
EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

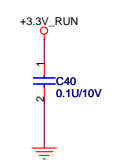
CLKREQA# CONTROL SRC5
 CLKREQB# CONTROL SRC2
 CLKREQC# CONTROL SRC0

Check AMD clock

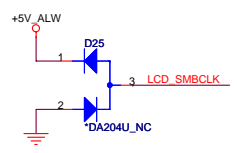




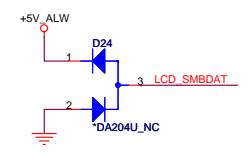
Close Connectot.



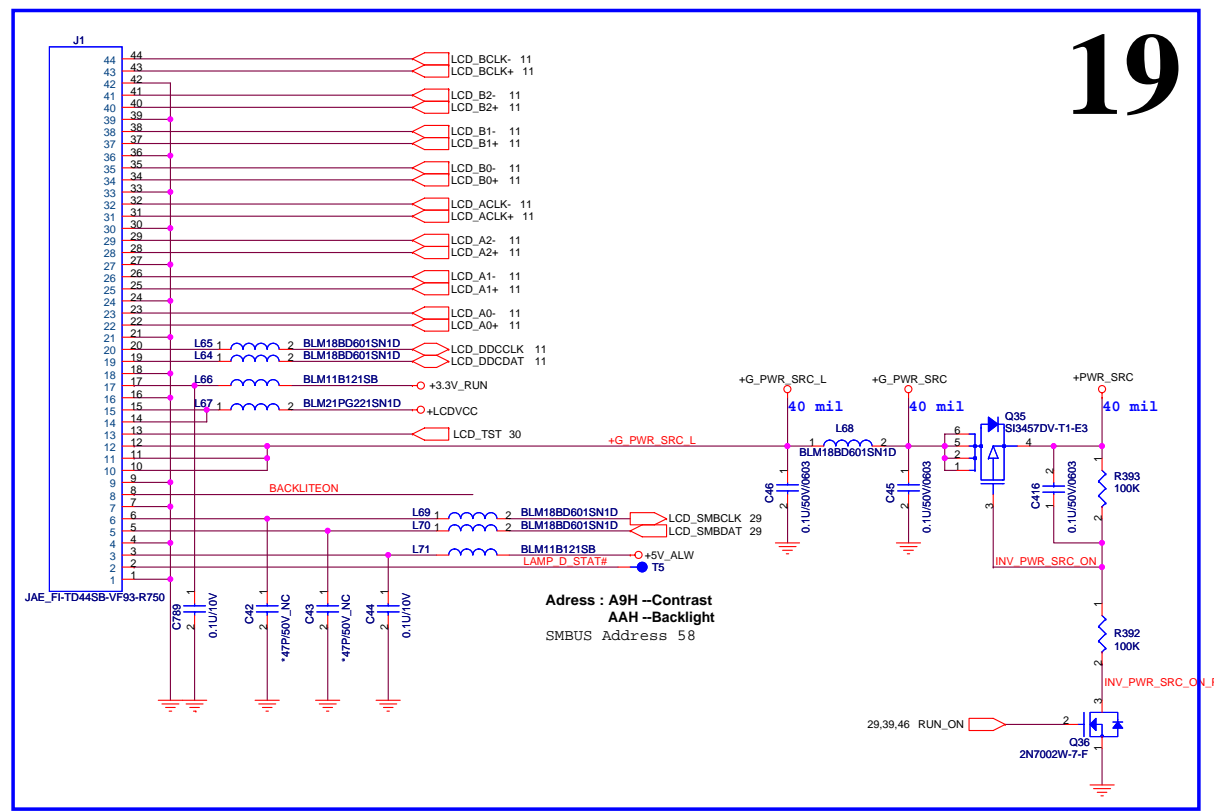
Close Connectot.



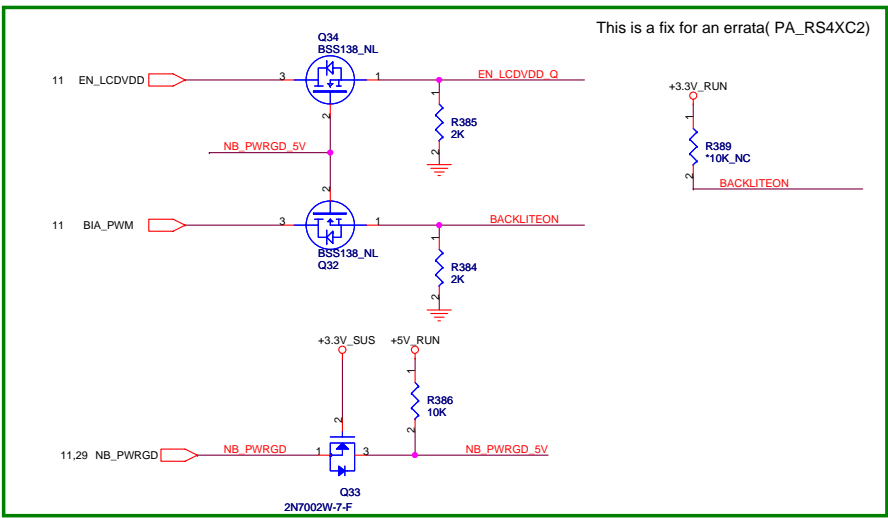
Close Connectot.



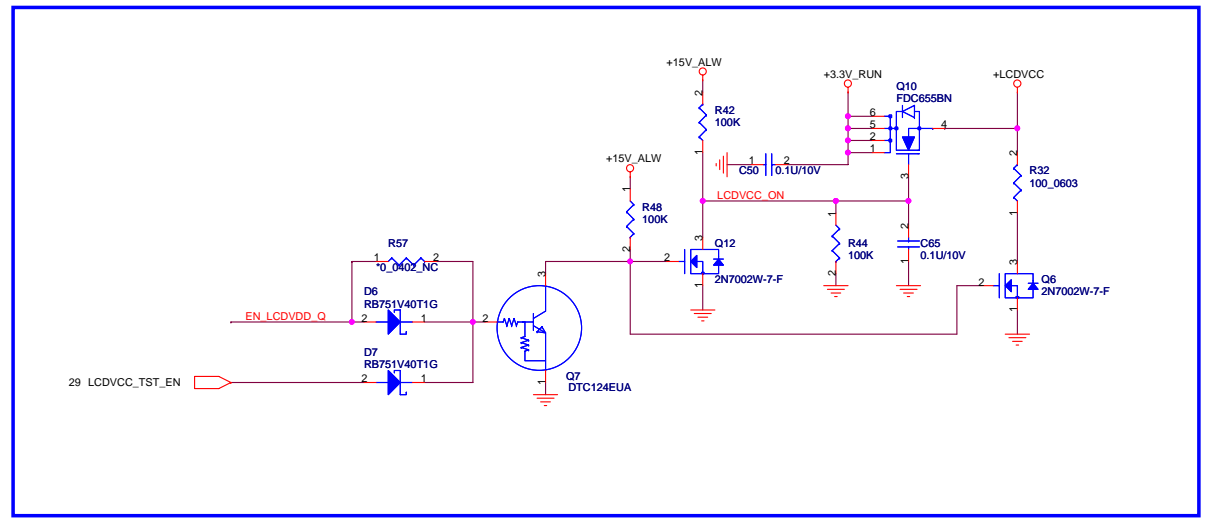
Close Connectot.

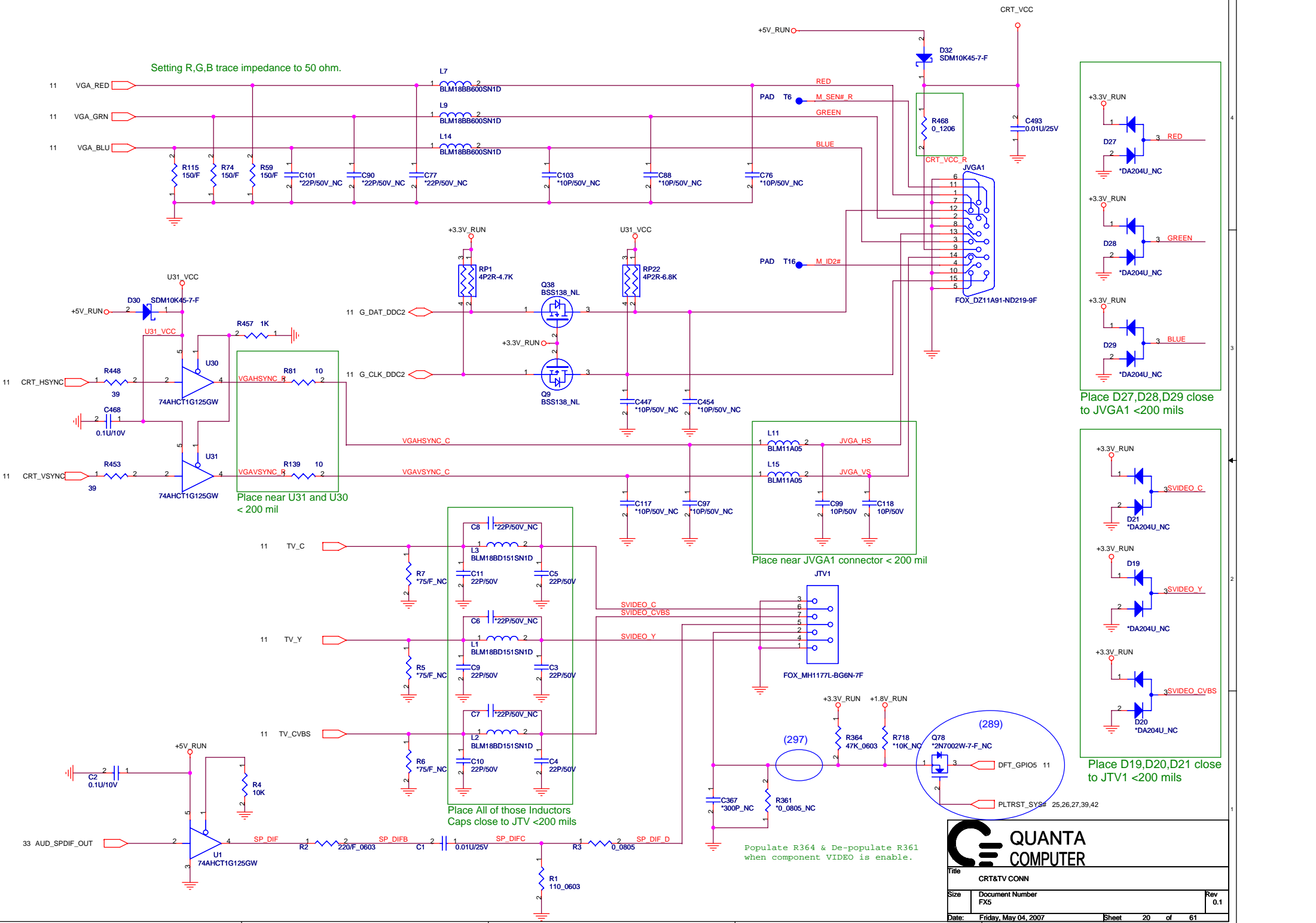


Address : A9H --Contrast
AAH --Backlight
SMBUS Address 58



This is a fix for an errata(PA_RS4XC2)





Setting R,G,B trace impedance to 50 ohm.

Place near U31 and U30 < 200 mil

Place All of those Inductors Caps close to JTV <200 mils

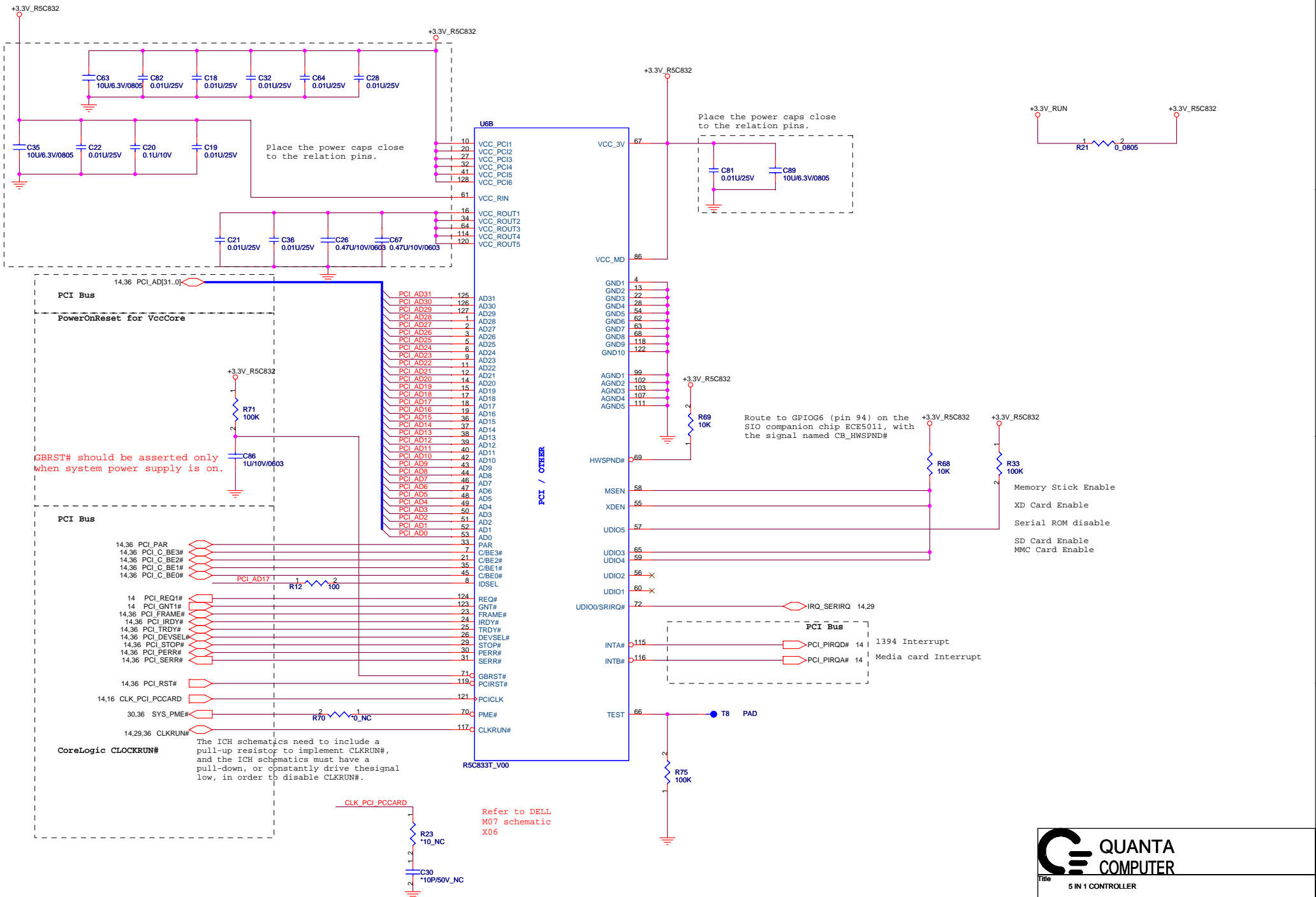
Place D27,D28,D29 close to JVGA1 <200 mils

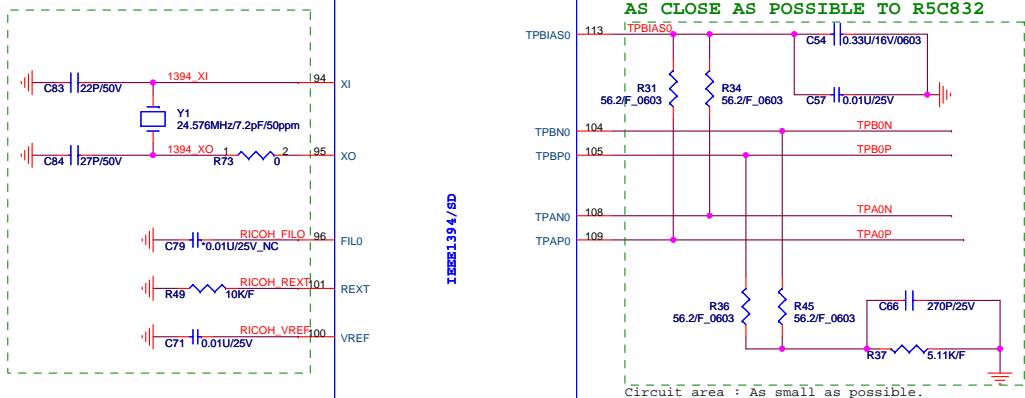
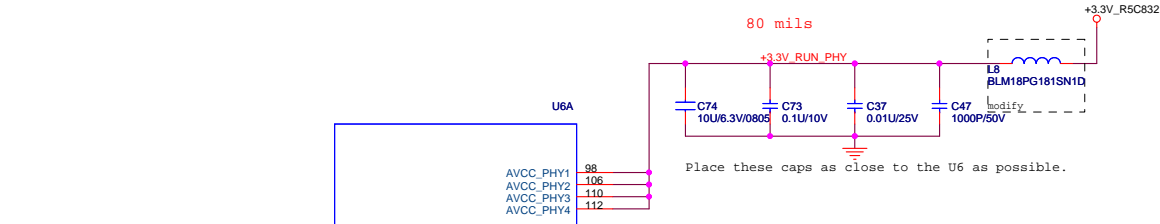
Place D19,D20,D21 close to JTV1 <200 mils

Populate R364 & De-populate R361 when component VIDEO is enable.

QUANTA COMPUTER

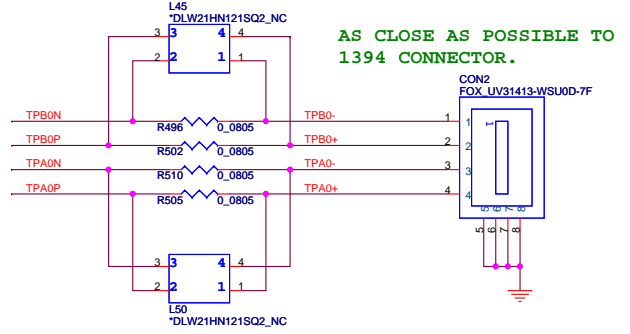
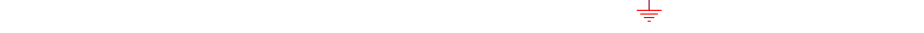
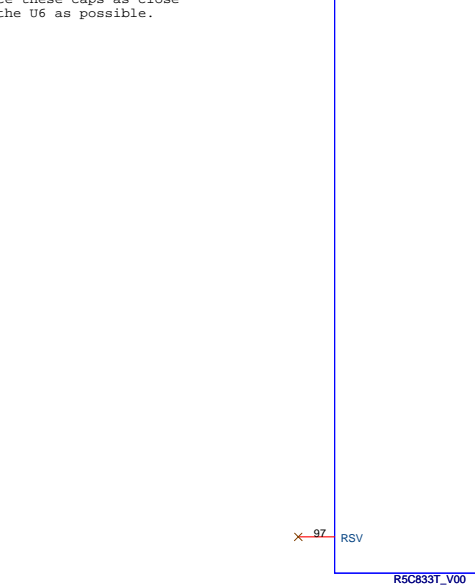
Title		CRT&TV CONN
Size	Document Number	Rev
FX5		0.1
Date:	Friday, May 04, 2007	Sheet 20 of 61

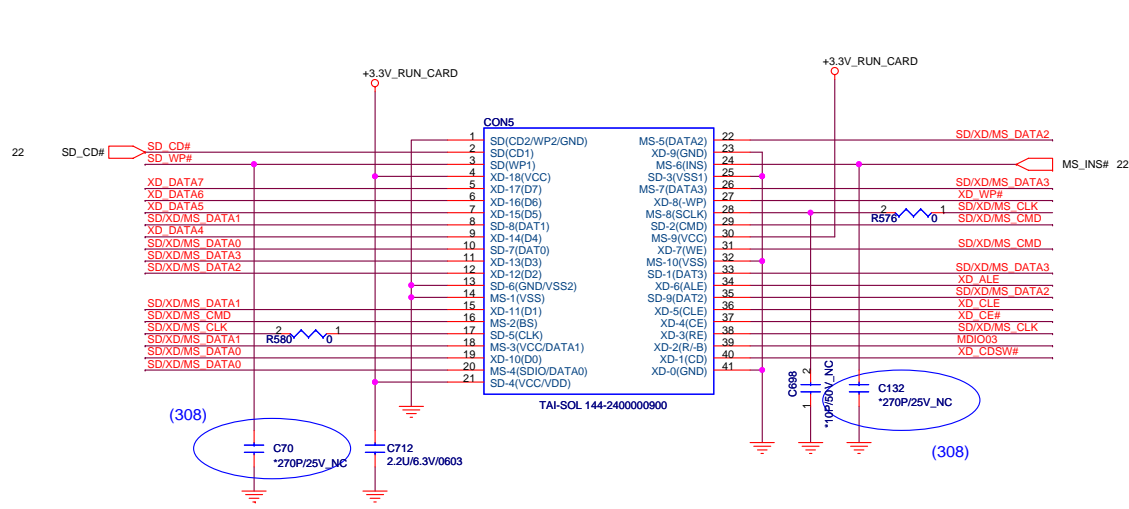




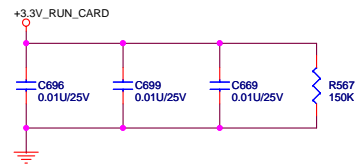
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
 *TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
 *Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

Place these caps as close to the U6 as possible.

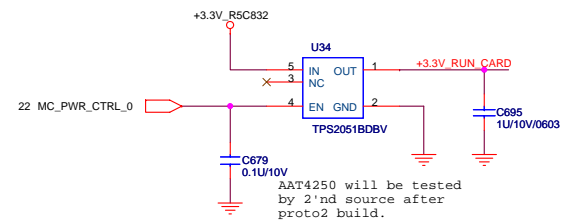
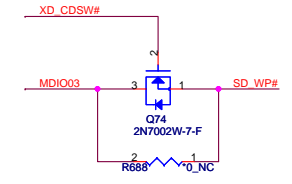




8 IN1 CARD READER

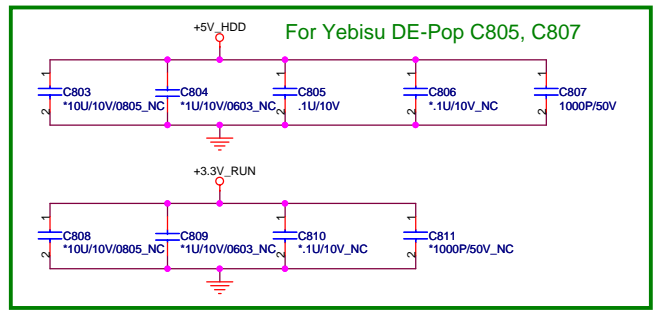
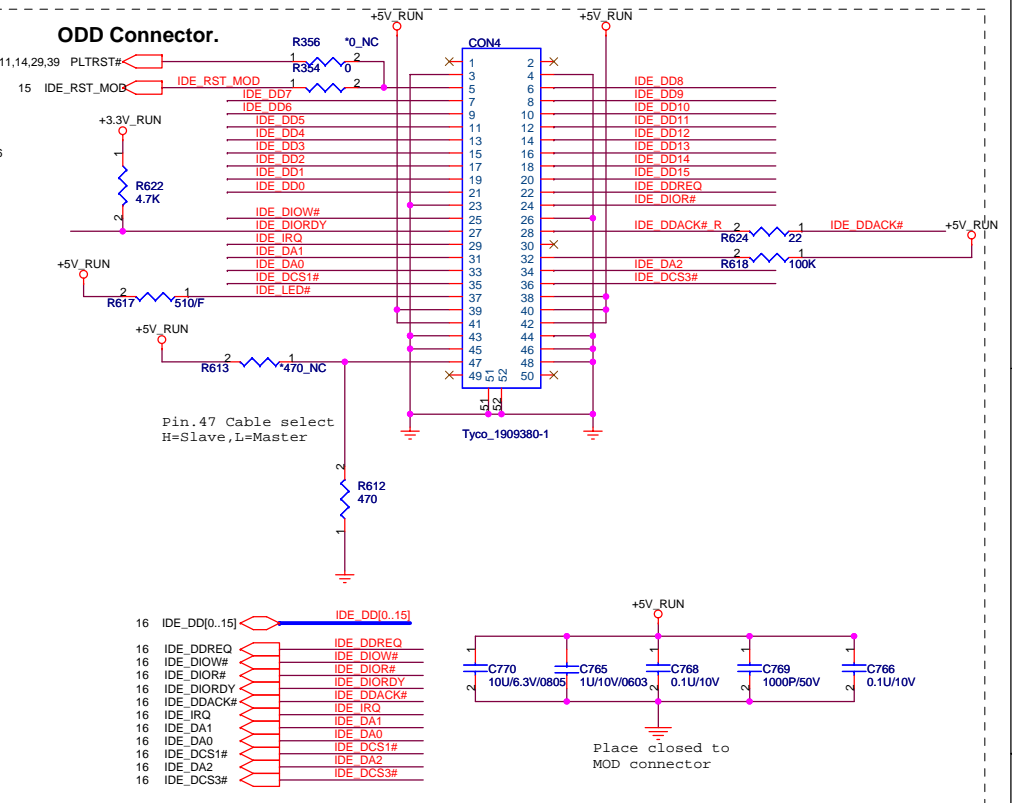
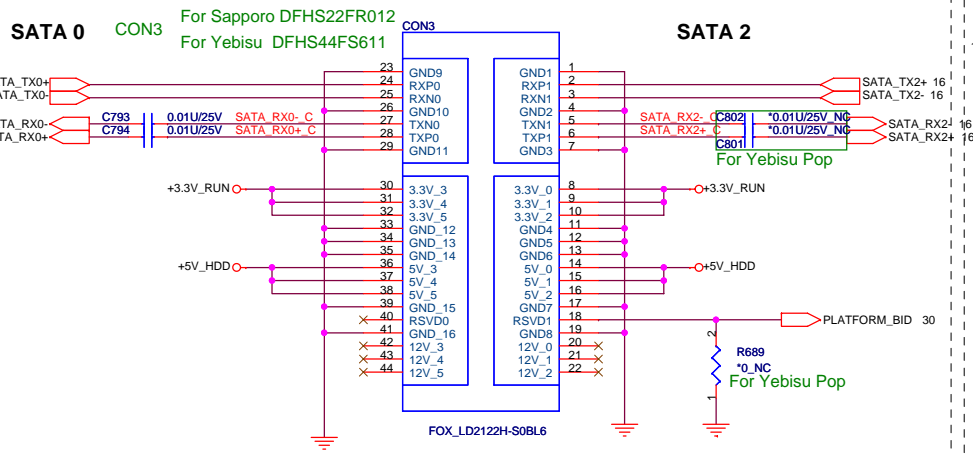


- 22 XD_CDSW#
- 22 MDIO03
- 22 XD_DATA7
- 22 XD_DATA6
- 22 XD_DATA5
- 22 XD_DATA4
- 22 SD_XD/MS_DATA3
- 22 SD_XD/MS_DATA2
- 22 SD_XD/MS_DATA1
- 22 SD_XD/MS_DATA0
- 22 SD_XD/MS_CMD
- 22 XD_WP#
- 22 XD_ALE
- 22 XD_CLE
- 22 XD_CE#
- 22 SD_XD/MS_CLK

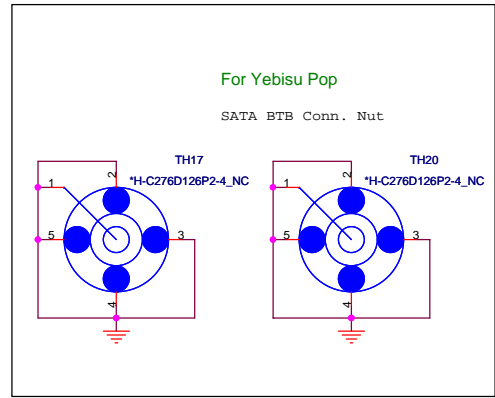
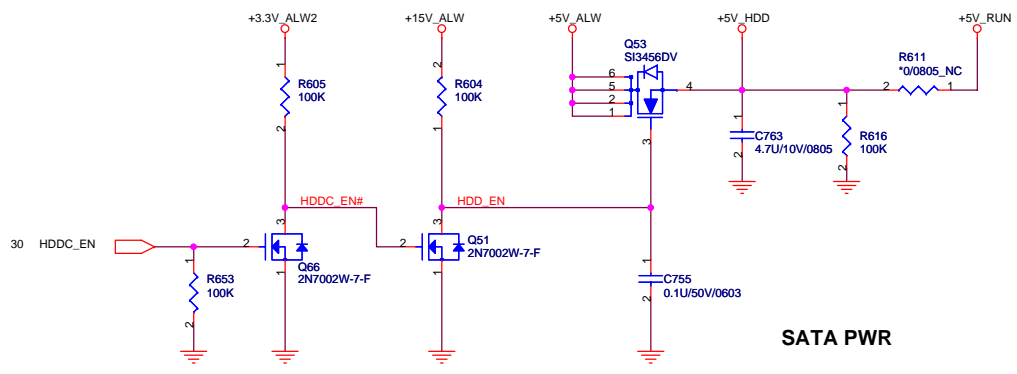


QUANTA
COMPUTER

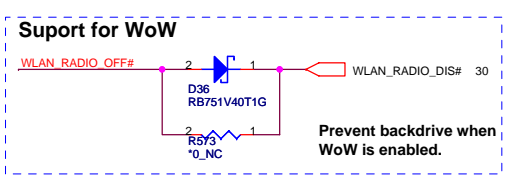
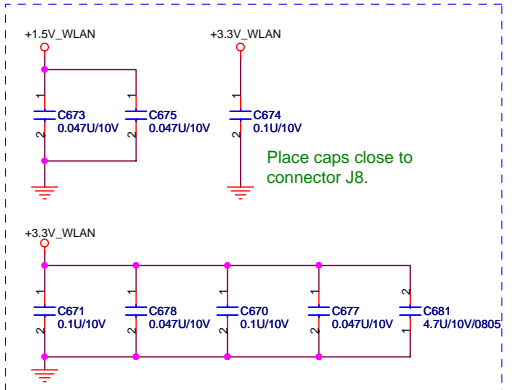
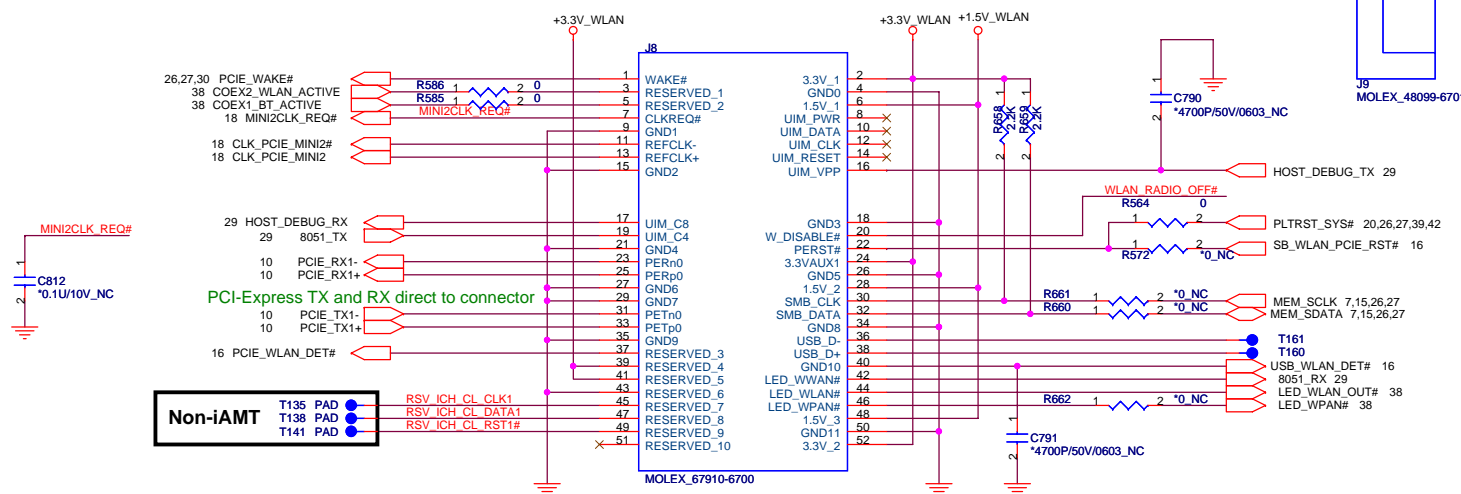
Title CARD READER CONN		
Size	Document Number FX5	Rev 0.1
Date:	Friday, May 04, 2007	Sheet 23 of 61



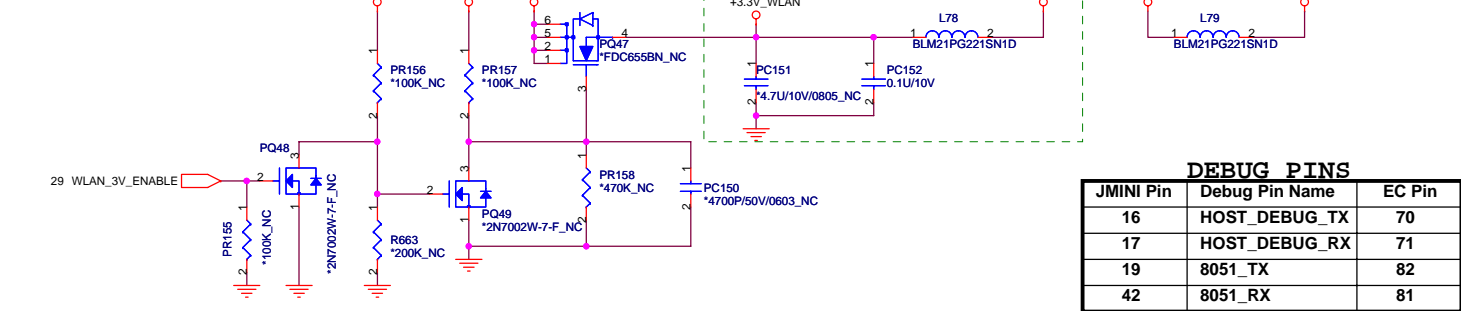
	FX5 (Sapporo)	GX2 (Yebisu)
R689	X	V
C801	X	V
C802	X	V
C805	V	X
C807	V	X



MiniCard WLAN connector

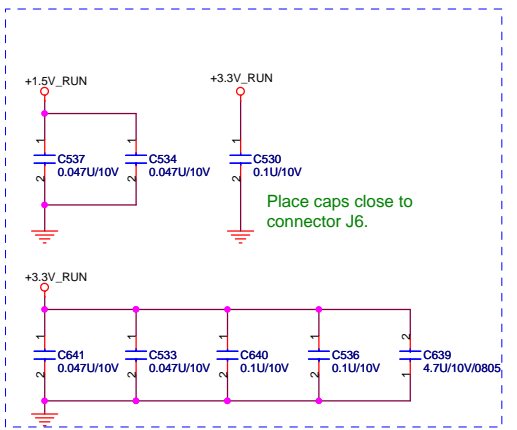


WLAN Power Switch

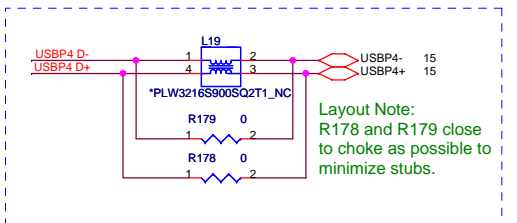
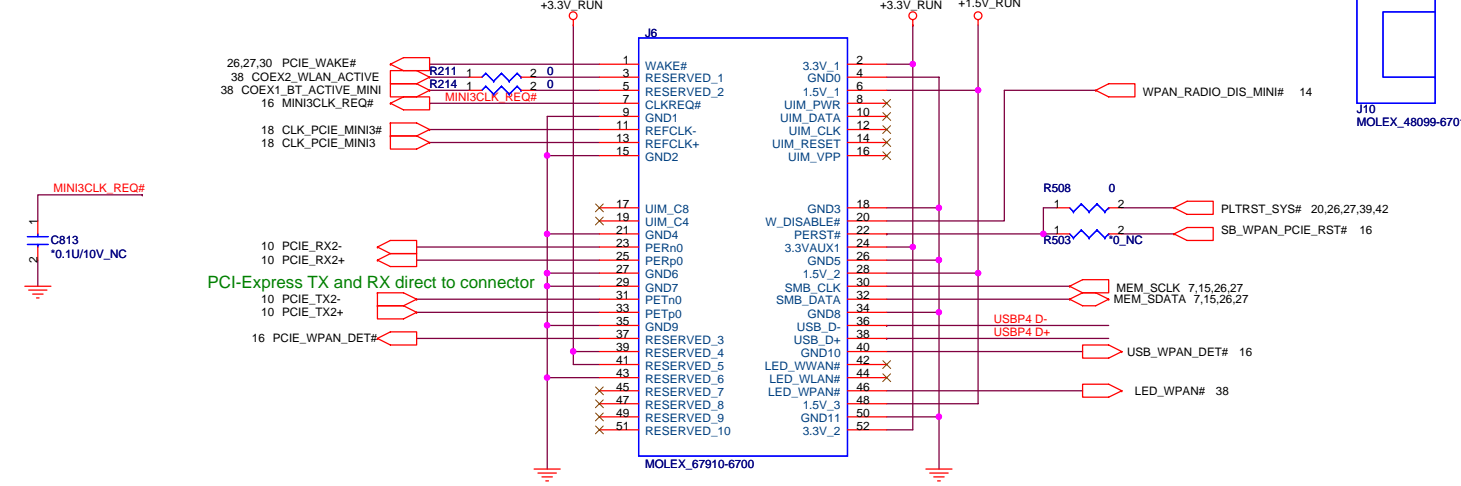


DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

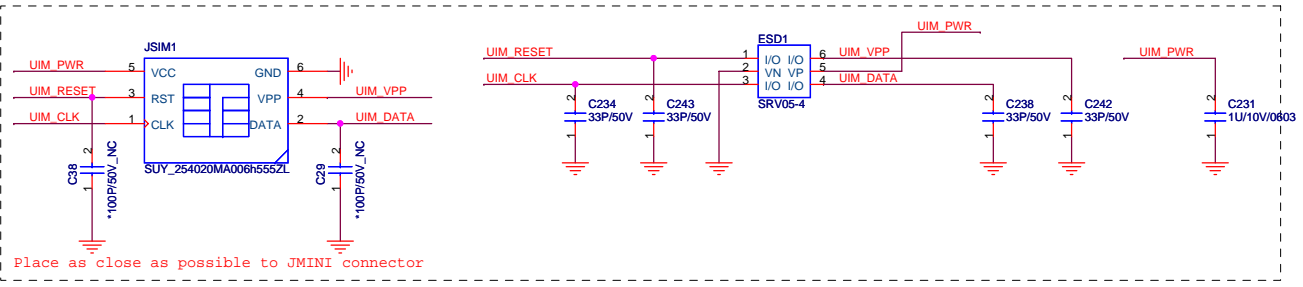
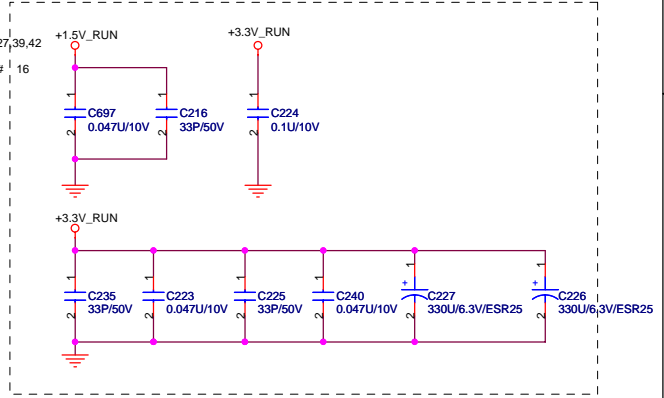
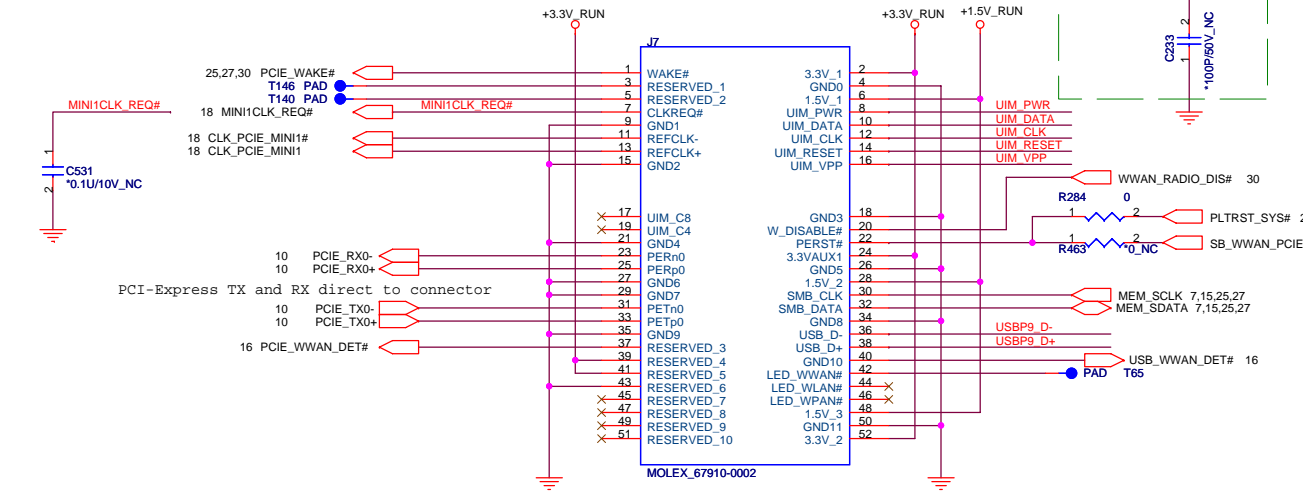
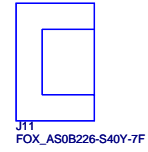


MiniCard WPAN connector



MiniCard WWAN connector

Need to close to WWAN MINI Card (J7) pin 12.



Place as close as possible to JMINI connector

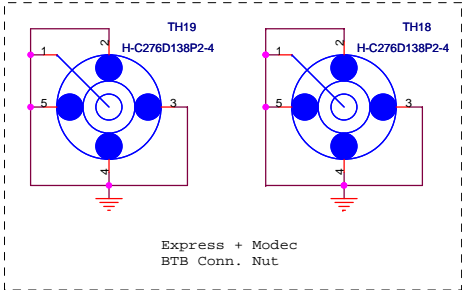
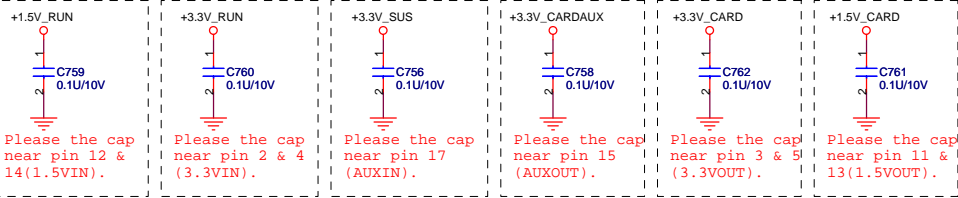
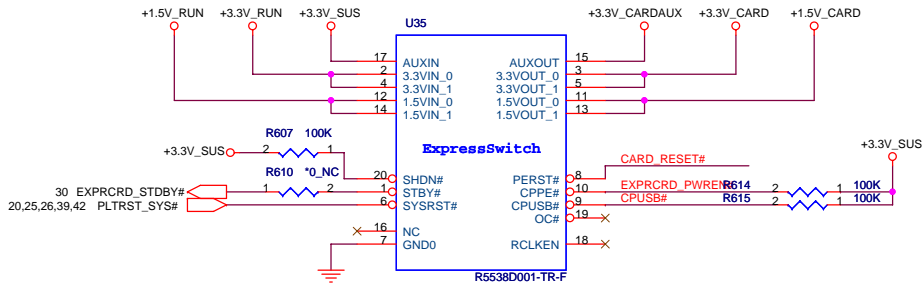
Layout Note:
R282 and R283
close to choke
as possible to
minimize stubs.



Title WWAN		
Size FX5	Document Number	Rev 0.1
Date: Friday, May 04, 2007	Sheet 26	of 61

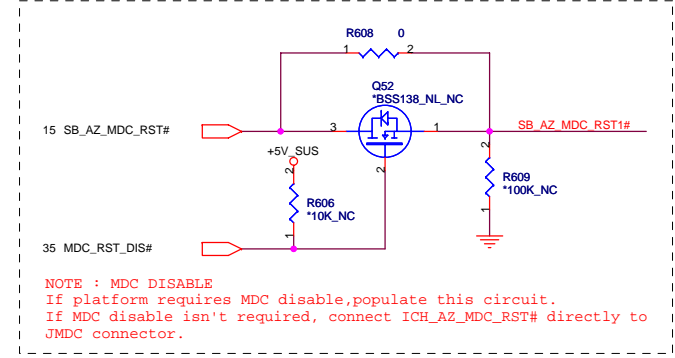
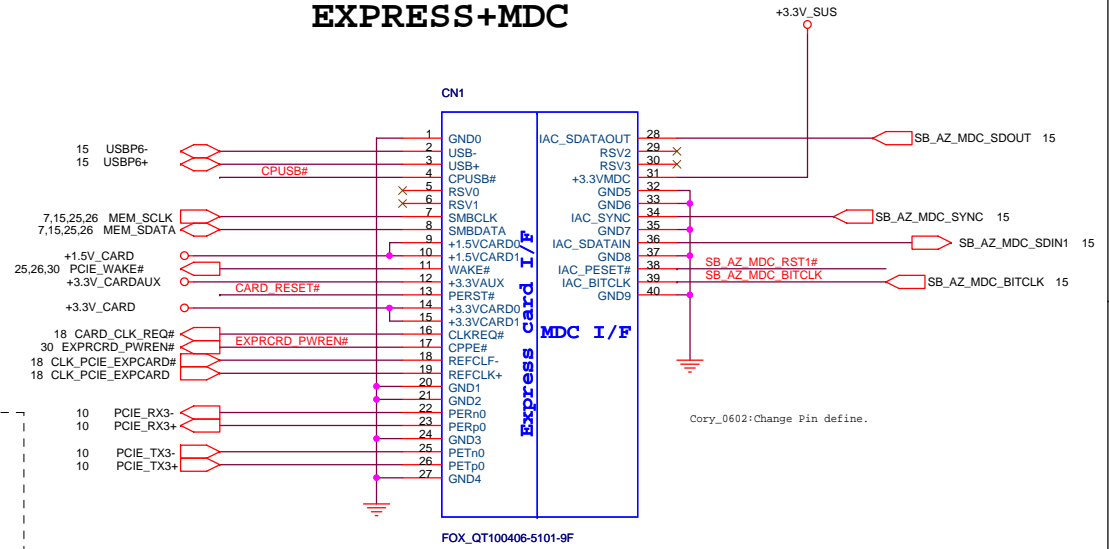
Express Card Power Switch

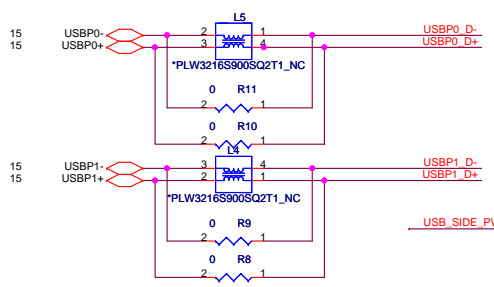
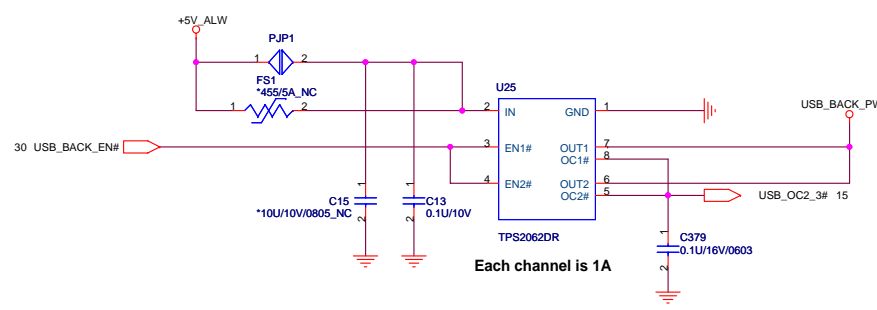
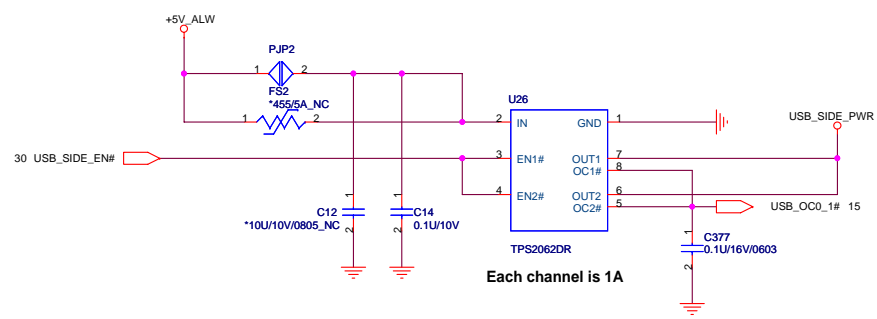
+1.5V_CARD Max. 650mA, Average 500mA.
 +3V_CARD Max. 1300mA, Average 1000mA.



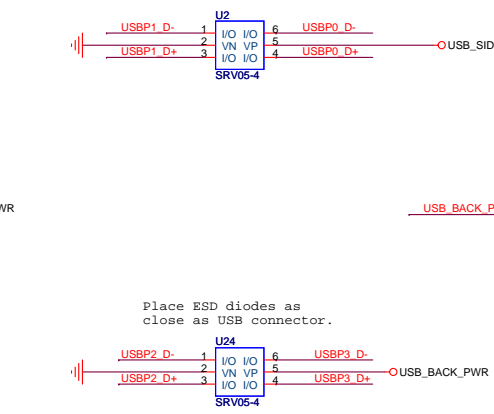
PCI-Express TX and RX direct to connector.

EXPRESS+MDC



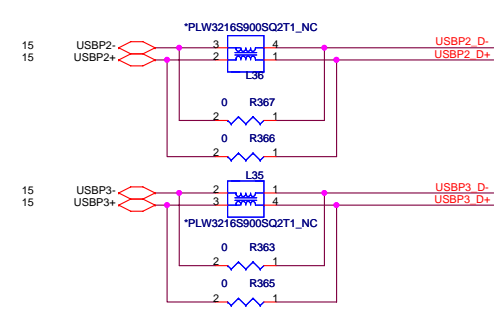
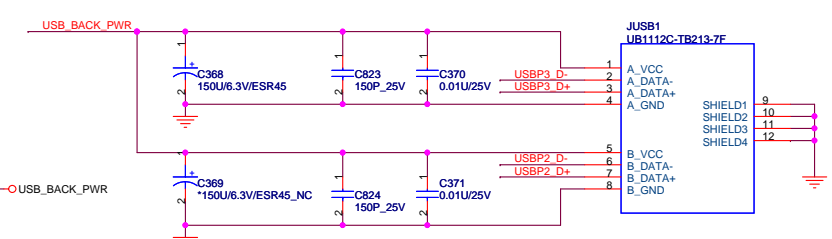
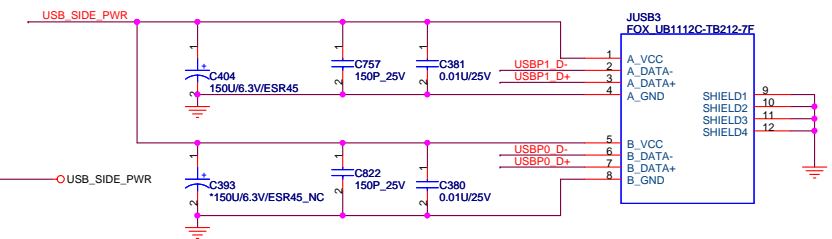


Place ESD diodes as close as possible to USB connector.

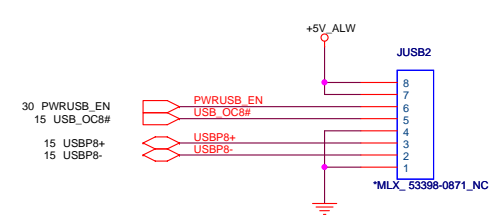


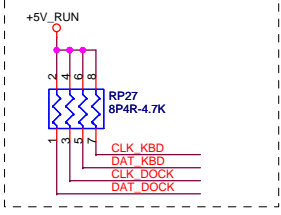
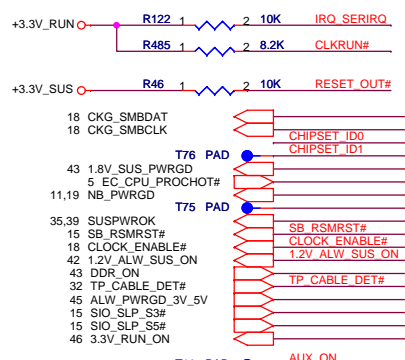
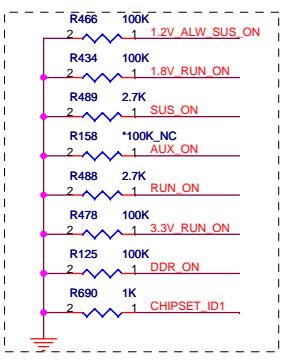
Place ESD diodes as close as possible to USB connector.

Layout Note:
R8,R9,R10 and R11 close to choke as possible to minimize stubs.

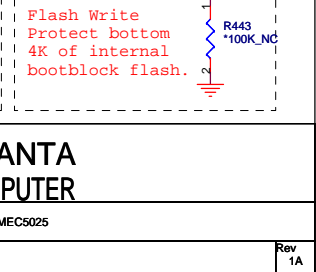
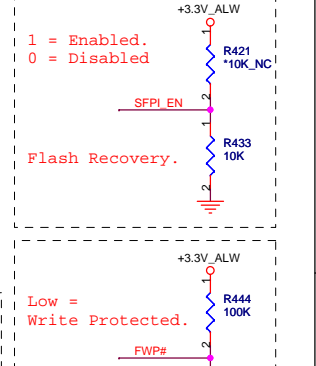
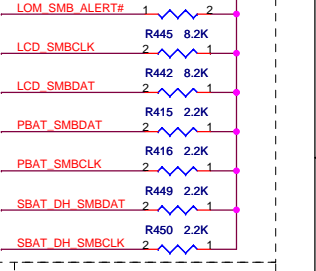
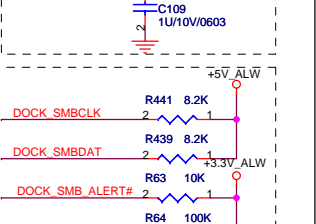
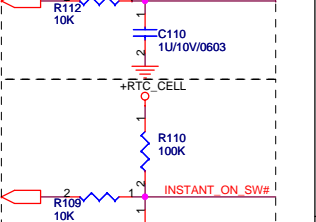
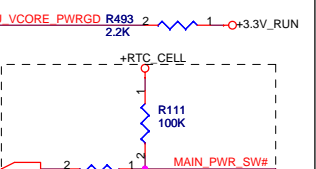
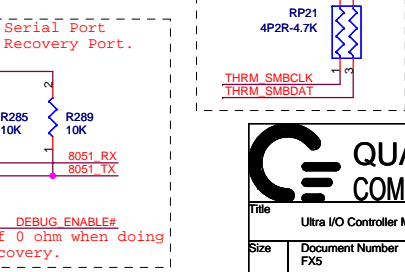
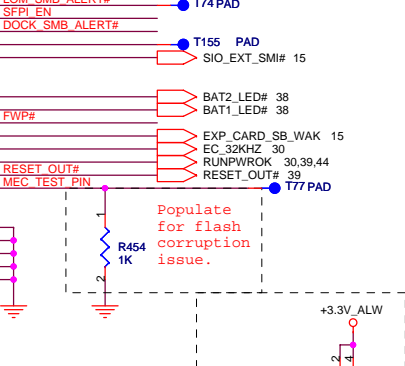
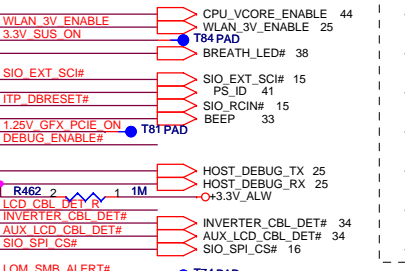
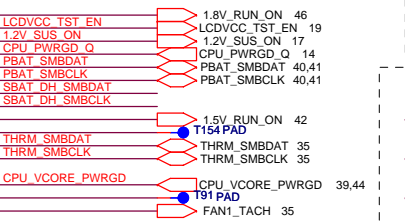
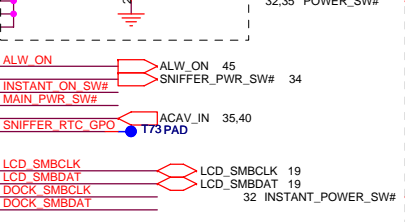
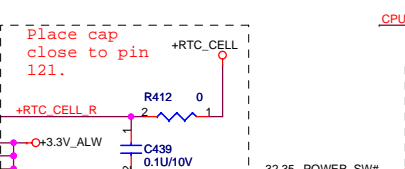
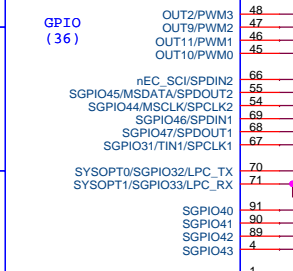
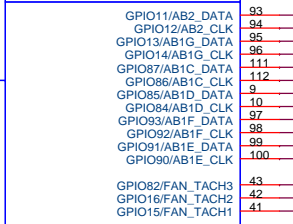
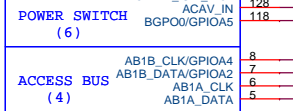
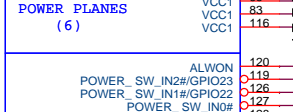
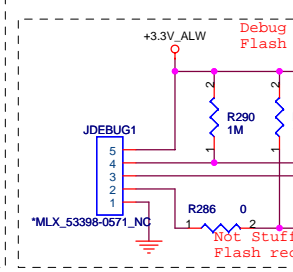
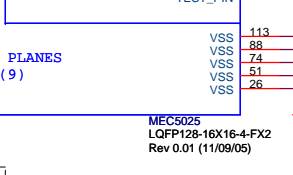
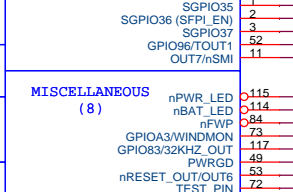
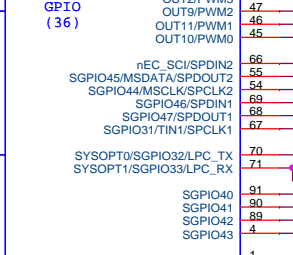
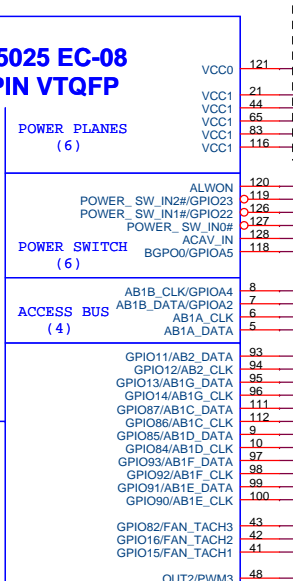
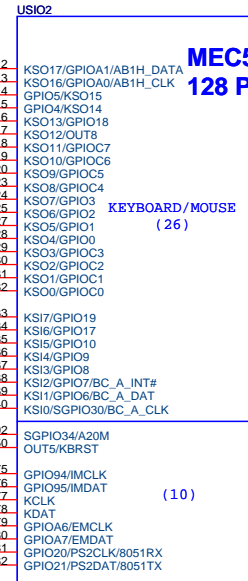
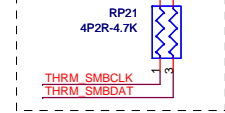
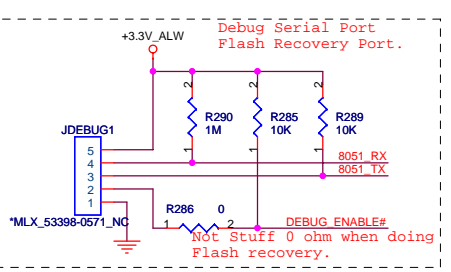
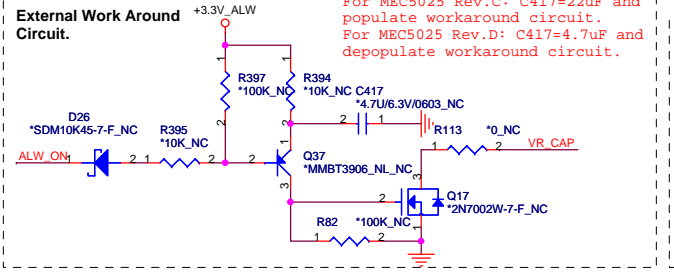
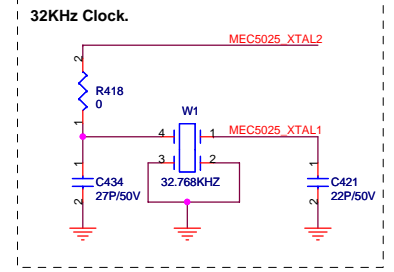
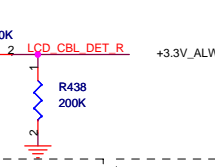
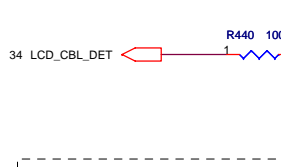
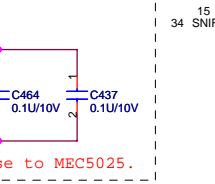
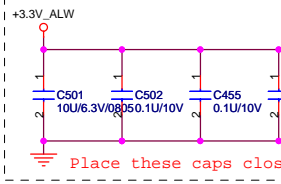
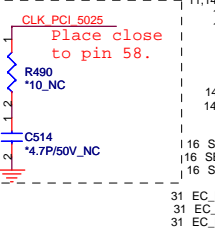
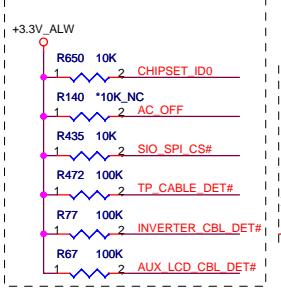


For Yebisu Pop





	GPIO4	GPIO5
Intel	0	0
AMD	0	1
TBD	1	0
Parker	1	1

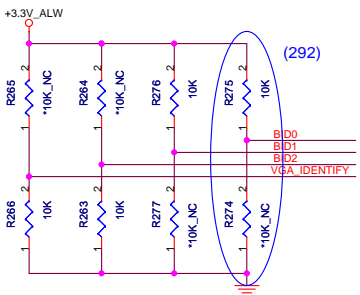
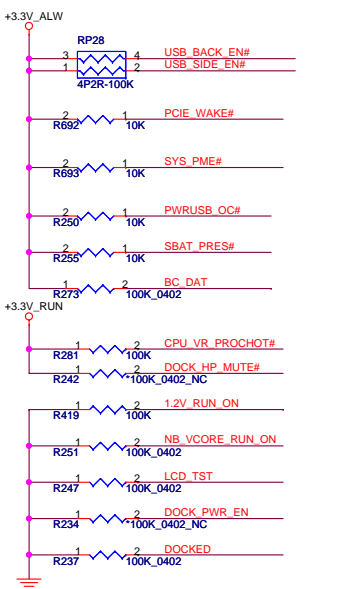


QUANTA COMPUTER

Title: Ultra I/O Controller MEC5025

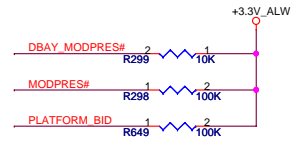
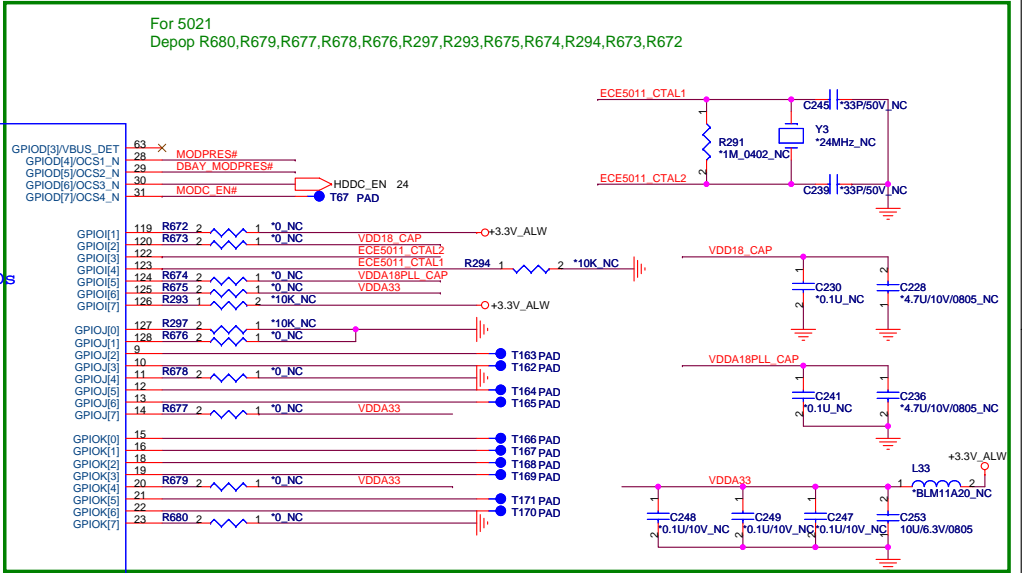
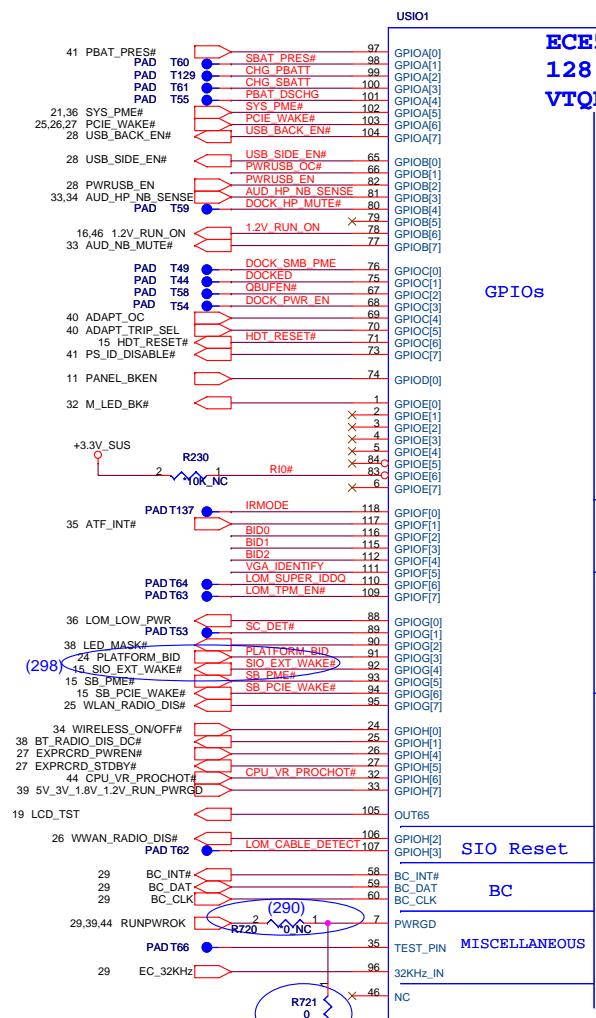
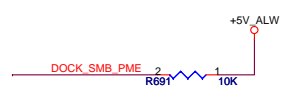
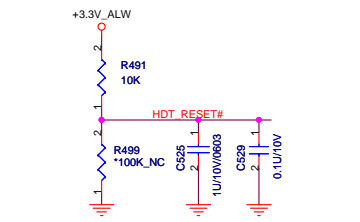
Size	Document Number	Rev
	FX5	1A

Date: Friday, May 04, 2007 Sheet 29 of 61



BID2	BID1	BID0	Board Revision
0	0	0	SST (X00)
0	0	1	PT (X01)
0	1	0	ST (X02)
0	1	1	QT (A00)

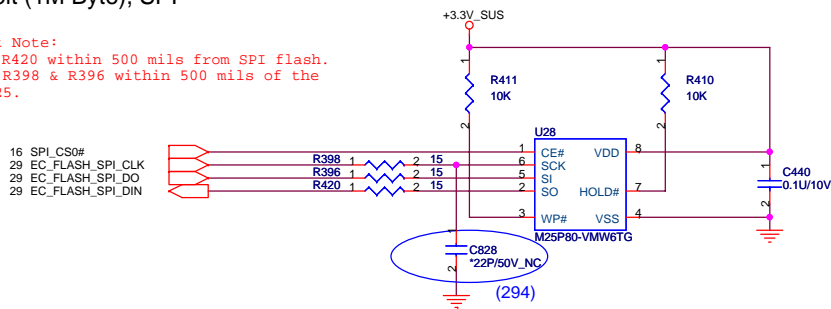
PROCHOT# change to CPU_PROCHOT# per ref schematic.



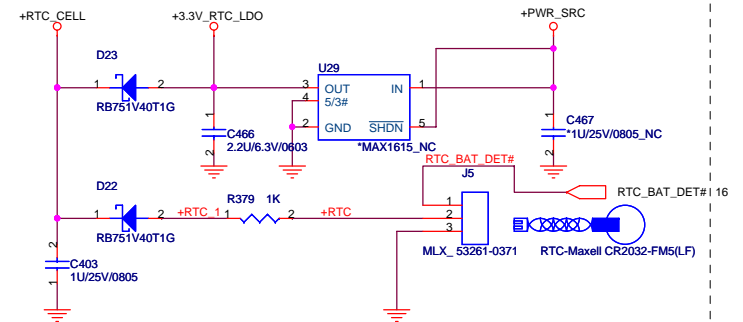
QUANTA COMPUTER
 Title SIO (GPIO/BC/USB/CIRRX)
 Size Document Number FX5 Rev 0.1
 Date: Friday, May 04, 2007 Sheet 30 of 61

8Mbit (1M Byte), SPI

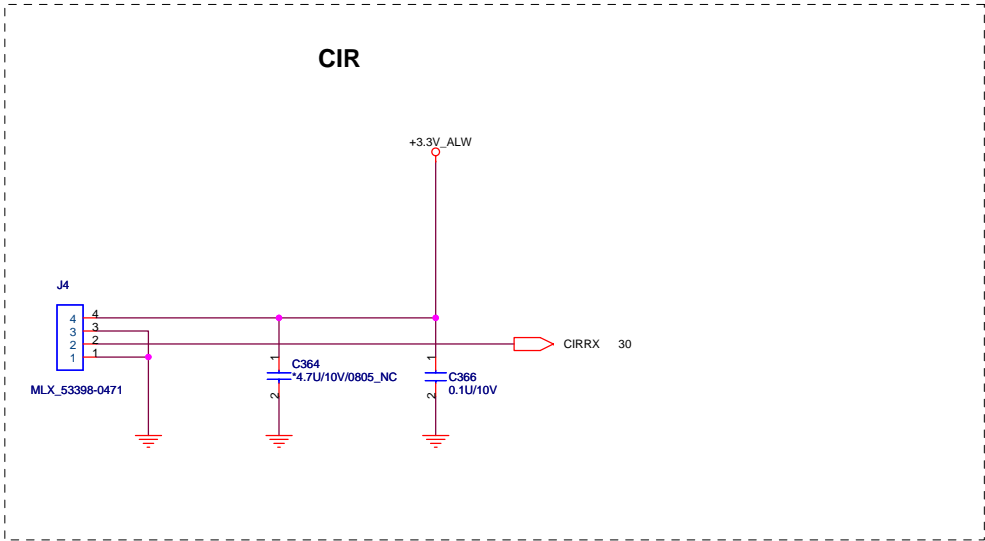
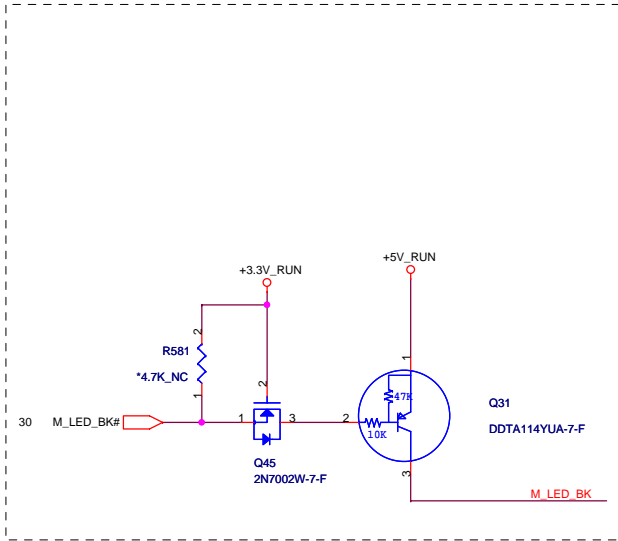
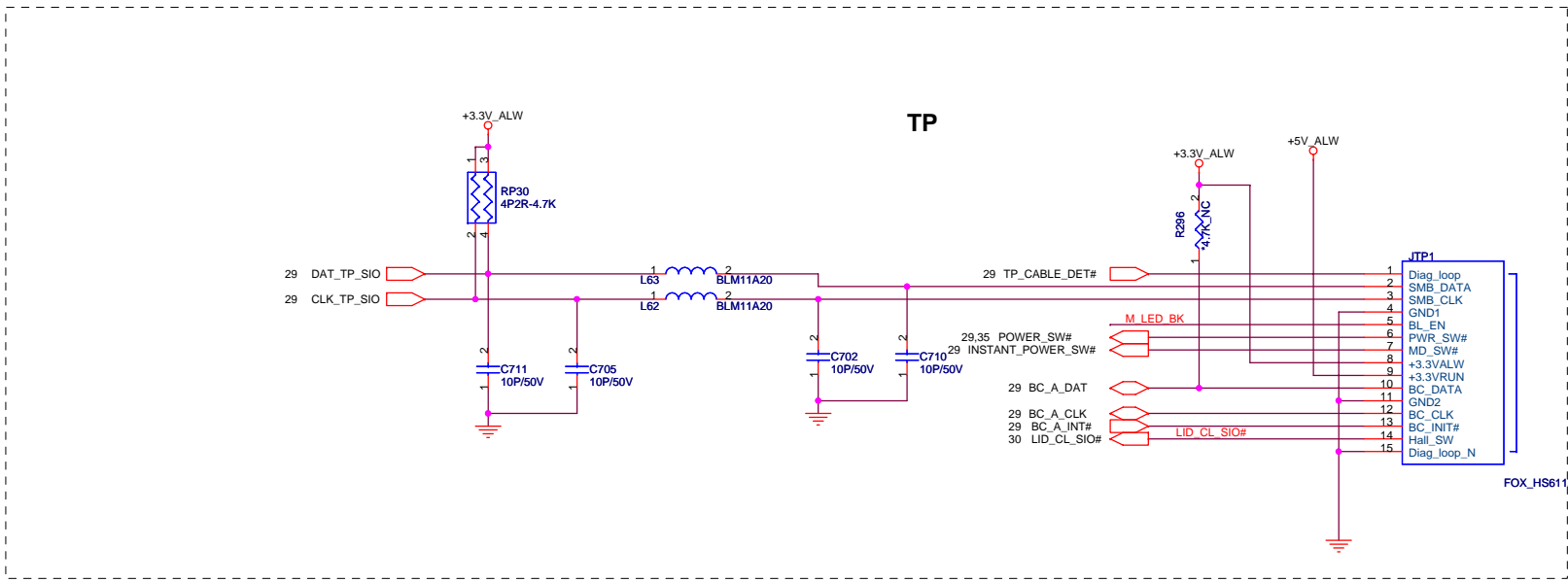
Layout Note:
Place R420 within 500 mils from SPI flash.
Place R398 & R396 within 500 mils of the
MEC5025.



RTC BATTERY

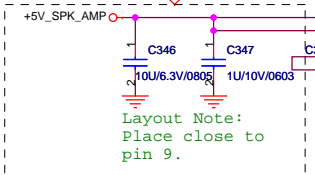
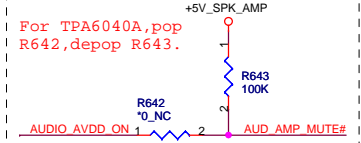
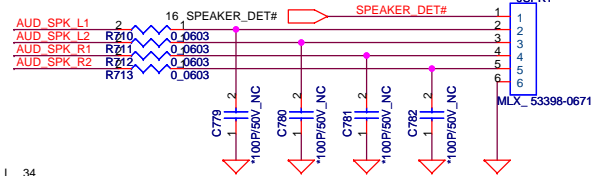
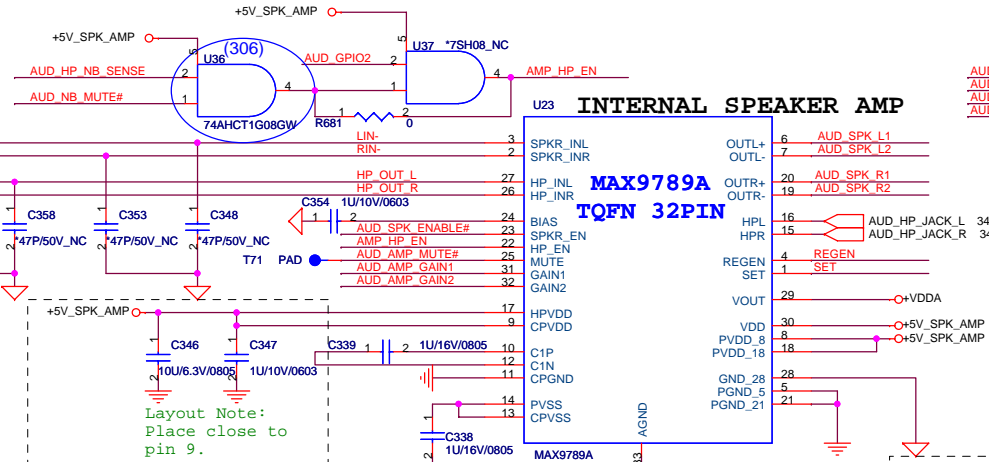


Title FLASH, RTC & KC		
Size	Document Number FX5	Rev 0.1
Date:	Friday, May 04, 2007	Sheet 31 of 61

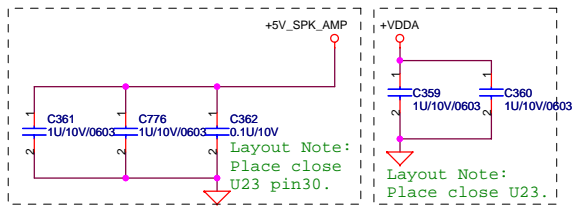


Package 1206 for THD+N performance for Vista Logo requirements.

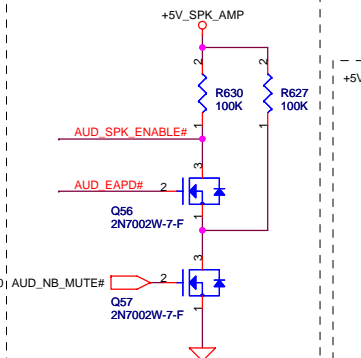
AUD_LINE_OUT_L C349 1 0.033/50V/1206
 AUD_LINE_OUT_R C355 1 0.033/50V/1206
 AUD_HP_OUT_L C363 2 1U/25V/1206
 AUD_HP_OUT_R C365 2 1U/25V/1206



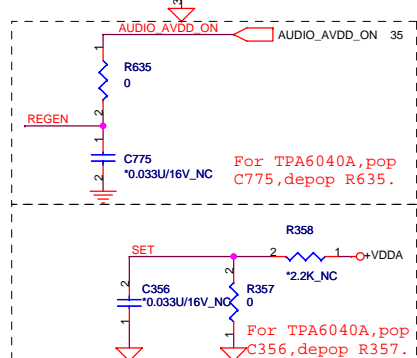
Layout Note:
Place close to pin 9.



Layout Note:
Place close to U23.

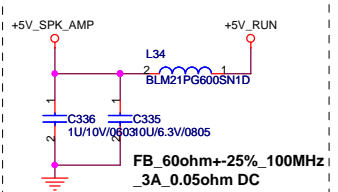


GAIN2	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



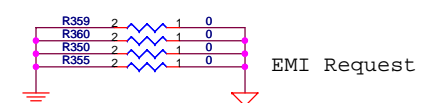
For TPA6040A, pop C775, depop R635.

For TPA6040A, pop C356, depop R357.

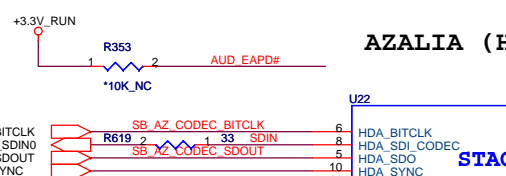
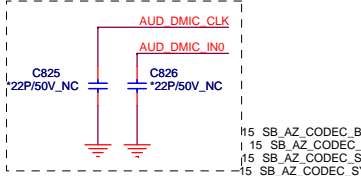


FB 60ohm+-25% 100MHz
_3A 0.05ohm DC

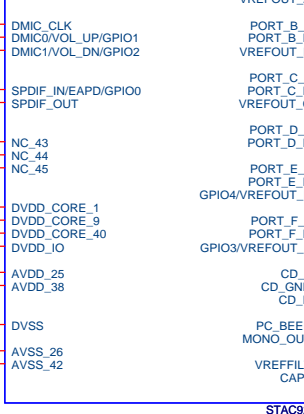
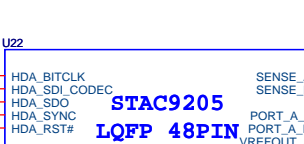
Layout Note:
Place close to pin 18.



EMI Request

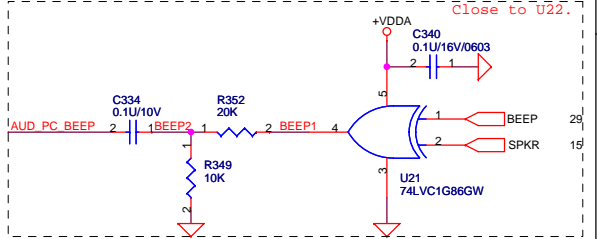
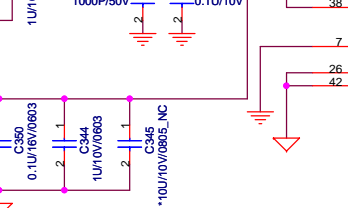
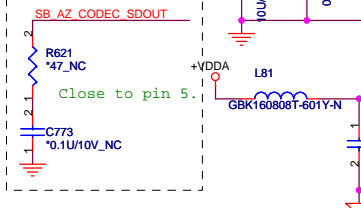
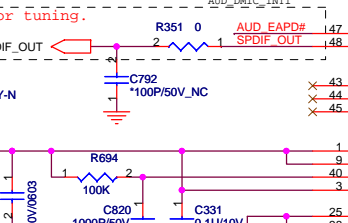
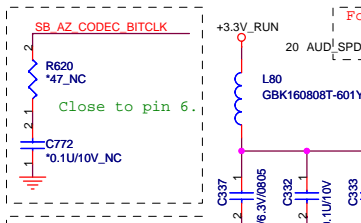
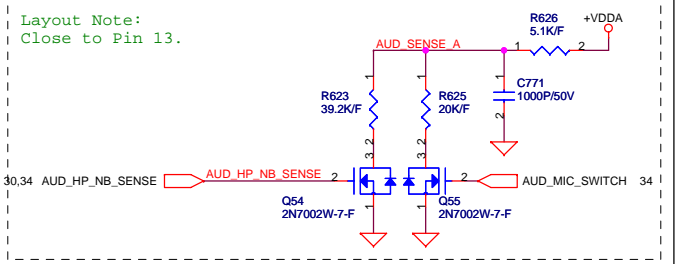


AZALIA (HD) CODEC

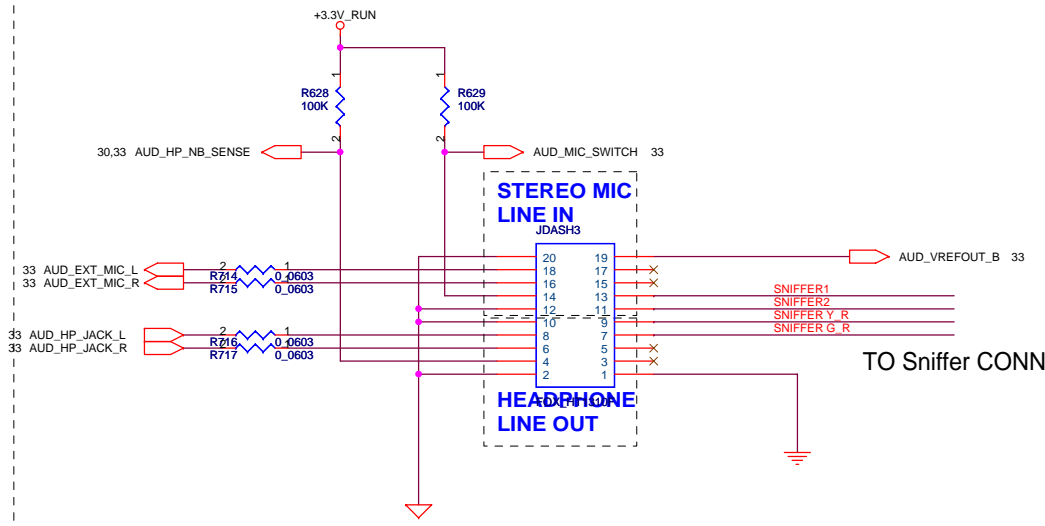


will support QFN package.

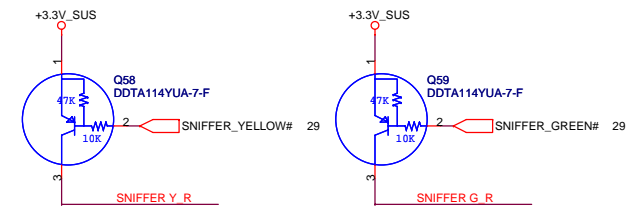
Layout Note:
Close to Pin 13.



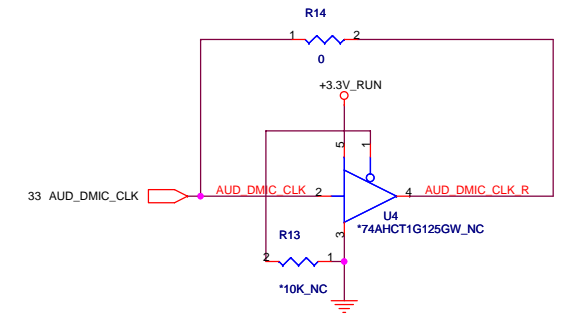
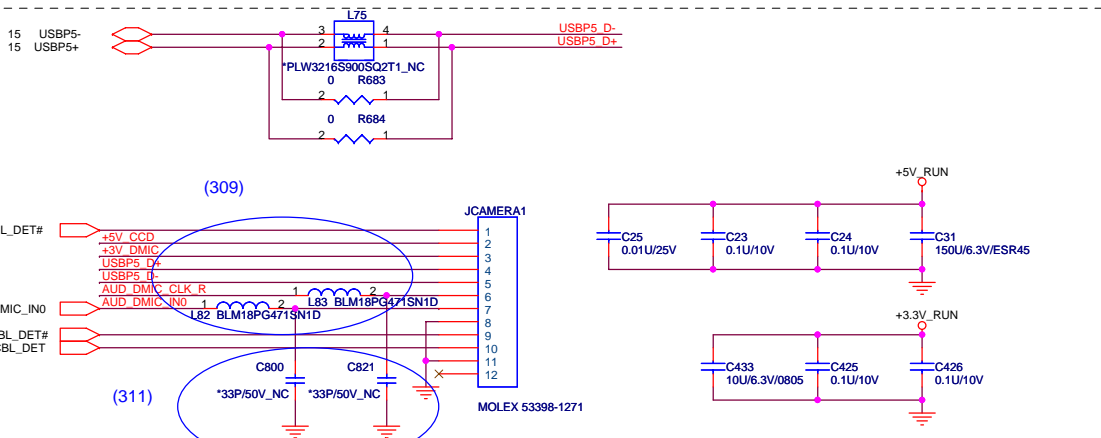
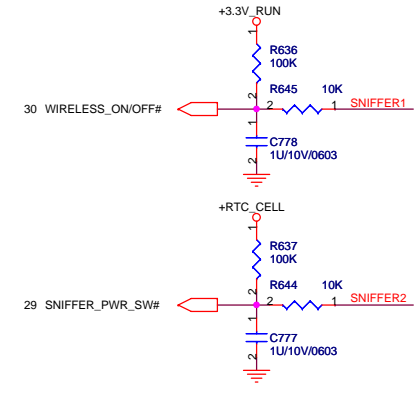
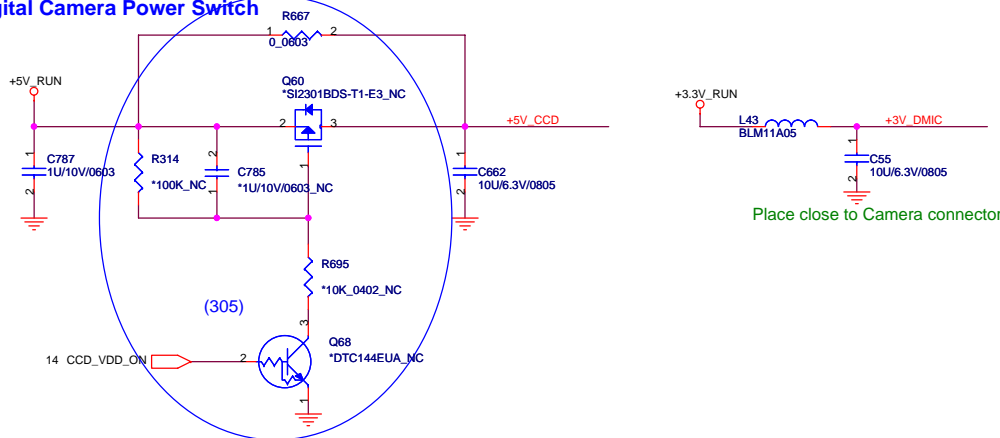
Audio Connect and Sniffer



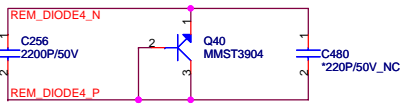
Sniffer LED



Digital Camera Power Switch

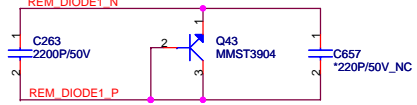


Title			AUDIO CONN Digital MIC/Camera		
Size			Document Number		Rev
FX5					1A
Date:	Friday, May 04, 2007	Sheet	34	of	61



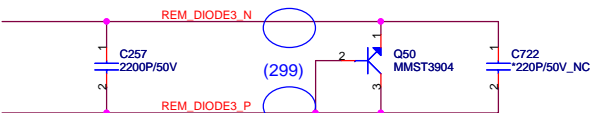
Put C256 close to Guardian.
Put C480 close to Diode

Place under ATI690



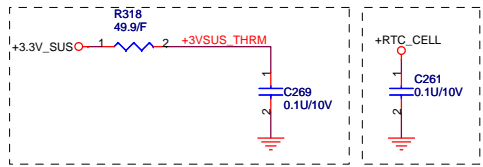
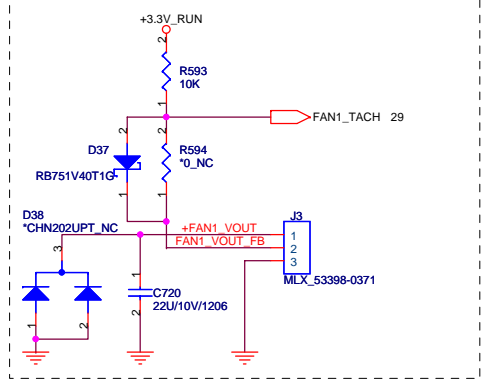
Put C263 close to Guardian.
Put C657 close to Diode

Place under CPU

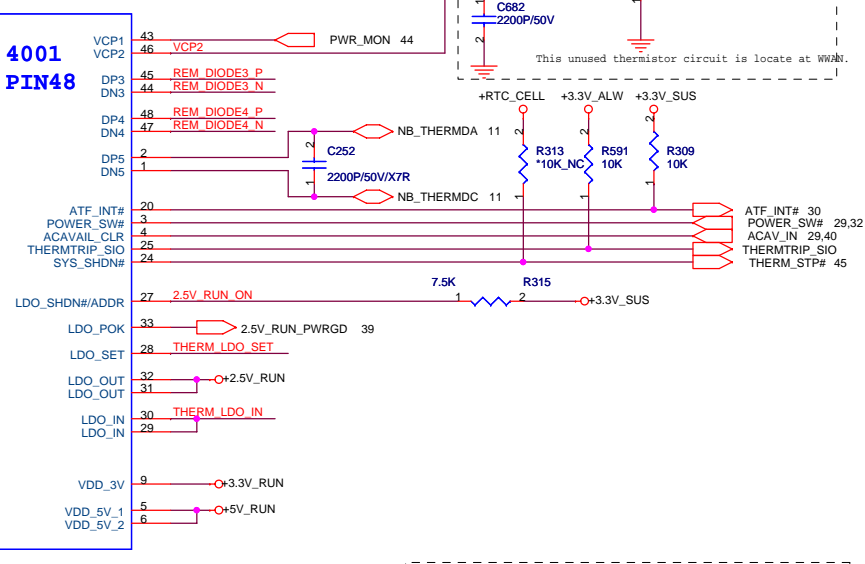
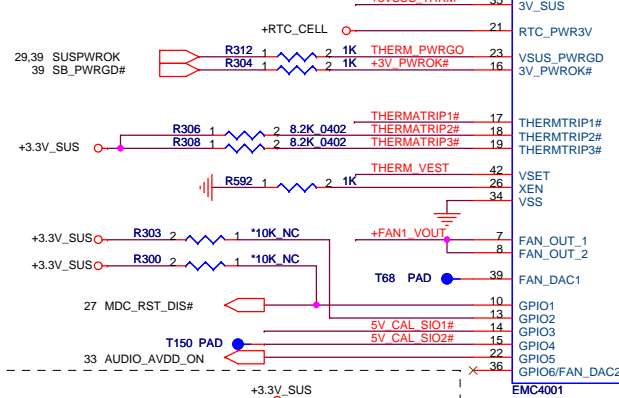
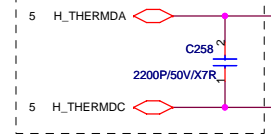


Put C257, R307 & R305 as close as possible to Guardian.
Put C722 close to Diode

UMA
Place near the bottom SODIMM

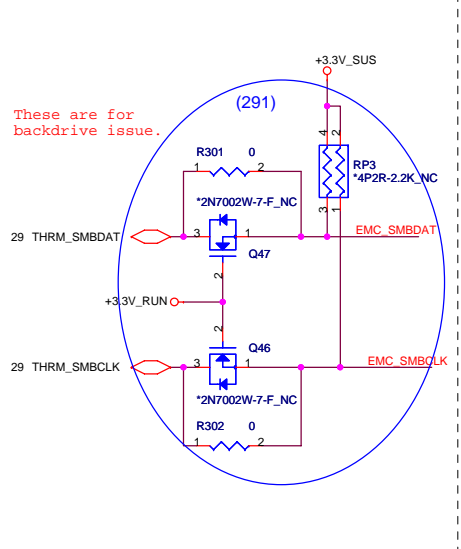


Put C258 close to Guardian.

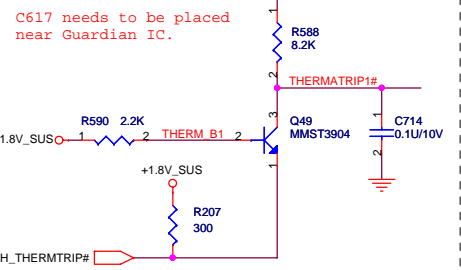


This unused thermistor circuit is locate at WW#N.

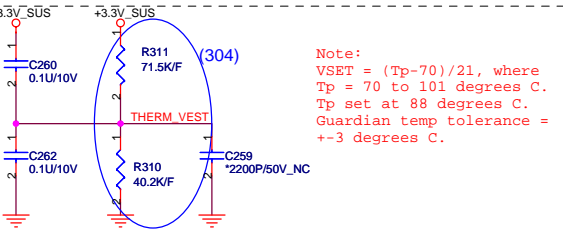
SMBus address D2



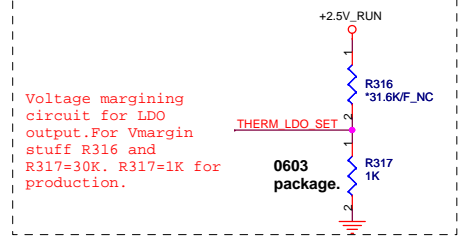
These are for backdrive issue.



C617 needs to be placed near Guardian IC.

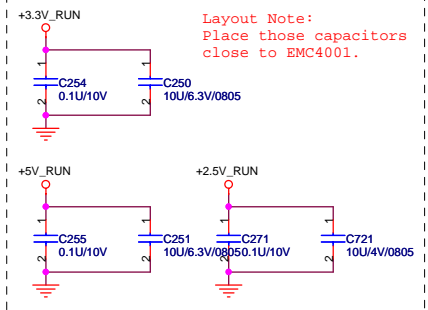


Note:
VSET = (Tp-70)/21, where
Tp = 70 to 101 degrees C.
Tp set at 88 degrees C.
Guardian temp tolerance =
+/-3 degrees C.

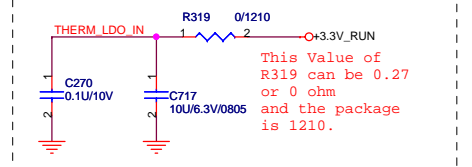


Voltage margining circuit for LDO output. For Vmargin stuff R316 and R317=30K, R317=1K for production.

0603 package.

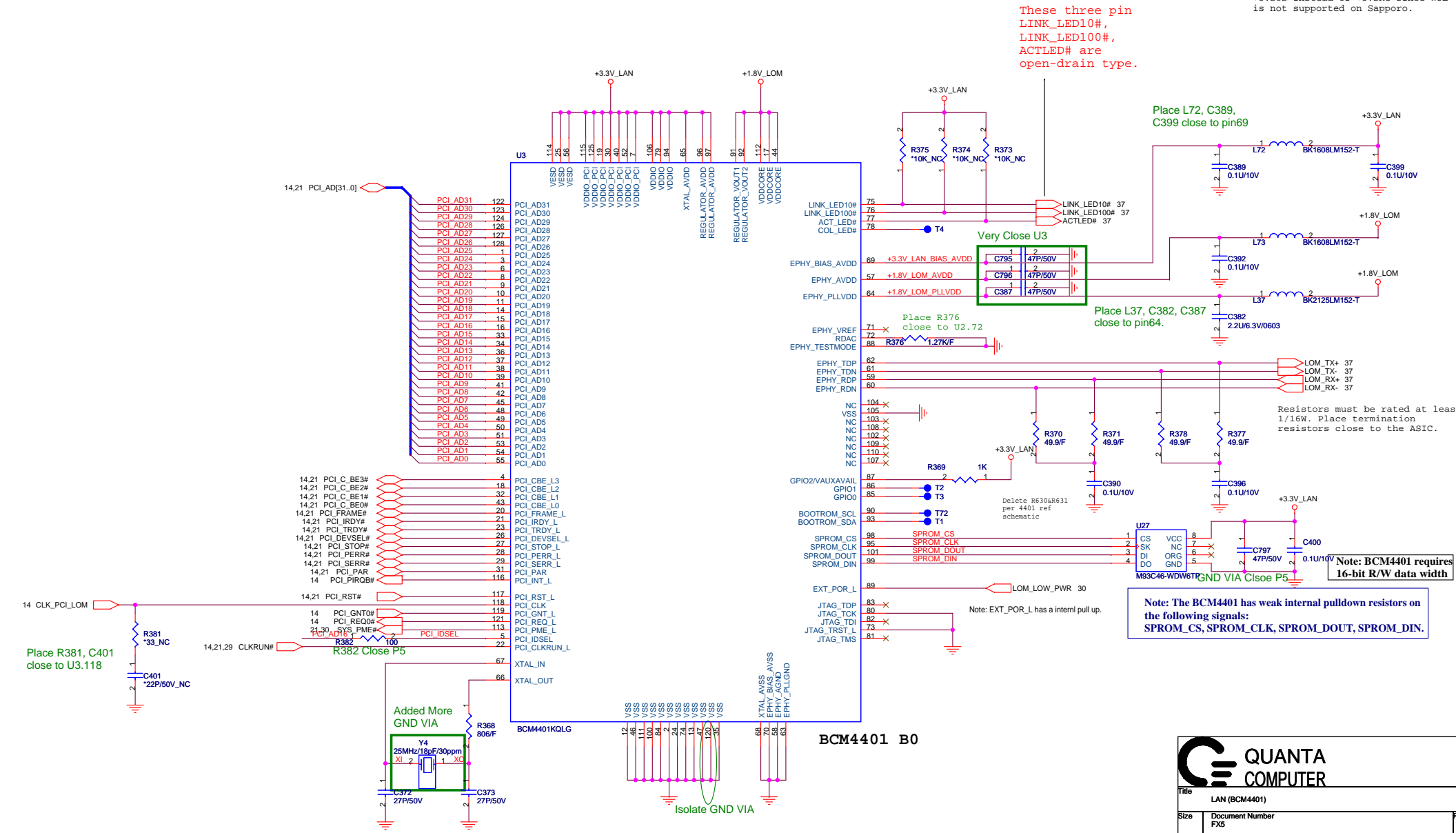
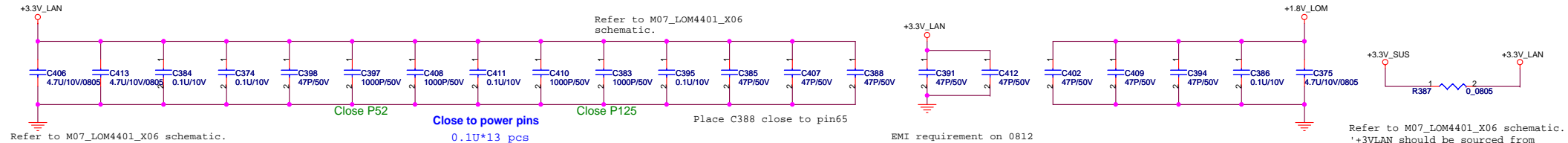


Layout Note:
Place those capacitors close to EMC4001.



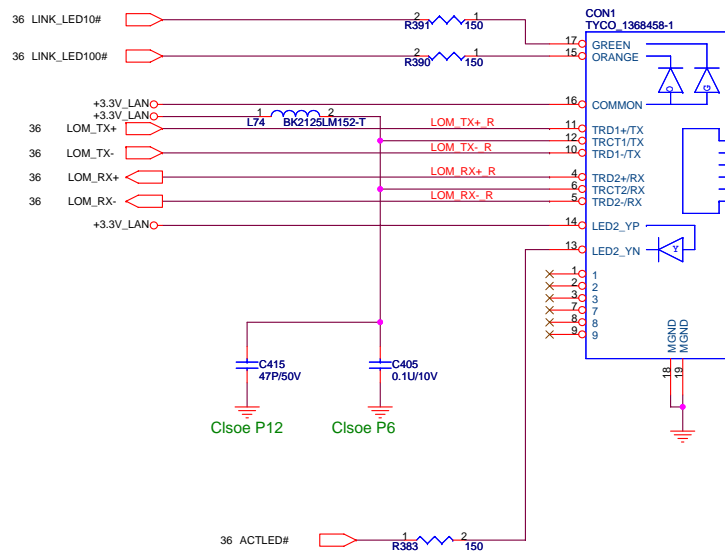
This Value of R319 can be 0.27 or 0 ohm and the package is 1210.



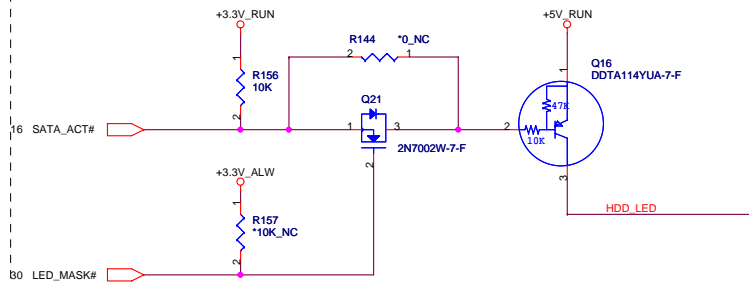


QUANTA COMPUTER

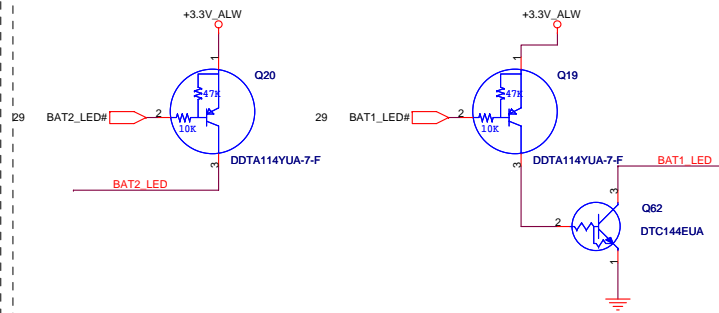
Title	LAN (BCM4401)		
Size	Document Number	FX5	Rev 0.1
Date:	Friday, May 04, 2007	Sheet	36 of 61



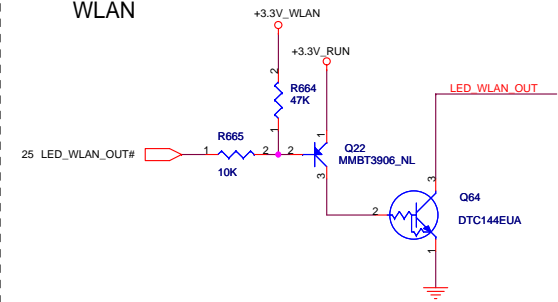
HDD activity LED.



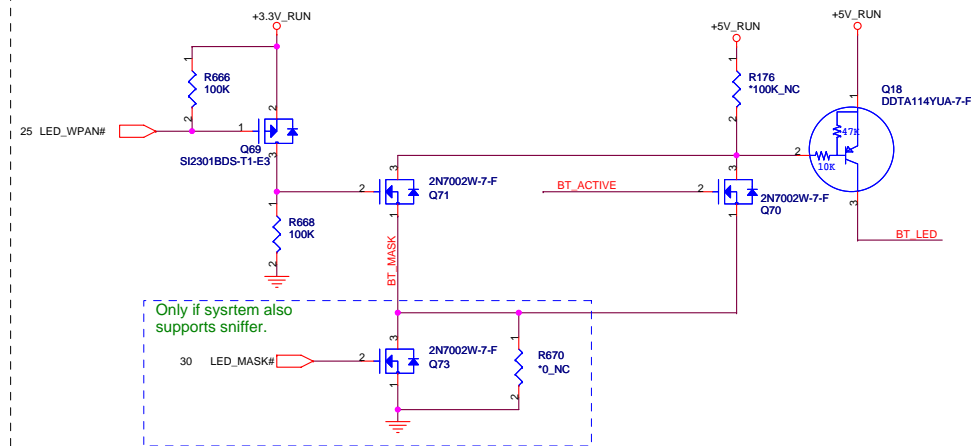
Battery status.



WLAN

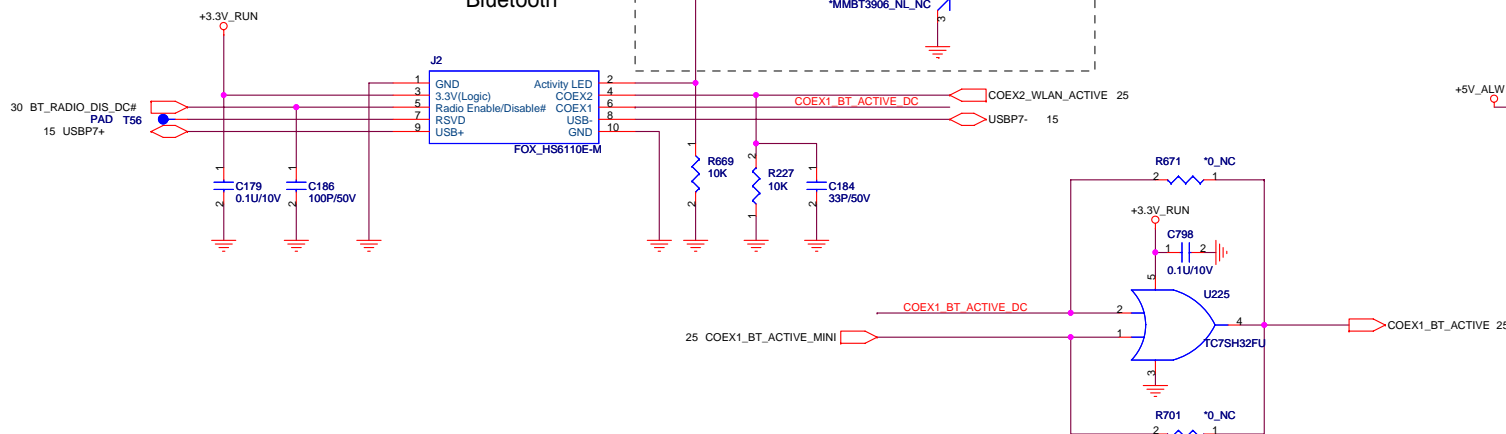


BT

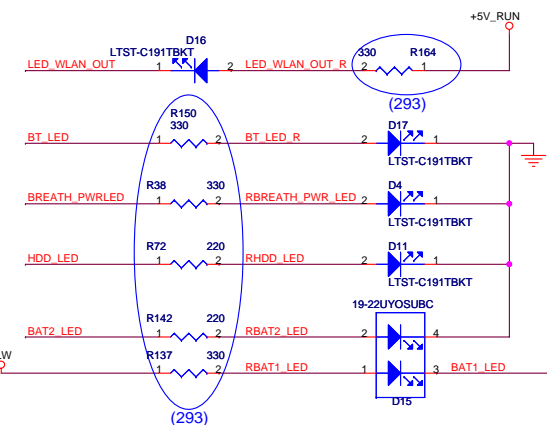
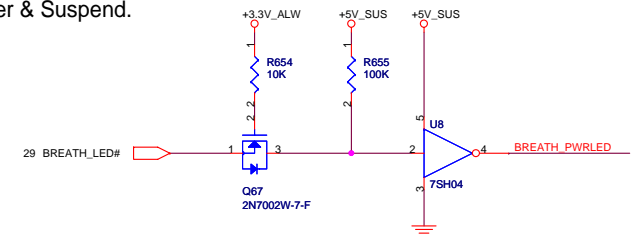


This circuit is only needed if the platform has the SNIFFER.

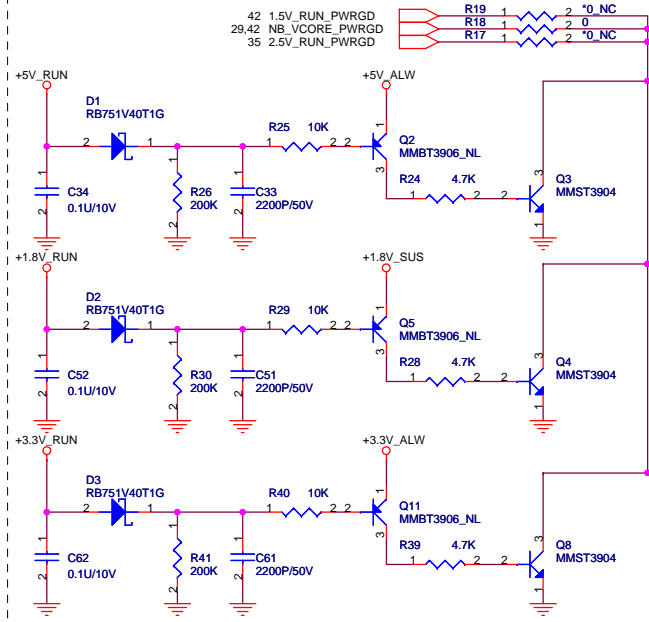
Bluetooth



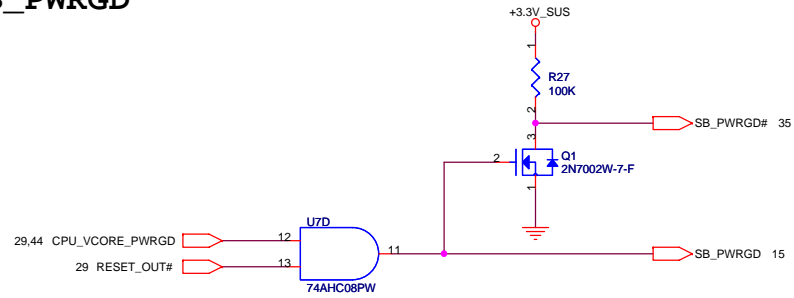
Power & Suspend.



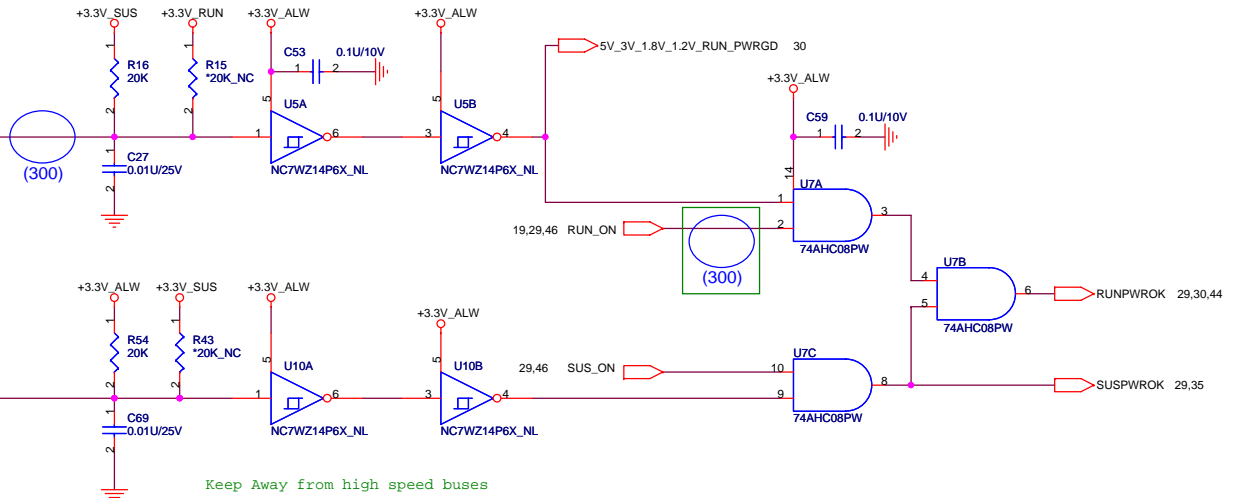
RUN_POWER



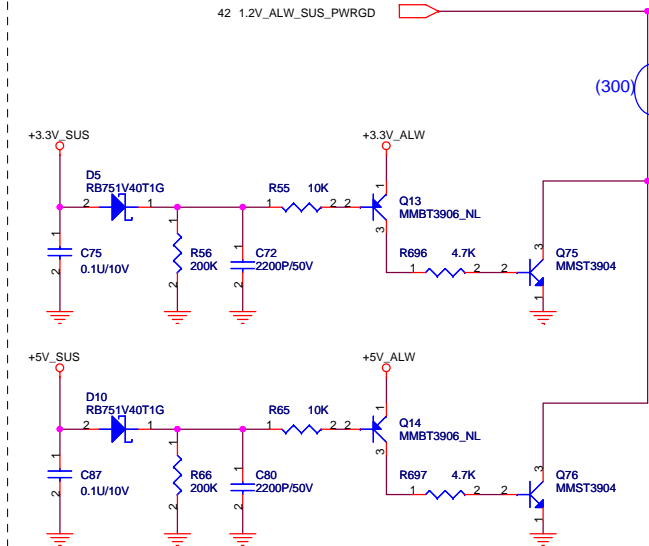
SB_PWRGD



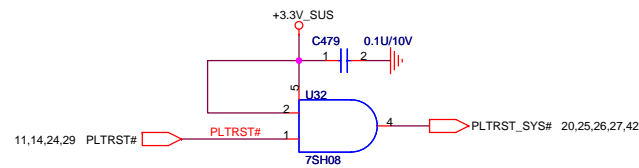
SUSPWROK and RUNPWROK

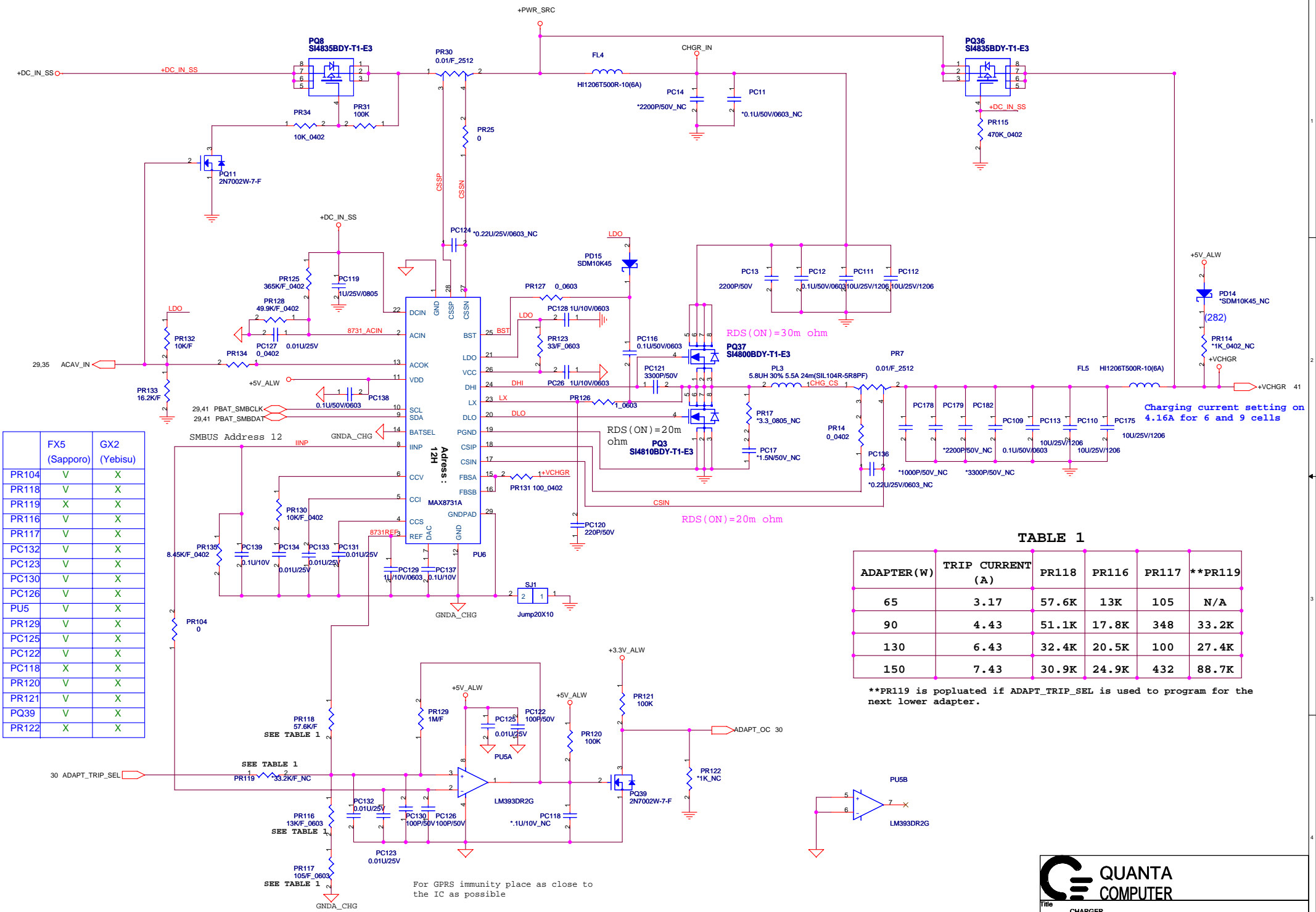


SUS_POWER



PLTRST Buffer





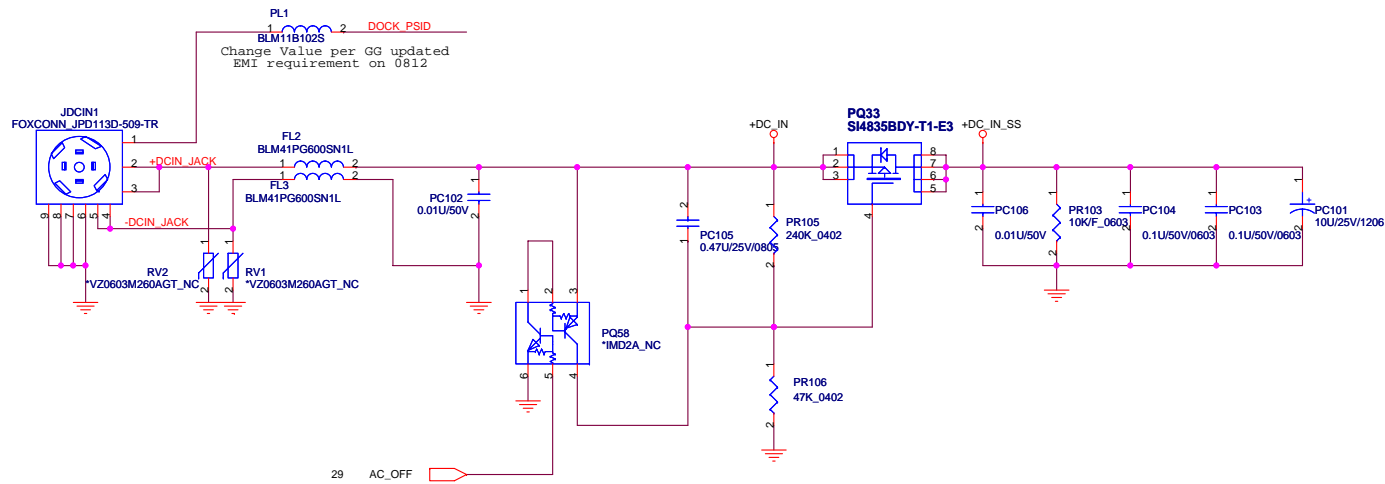
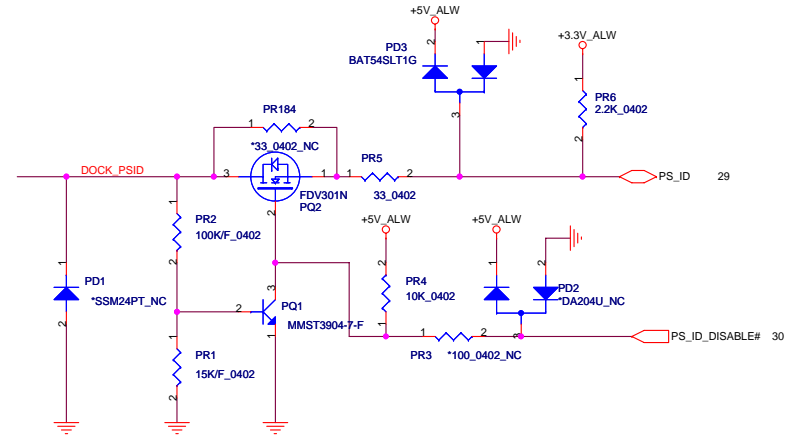
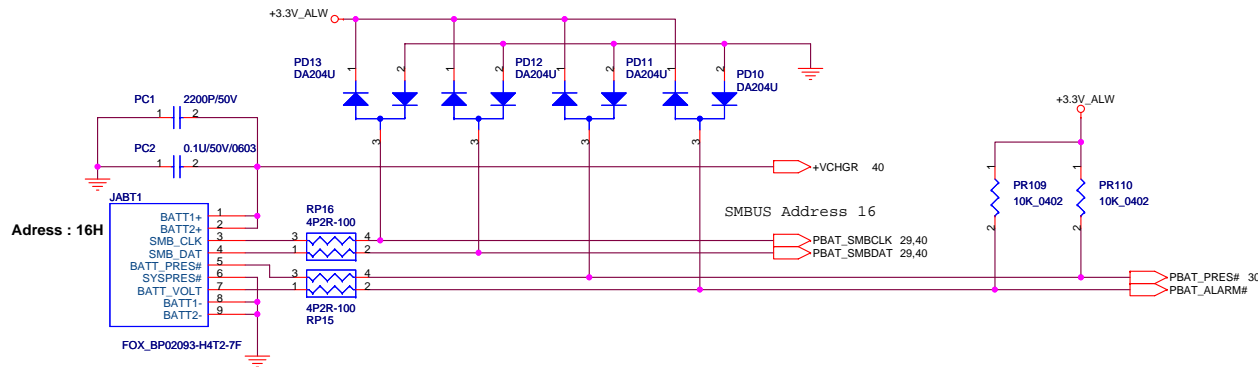
	FX5 (Sapporo)	GX2 (Yebisu)
PR104	V	X
PR118	V	X
PR119	X	X
PR116	V	X
PR117	V	X
PC132	V	X
PC123	V	X
PC130	V	X
PC126	V	X
PU5	V	X
PR129	V	X
PC125	V	X
PC122	V	X
PC118	X	X
PR120	V	X
PR121	V	X
PQ39	V	X
PR122	X	X

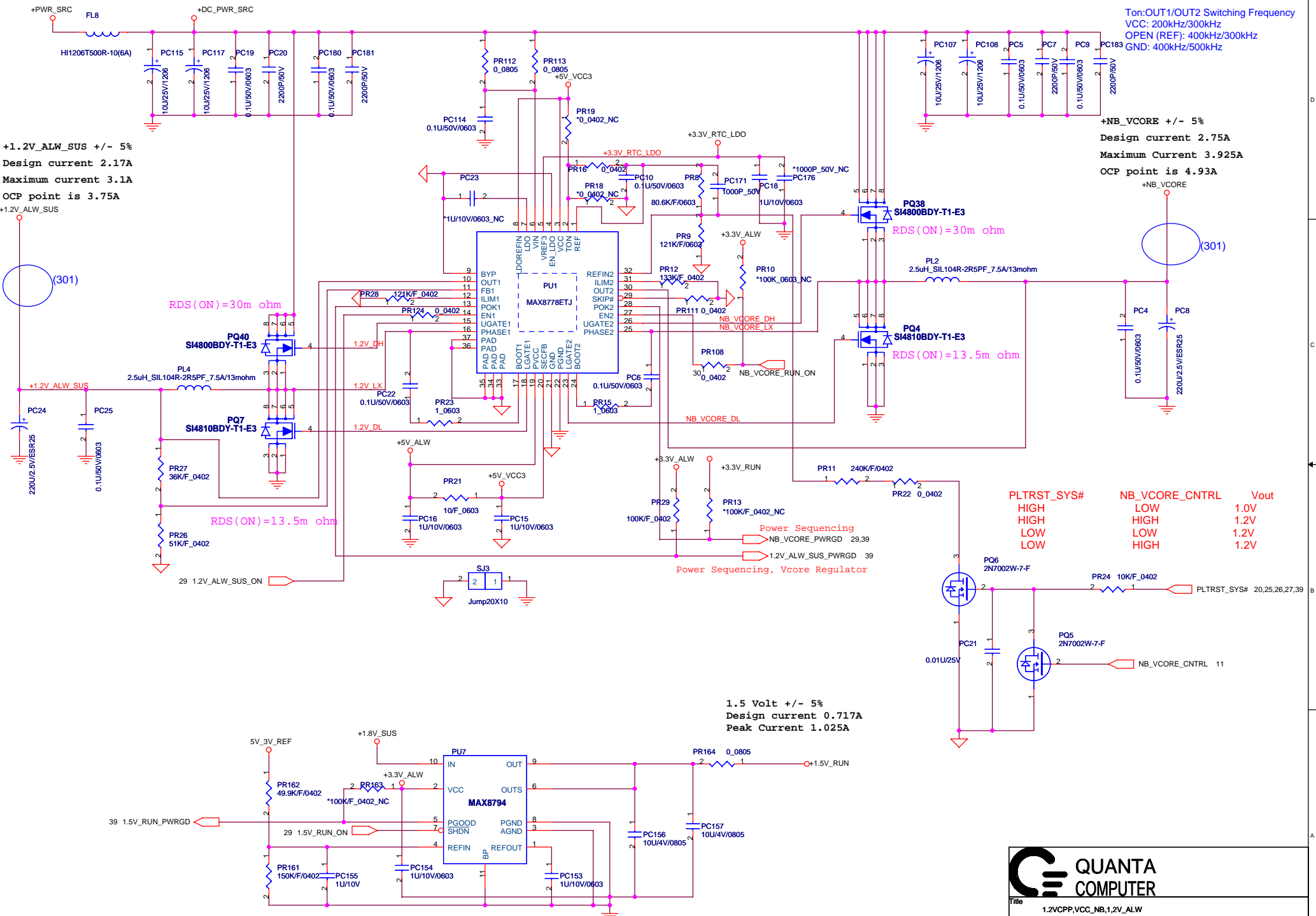
TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	PR118	PR116	PR117	**PR119
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K

**PR119 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

For GPRS immunity place as close to the IC as possible

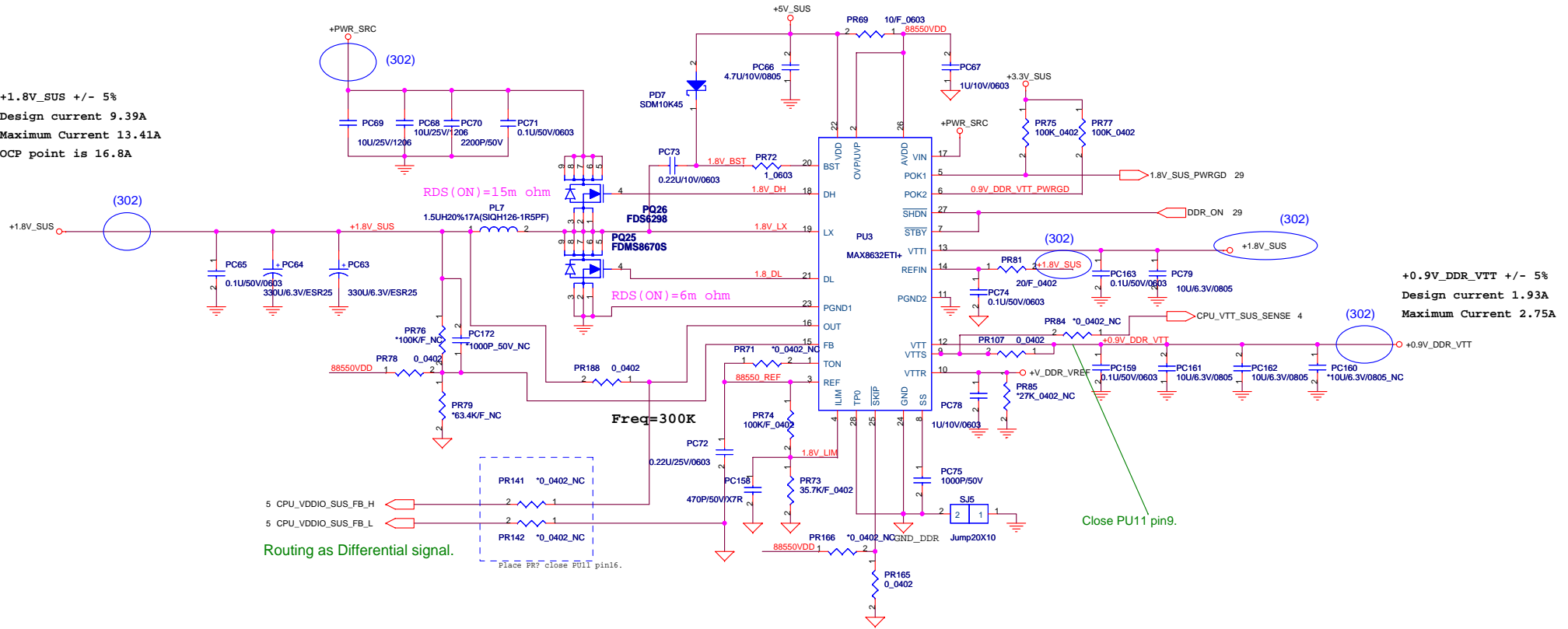




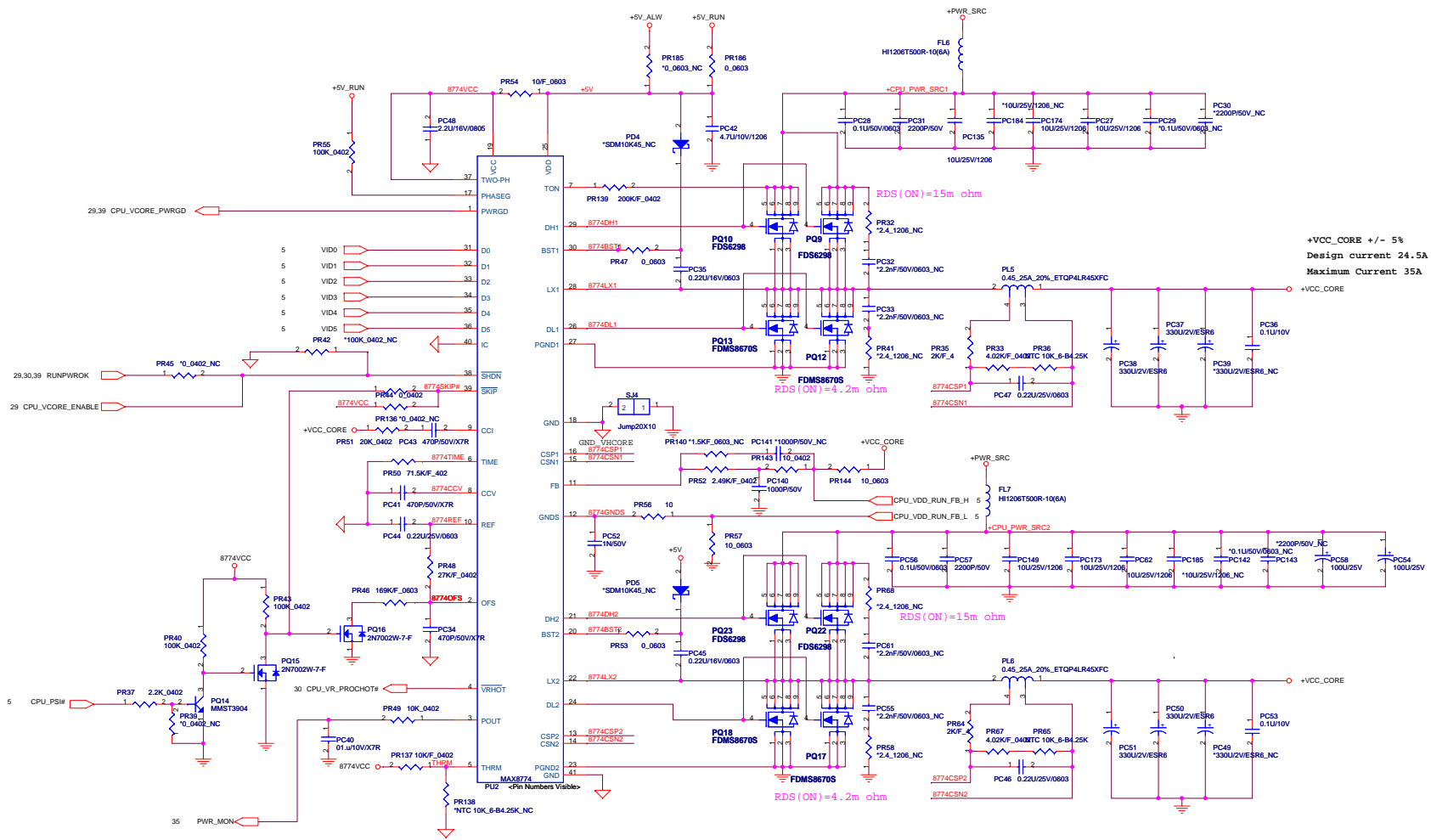
Ton:OUT1/OUT2 Switching Frequency
 VCC: 200kHz/300kHz
 OPEN (REF): 400kHz/300kHz
 GND: 400kHz/500kHz



+1.8V_SUS +/- 5%
 Design current 9.39A
 Maximum Current 13.41A
 OCP point is 16.8A



+0.9V_DDR_VTT +/- 5%
 Design current 1.93A
 Maximum Current 2.75A



+VCC_CORE +/- 5%
 Design current 24.5A
 Maximum Current 35A

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V	1	0	0	0	0	0	0.7550V
0	0	0	0	0	1	1.5250V	1	0	0	0	0	1	0.7500V
0	0	0	0	1	0	1.5000V	1	0	0	0	1	0	0.7375V
0	0	0	0	1	1	1.4750V	1	0	0	0	1	1	0.7250V
0	0	0	1	0	0	1.4500V	1	0	0	1	0	0	0.7125V
0	0	0	1	0	1	1.4250V	1	0	0	1	0	1	0.7000V
0	0	0	1	1	0	1.4000V	1	0	0	1	1	0	0.6875V
0	0	0	1	1	1	1.3750V	1	0	0	1	1	1	0.6750V
0	0	1	0	0	0	1.3500V	1	0	1	0	0	0	0.6625V
0	0	1	0	0	1	1.3250V	1	0	1	0	1	0	0.6500V
0	0	1	0	1	0	1.3000V	1	0	1	0	1	0	0.6375V
0	0	1	0	1	1	1.2750V	1	0	1	0	1	1	0.6250V
0	0	1	1	0	0	1.2500V	1	0	1	1	0	0	0.6125V
0	0	1	1	0	1	1.2250V	1	0	1	1	0	1	0.6000V
0	0	1	1	1	0	1.2000V	1	0	1	1	0	0	0.5875V
0	0	1	1	1	1	1.1750V	1	0	1	1	1	1	0.5750V
0	1	0	0	0	0	1.1500V	1	1	0	0	0	0	0.5625V
0	1	0	0	0	1	1.1250V	1	1	0	0	1	0	0.5500V
0	1	0	0	1	0	1.1000V	1	1	0	0	1	0	0.5375V
0	1	0	0	1	1	1.0750V	1	1	0	0	1	1	0.5250V
0	1	0	1	0	0	1.0500V	1	1	0	1	0	0	0.5125V
0	1	0	1	0	1	1.0250V	1	1	0	1	0	1	0.5000V
0	1	0	1	1	0	1.0000V	1	1	0	1	1	0	0.4875V
0	1	0	1	1	1	0.9750V	1	1	0	1	1	1	0.4750V
0	1	1	0	0	0	0.9500V	1	1	1	0	0	0	0.4625V
0	1	1	0	0	1	0.9250V	1	1	1	0	1	0	0.4500V
0	1	1	0	1	0	0.9000V	1	1	1	0	1	1	0.4375V
0	1	1	0	1	1	0.8750V	1	1	1	0	1	1	0.4250V
0	1	1	1	0	0	0.8500V	1	1	1	1	0	0	0.4125V
0	1	1	1	0	1	0.8250V	1	1	1	1	0	1	0.4000V
0	1	1	1	1	0	0.8000V	1	1	1	1	1	0	0.3875V
0	1	1	1	1	1	0.7750V	1	1	1	1	1	1	0.3750V

QUANTA COMPUTER

File: VHCORE (MAX8774)
 Size: Document Number
 Date: Fidsk, Nov 04, 2007
 Sheet: 44 of 61

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

Ton:OUT1/OUT2 Switching Frequency
 VCC: 200kHz/300kHz
 OPEN (REF): 400kHz/300kHz
 GND: 400kHz/500kHz

Place these CAPS close to FETs

Place these CAPS close to FETs

5 Volt +/- 5%
 Design Current: 7.34 A
 Maximum current: 10.49A
 OCP point is 13.1A

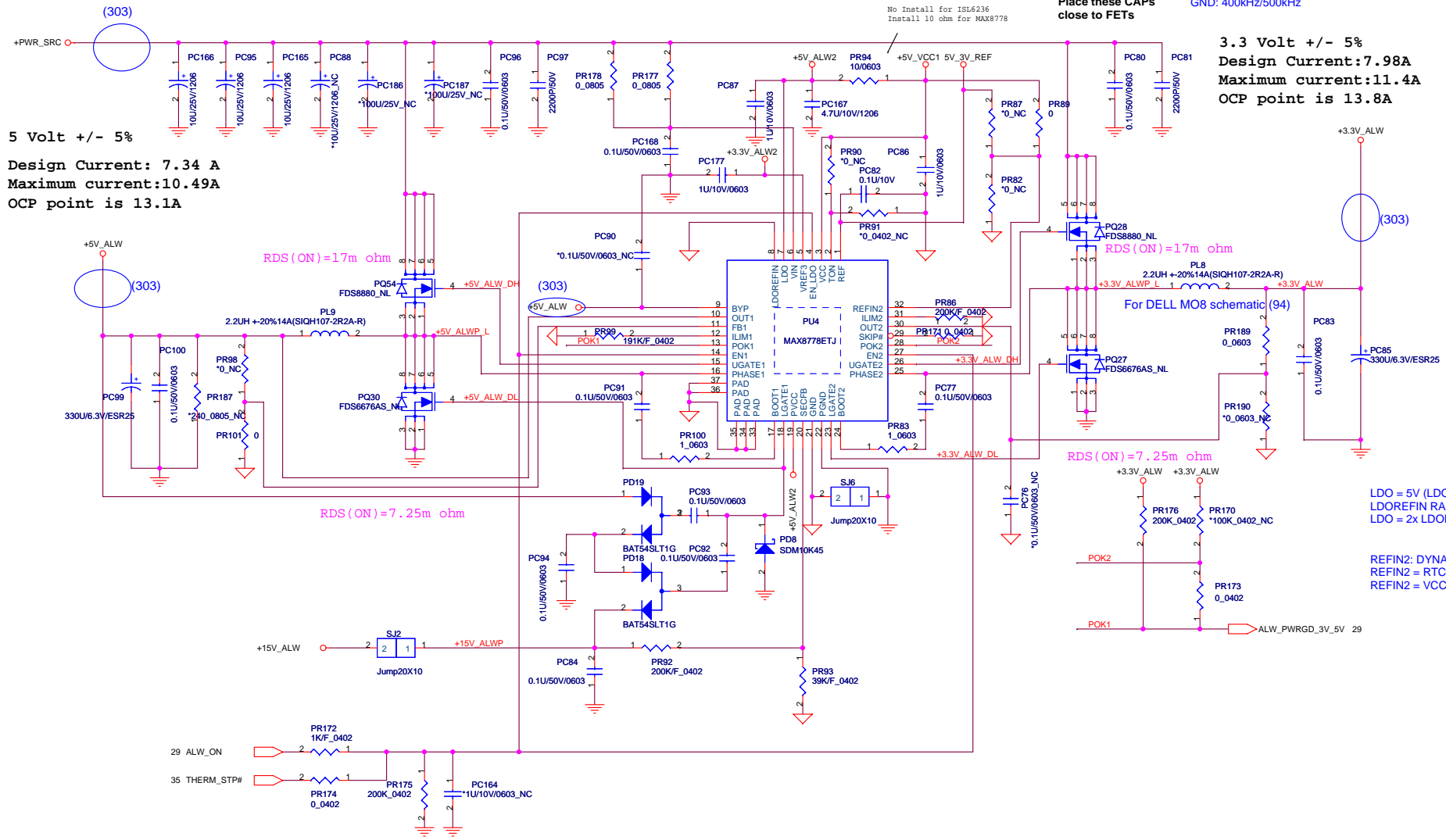
3.3 Volt +/- 5%
 Design Current: 7.98A
 Maximum current: 11.4A
 OCP point is 13.8A

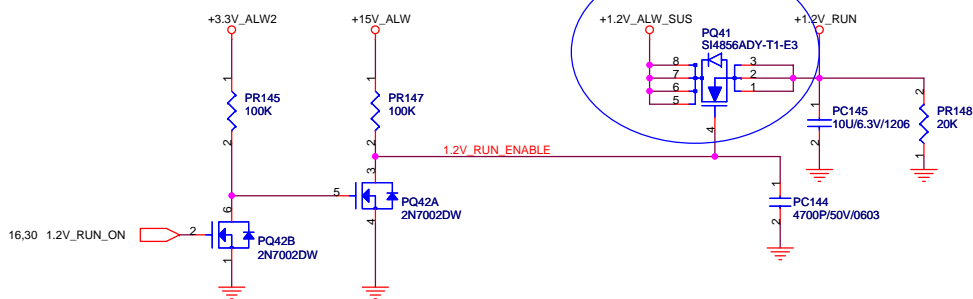
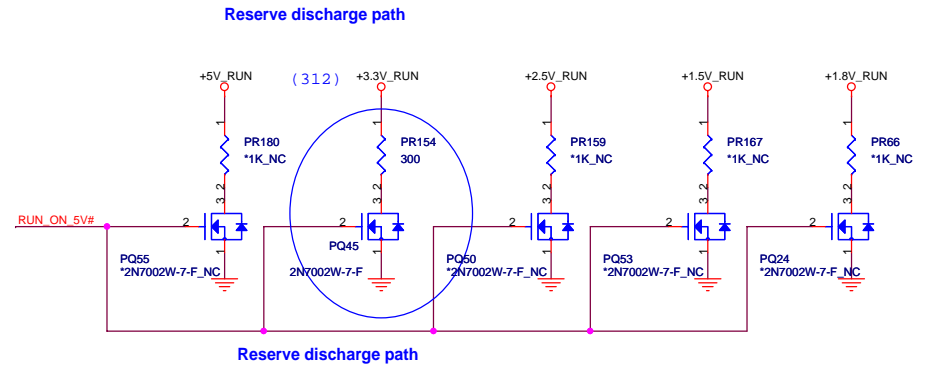
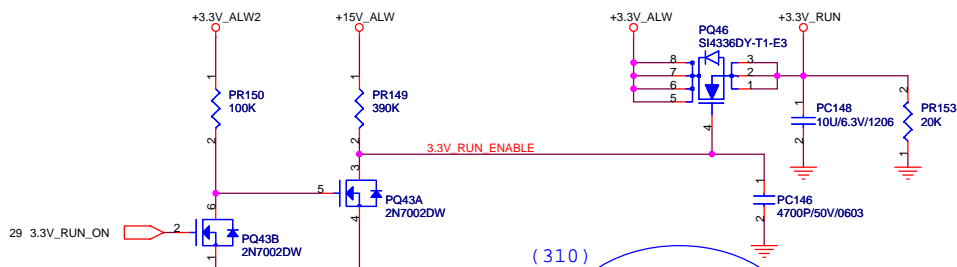
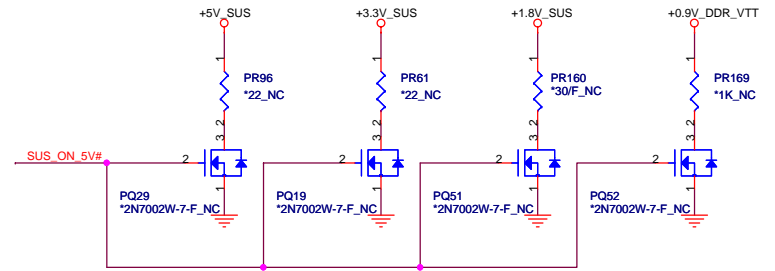
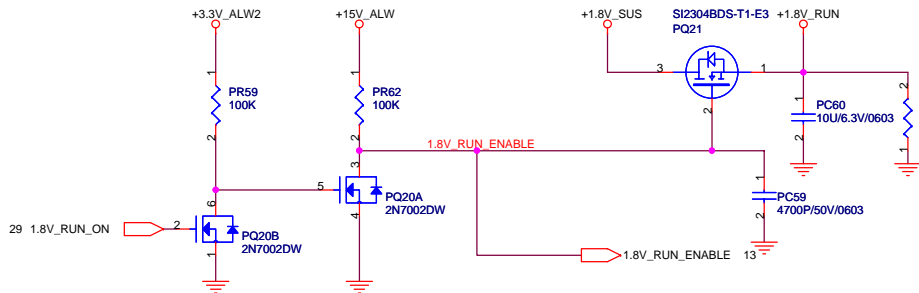
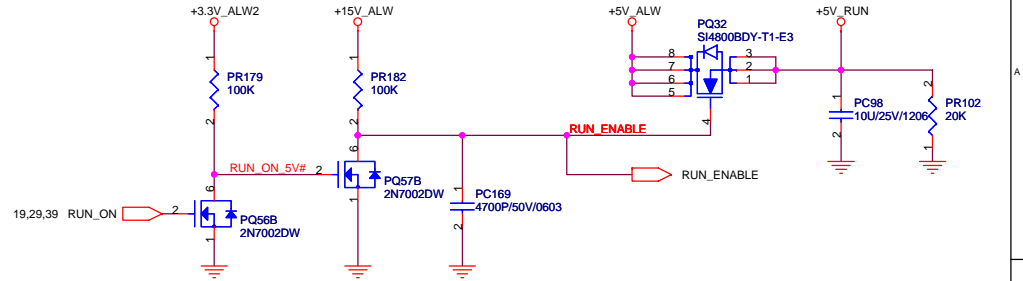
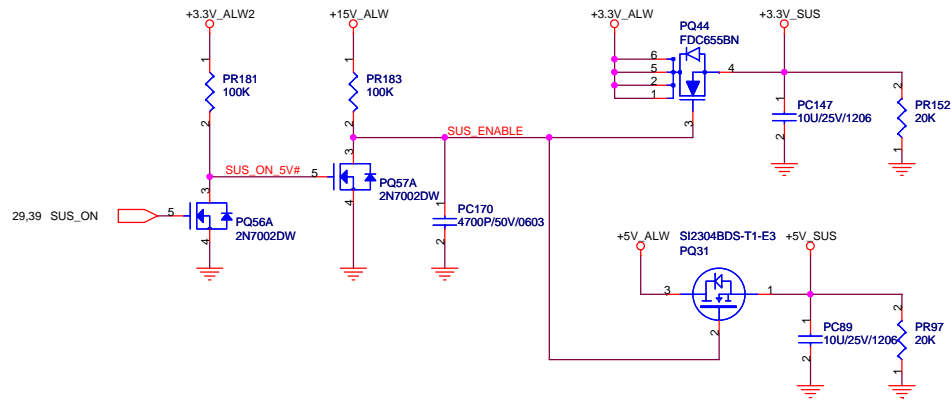
+5V_ALW
 RDS(ON) = 17m ohm
 RDS(ON) = 7.25m ohm

+3.3V_ALW
 RDS(ON) = 17m ohm
 For DELL MO8 schematic (94)

LDO = 5V (LDOREFIN = GND) or
 LDOREFIN RANGE: 0.3V to 2V
 LDO = 2x LDOREFIN

REFIN2: DYNAMIC 0 to 2V
 REFIN2 = RTC: 1.05V Fixed
 REFIN2 = VCC: 3.3V Fixed



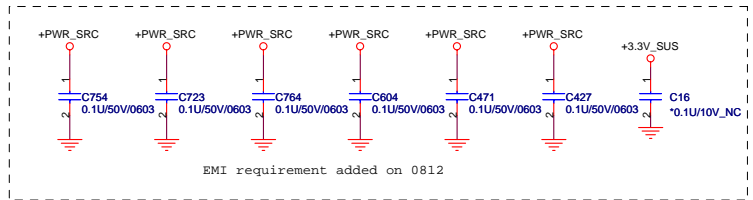
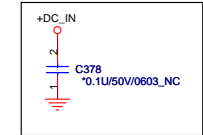
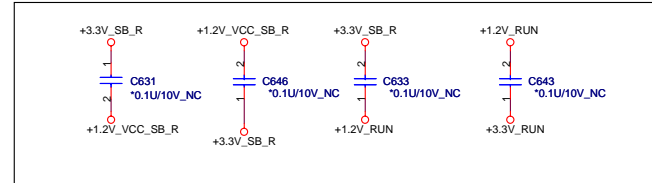
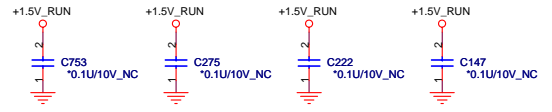
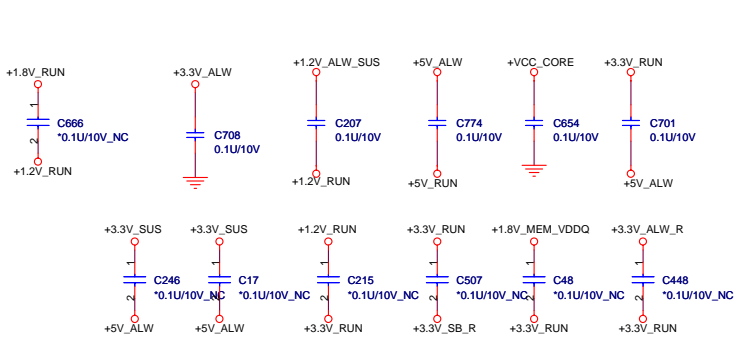
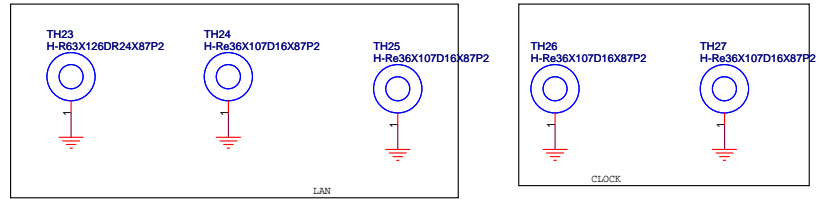
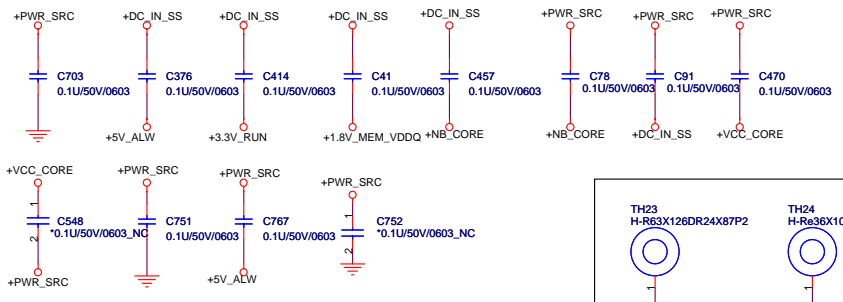
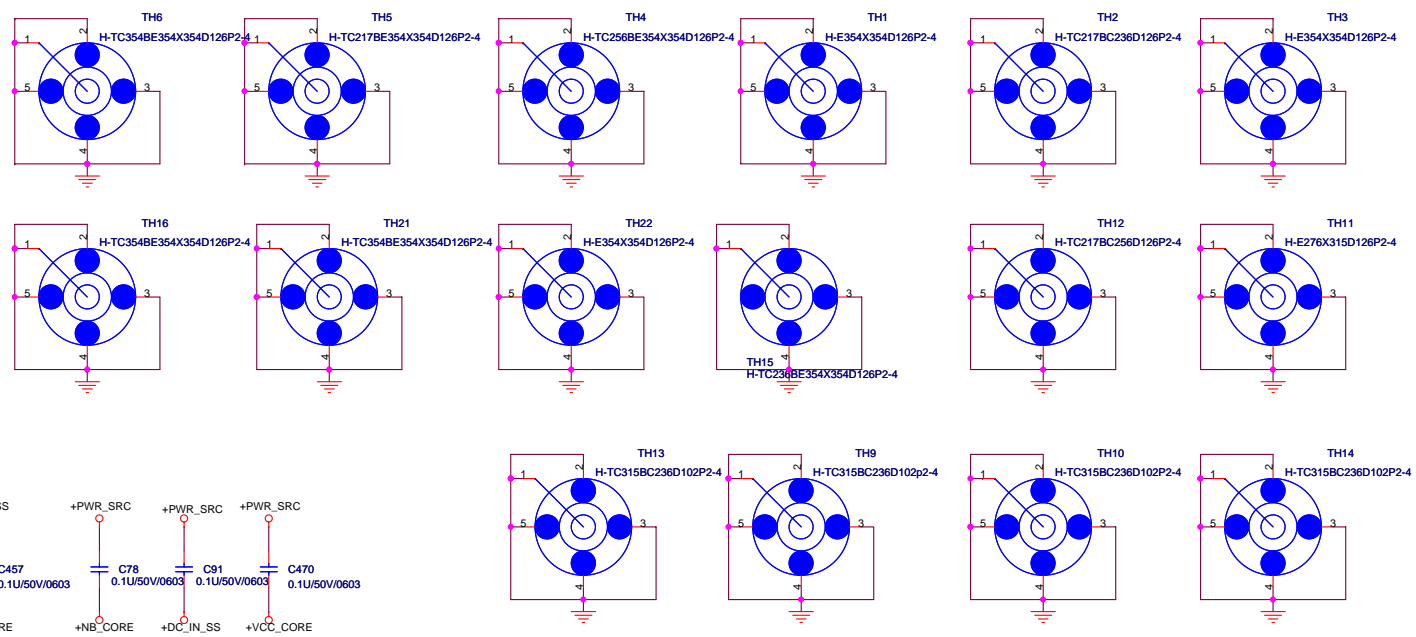
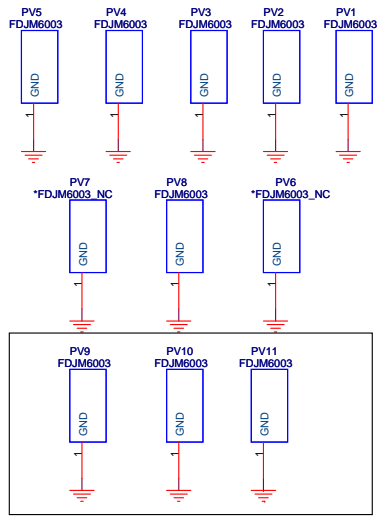


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Title: RUN POWER SW

Size: FX5	Document Number: FX5	Rev: 1A
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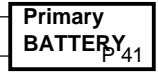
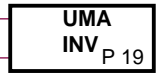
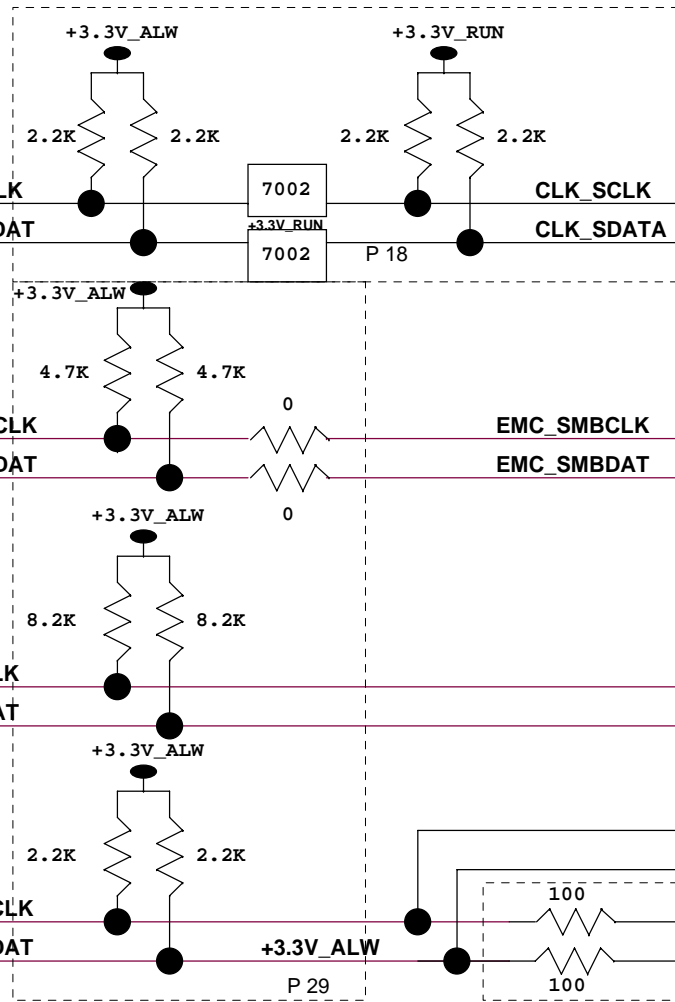
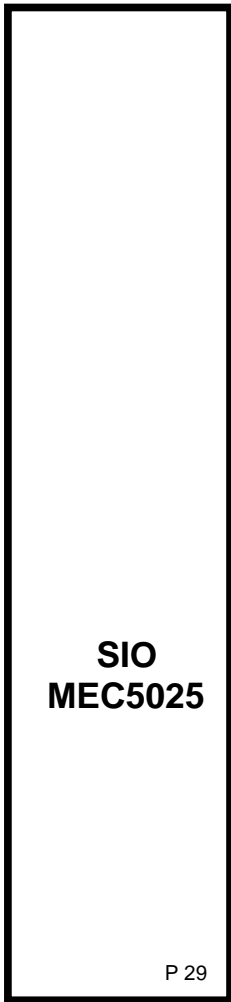
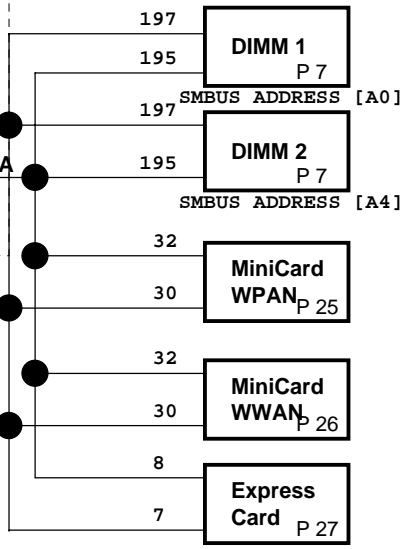
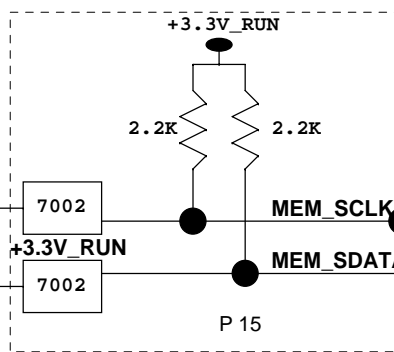
Date: Friday, May 04, 2007 Sheet 46 of 61



**QUANTA
COMPUTER**

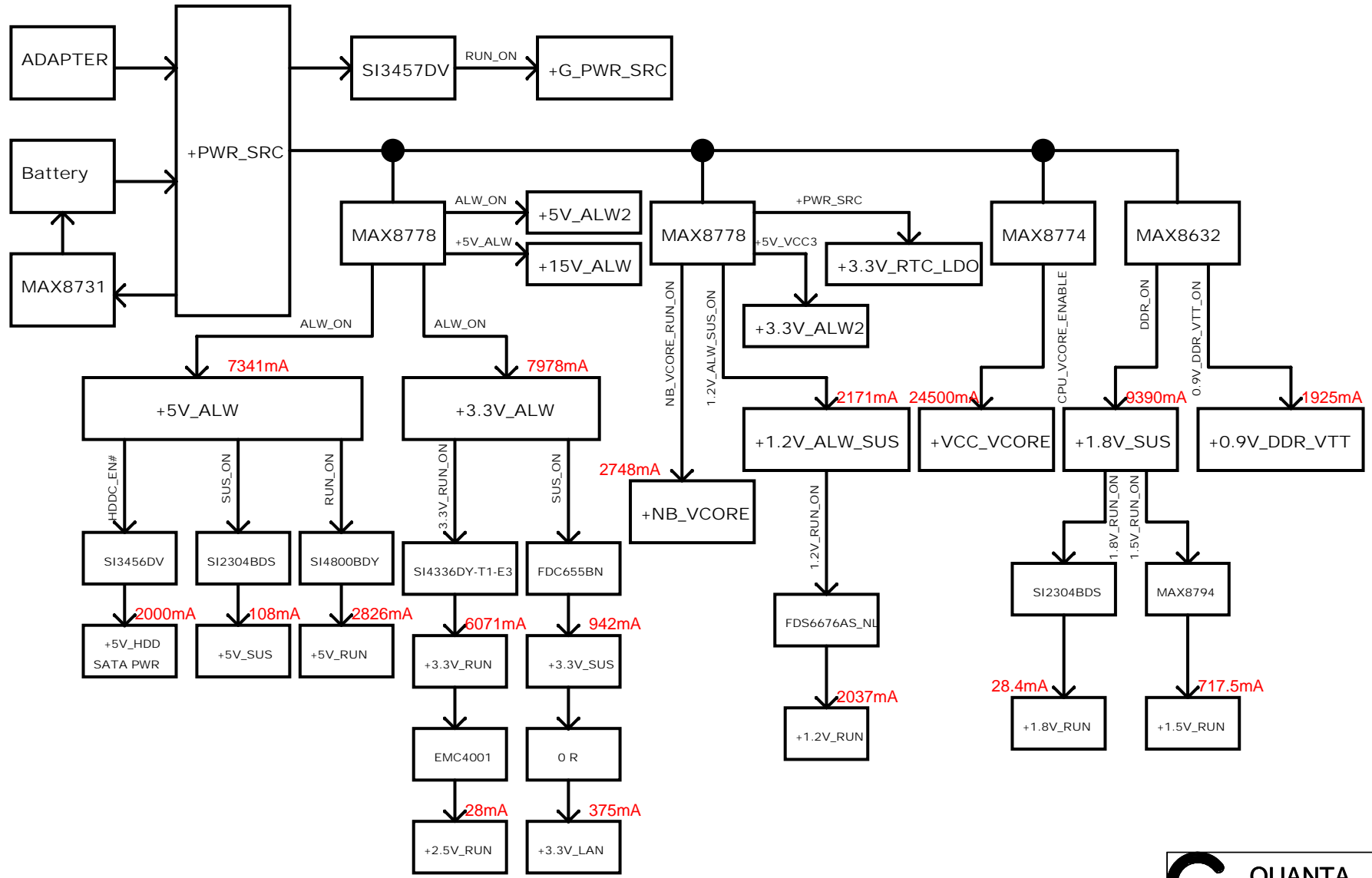
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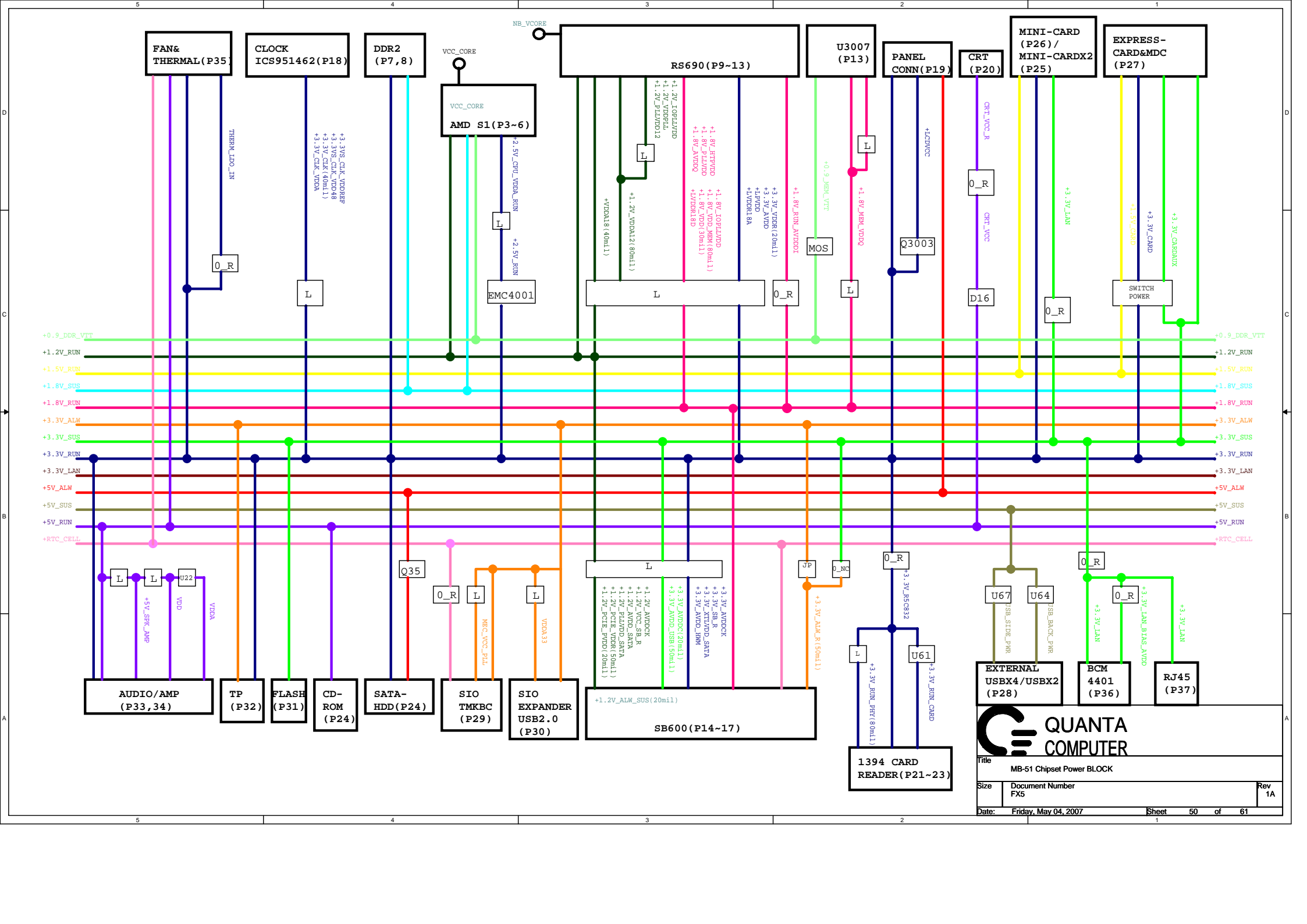
Size: FX5	Document Number: FX5	Rev: 1A
Date: Friday, May 04, 2007		Sheet: 47 of 61



Title SMBUS BLOCK		
Size FX5	Document Number FX5	Rev 1A
Date: Friday, May 04, 2007	Sheet 48	of 61

Power Design Block Diagram





QUANTA
COMPUTER

Title		MB-51 Chipset Power BLOCK
Size	Document Number	Rev
	FX5	1A
Date:	Friday, May 04, 2007	Sheet 50 of 61

