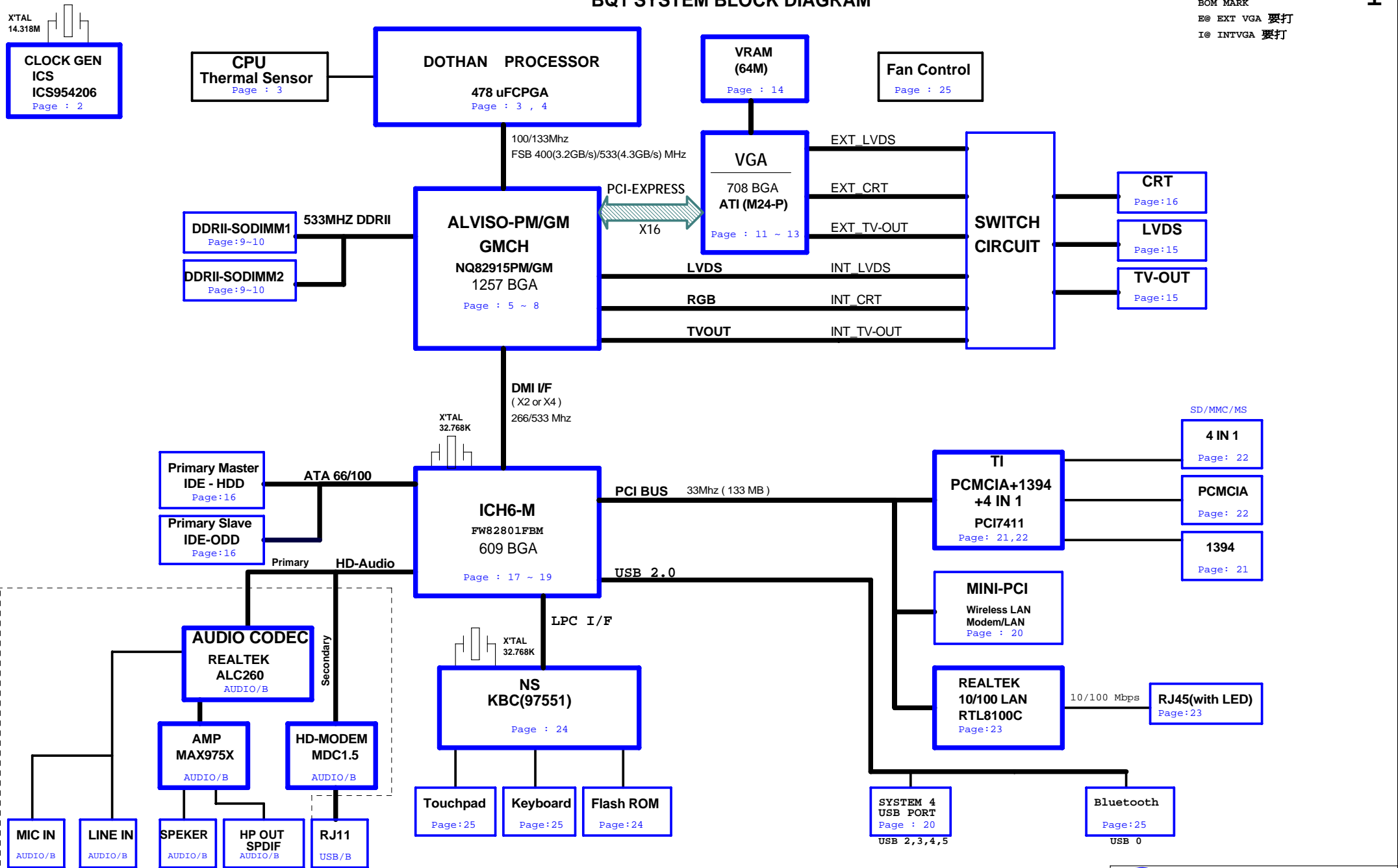


# BQ1 SYSTEM BLOCK DIAGRAM

BOM MARK  
 E@ EXT VGA 要打  
 I@ INTVGA 要打



Audio Board

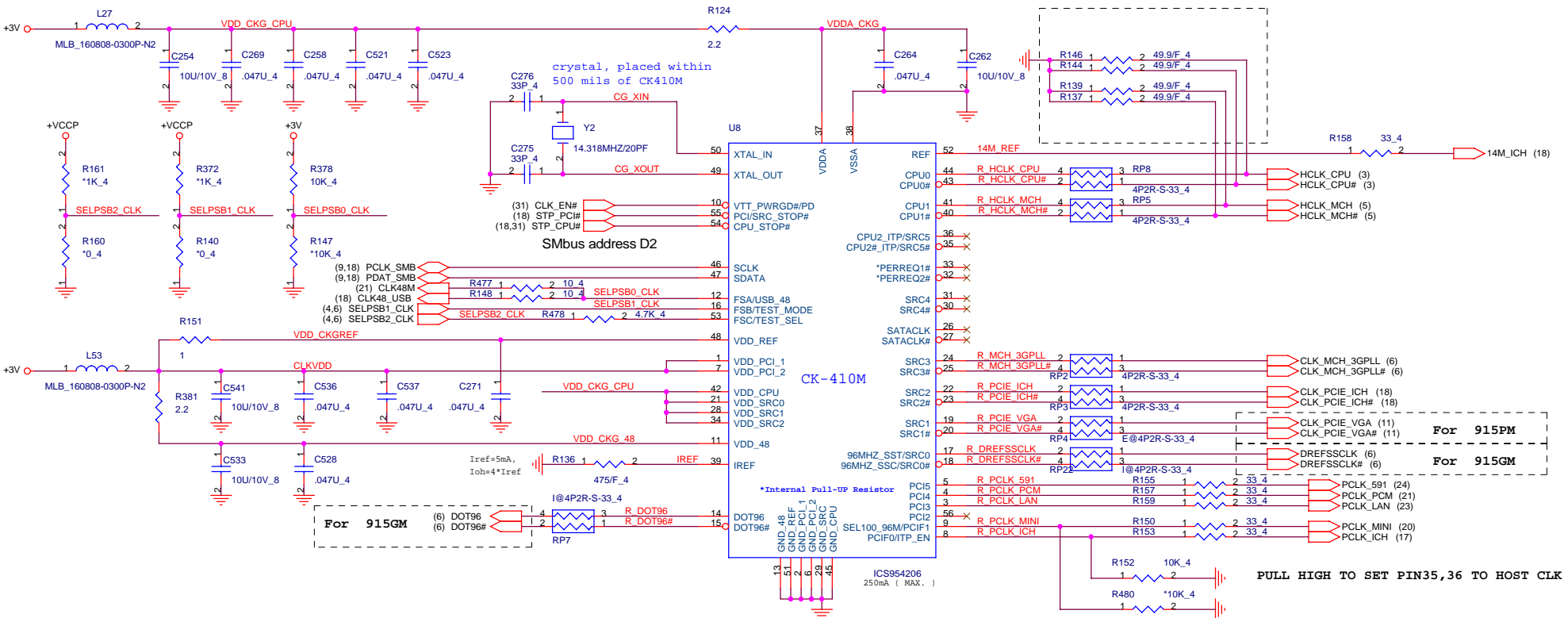
**PCI ROUTING TABLE**

REQ#	GNT#	IDSEL	INTERUPT	DEVICE
REQ0#	GNT0#	AD24	INTA#	REALTEK LAN
REQ2#	GNT2#	AD19	INTB# , INTD#	MINI-PCI
REQ1#	GNT1#	AD17	INTC#, INTD#, INTA#	TI 7411

**PROJECT : BQ1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>BLOCK DIAGRAM</b>	1A
Date:	Thursday, August 18, 2005	Sheet 1 of 32

Place these termination to close CK410M.



For 915GM (6) DOT96 (6) DOT96#

For 915PM CLK\_PCIE\_VGA (11) CLK\_PCIE\_VGA# (11) DREFSSCLK (6) DREFSSCLK# (6)

PULL HIGH TO SET PIN35,36 TO HOST CLK

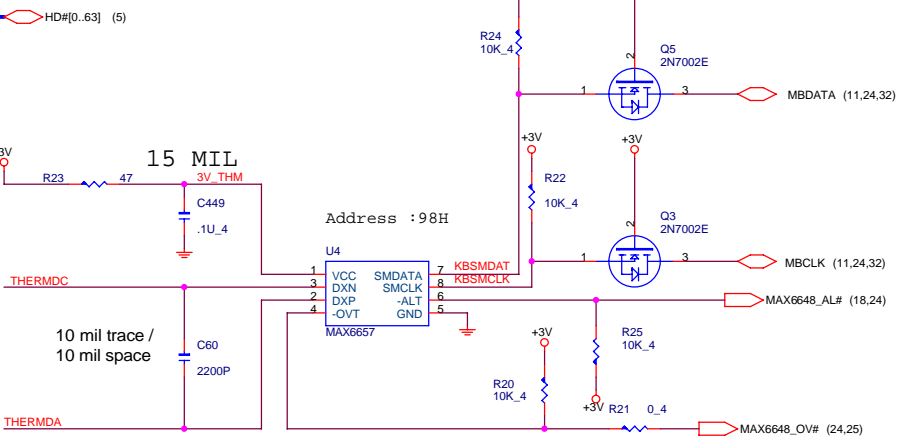
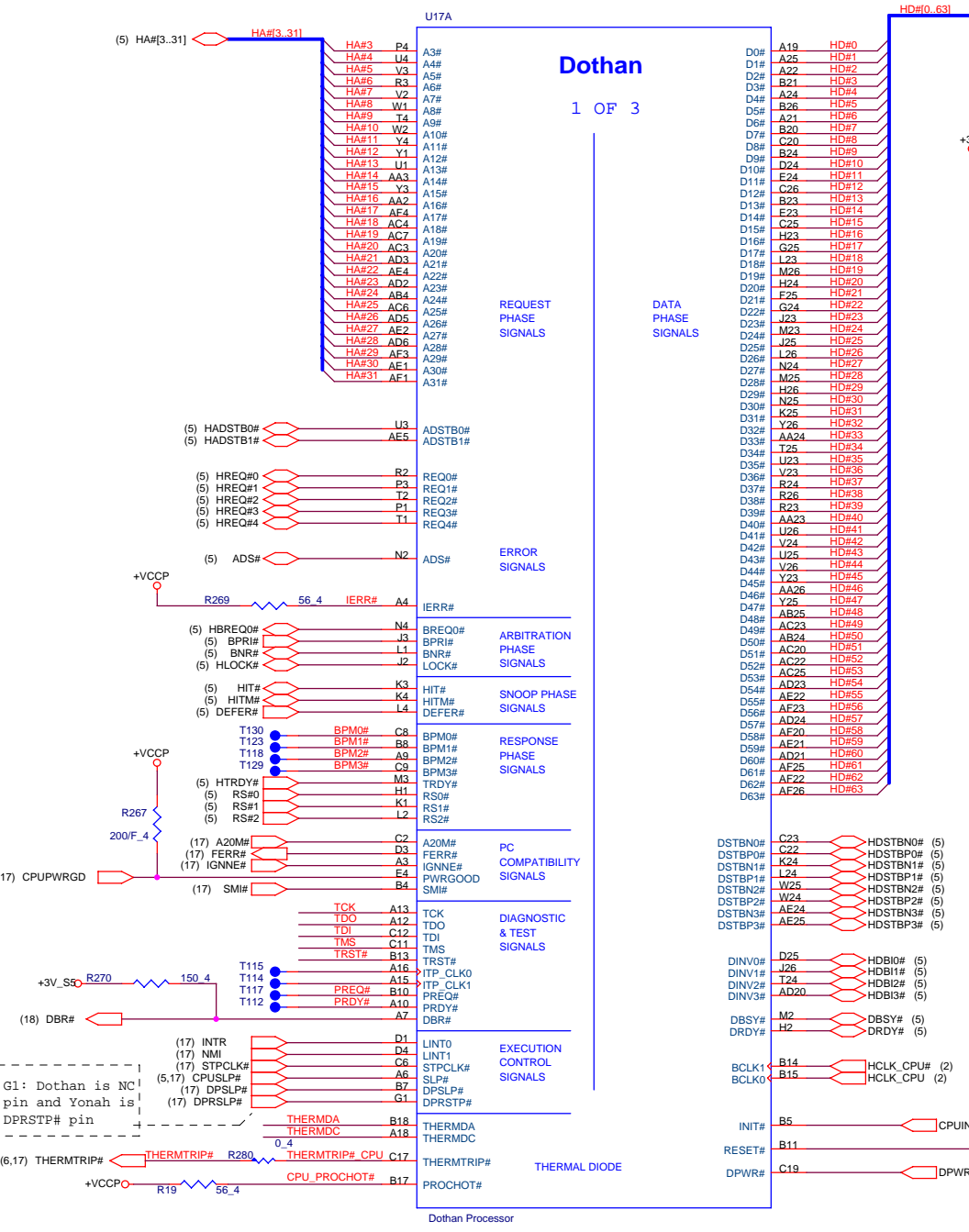
- DOT96 R529 1 2 I@49.9/F 4
- DOT96# R530 1 2 I@49.9/F 4
- CLK\_PCIE\_VGA R138 1 2 E@49.9/F 4
- CLK\_PCIE\_VGA# R135 1 2 E@49.9/F 4
- CLK\_MCH\_3GPLL R360 1 2 49.9/F 4
- CLK\_MCH\_3GPLL# R359 1 2 49.9/F 4
- DREFSSCLK R143 1 2 I@49.9/F 4
- DREFSSCLK# R141 1 2 I@49.9/F 4
- CLK\_PCIE\_ICH R367 1 2 49.9/F 4
- CLK\_PCIE\_ICH# R364 1 2 49.9/F 4

DOETHAN-A 400  
DOETHAN-A 533

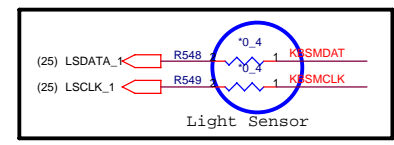
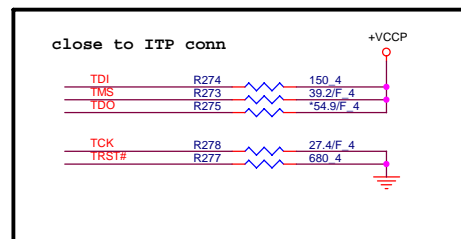
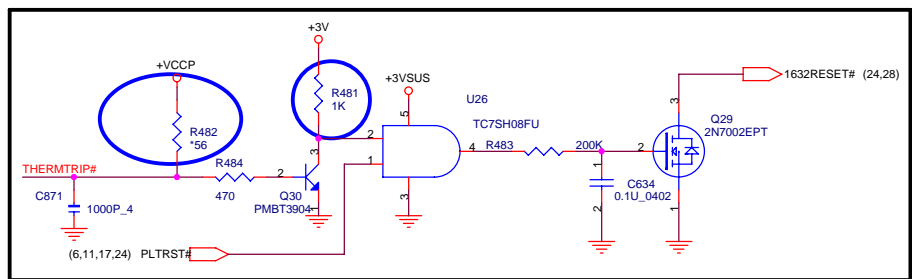
	FSC	FSB	FSA	CPU	SRC	PCI
DOETHAN-A 400	1	0	1	100	100	33
DOETHAN-A 533	0	0	1	133	100	33
	0	1	1	166	100	33
	0	1	0	200	100	33
	0	0	0	266	100	33
	1	0	0	333	100	33
	1	1	0	400	100	33
	1	1	1	RSVD	100	33

Place these termination to close CK410M.

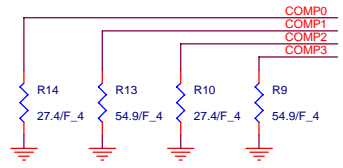




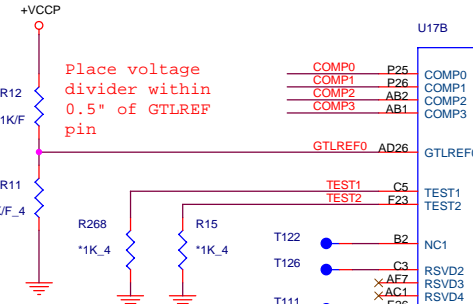
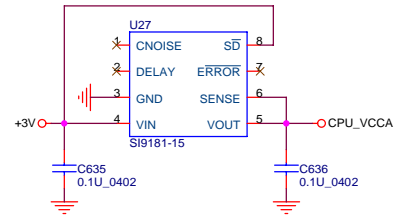
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	VTT	Within 2.0" of the CPU



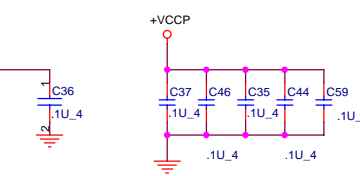
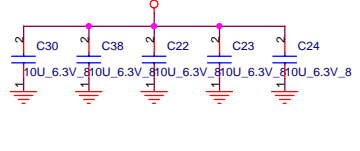
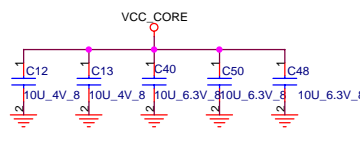
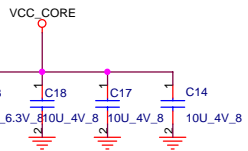
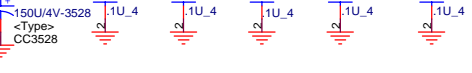
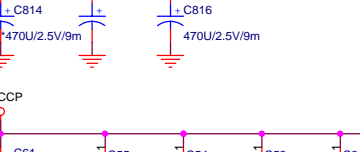
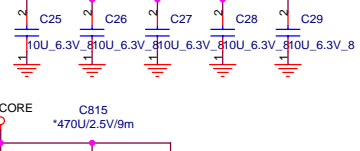
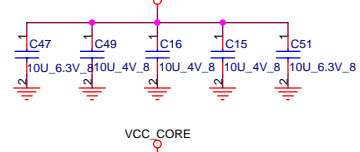
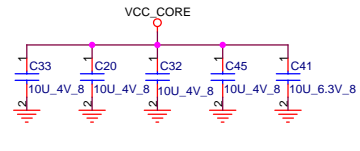
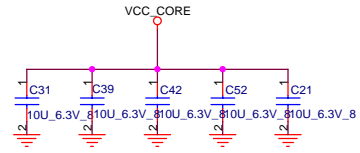
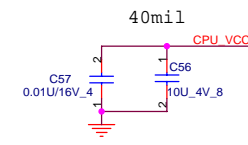
COMP0, COMP2 Trace should be 27.4 ± 15%  
COMP1, COMP3 Trace should be 55 ± 15%



Place pulldown resistors within 0.5" of COMP pins



Place voltage divider within 0.5" of GTLREF pin



**U17B**

COMP0	P25	VSS00	A2
COMP1	P26	VSS01	A5
COMP2	AB2	VSS02	A8
COMP3	AB1	VSS03	A11
		VSS04	A14
		VSS05	A17
		VSS06	A20
		VSS07	A23
		VSS08	A26
		VSS09	B3
		VSS10	B6
		VSS11	B9
		VSS12	B12
		VSS13	B15
		VSS14	B18
		VSS15	B21
		VSS16	B24
		VSS17	C1
		VSS18	C4
		VSS19	C7
		VSS20	C10
		VSS21	C13
		VSS22	C15
		VSS23	C18
		VSS24	C21
		VSS25	C24
		VSS26	D2
		VSS27	D5
		VSS28	D8
		VSS29	D11
		VSS30	D14
		VSS31	D17
		VSS32	D20
		VSS33	D23
		VSS34	D26
		VSS35	D29
		VSS36	D32
		VSS37	E3
		VSS38	E6
		VSS39	E9
		VSS40	E12
		VSS41	E15
		VSS42	E18
		VSS43	E21
		VSS44	E24
		VSS45	E27
		VSS46	E30
		VSS47	E33
		VSS48	E36
		VSS49	E39
		VSS50	E42
		VSS51	E45
		VSS52	E48
		VSS53	E51
		VSS54	E54
		VSS55	E57
		VSS56	E60
		VSS57	E63
		VSS58	E66
		VSS59	E69
		VSS60	E72
		VSS61	E75
		VSS62	E78
		VSS63	E81
		VSS64	E84
		VSS65	E87
		VSS66	E90
		VSS67	E93
		VSS68	E96
		VSS69	E99
		VSS70	J1
		VSS71	J4
		VSS72	J7
		VSS73	J10
		VSS74	J13
		VSS75	J16
		VSS76	J19
		VSS77	J22
		VSS78	J25
		VSS79	J28
		VSS80	J31
		VSS81	L3
		VSS82	L6
		VSS83	L9
		VSS84	L12
		VSS85	L15
		VSS86	L18
		VSS87	L21
		VSS88	L24
		VSS89	L27
		VSS90	L30
		VSS91	L33
		VSS92	L36
		VSS93	L39
		VSS94	L42
		VSS95	L45
		VSS96	L48
		VSS97	L51
		VSS98	L54
		VSS99	L57

**U17C**

D10	VCCP0	VSS120	W23
D12	VCCP1	VSS121	Y2
D14	VCCP2	VSS122	Y5
D16	VCCP3	VSS123	Y8
E11	VCCP4	VSS124	Y21
E13	VCCP5	VSS125	Y24
E15	VCCP6	VSS126	AA1
F10	VCCP7	VSS127	AA4
F12	VCCP8	VSS128	AA6
F14	VCCP9	VSS129	AA8
F16	VCCP10	VSS130	AA10
K6	VCCP11	VSS131	AA12
L5	VCCP12	VSS132	AA16
L21	VCCP13	VSS133	AA18
M6	VCCP14	VSS134	AA20
M22	VCCP15	VSS135	AA22
N2	VCCP16	VSS136	AA25
N6	VCCP17	VSS137	AB3
P6	VCCP18	VSS138	AB5
P22	VCCP19	VSS139	AB7
R5	VCCP20	VSS140	AB9
R21	VCCP21	VSS141	AB11
T6	VCCP22	VSS142	AB13
T2	VCCP23	VSS143	AB15
U21	VCCP24	VSS144	AB17
P23	VCCQ0	VSS145	AB19
W4	VCCQ1	VSS146	AB21
		VSS147	AB23
		VSS148	AB26
		VSS149	AC2
		VSS150	AC5
		VSS151	AC8
		VSS152	AC10
		VSS153	AC12
		VSS154	AC14
		VSS155	AC16
		VSS156	AC18
		VSS157	AC21
		VSS158	AC24
		VSS159	AD1
		VSS160	AD4
		VSS161	AD7
		VSS162	AD9
		VSS163	AD11
		VSS164	AD13
		VSS165	AD15
		VSS166	AD17
		VSS167	AD19
		VSS168	AD22
		VSS169	AD25
		VSS170	AE3
		VSS171	AE6
		VSS172	AE8
		VSS173	AE10
		VSS174	AE12
		VSS175	AE14
		VSS176	AE16
		VSS177	AE18
		VSS178	AE20
		VSS179	AE23
		VSS180	AE26
		VSS181	AF2
		VSS182	AF5
		VSS183	AF9
		VSS184	AF11
		VSS185	AF13
		VSS186	AF15
		VSS187	AF17
		VSS188	AF19
		VSS189	AF21
		VSS190	AF24
		VSS191	

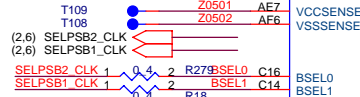
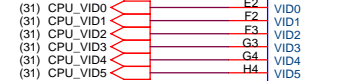
**Dothan**  
2 OF 3

POWER, GROUND, RESERVED SIGNALS

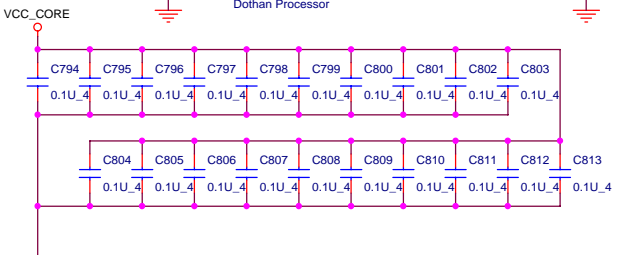
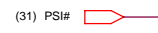
**Dothan**  
3 OF 3

POWER, GROUND AND NC

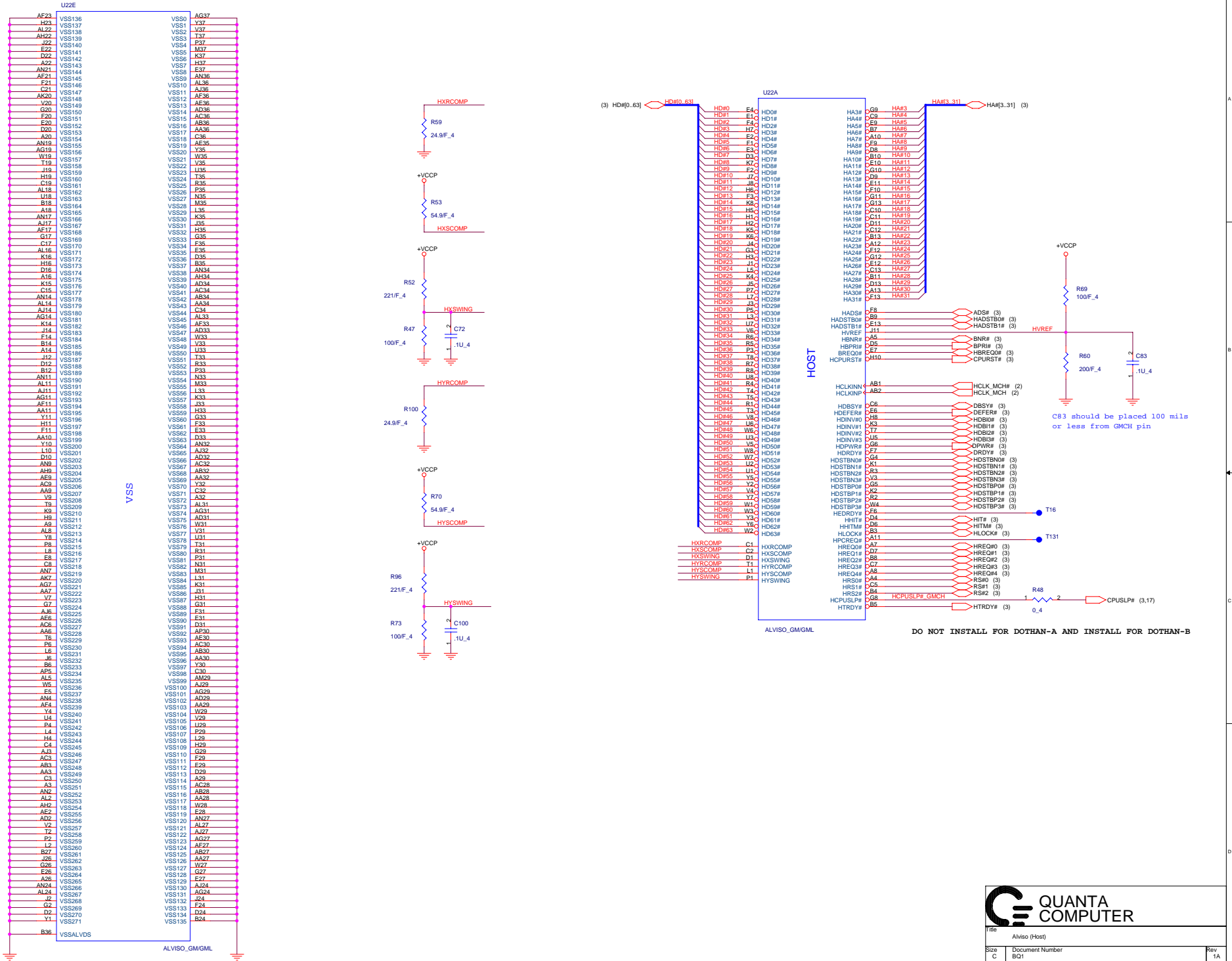
**VID**



**DOTHAN-A NC**  
**DOTHAN-B POP**  
06/21: Auto select



Title: Dothan Processor (POWER)		
Size:	Document Number: BQ1	Rev: 1A
Date:	Thursday, August 18, 2005	Sheet 4 of 32



**QUANTA COMPUTER**

Title: Alviso (Host)		
Size: C	Document Number: BQ1	Rev: 1A
Date: Thursday, August 18, 2005	Sheet: 5	of 32

I@ is only for Internal VGA;  
E@ is only for External VGA;

CFG3 R54 1K.4  
FOR DDR533  
CFG0:2=100 FOR FSB 533  
CFG0:2=101 FOR FSB 400

CFG5 Low=DMIX4 \*High=DMIX4  
CFG6 \*Low=DDR2 High=DDR  
CFG7 Low=Mobile Prescott \*High=Dothan  
CFG18 \*Low=CPU Core VCC 1.05V High=CPU Core VCC 1.5V

(11) GMCHEXP\_TXP0[0..15] GMCHEXP\_TXP0\_15  
(11) GMCHEXP\_TXN0[0..15] GMCHEXP\_TXN0\_15  
(11) GMCHEXP\_RXP0[0..15] GMCHEXP\_RXP0\_15  
(11) GMCHEXP\_RXN0[0..15] GMCHEXP\_RXN0\_15

VCC3G\_PCIE (1.5V)  
U2ZF

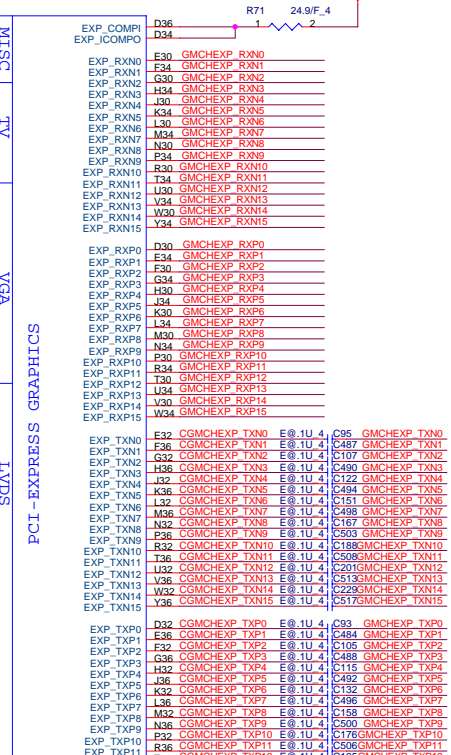
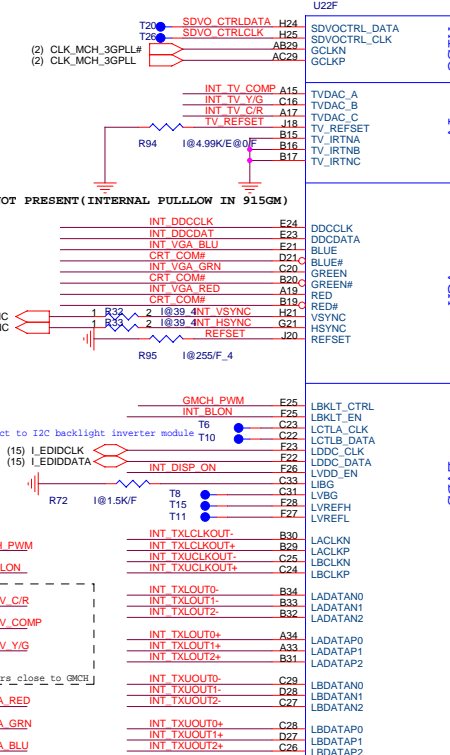
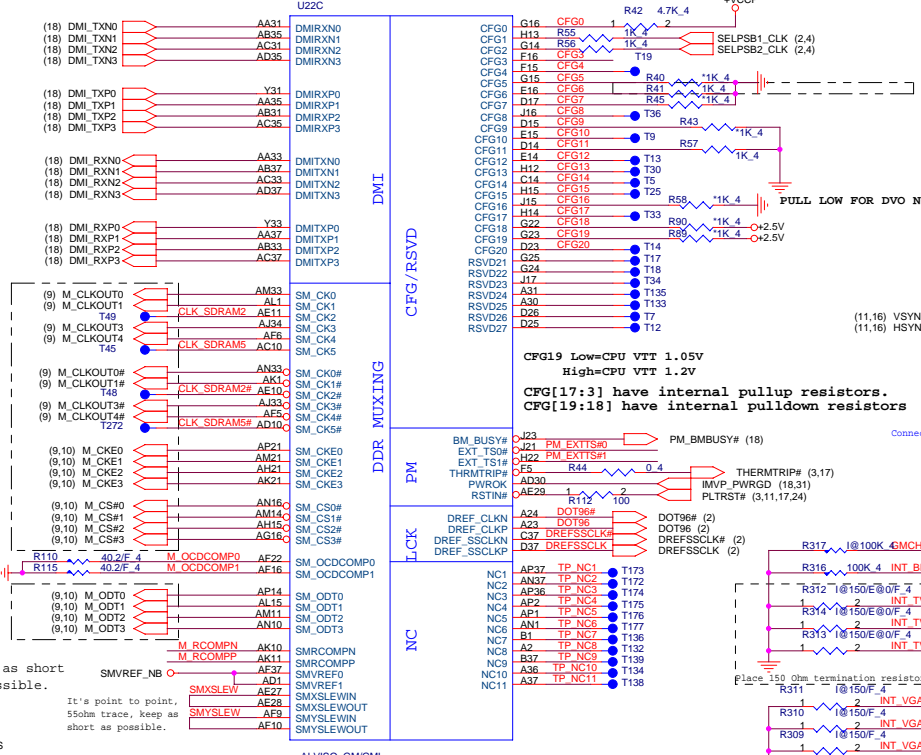
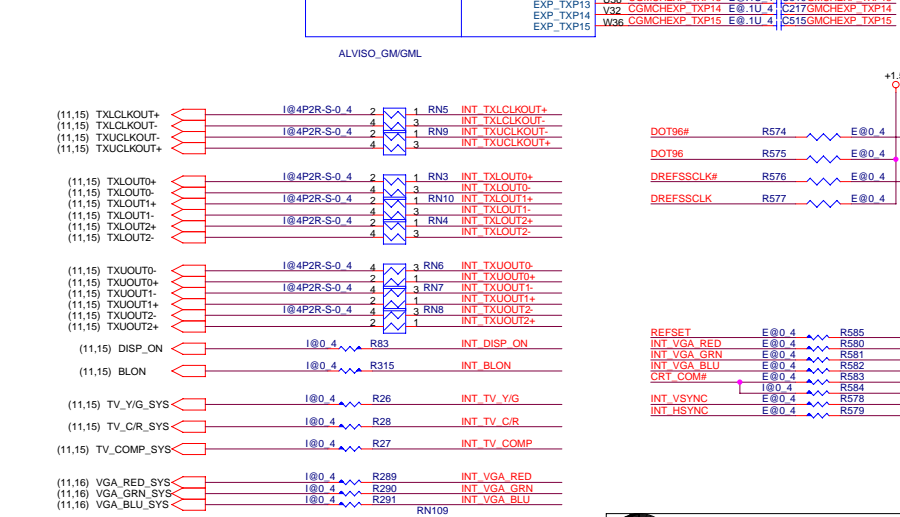
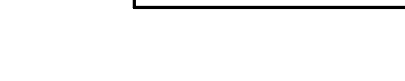
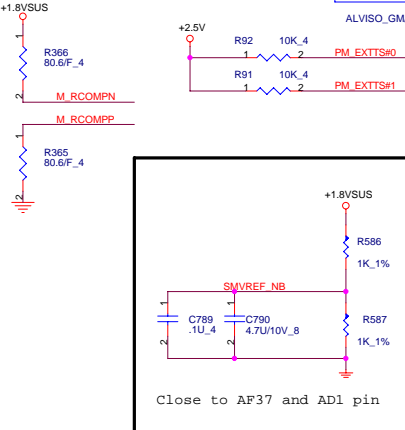


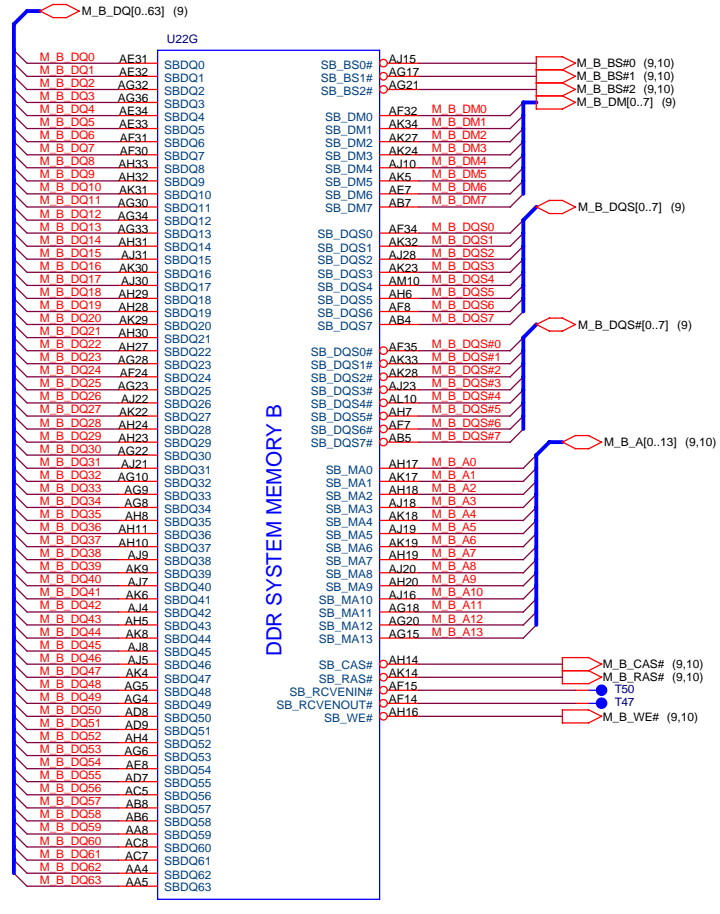
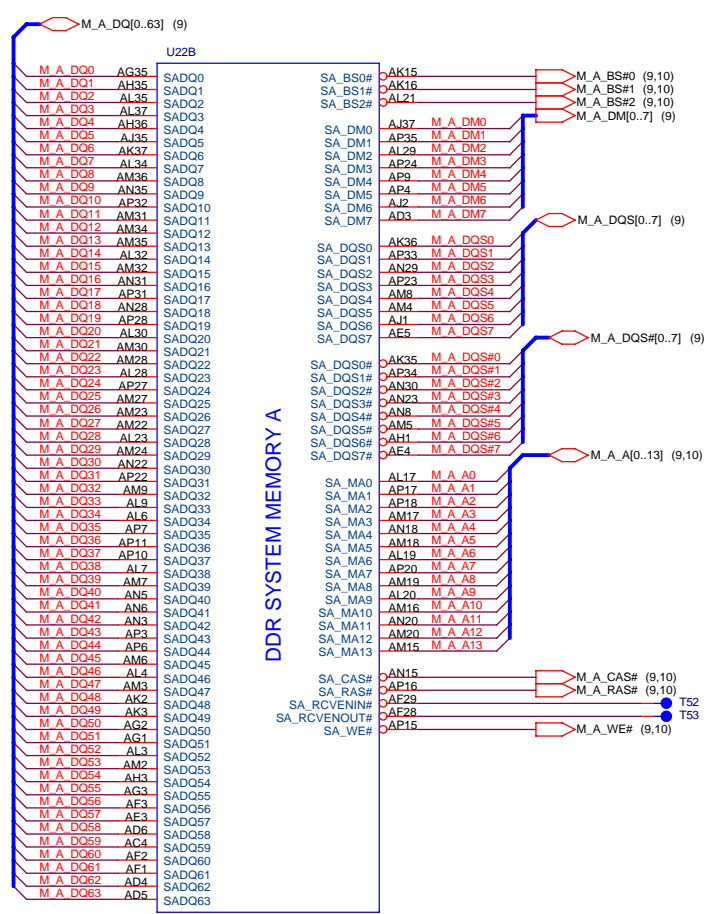
Table with 3 columns: Signal, 915GM, and 915PM. It lists various signals and their termination values for different CPU configurations.



Route as short as possible.  
SMVREF\_NB 0  
It's point to point, 550m trace, keep as short as possible.



QUANTA COMPUTER logo and product information including File name (Alviso (VGA,DMI)), Schematic Document Number (BO1), Date (Thursday, August 18, 2005), Sheet (6 of 32), and Revision (1A).



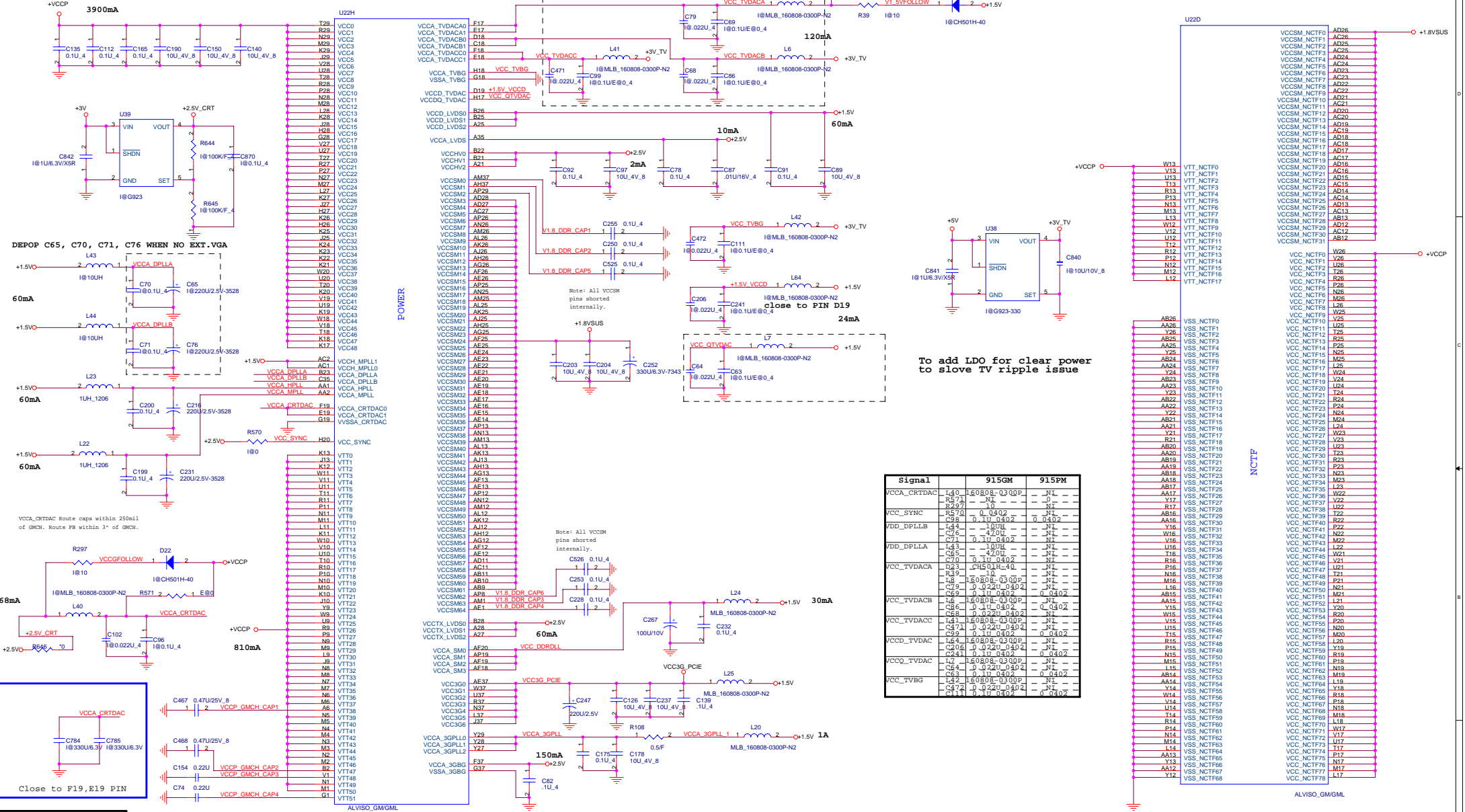
**QUANTA COMPUTER**

Title: Alviso (DDRII)

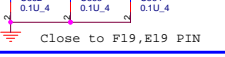
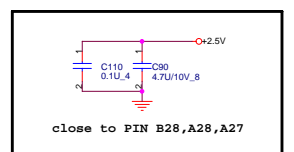
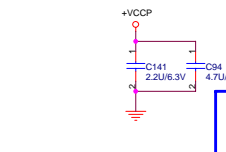
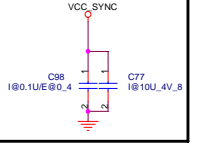
Size	Document Number	Rev
	BQ1	1A

Date: Thursday, August 18, 2005 Sheet 7 of 32

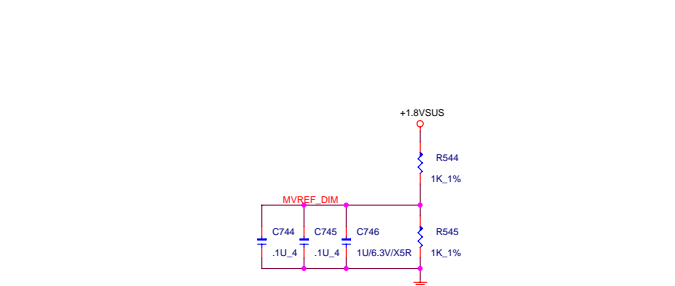
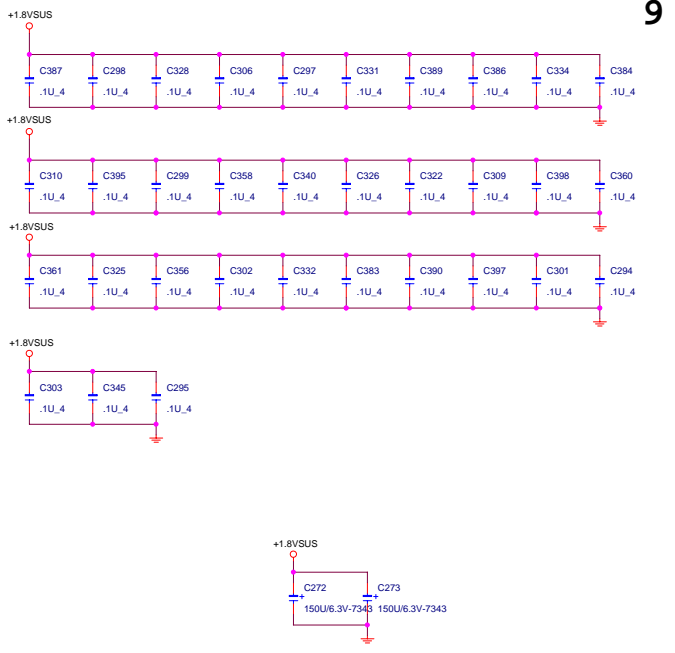
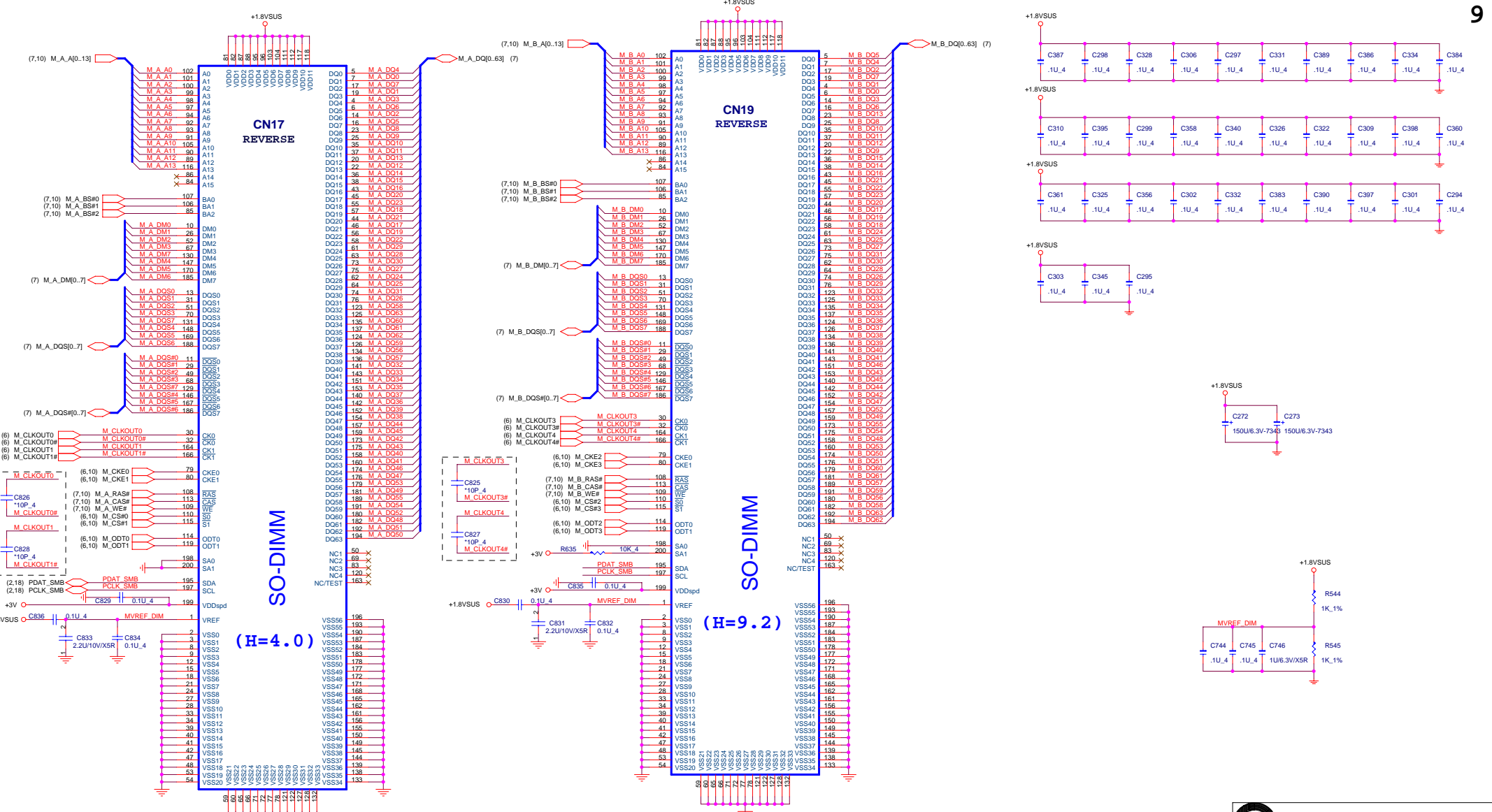
I@ is only for Internal VGA;  
E@ is only for External VGA;



Signal	915GM	915PM
VCCA_CRTDAC	L40 1.60808-0.300P	NI
VCC_SYNC	R571 0 0.0402	NI
VDD_DPLLLB	R297 0 0.0402	NI
VDD_DPLLA	R570 0 0.0402	NI
VCC_TVDACA	R39 1.0 0.0402	NI
VCC_TVDACB	L8 1.60808-0.300P	NI
VCC_TVDACC	C68 0.22u 0.402	NI
VCCD_TVDAC	C99 0.1u 0.402	NI
VCCQ_TVDAC	C64 0.22u 0.402	NI
VCC_TVDBG	C71 0.1u 0.402	NI







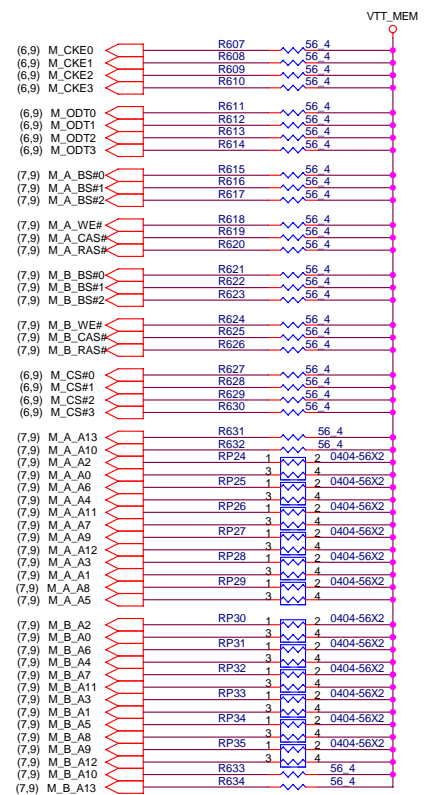
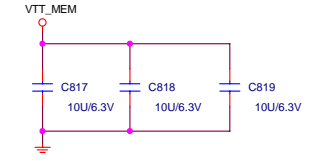
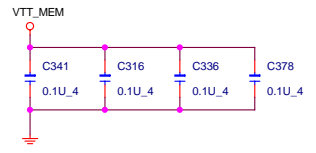
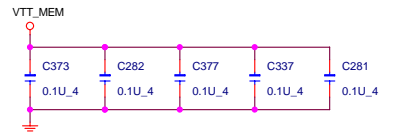
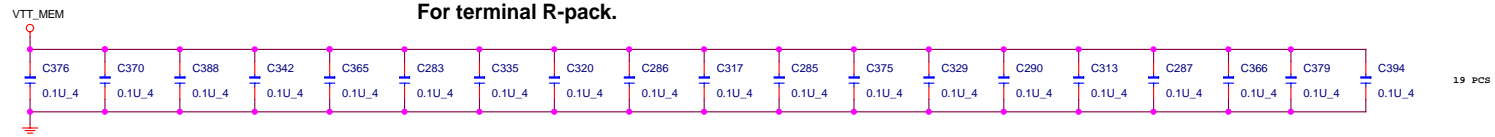
QUANTA  
COMPUTER

Title: DDR SO-DIMM (200P)

Size: Document Number BQ1 Rev 1A

Date: Thursday, August 18, 2005 Sheet 9 of 32

For terminal R-pack.



**QUANTA COMPUTER**

Title: DDRII TERMINATION

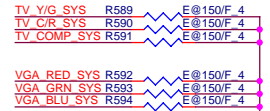
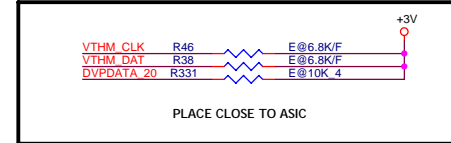
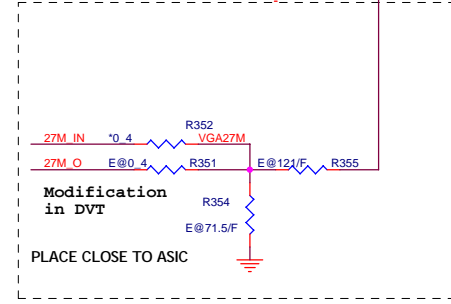
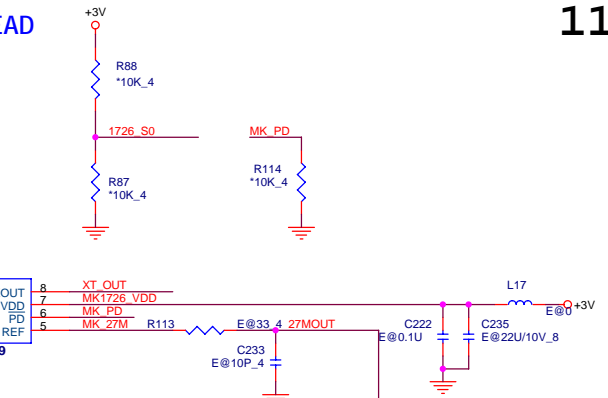
Size	Document Number	Rev
	BQ1	1A

Date: Thursday, August 18, 2005 Sheet 10 of 32

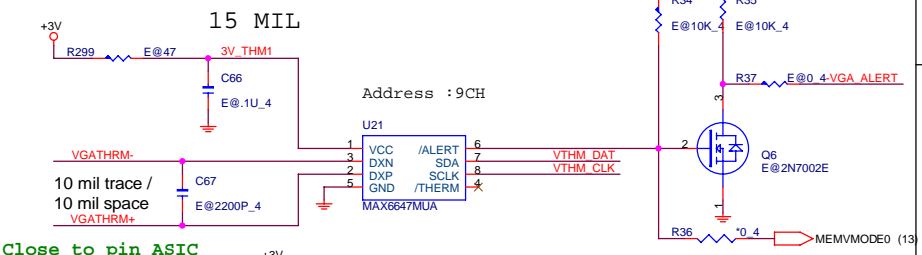
### MEMORY CLOCK SPREAD SPECTRUM

SRS = 1 DOWN -2.5%  
0 DOWN -1.8%  
M DOWN -0.6%

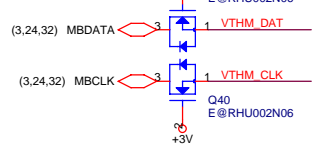
VGA\_PWR to control 1.0V/1.2V



ADD ON 2/21



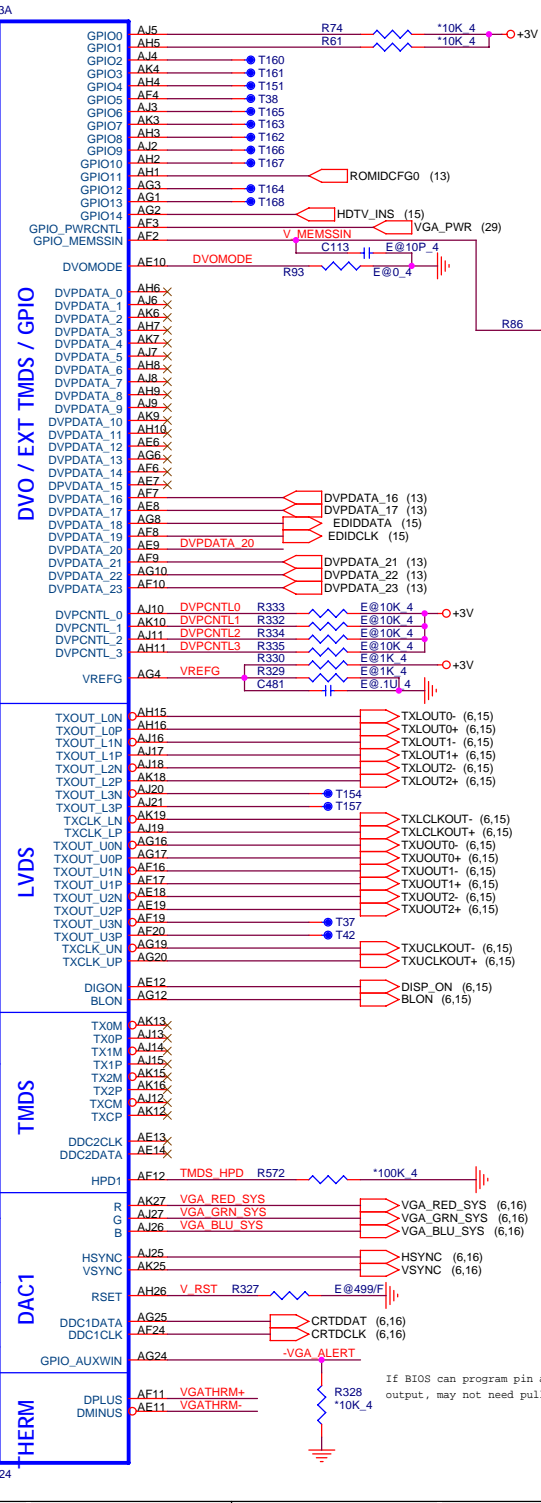
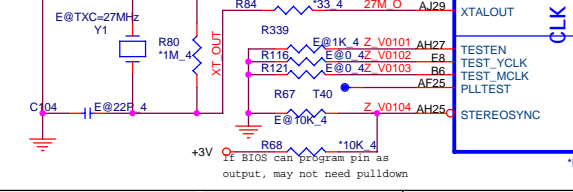
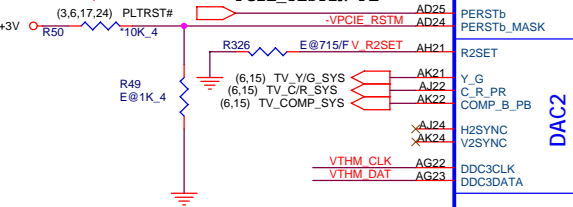
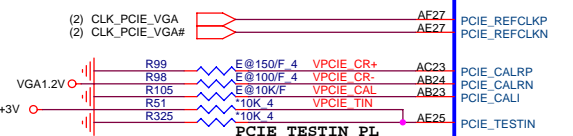
Close to pin ASIC



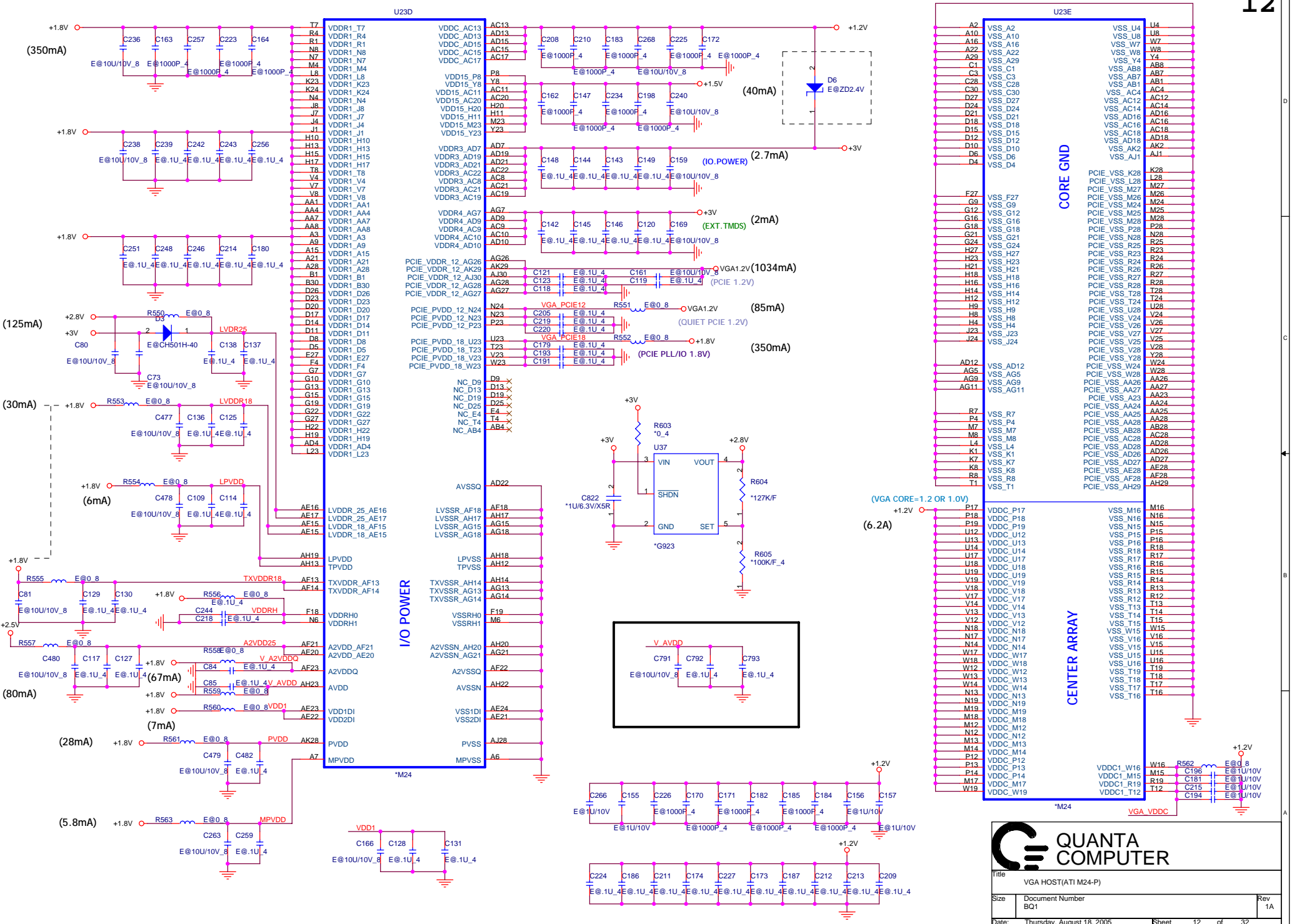
Title: VGA HOST(ATI M24-P)		
Size:	Document Number: BQ1	Rev: 1A
Date:	Thursday, August 18, 2005	Sheet 11 of 32

(6) GMCHEXP_TXP[0..15]	GMCHEXP_TXP0 AH30	PCIE_RX0P
	GMCHEXP_TXN0 AG30	PCIE_RX0N
	GMCHEXP_TXP1 AG29	PCIE_RX1P
	GMCHEXP_TXN1 AF29	PCIE_RX1N
(6) GMCHEXP_TXN[0..15]	GMCHEXP_TXP2 AF29	PCIE_RX2P
	GMCHEXP_TXN2 AE30	PCIE_RX2N
	GMCHEXP_TXP3 AD30	PCIE_RX3P
	GMCHEXP_TXN3 AD29	PCIE_RX3N
(6) GMCHEXP_RXP[0..15]	GMCHEXP_TXP4 AC29	PCIE_RX4P
	GMCHEXP_TXN4 AB30	PCIE_RX4N
	GMCHEXP_TXP5 AB30	PCIE_RX5P
	GMCHEXP_TXN5 AA30	PCIE_RX5N
(6) GMCHEXP_RXN[0..15]	GMCHEXP_TXP6 AA29	PCIE_RX6P
	GMCHEXP_TXN6 Y28	PCIE_RX6N
	GMCHEXP_TXP7 W28	PCIE_RX7P
	GMCHEXP_TXN7 W30	PCIE_RX7N
	GMCHEXP_TXP8 V30	PCIE_RX8P
	GMCHEXP_TXN8 V29	PCIE_RX8N
	GMCHEXP_TXP9 U29	PCIE_RX9P
	GMCHEXP_TXN9 T28	PCIE_RX9N
	GMCHEXP_TXP10 T28	PCIE_RX10P
	GMCHEXP_TXN10 R30	PCIE_RX10N
	GMCHEXP_TXP11 R29	PCIE_RX11P
	GMCHEXP_TXN11 P29	PCIE_RX11N
	GMCHEXP_TXP12 N28	PCIE_RX12P
	GMCHEXP_TXN12 N30	PCIE_RX12N
	GMCHEXP_TXP13 M30	PCIE_RX13P
	GMCHEXP_TXN13 M29	PCIE_RX13N
	GMCHEXP_TXP14 L29	PCIE_RX14P
	GMCHEXP_TXN14 K28	PCIE_RX14N
	GMCHEXP_TXP15 K30	PCIE_RX15P
	GMCHEXP_TXN15 J30	PCIE_RX15N

GMCHEXP_RXP0 C485	E@1.0V 4V GMCHEXP_RXP0 AF26	PCIE_TX0P
GMCHEXP_RXN0 C486	E@1.0V 4V GMCHEXP_RXN0 AF26	PCIE_TX0N
GMCHEXP_RXP1 C489	E@1.0V 4V GMCHEXP_RXP1 AB25	PCIE_TX1P
GMCHEXP_RXN1 C491	E@1.0V 4V GMCHEXP_RXN1 AB25	PCIE_TX1N
GMCHEXP_RXP2 C106	E@1.0V 4V GMCHEXP_RXP2 AC27	PCIE_TX2P
GMCHEXP_RXN2 C108	E@1.0V 4V GMCHEXP_RXN2 AB27	PCIE_TX2N
GMCHEXP_RXP3 C493	E@1.0V 4V GMCHEXP_RXP3 AC26	PCIE_TX3P
GMCHEXP_RXN3 C495	E@1.0V 4V GMCHEXP_RXN3 AB26	PCIE_TX3N
GMCHEXP_RXP4 C116	E@1.0V 4V GMCHEXP_RXP4 W25	PCIE_TX4P
GMCHEXP_RXN4 C124	E@1.0V 4V GMCHEXP_RXN4 W25	PCIE_TX4N
GMCHEXP_RXP5 C497	E@1.0V 4V GMCHEXP_RXP5 Y27	PCIE_TX5P
GMCHEXP_RXN5 C499	E@1.0V 4V GMCHEXP_RXN5 W27	PCIE_TX5N
GMCHEXP_RXP6 C133	E@1.0V 4V GMCHEXP_RXP6 Y26	PCIE_TX6P
GMCHEXP_RXN6 C152	E@1.0V 4V GMCHEXP_RXN6 W26	PCIE_TX6N
GMCHEXP_RXP7 C501	E@1.0V 4V GMCHEXP_RXP7 U25	PCIE_TX7P
GMCHEXP_RXN7 C504	E@1.0V 4V GMCHEXP_RXN7 T25	PCIE_TX7N
GMCHEXP_RXP8 C160	E@1.0V 4V GMCHEXP_RXP8 U27	PCIE_TX8P
GMCHEXP_RXN8 C168	E@1.0V 4V GMCHEXP_RXN8 T27	PCIE_TX8N
GMCHEXP_RXP9 C507	E@1.0V 4V GMCHEXP_RXP9 U26	PCIE_TX9P
GMCHEXP_RXN9 C509	E@1.0V 4V GMCHEXP_RXN9 T26	PCIE_TX9N
GMCHEXP_RXP10 C177	E@1.0V 4V GMCHEXP_RXP10 P25	PCIE_TX10P
GMCHEXP_RXN10 C189	E@1.0V 4V GMCHEXP_RXN10 N25	PCIE_TX10N
GMCHEXP_RXP11 C511	E@1.0V 4V GMCHEXP_RXP11 P27	PCIE_TX11P
GMCHEXP_RXN11 C514	E@1.0V 4V GMCHEXP_RXN11 N27	PCIE_TX11N
GMCHEXP_RXP12 C197	E@1.0V 4V GMCHEXP_RXP12 P26	PCIE_TX12P
GMCHEXP_RXN12 C192	E@1.0V 4V GMCHEXP_RXN12 N26	PCIE_TX12N
GMCHEXP_RXP13 C516	E@1.0V 4V GMCHEXP_RXP13 L25	PCIE_TX13P
GMCHEXP_RXN13 C518	E@1.0V 4V GMCHEXP_RXN13 K25	PCIE_TX13N
GMCHEXP_RXP14 C221	E@1.0V 4V GMCHEXP_RXP14 K27	PCIE_TX14P
GMCHEXP_RXN14 C230	E@1.0V 4V GMCHEXP_RXN14 K27	PCIE_TX14N
GMCHEXP_RXP15 C519	E@1.0V 4V GMCHEXP_RXP15 L26	PCIE_TX15P
GMCHEXP_RXN15 C520	E@1.0V 4V GMCHEXP_RXN15 K26	PCIE_TX15N

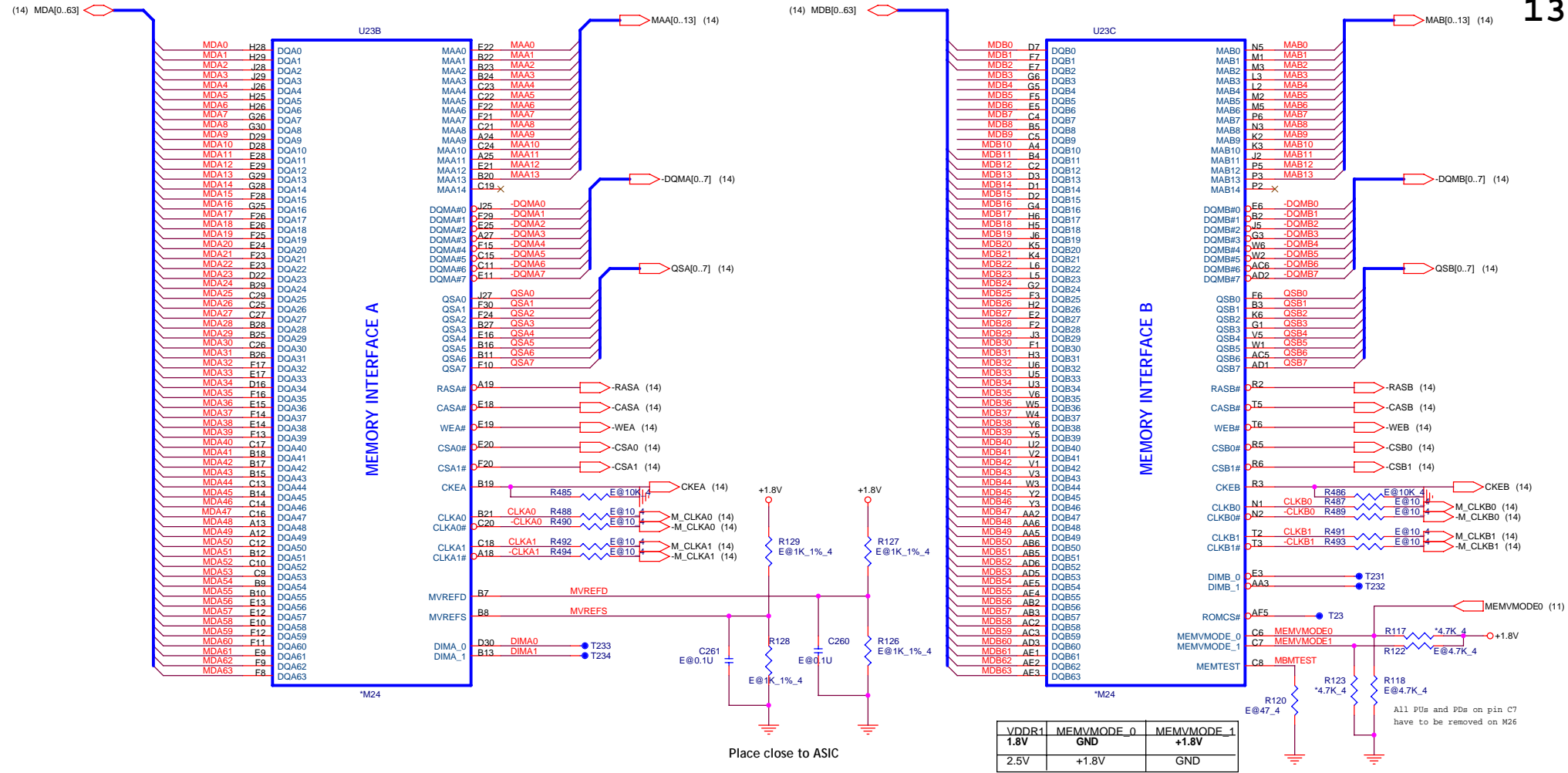


If BIOS can program pin as output, may not need pulldown



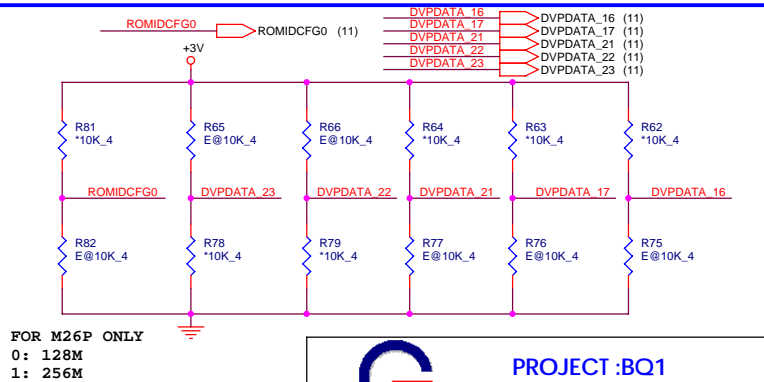
**QUANTA COMPUTER**

Title: VGA HOST(ATI M24-P)		
Size:	Document Number: BQ1	Rev: 1A
Date:	Thursday, August 18, 2005	Sheet: 12 of 32



**STRAPS PIN**

GPIO_0	PCI-Express Current Calibration Bandgap Backup 0: use reference voltage from Bandgap 1: use reference voltage from resistor divider	GPIO_6	PCI-Express transmitter current compensation 0: Normal 1: Inject extra current for output buffer switching
GPIO_1	PCI-Express PLL Calibration force enable 0: Disable PLL force calibration 1: Enable PLL force calibration	GPIO_8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible
GPIO_(3,2)	00: PCI Express 1.0 mode 01: RESERVED 10: PCI Express 1.0 mode 11: RESERVED	GPIO(9,13:11)	ROMIDCFG 0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 1000: Parallel ROM, Chip ID's from ROM 1000: Parallel ROM, Chip ID's from ROM
GPIO_4	Turn off PCI-Express impedance / strength calibration 0: enable 1: disable	DVPDATA_21-23	MEM TYPE DVPDATA_21: 0=4Mx32 1=8Mx32 DVPDATA_22: 0=128M 1=64M DVPDATA_23: 0=Hynix 1=Samsung
GPIO_5	Bypass PCI-Express PLL		



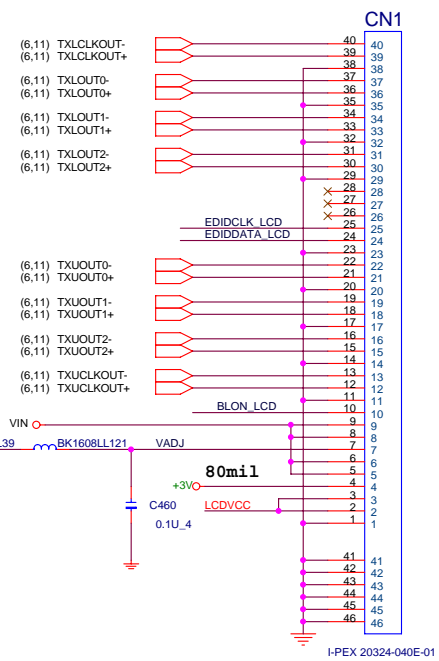
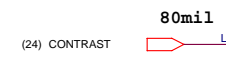
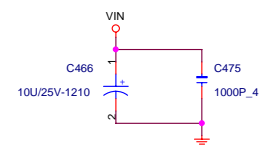
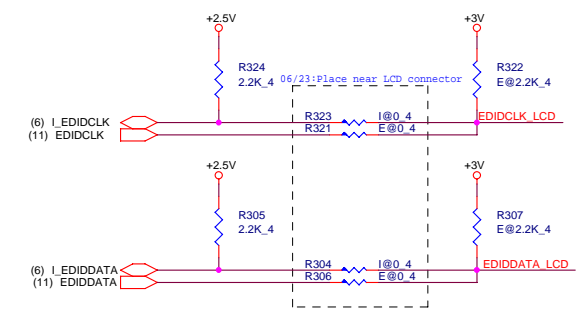
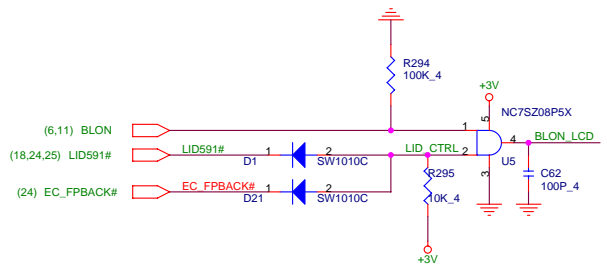
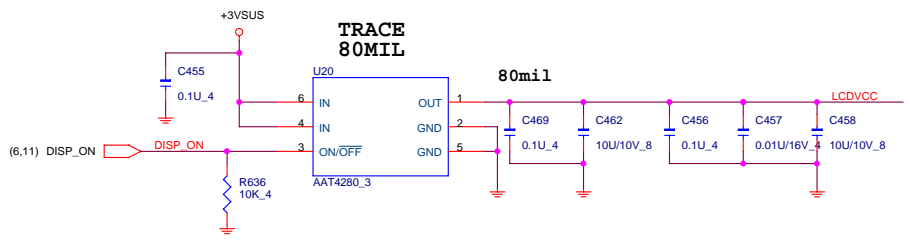
FOR M26P ONLY  
0: 128M  
1: 256M

**PROJECT :BQ1**  
**Quanta Computer Inc.**

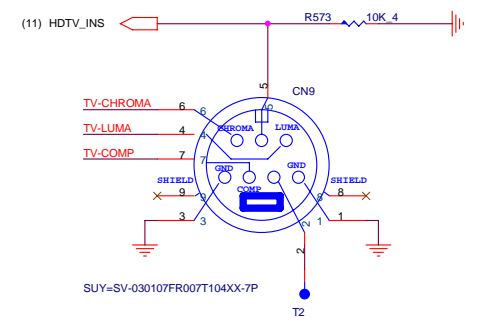
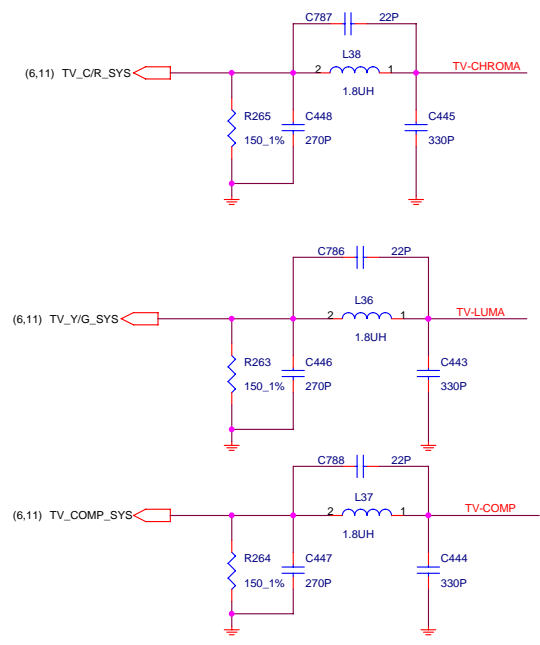
Size Custom | Document Number | Rev 1A  
**ATI M24-P MEM/STRAPS**

Date: Thursday, August 18, 2005 | Sheet 13 of 32



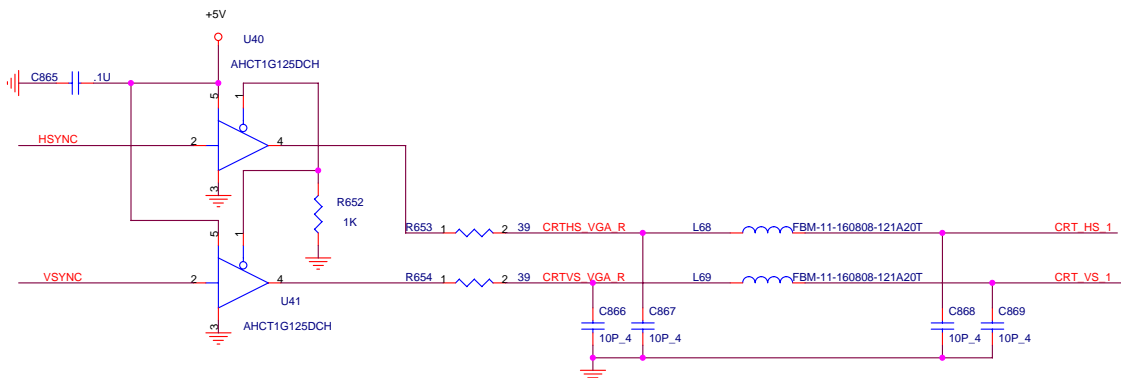
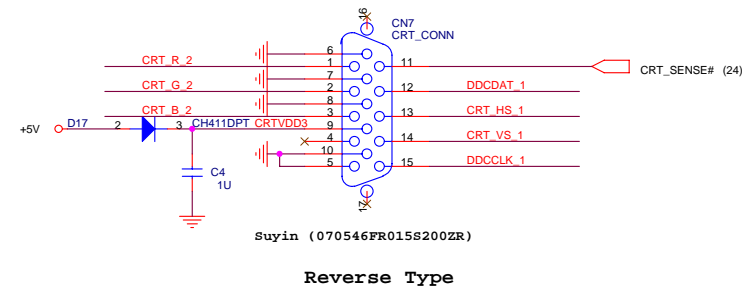
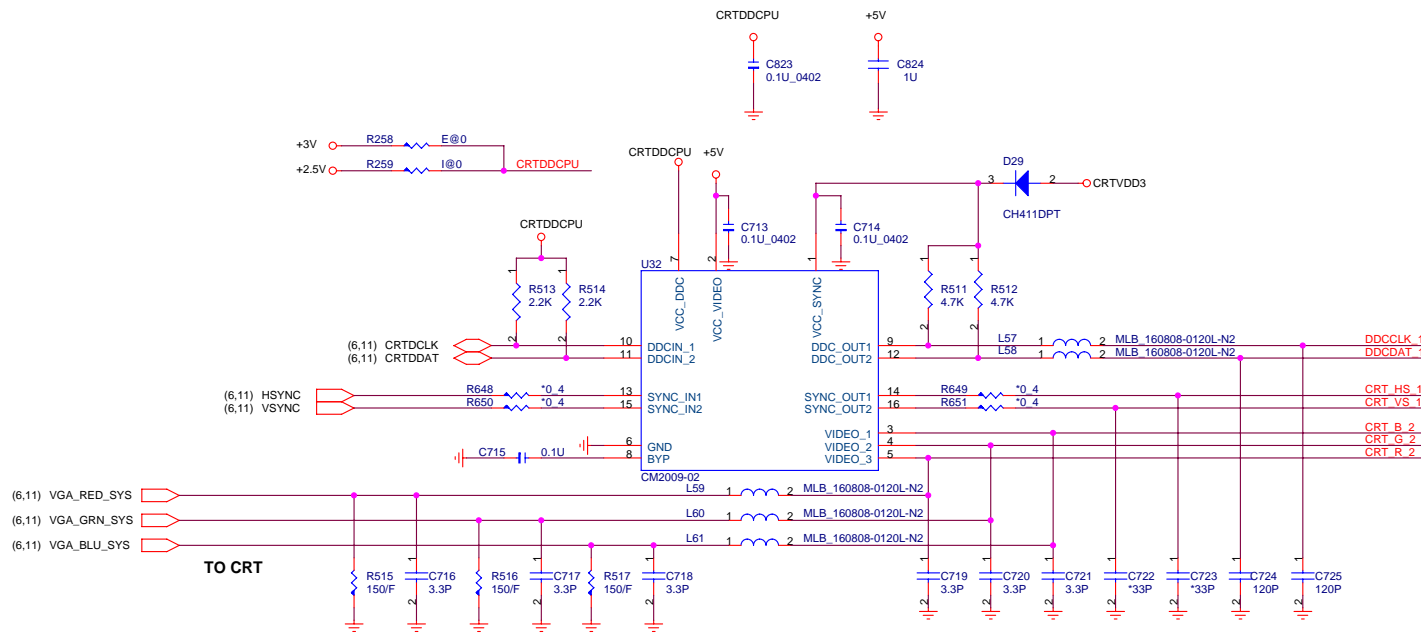


# S-Video



**PROJECT : BQ1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>LVDS &amp; S-VIDEO</b>	1A
Date:	Thursday, August 18, 2005	Sheet 15 of 32

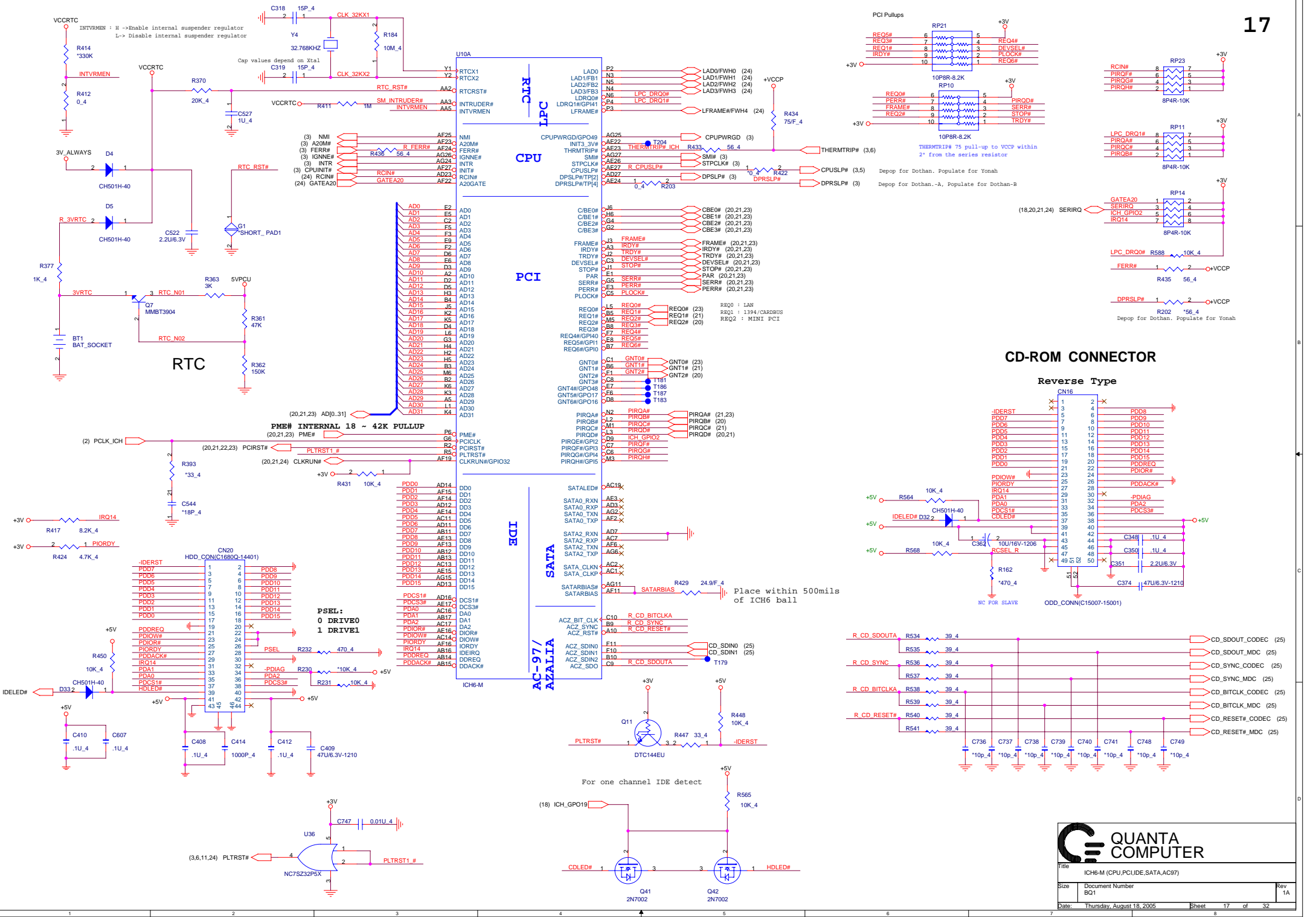


33BQ1AB0002  
43BQ1SS0007

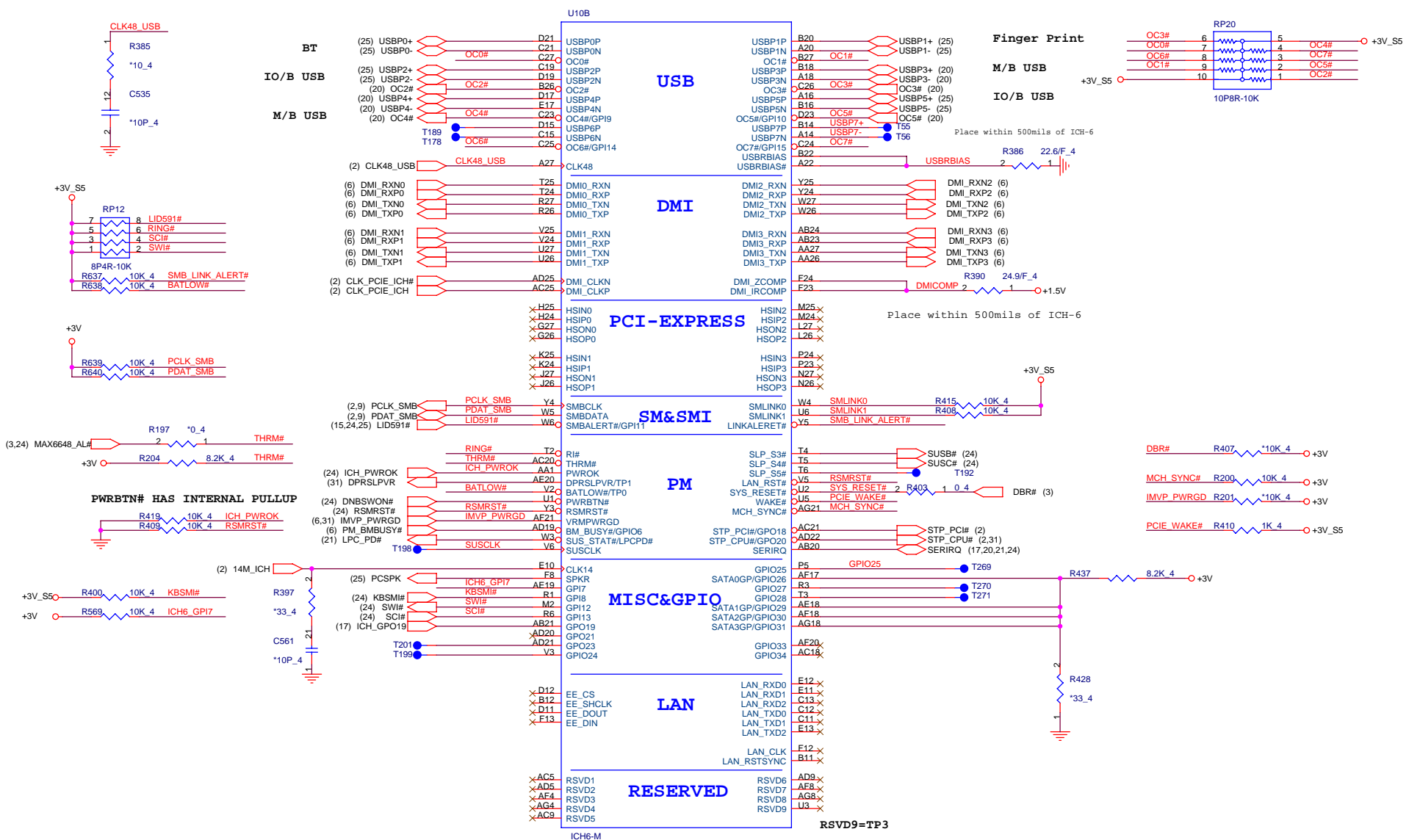
**PROJECT : BQ1**  
**Quanta Computer Inc.**


Size	Document Number	Rev
	CRT	1A
Date:	Thursday, August 18, 2005	Sheet 16 of 32





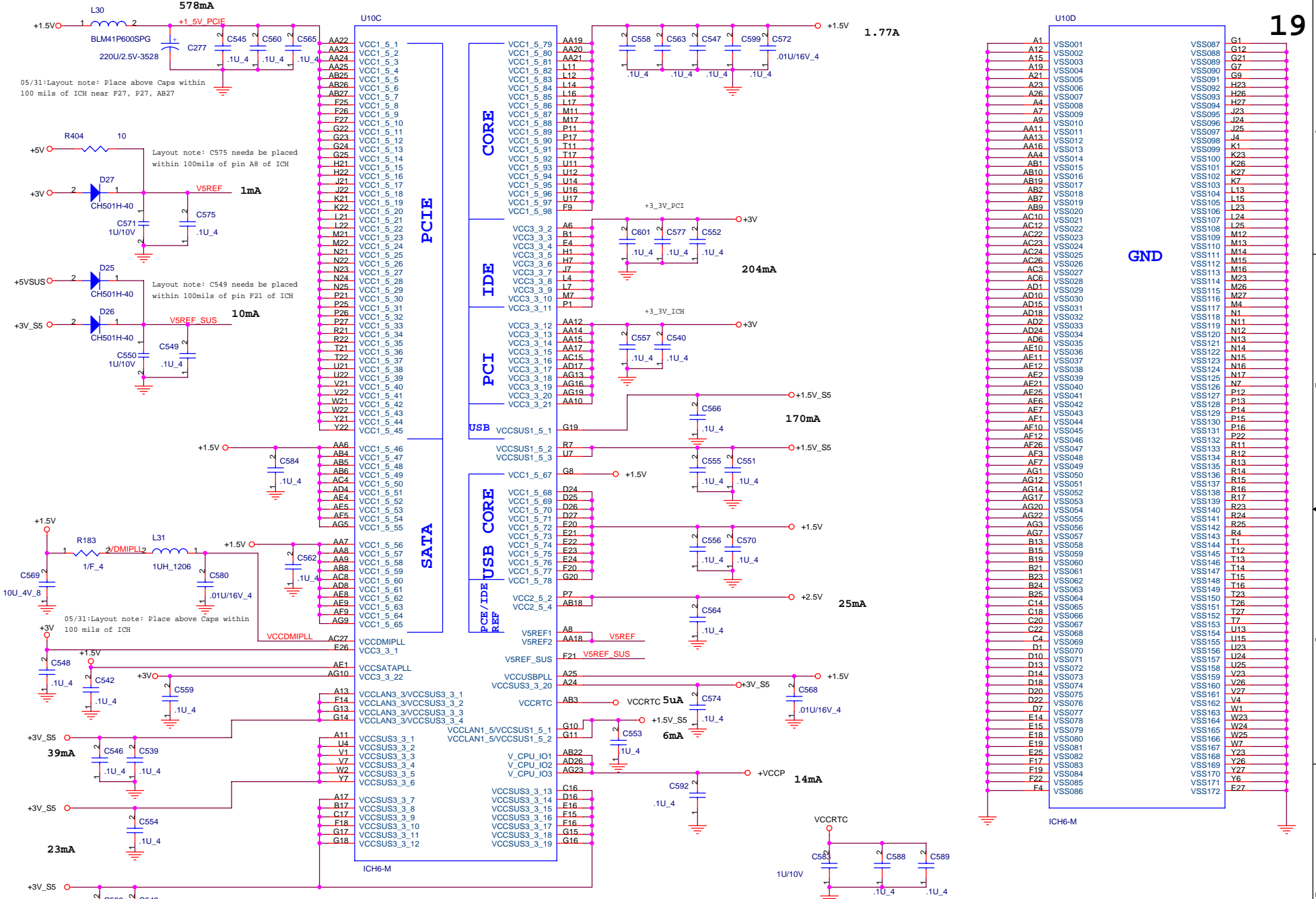
Title		ICH6-M (CPU,P.C.I./L.I.D.E./S.A.T.A./A.Z.A.L.I.A.)	
Size	Document Number	Rev	
	BC1	1A	
Date:	Thursday, August 18, 2005	Sheet	17 of 32





# QUANTA COMPUTER

Title			IC#6-M (USB,DMI,LPC)		
Size	Document Number				Rev
	BQ1				1A
Date:	Thursday, August 18, 2005		Sheet	18 of 32	



**QUANTA COMPUTER**

Title: ICH6-M (POWER&GND)

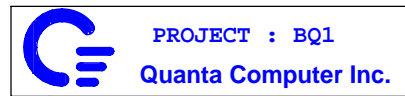
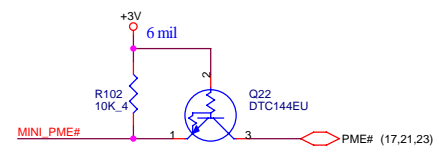
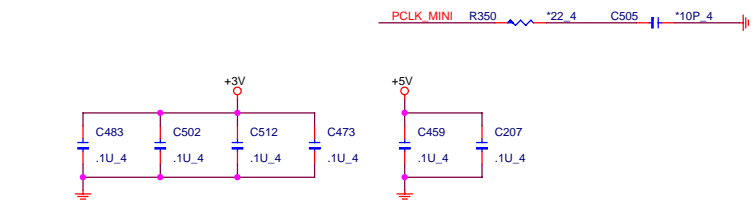
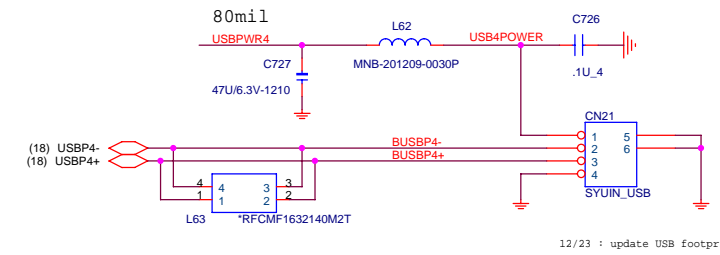
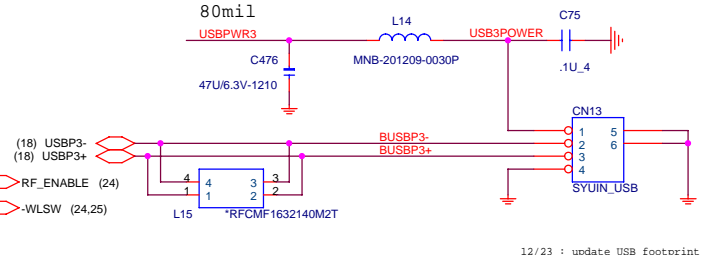
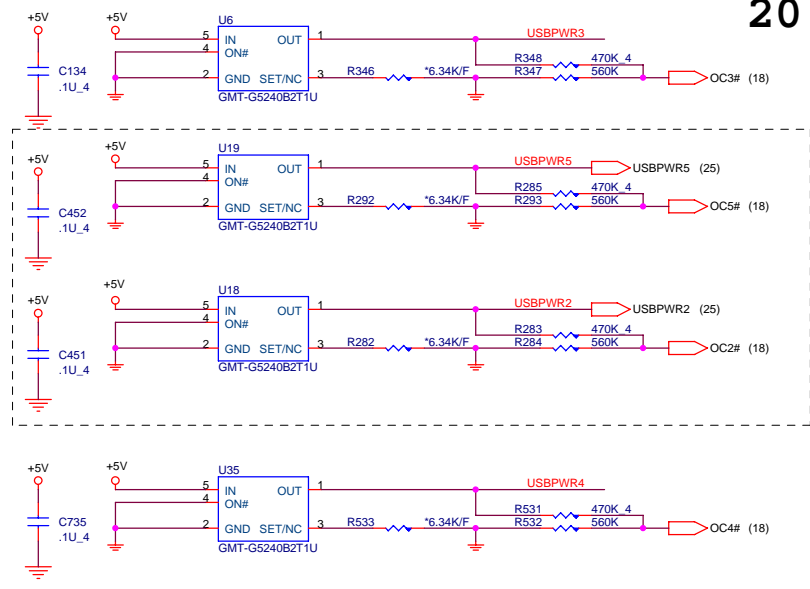
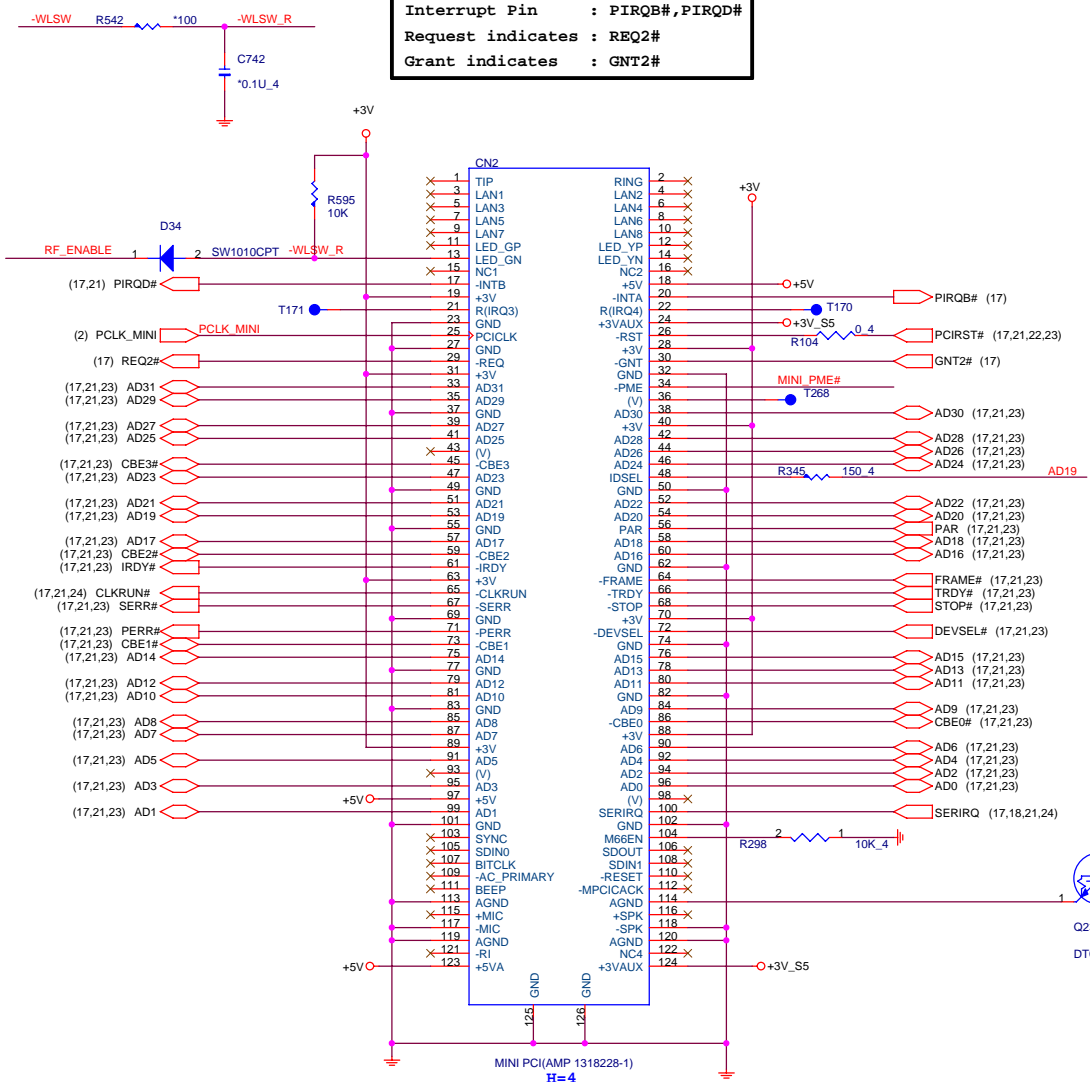
Size	Document Number	Rev
	BQ1	1A

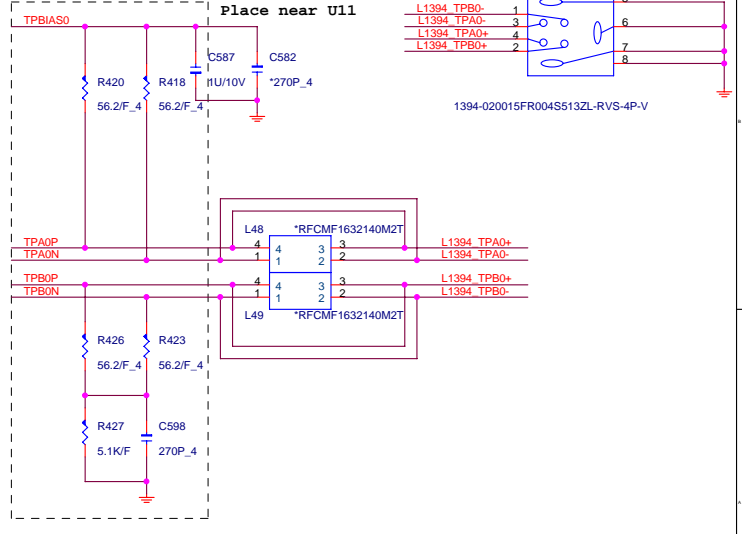
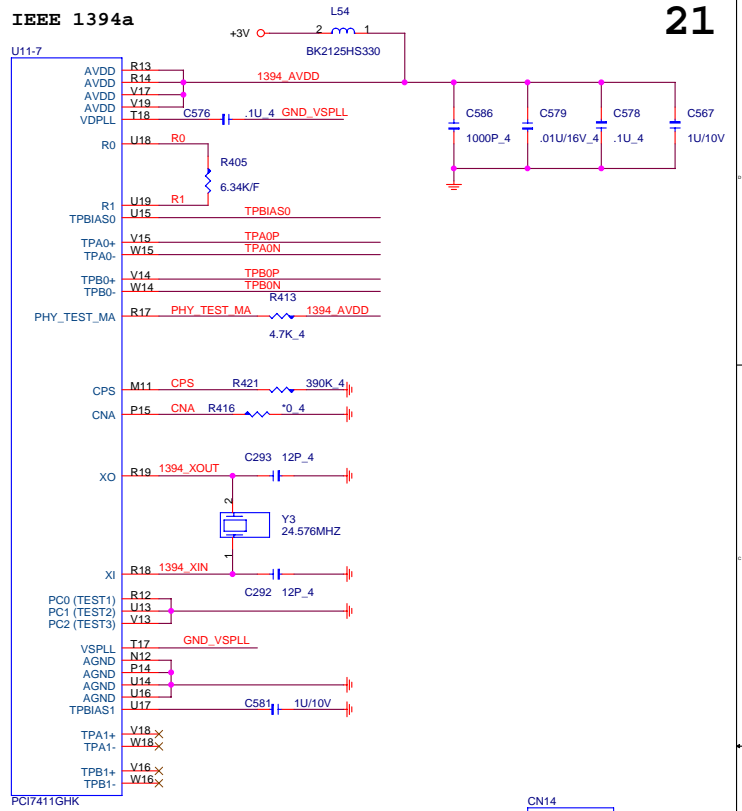
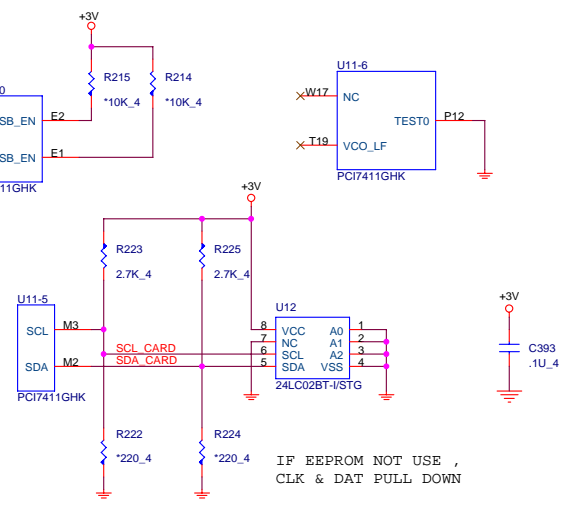
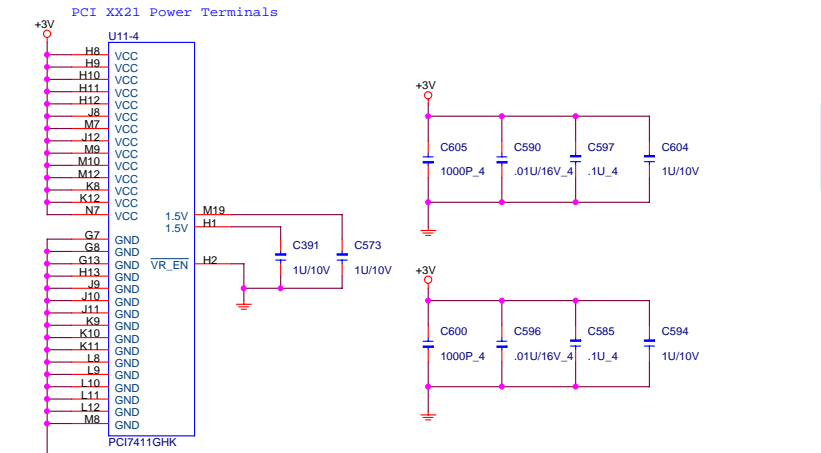
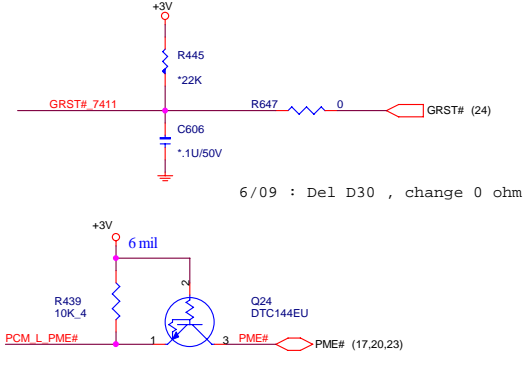
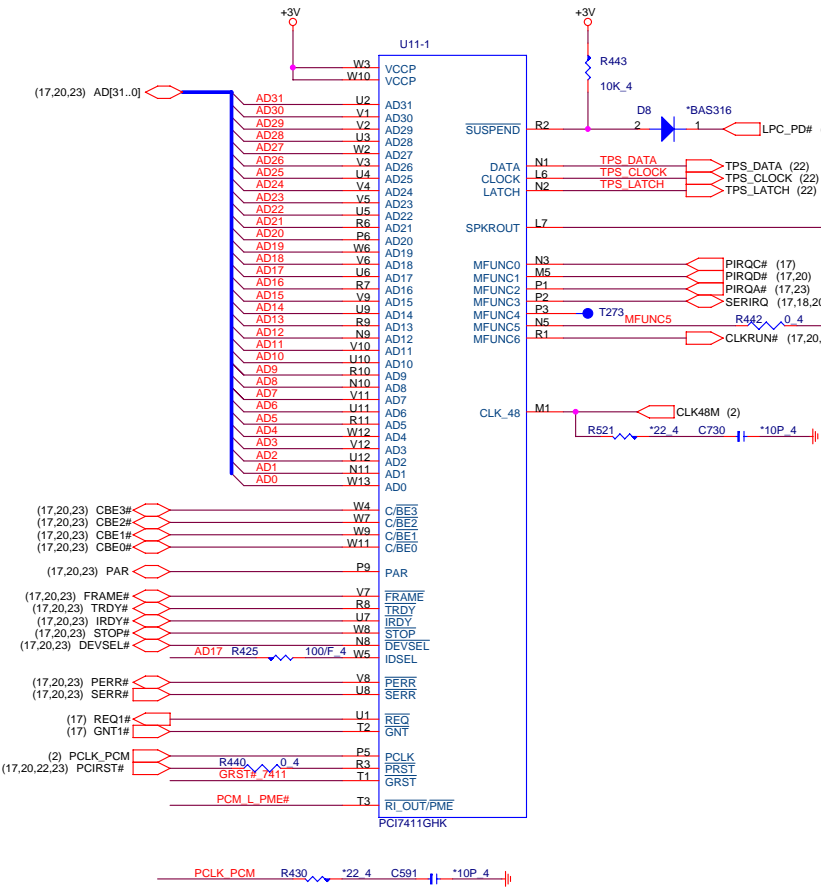
Date: Thursday, August 18, 2005 Sheet 19 of 32

MINI PCI SOCKET

**ID Select** : AD19  
**Interrupt Pin** : PIRQB#,PIRQD#  
**Request indicates** : REQ2#  
**Grant indicates** : GNT2#

MINI-PCI





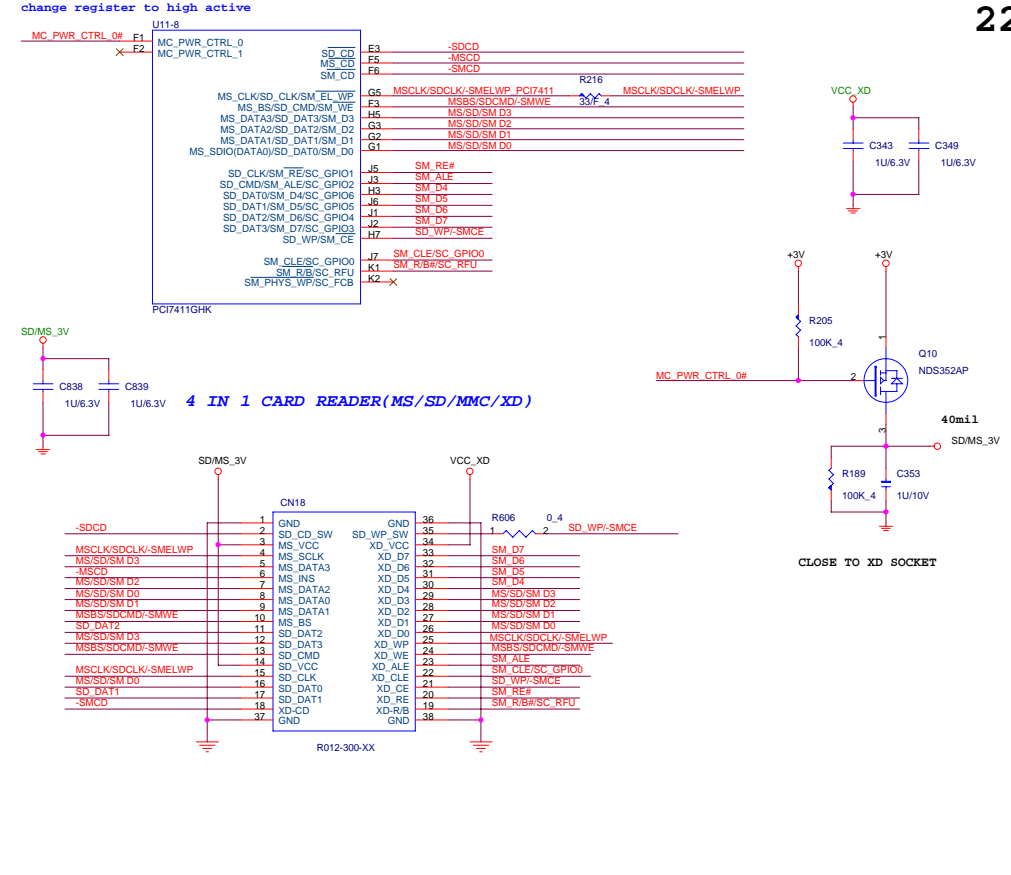
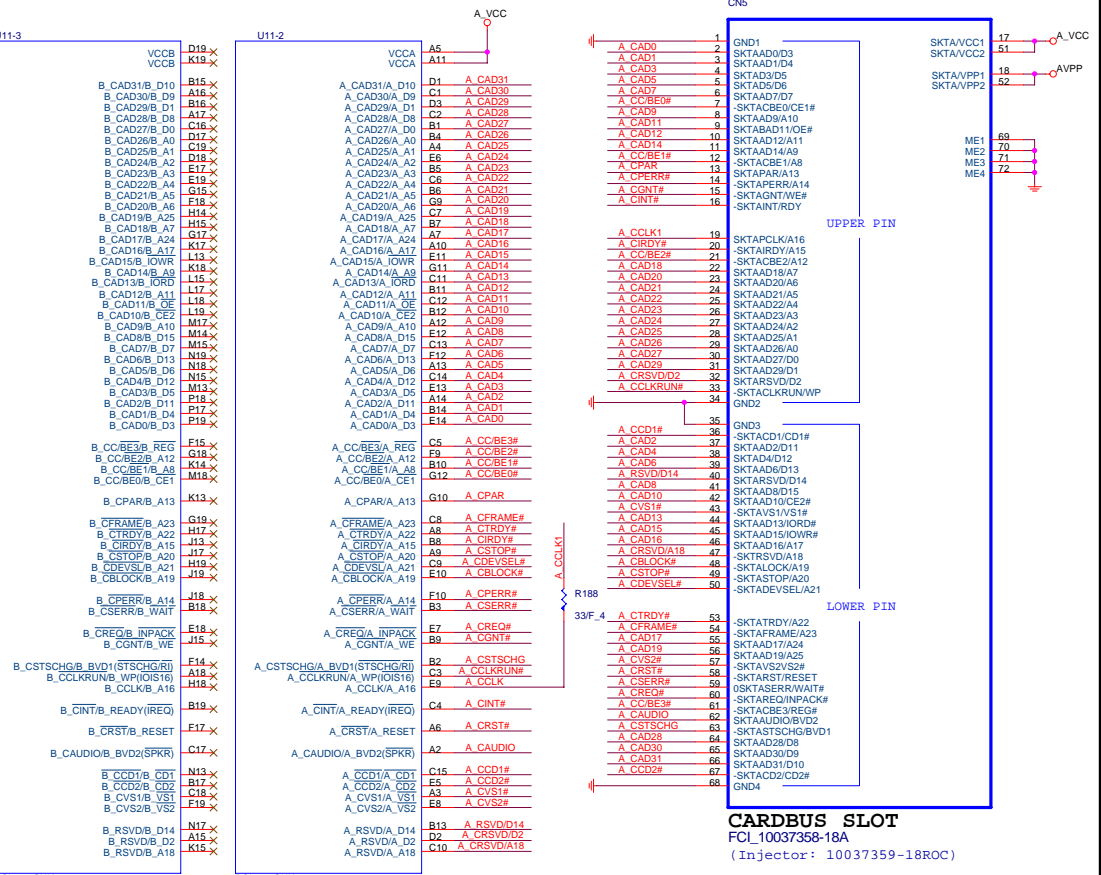
6/09 : To Solve CardBus no sound .

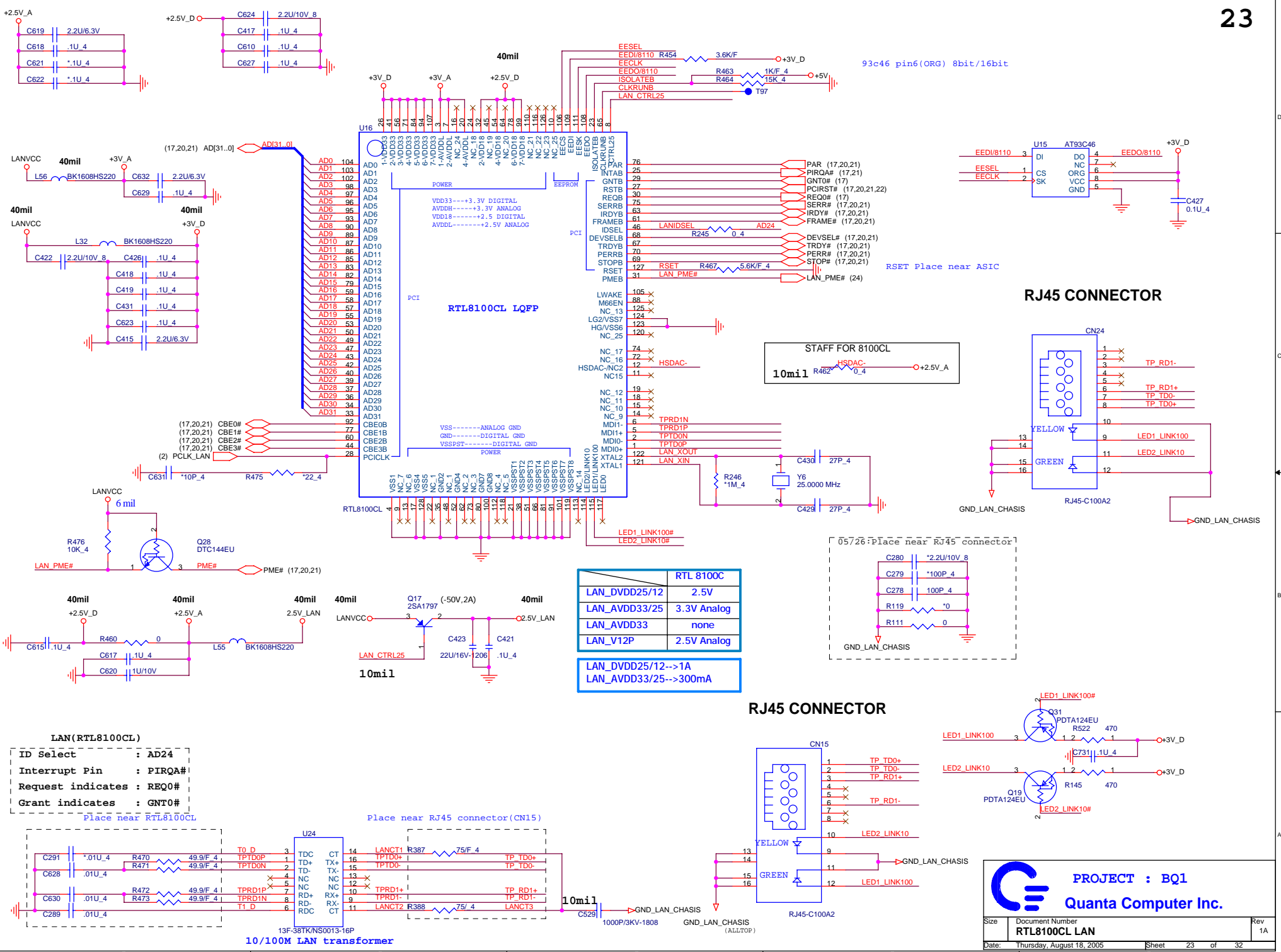
6/09 : Del D30 , change 0 ohm

**PROJECT : BQ1**  
**Quanta Computer Inc.**

Size Document Number Rev 1A  
**PCMCIA CONTROLLER**

Date: Thursday, August 18, 2005 Sheet 21 of 32

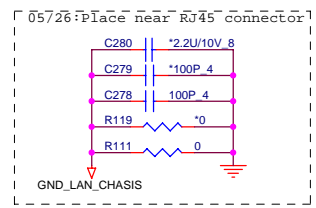
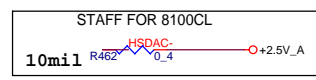
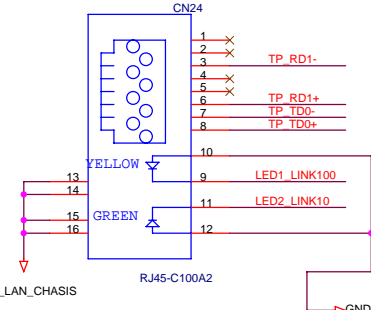
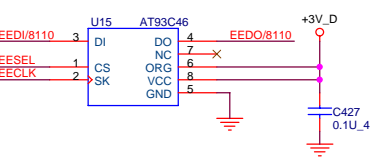




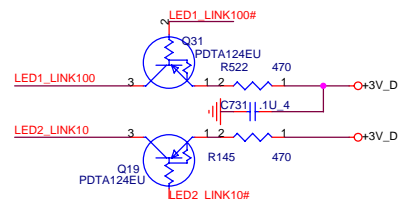
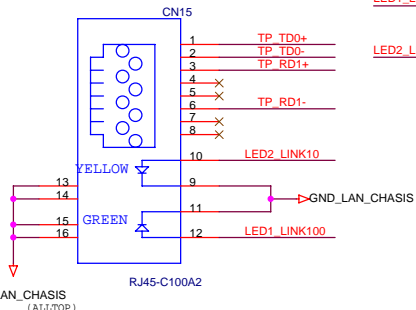
93c46 pin6(ORG) 8bit/16bit

RSET Place near ASIC

### RJ45 CONNECTOR

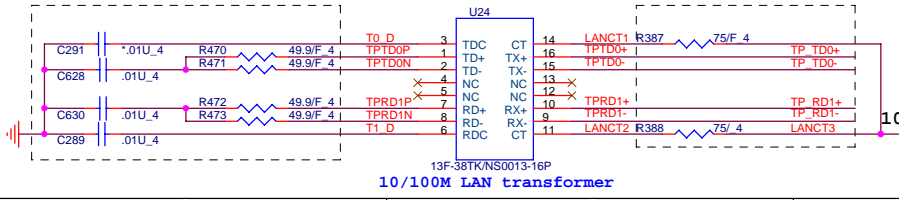


### RJ45 CONNECTOR

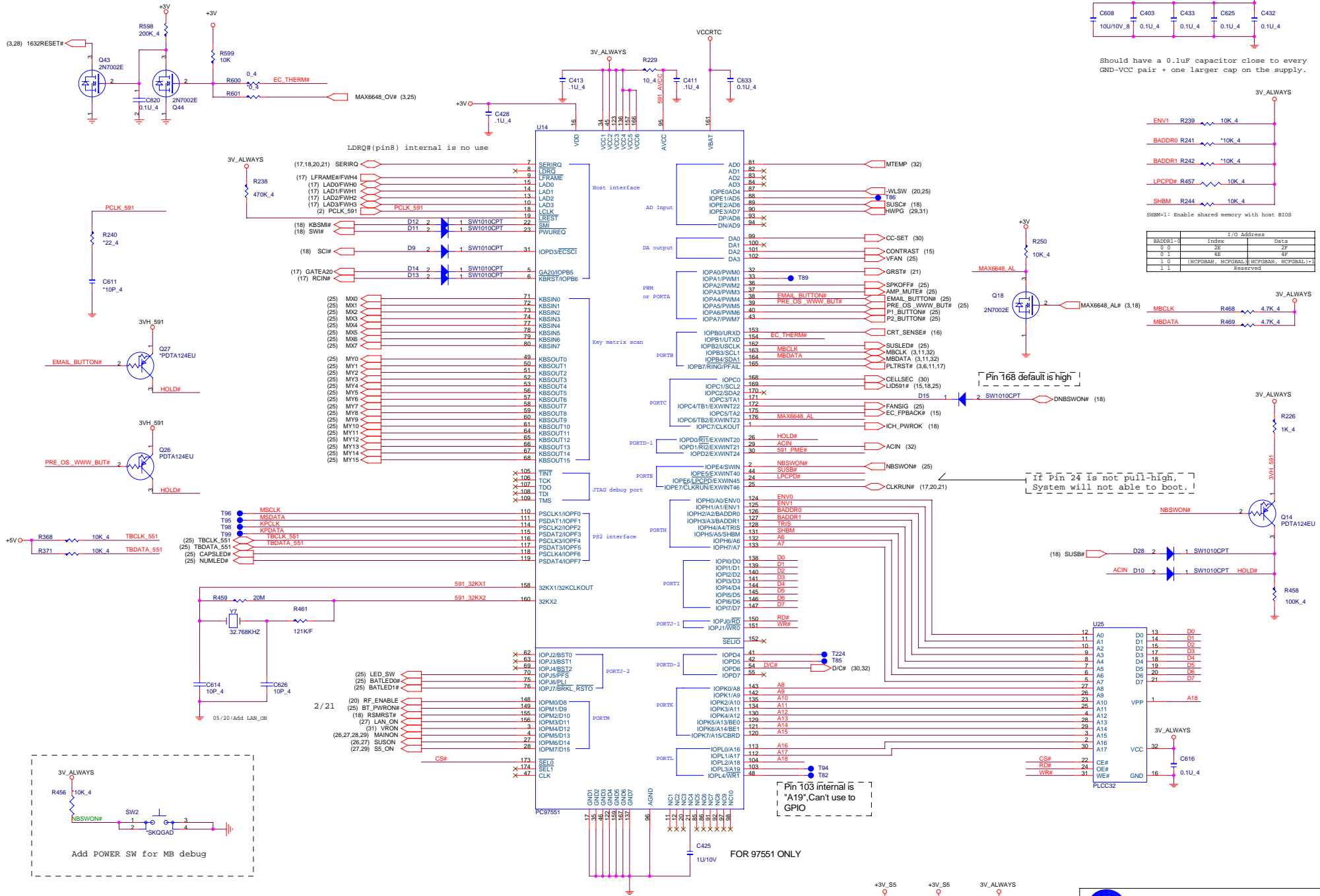


**LAN (RTL8100CL)**  
 ID Select : AD24  
 Interrupt Pin : PIRQA#  
 Request indicates : REQ0#  
 Grant indicates : GNT0#  
 Place near RTL8100CL

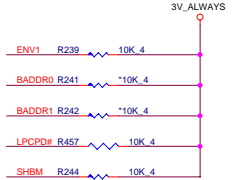
Place near RJ45 connector (CN15)



**PROJECT : BQ1**  
**Quanta Computer Inc.**



Should have a 0.1µF capacitor close to every GND-VCC pair + one larger cap on the supply.



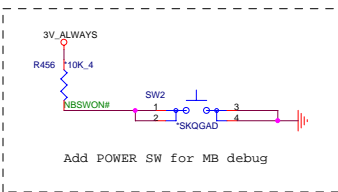
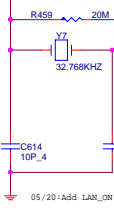
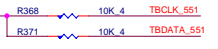
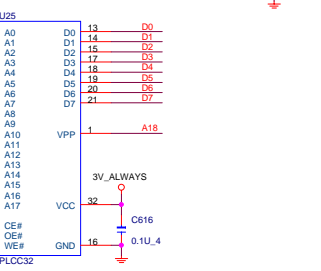
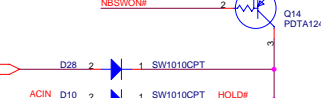
SHBM=1: Enable shared memory with host BIOS

T/I/O Address	Index	Data
BADDR0=0	0	2F
U-1	0	4E
I-0	0	4E
I-1	0	Reserved



"Pin 168 default is high"

"If Pin 24 is not pull-high, System will not able to boot."



INTERNAL PULLUP IN SB

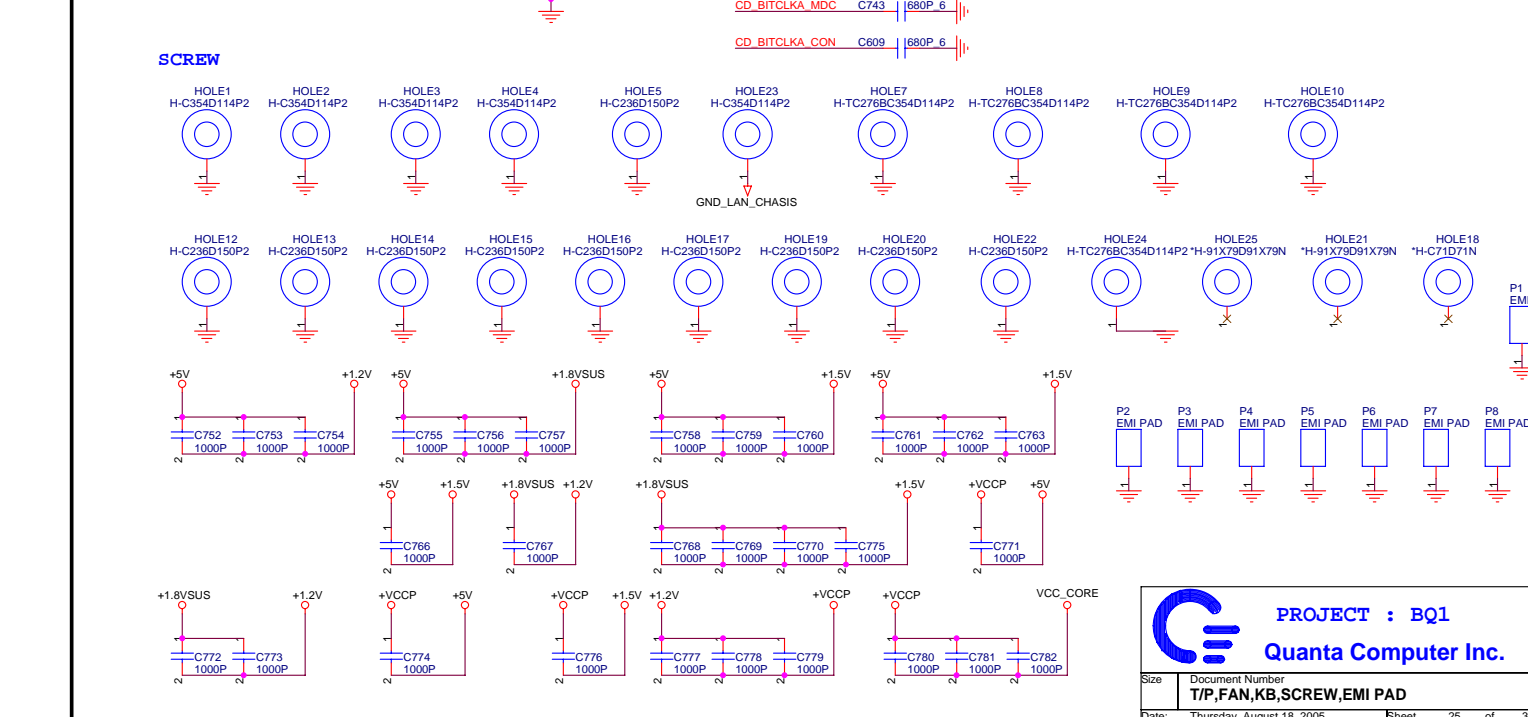
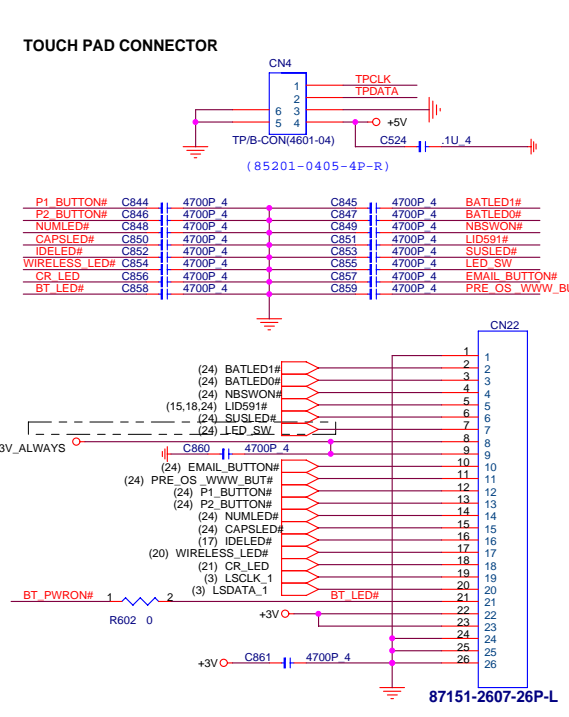
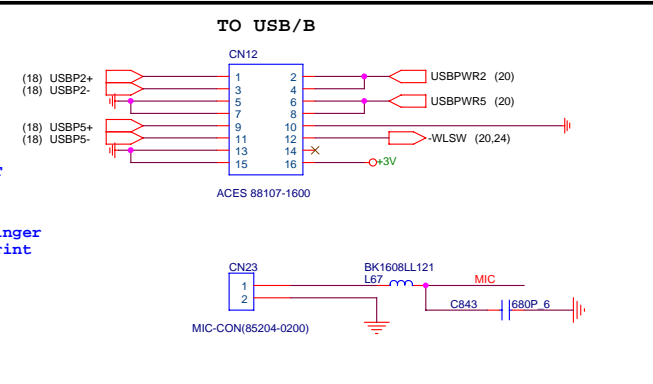
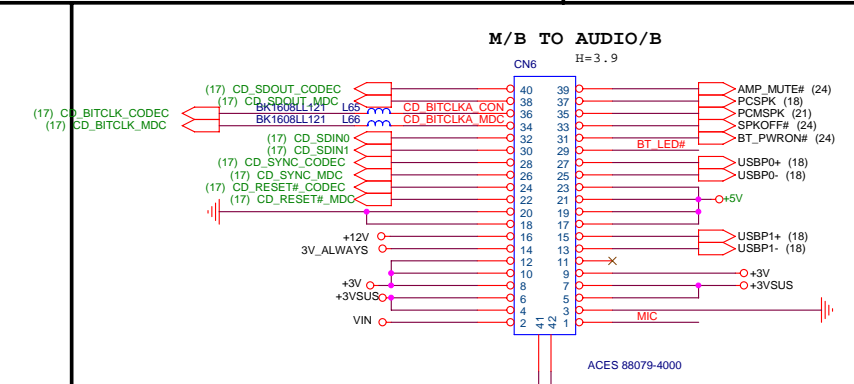
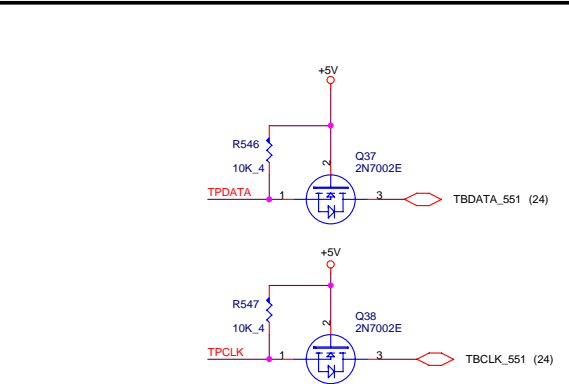
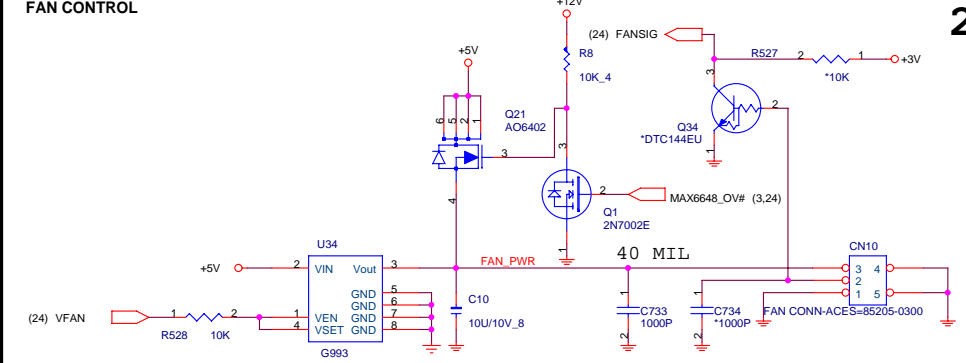
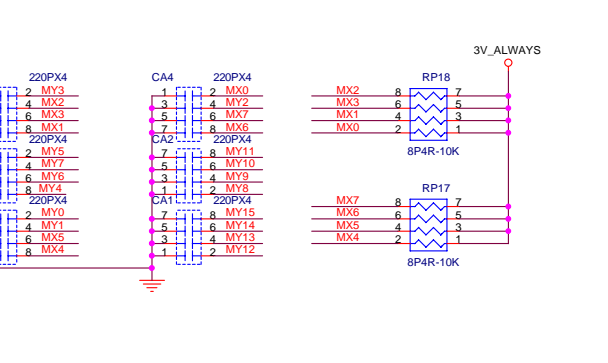
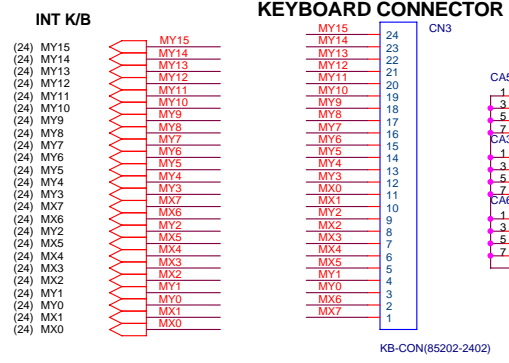


**PROJECT : BQ1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>97551 &amp; FLASH</b>	1A

Date: Thursday, August 18, 2005 Sheet 24 of 32

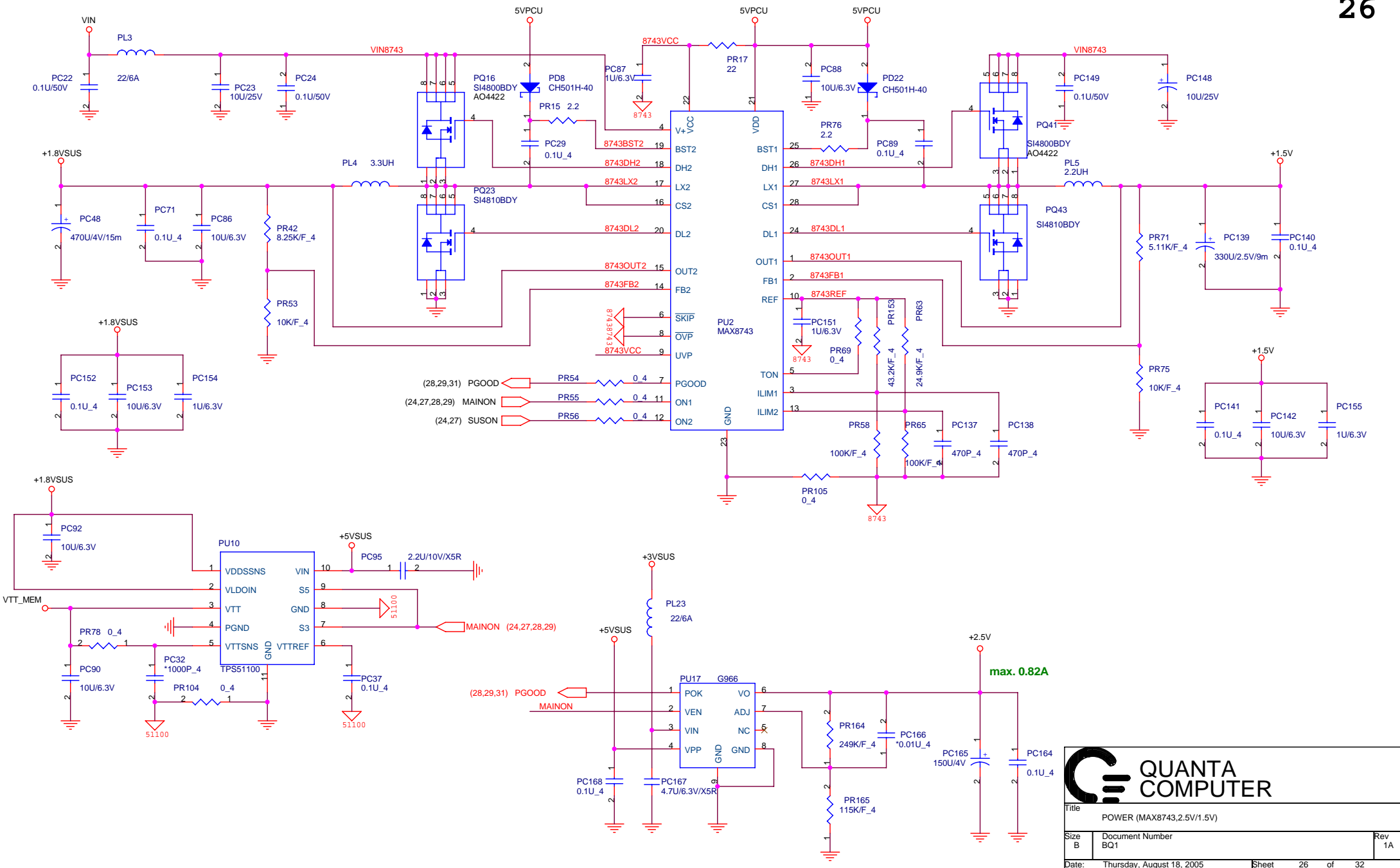




**PROJECT : BQ1**  
**Quanta Computer Inc.**

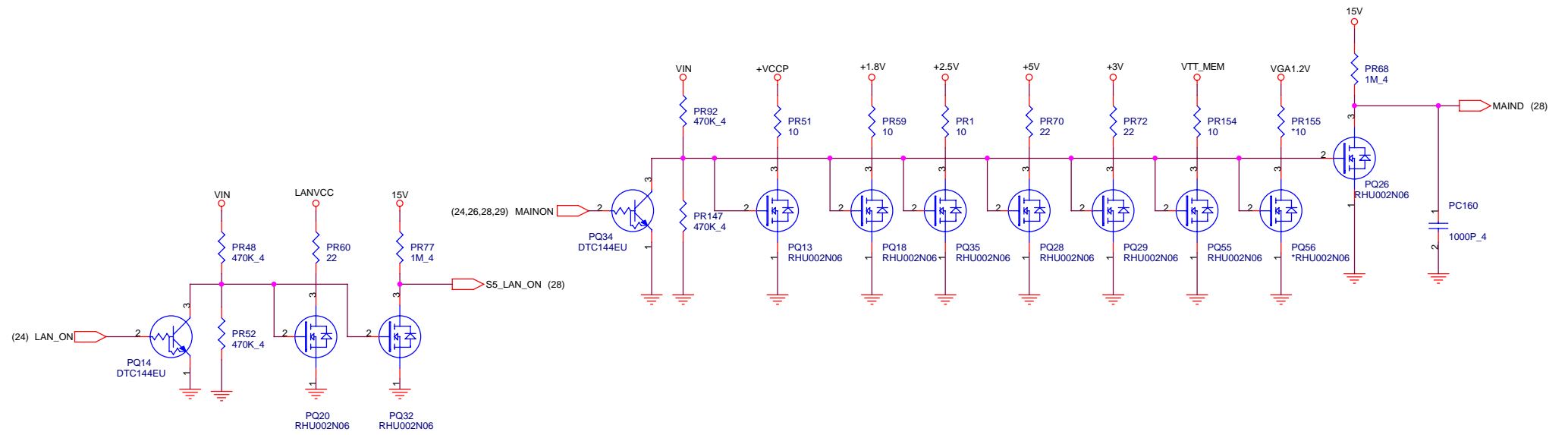
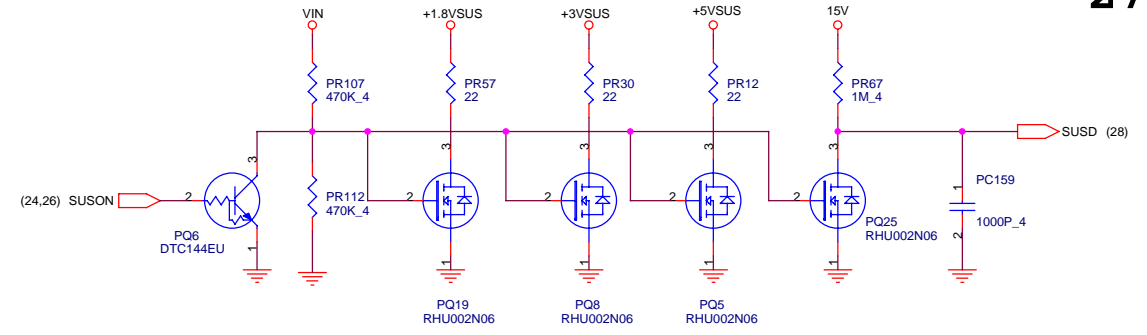
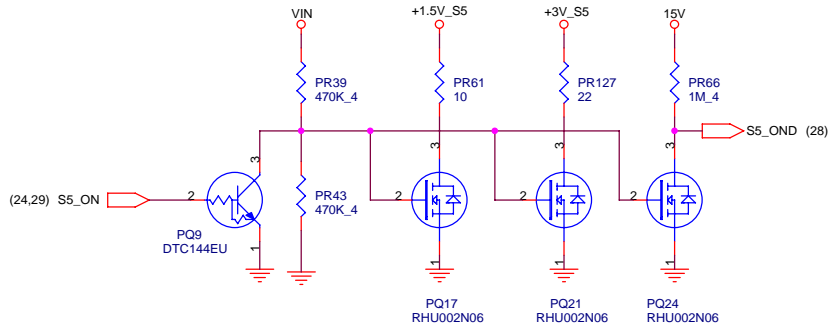
Size Document Number  
**T/P,FAN,KB,SCREW,EMI PAD** Rev 1A

Date: Thursday, August 18, 2005 Sheet 25 of 32



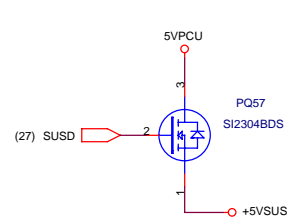
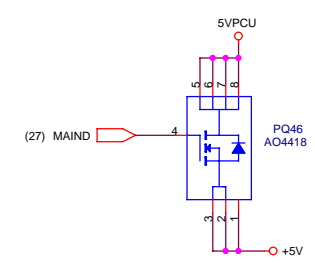
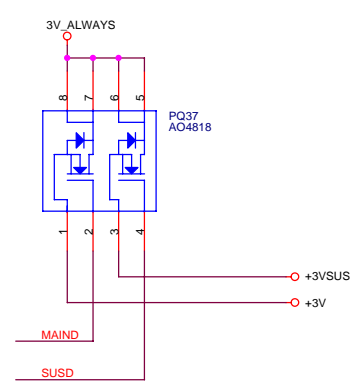
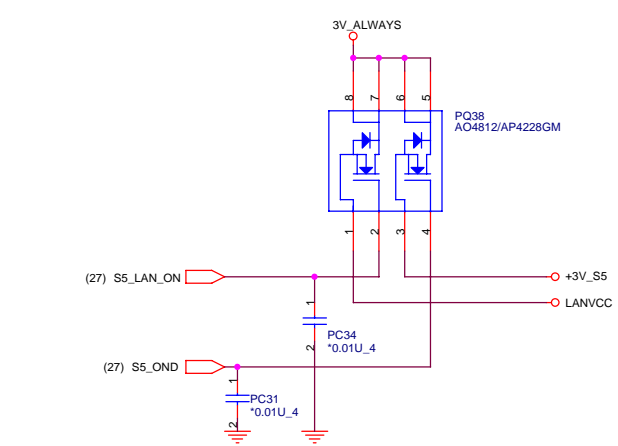
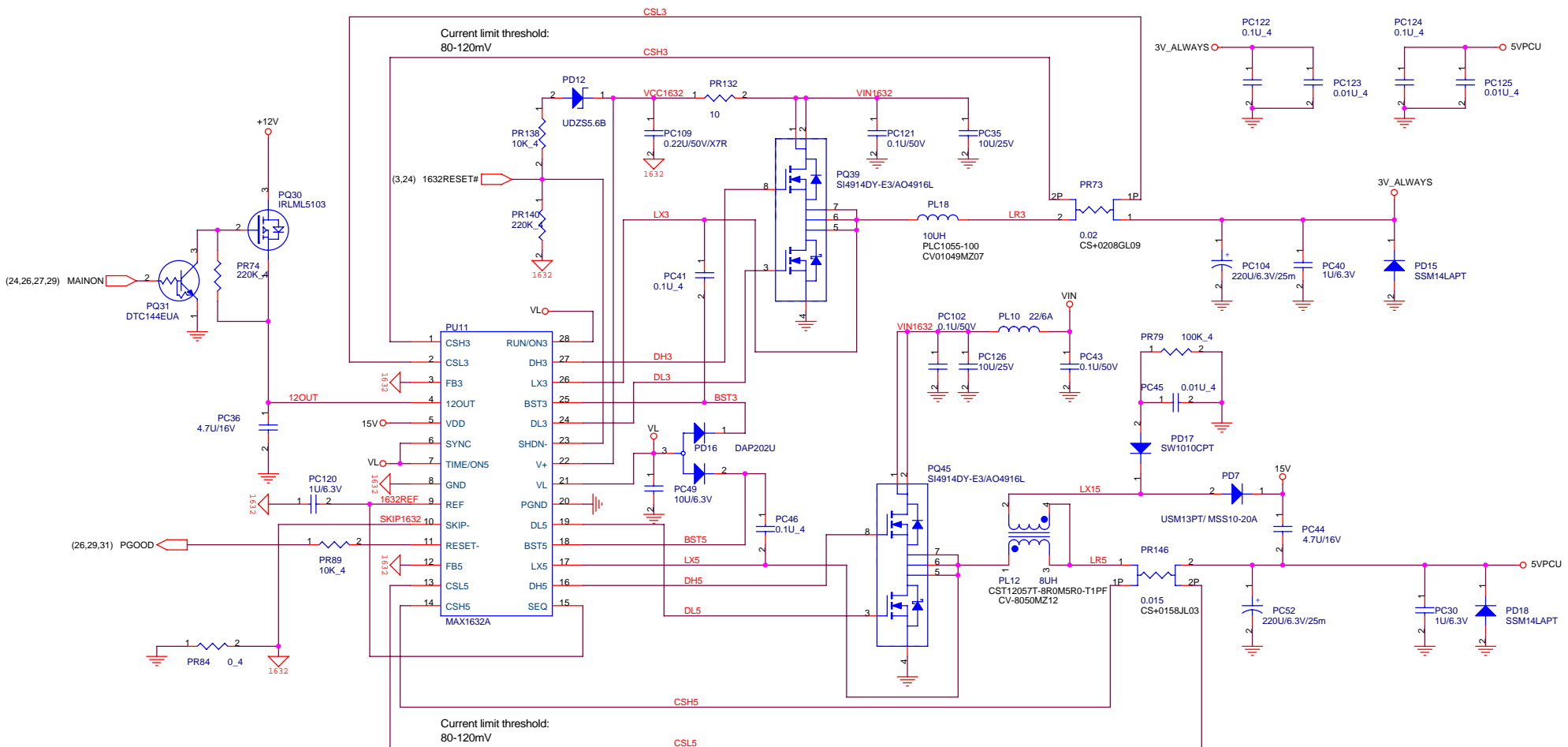
## QUANTA COMPUTER

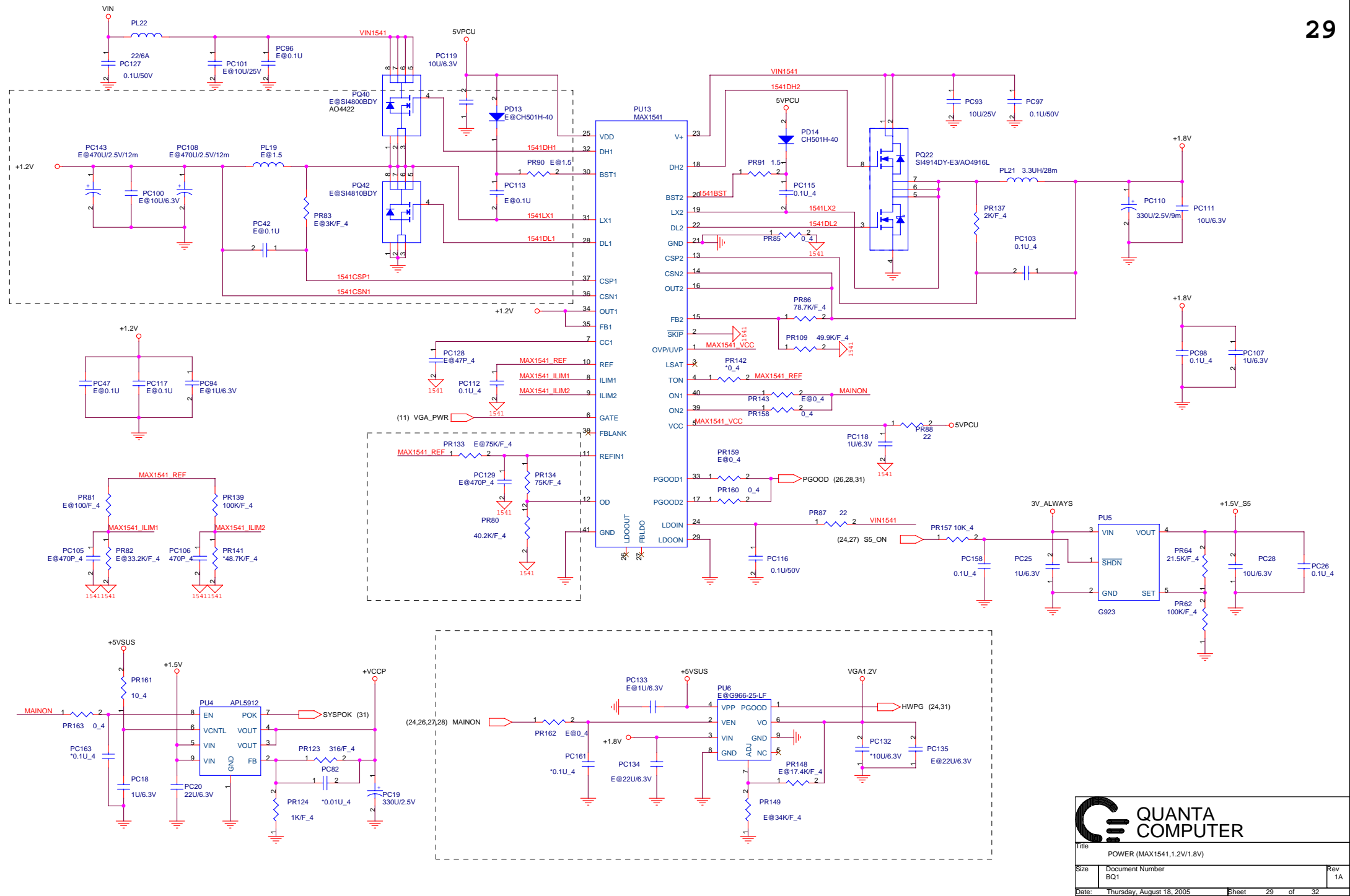
Title POWER (MAX8743,2.5V/1.5V)		
Size B	Document Number BQ1	Rev 1A
Date: Thursday, August 18, 2005		Sheet 26 of 32



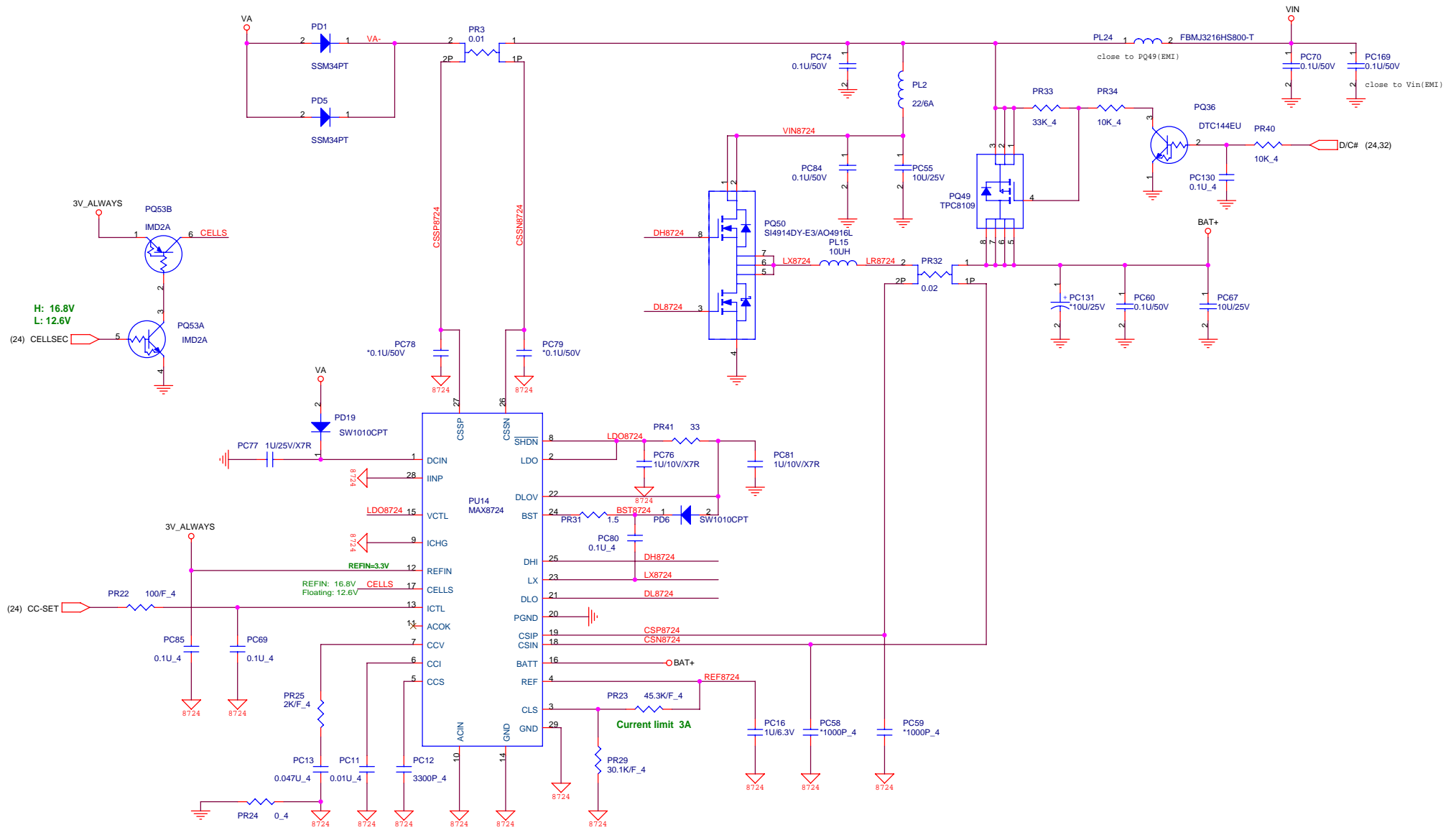
**QUANTA  
COMPUTER**

Title		POWER (DISCHARGE)
Size	Document Number	Rev
	BQ1	1A
Date:	Thursday, August 18, 2005	Sheet 27 of 32





Title POWER (MAX1541, 1.2V/1.8V)		
Size	Document Number BQ1	Rev 1A
Date:	Thursday, August 18, 2005	Sheet 29 of 32



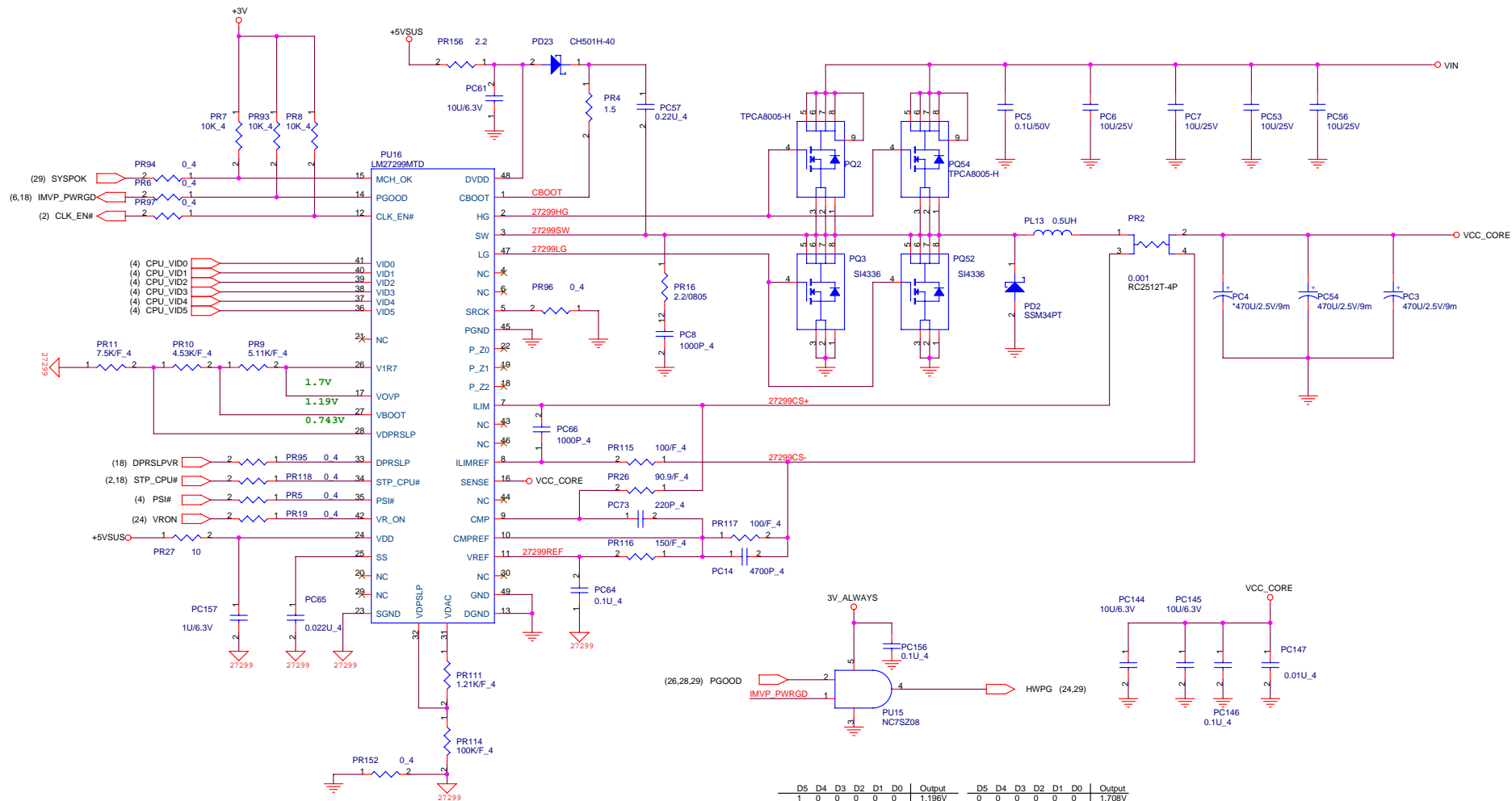
H: 16.8V  
L: 12.6V

REFIN=3.3V  
CELLS  
REFIN: 16.8V  
Floating: 12.6V

Current limit 3A

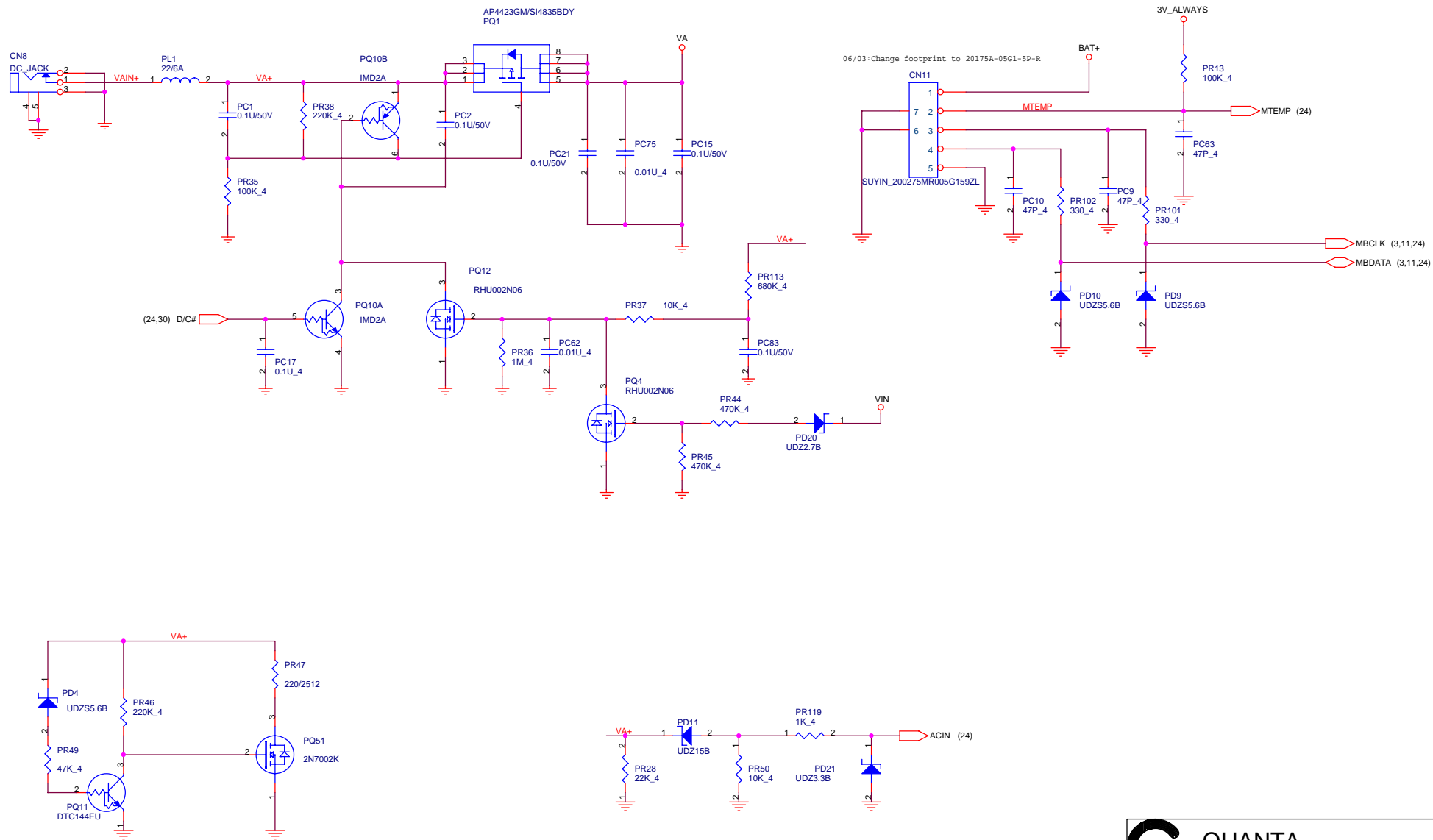
**QUANTA COMPUTER**

Title		POWER (MAX8743, 2.5V/1.8V)
Size	Document Number	Rev
	BQ1	1A
Date:	Thursday, August 18, 2005	Sheet 30 of 32



D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	0	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	0	1	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	0	1	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	0	1	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V





06/03: Change footprint to 20175A-05G1-5P-R



Title		
POWER (ADAPTER IN)		
Size	Document Number	Rev
	BQ1	1A
Date:	Thursday, August 18, 2005	Sheet 32 of 32