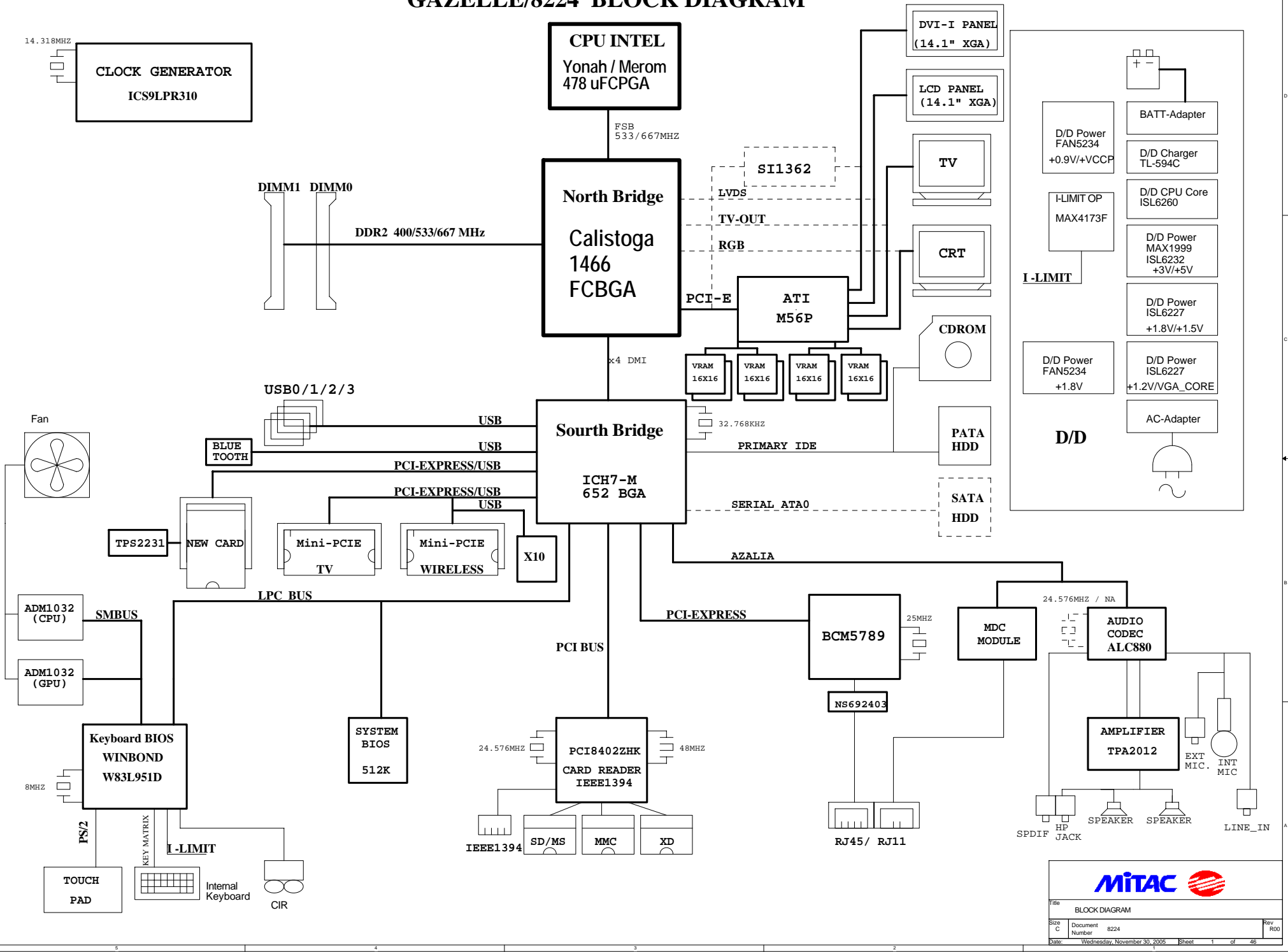


GAZELLE/8224 BLOCK DIAGRAM



MITAC		
File	BLOCK DIAGRAM	
Size	Document	Rev
C	8224	R00
Date	Wednesday, November 30, 2005	Sheet 1 of 46

8224 R00

PROJECT CODE- G239
PRODUCT CODE- 8044

PCB P/N:XXXXXXXXXXXX
ASSY P/N:XXXXXXXXXXXX

- PAGE 1 BLOCK DIAGRAM
- PAGE 2 TITLE
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- PAGE 4 CPU-YONAH(2/2)
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- PAGE 6 NB-CALISTOGA(2/3)
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- PAGE 9 DDR2-SODIMM
- PAGE 10 ATI M5X FAMILY(1/3)
- PAGE 11 ATI M5X FAMILY(2/3)
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- PAGE 25 MINI PCI-E
- PAGE 26 CARD READER(W83L528A-F)
- PAGE 27 IEEE1394(VT6301)
- PAGE 28 VIDALIA LAN(INTEL82537L)
- PAGE 29 LAN CONNECTOR
- PAGE 30 KBC(W83L591D)
- PAGE 31 FWH/LED/TOUCH PAD/DTB
- PAGE 32 PULL HIGH
- PAGE 33 PERIPHERAL
- PAGE 34 ADINP
- PAGE 35 CHARGER(TL594C)
- PAGE 36 CPU_CORE(6260/6208)
- PAGE 37 VCCP(1.05V) / 0.9V(FAN5234)
- PAGE 38 +1.8V / +1.5V(ISL6227)
- PAGE 39 VGA(1.2V)/1.0V (ISL6227)
- PAGE 40 VGA(1.8V)(FAN5234)
- PAGE 41 MINI PCI

PCI DEVICE	INTERRUPT	REQ#GNT	IDSEL
CARDREADER	PCI_INTA#	PCI_REQ0#/ PCI_GNT0#	AD20
IEEE1394	PCI_INTB#	PCI_REQ1#/ PCI_GNT1#	AD21
MINIPCI	PCI_INTD#	PCI_REQ2#/ PCI_GNT2#	AD17

POWER STATUS

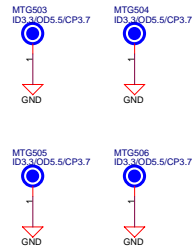
CONTROL SIGNAL	S0/S1	S3	S4	S5	POWER	NOTE
ADP/BATT IN	V	V	V	V	+DVMAIN	
ADP/BATT IN	V	V	V	V	+VDD3_A	
ADP/BATT IN	V	V	V	V	+VDD3_AVREF/+VDD3	
ADP/BATT IN	V	V	V	V	+VDD5_A	
KBC_PWRON_VDD3S	V	V	V	V	+VDD3S	
DCON5V	V	V			+5V	
DCON3V	V	V			+3V	
DCON3V	V	V			+2.5V	
SUSC1.8V	V	V			+1.8VDD5	
SUSC1.2V	V	V			+1.2V	
SUSB0.9V	V	V			+0.9VS	
SUSB5V	V				+5VS	
SUSB3V	V				+3VS	
SUSB2.5V	V				2.5VDDM	
SUSB1.8V	V				1.8VDDM	
SUSB1.5V	V				+1.5VS	
SUSB1.2V	V				1.2VDDM	
SUSB_VGA_C	V				+VGA_CORE(1.2V)	
SUSB_VCCP	V				+VCCP(+1.05V)	
SUSB_VCC_CORE	V				+VCC_CORE	

PCB STACK 1.2mm

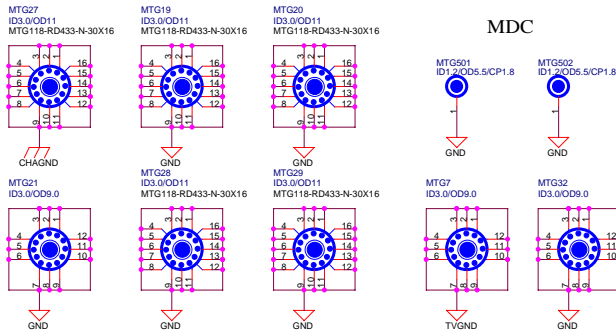
Layer	Material	Thickness	Notes
layer 1	Component side	1/2 oz	
layer 2	Ground 1	1 oz	
layer 3	Signal layer (IN1)	1 oz	
layer 4	Ground 3 (IN2)	1 oz	
layer 5	Power layer	1 oz	
layer 6	Signal layer (IN3)	1 oz	
layer 7	Ground 2	1 oz	
layer 8	Solder side	1/2 oz	

	Impedance	Differential Pair (width/space/width)	Single end (width/space/width)
1.Host clk	100 ohm	4/7/4	
2.DMI	100 ohm	4/7/4	
3.LVDS	100 ohm	4/7/4	
4.USB	90 ohm	4/5/4	
5.DDR2	70 ohm	7/4/7	7/4/7
6.CRT	37.5 ohm	x	9/20/9
7.LAN	100 ohm	4/7/4	
8.DVI-D	100 ohm	4/7/4	

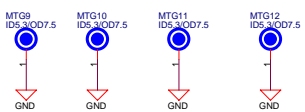
MINI-PCIE



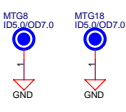
MDC



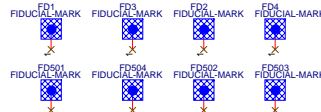
CPU定位孔



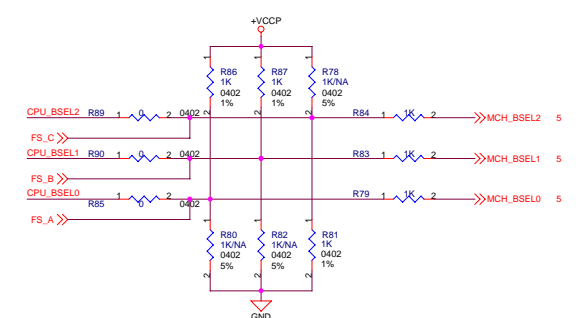
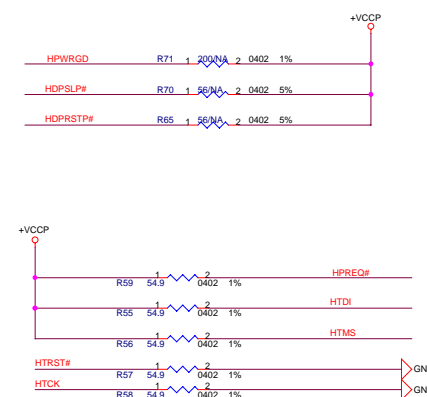
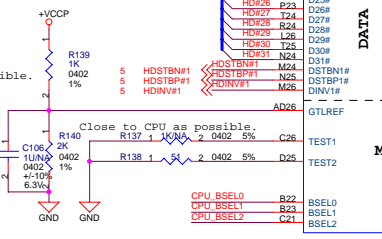
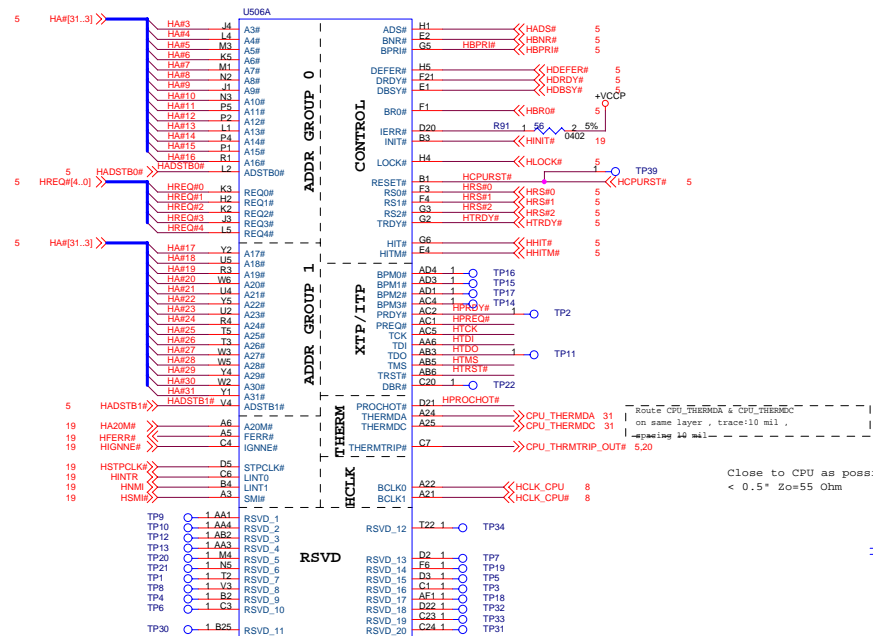
VGA定位孔



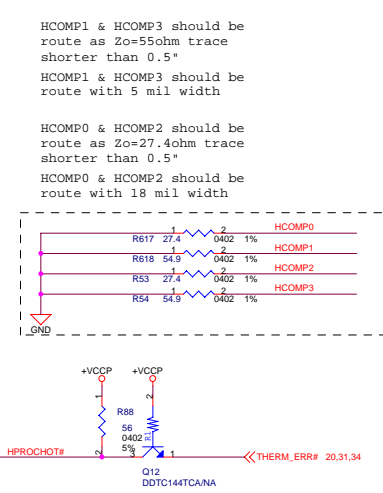
光學定位點



DRAWN	DESIGN	CHECK	ISSUES	
File: TITLE				
Size C Document Number 8224 Rev R00				
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FSB Freq (MHz)	533	PS_A => L PS_B => H PS_C => H
	667	PS_A => H PS_B => L PS_C => L



File: YONAH(1/2)

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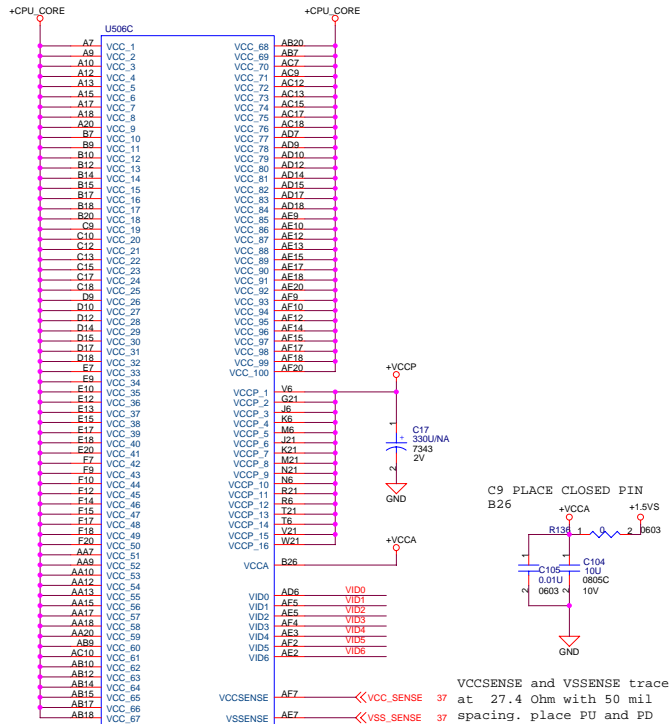
PLACEMENT MAX. 3" FROM CPU.
Don't overlay by CHOKE or vibrating signals.

HCOMP1 & HCOMP3 should be route as Zo=55ohm trace shorter than 0.5"

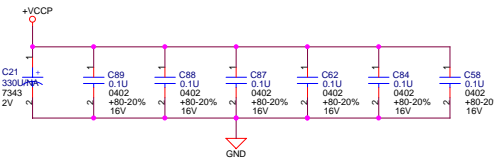
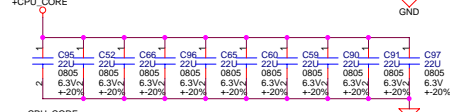
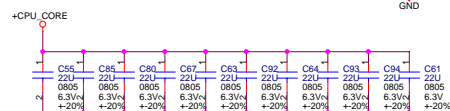
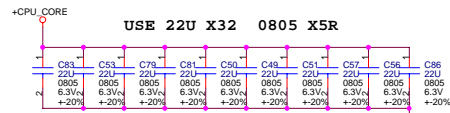
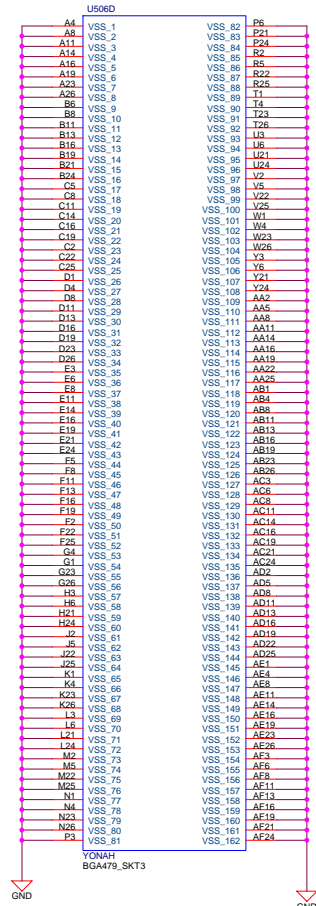
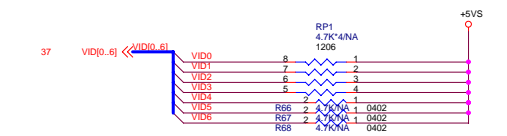
HCOMP1 & HCOMP3 should be route with 5 mil width

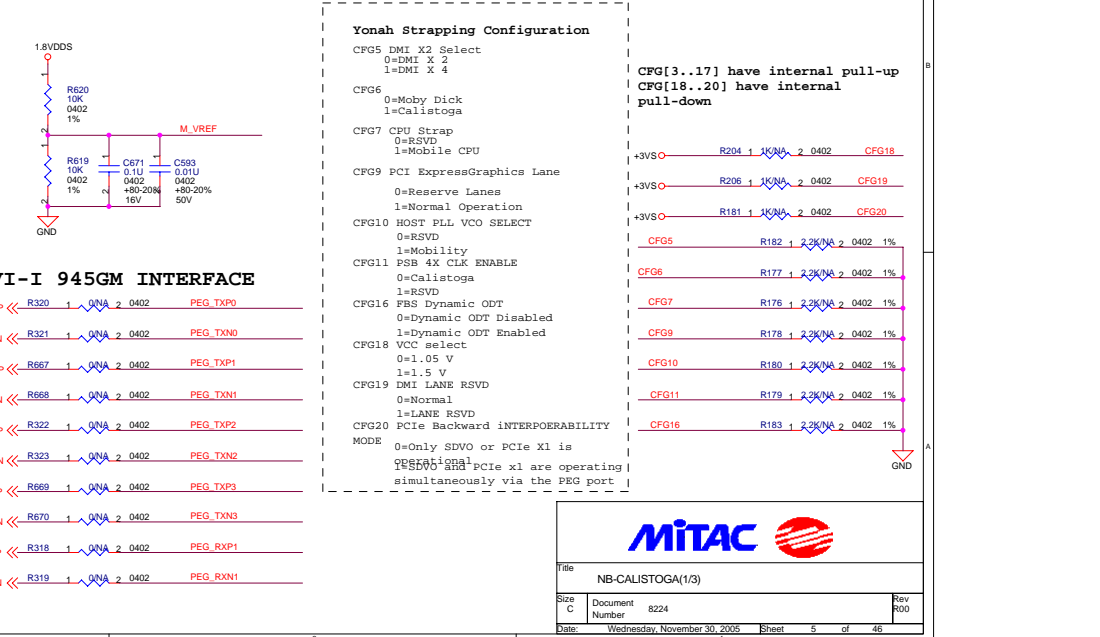
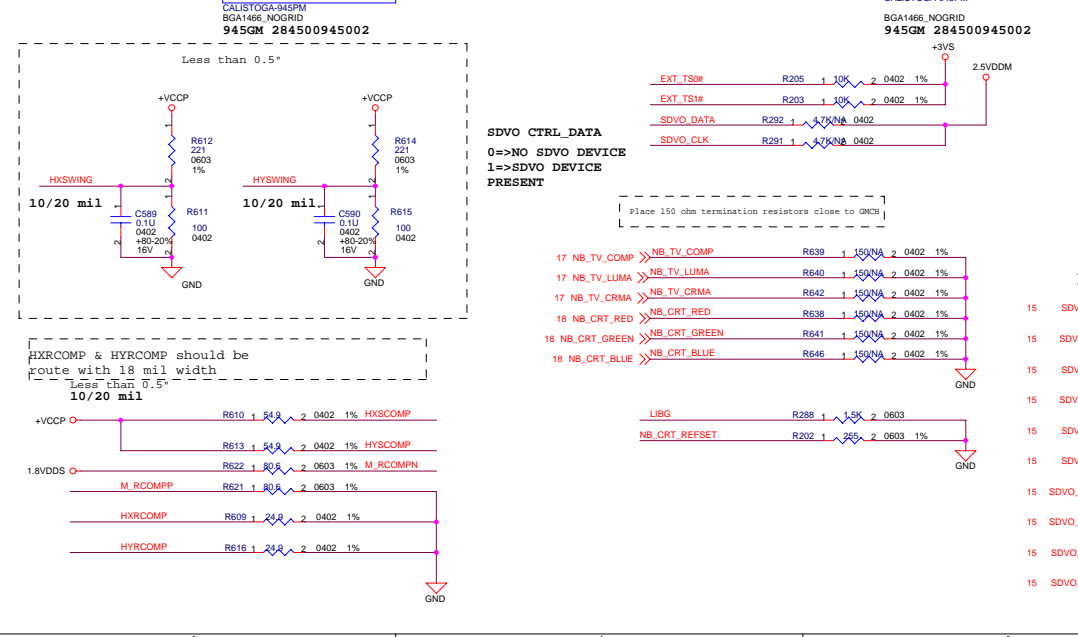
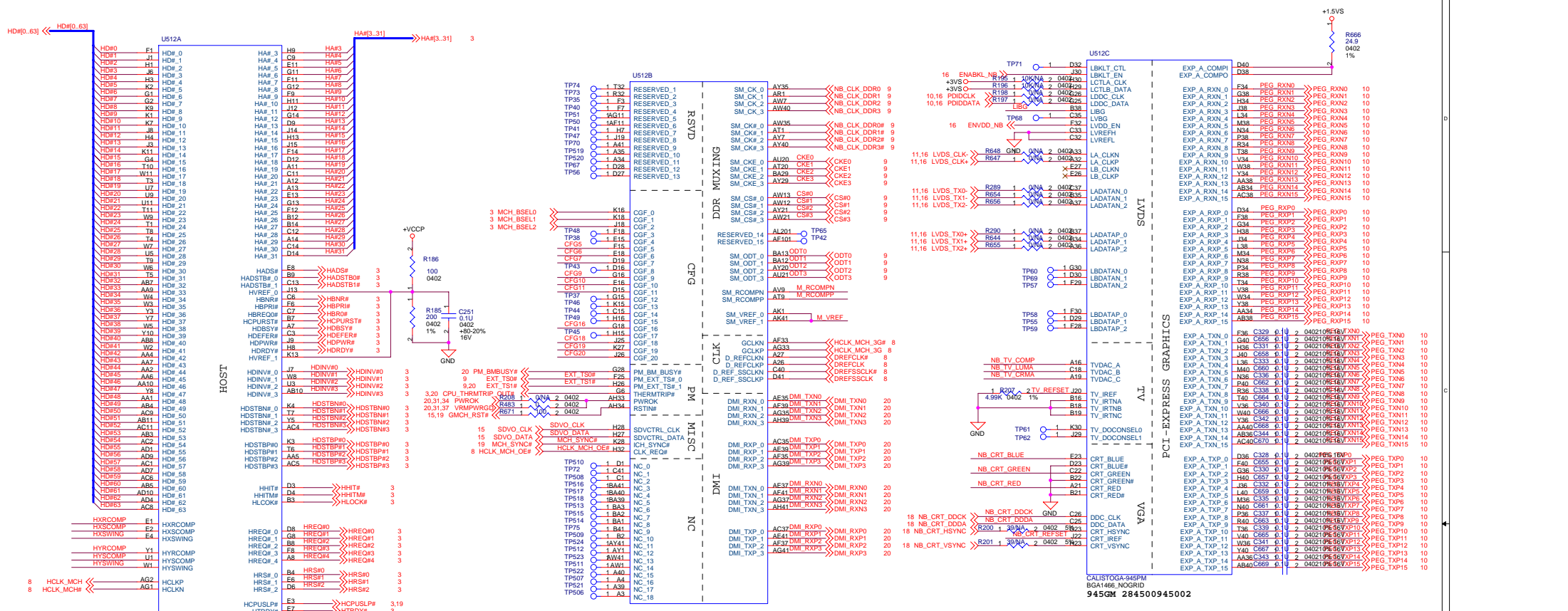
HCOMP0 & HCOMP2 should be route as Zo=27.4ohm trace shorter than 0.5"

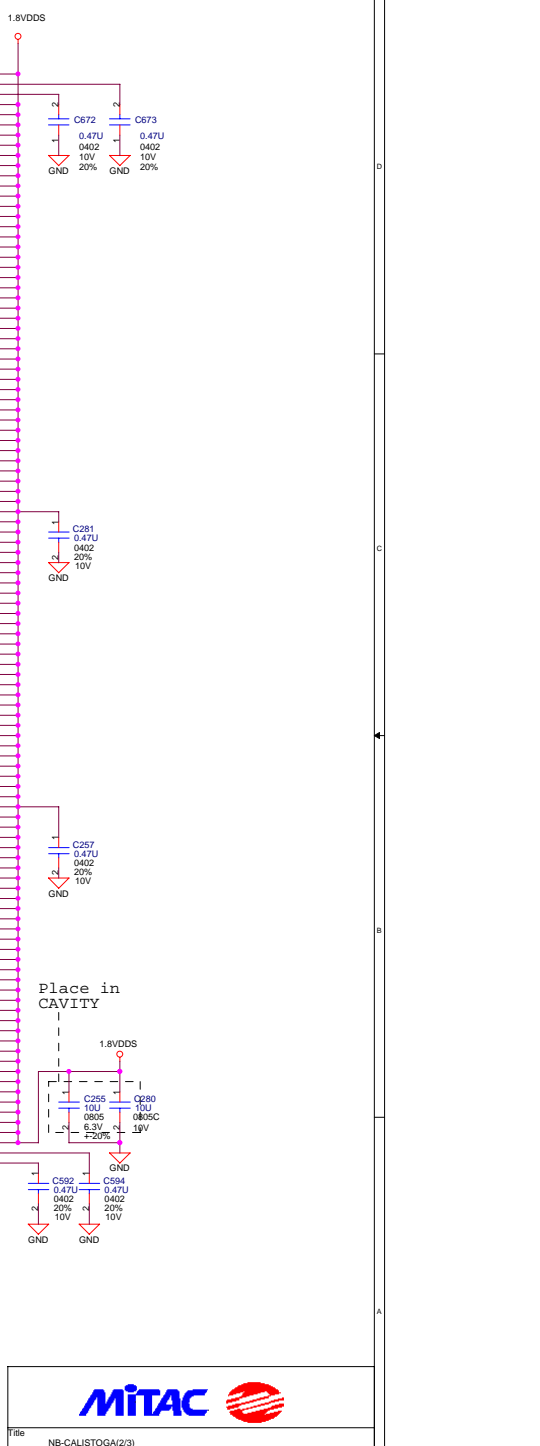
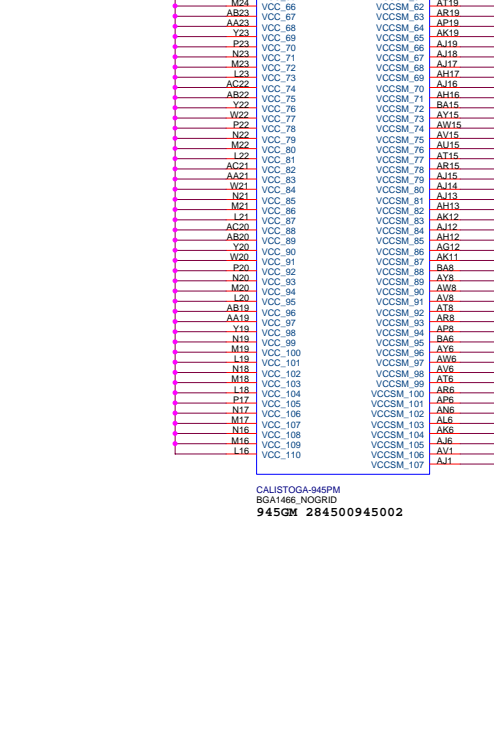
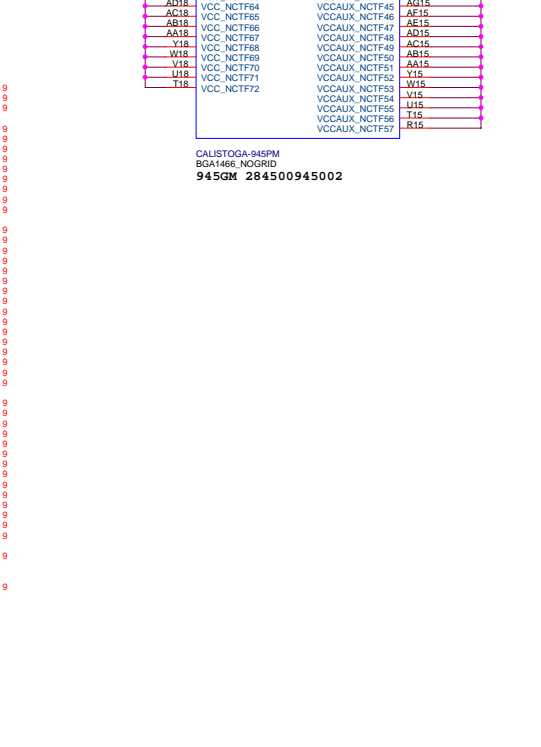
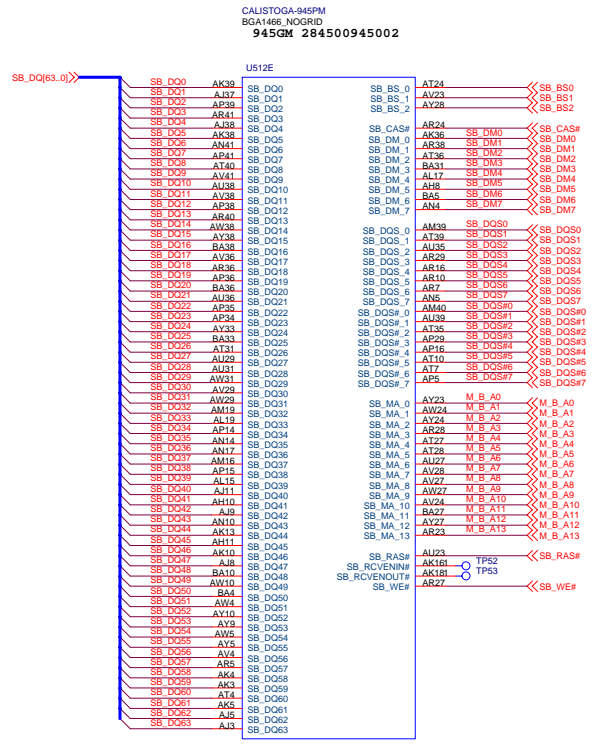
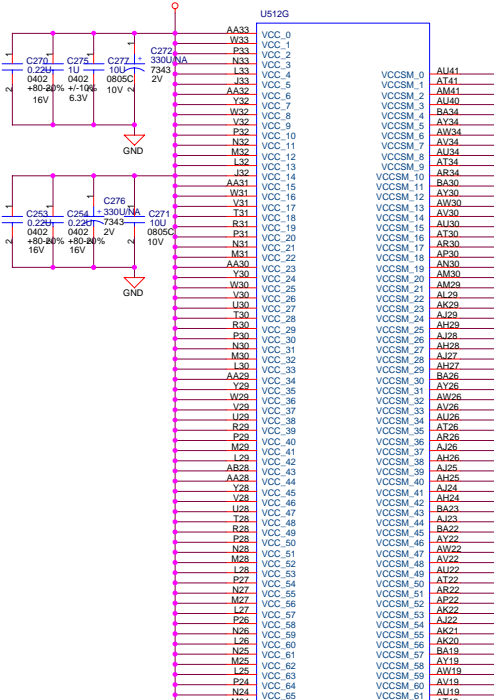
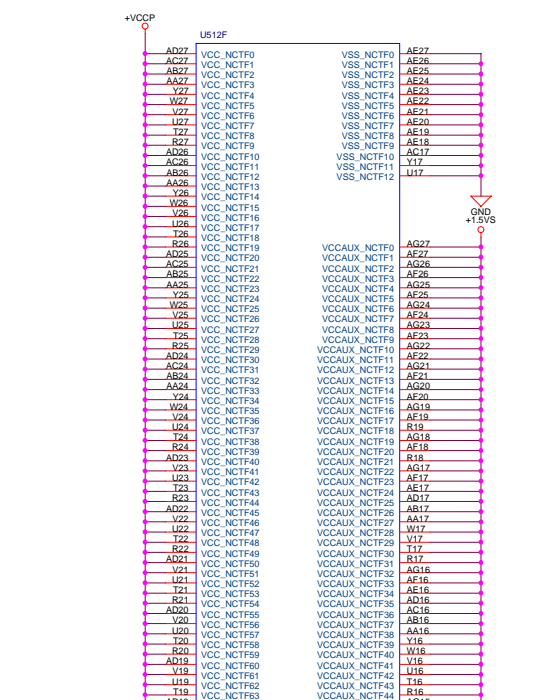
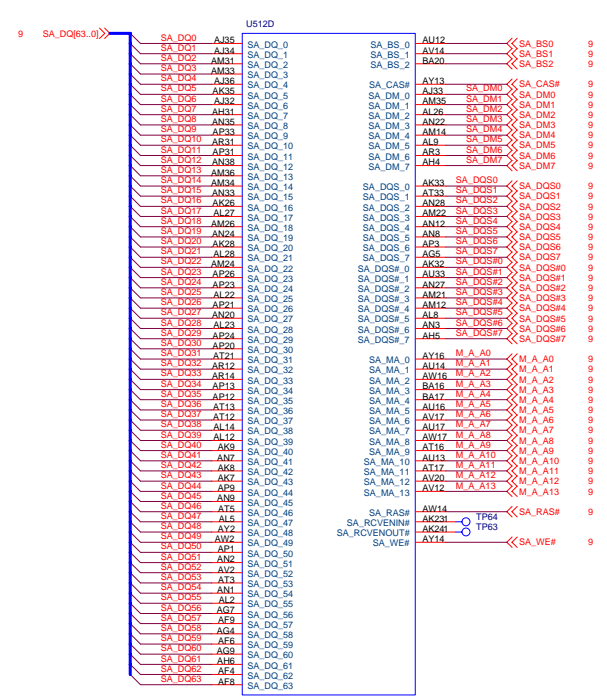
HCOMP0 & HCOMP2 should be route with 18 mil width

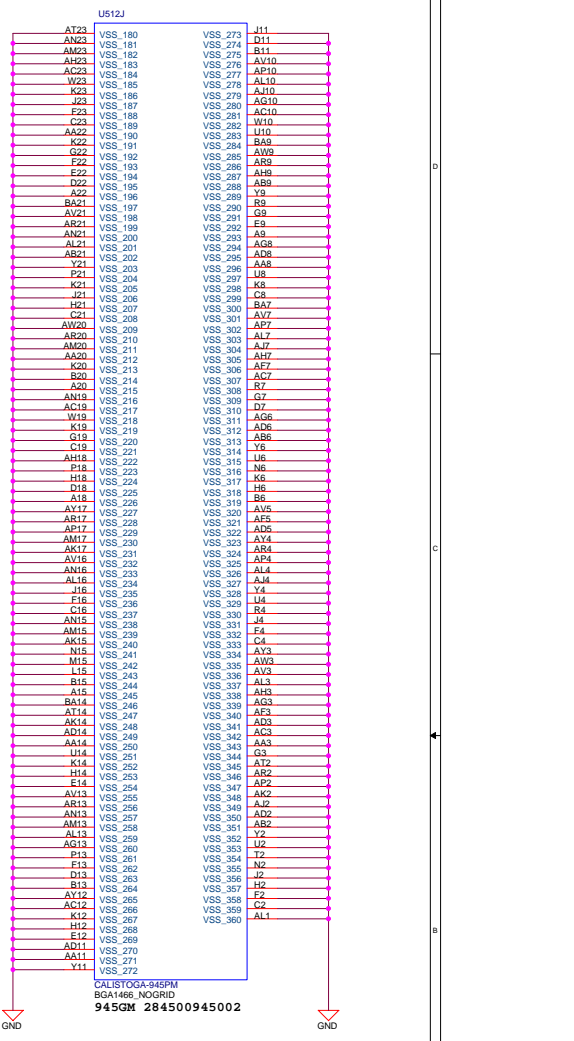
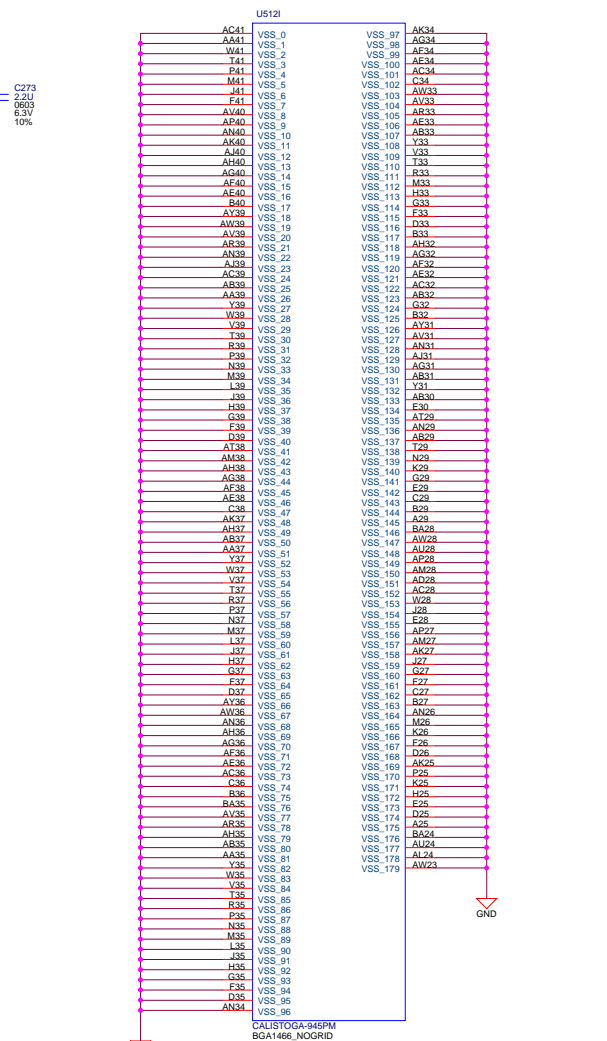
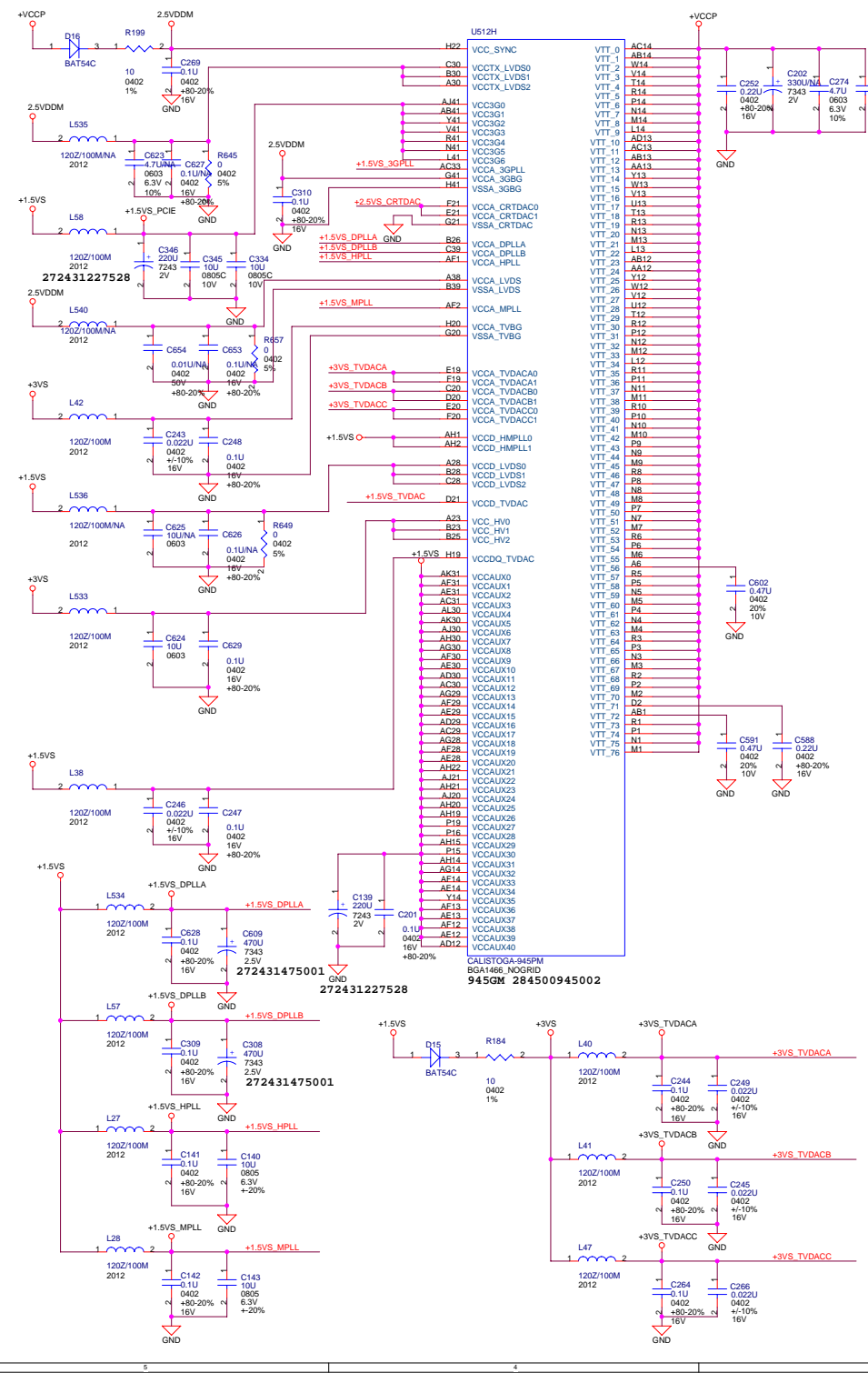


VCCSENSE and VSSSENSE trace at 27.4 Ohm with 50 mil spacing. place PU and PD within 1" of CPU

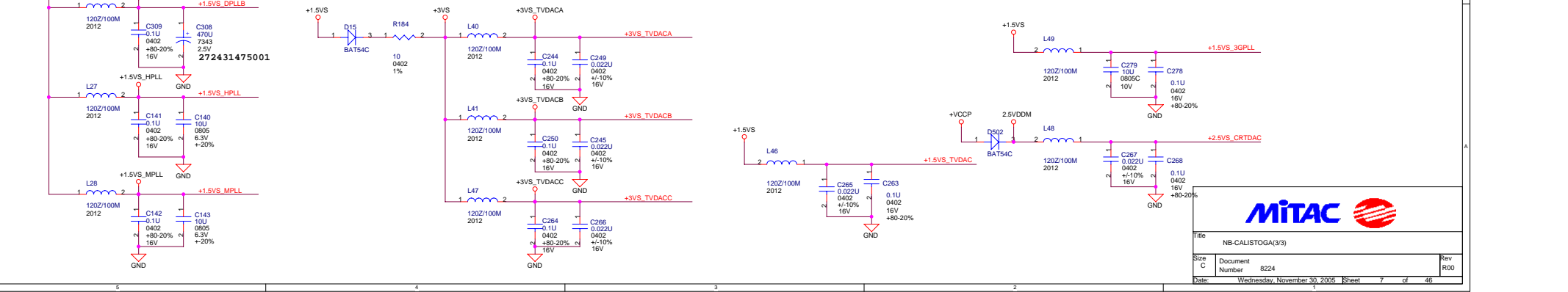








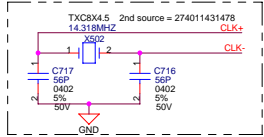
Route VSSA_LVDS, VSSA_CRTDAC, VSSA_TVBG GND from GMCH to decoupling cap ground lead and connect to the GND plane



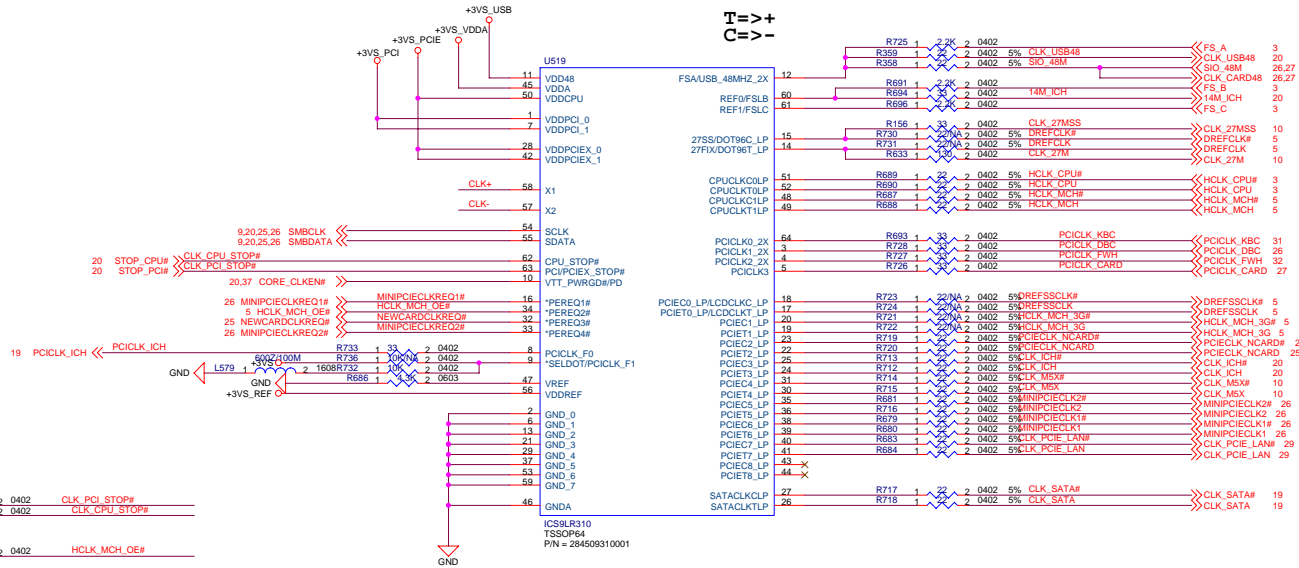
File: NB-CALISTOGA(3/3)		
Size: C	Document Number: 8224	Rev: R00
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CLOCK SYNTHESIZER

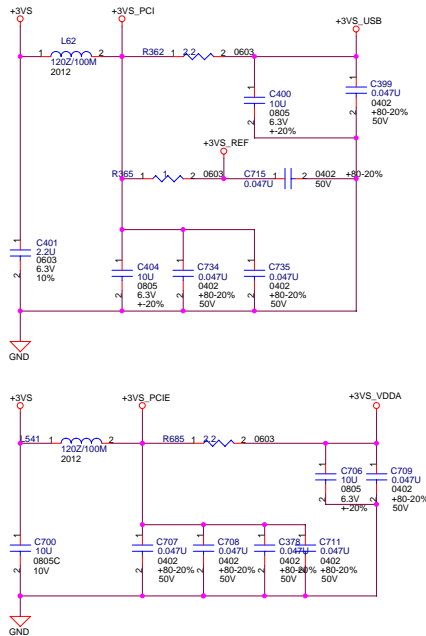
Layout note: Place crystal within 500 mils of CLK Gen.



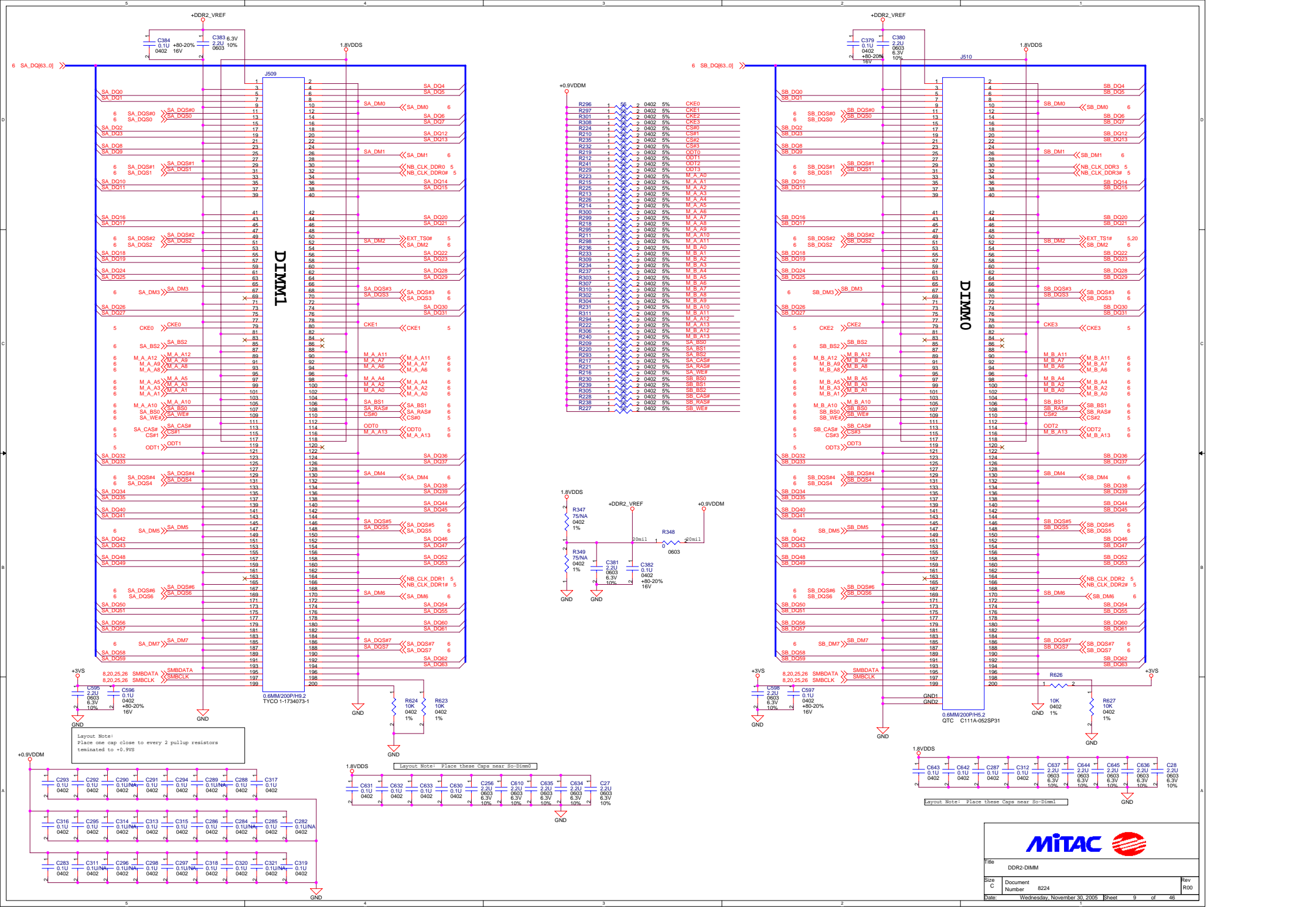
$$C_e = 2 * CL - (C_0 + C_1)$$



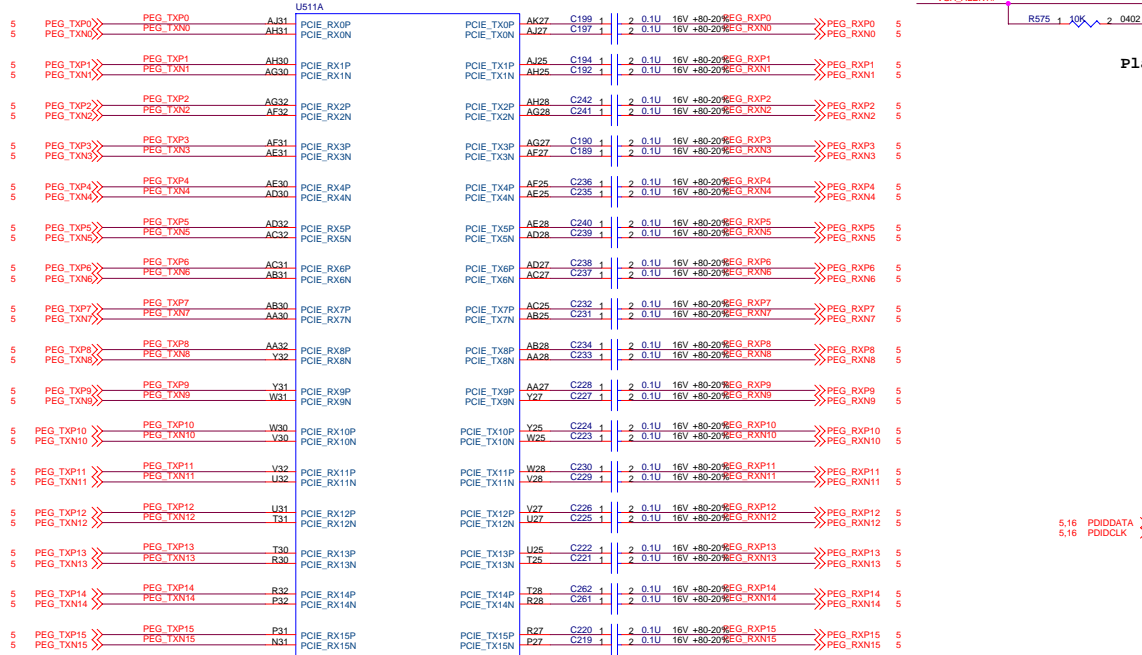
PCICLK_CARD	C402	1	2	10P/NA	0402
PCICLK_FWH	C403	1	2	10P	0402
PCICLK_KBC	C719	1	2	10P	0402
PCICLK_DBC	C405	1	2	10P/NA	0402
CLK_USB48	C398	1	2	10P	0402
SIO_48M	C395	1	2	10P	0402
14M_ICH	C718	1	2	10P/NA	0402
PCICLK_ICH	C737	1	2	10P	0402
PCIECLK_NCARD	C730	1	2	10P/NA	0402
PCIECLK_NCARD#	C731	1	2	10P/NA	0402
MINIPICIECLK1	C702	1	2	10P/NA	0402
MINIPICIECLK1#	C701	1	2	10P/NA	0402
MINIPICIECLK2	C732	1	2	10P/NA	0402
MINIPICIECLK2#	C703	1	2	10P/NA	0402
CLK_PCIE_LAN	C705	1	2	10P/NA	0402
CLK_PCIE_LAN#	C704	1	2	10P/NA	0402
CLK_MSX	C727	1	2	10P/NA	0402
CLK_MSX#	C728	1	2	10P/NA	0402
CLK_ICH	C729	1	2	10P	0402
CLK_ICH#	C726	1	2	10P	0402
HCLK_CPU	C714	1	2	10P/NA	0402
HCLK_CPU#	C713	1	2	10P/NA	0402
FS_A	C733	1	2	10P	0402
FS_B	C720	1	2	10P/NA	0402
FS_C	C721	1	2	10P/NA	0402
HCLK_MCH	C712	1	2	10P/NA	0402
HCLK_MCH#	C710	1	2	10P/NA	0402



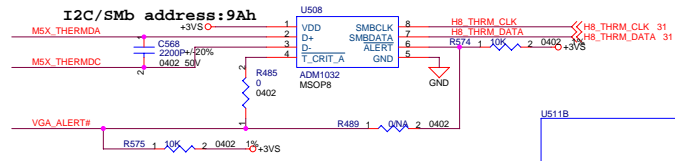
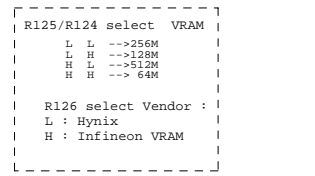
File	ICS CLOCK GENERATOR	
Size	Document	Rev
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Date	Wednesday, November 30, 2005	Sheet 8 of 46



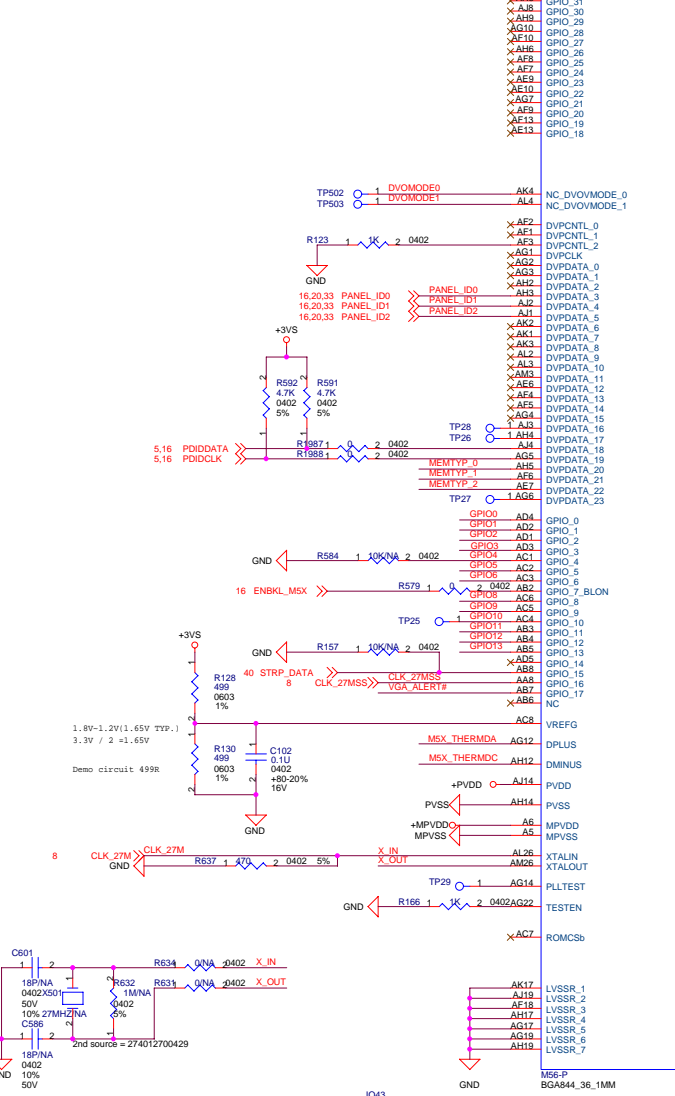
ATI M56-P (1/3)



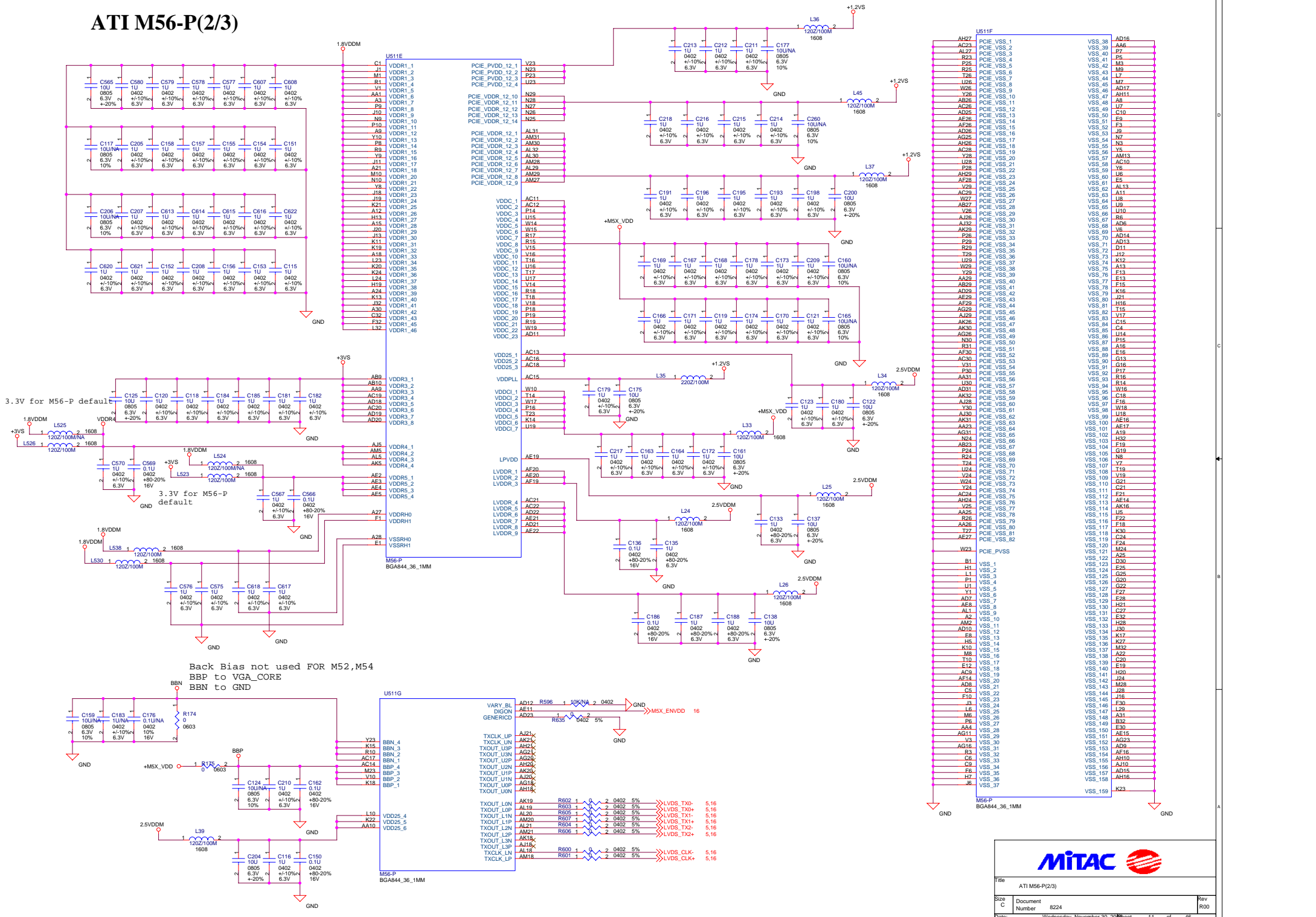
GPIO have internal PD



Place close at GPU side



ATI M56-P(2/3)



Back Bias not used FOR M52,M54
BBP to VGA_CORE
BBN to GND

File		ATI M56-P(2/3)	
Size	C	Document	8224
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ATI M56-P (3/3)

13 MEMA_MD[0..63]

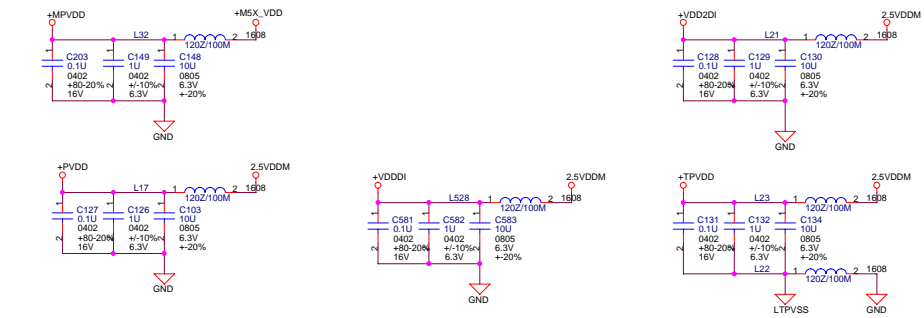
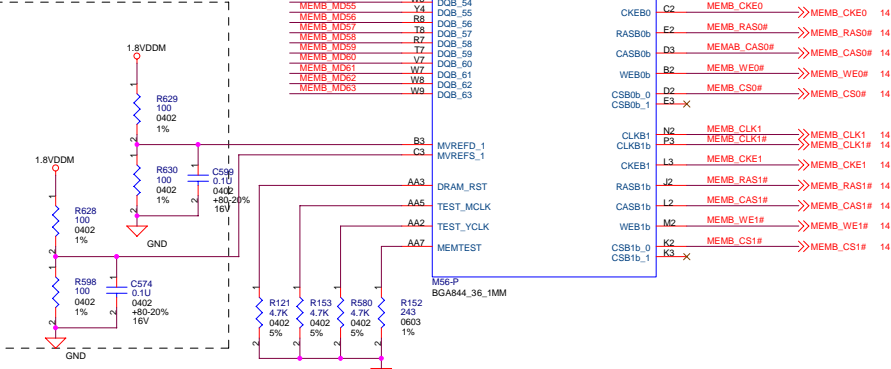
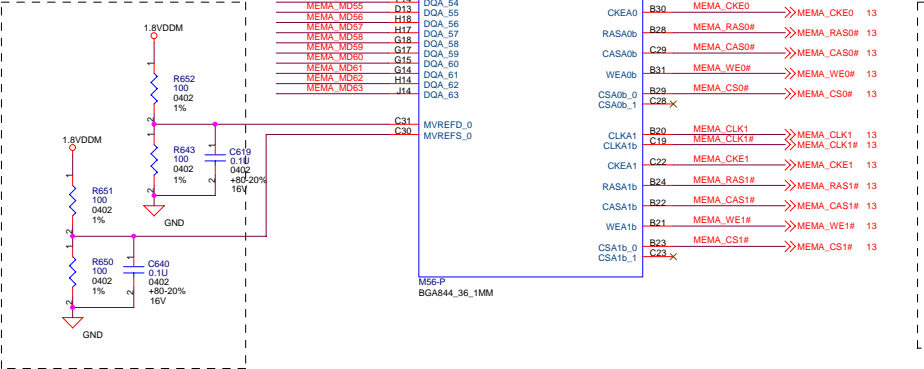
14 MEMB_MD[0..63]

U511C						
MEMA_MD0	M31	MAA_0	D26	MEMA_MAO	MEMA_MAO	13
MEMA_MD1	M30	MAA_1	E28	MEMA_MAI	MEMA_MAI	13
MEMA_MD2	L31	MAA_2	D28	MEMA_MAJ	MEMA_MAJ	13
MEMA_MD3	L30	MAA_3	D26	MEMA_MAK	MEMA_MAK	13
MEMA_MD4	H30	MAA_4	E24	MEMA_MAL	MEMA_MAL	13
MEMA_MD5	G31	MAA_5	E26	MEMA_MAM	MEMA_MAM	13
MEMA_MD6	G30	MAA_6	D27	MEMA_MAN	MEMA_MAN	13
MEMA_MD7	F31	MAA_7	F25	MEMA_MAO	MEMA_MAO	13
MEMA_MD8	M27	MAA_8	C26	MEMA_MAI	MEMA_MAI	13
MEMA_MD9	M29	MAA_9	B26	MEMA_MAJ	MEMA_MAJ	13
MEMA_MD10	L28	MAA_10	D29	MEMA_MAK	MEMA_MAK	13
MEMA_MD12	J27	MAA_12	R27	MEMA_MAL	MEMA_MAL	13
MEMA_MD13	L27	MAA_13	E27	MEMA_MAM	MEMA_MAM	13
MEMA_MD14	H29	MAA_14	E29	MEMA_MAN	MEMA_MAN	13
MEMA_MD15	G27	MAA_15	R25	MEMA_BA0	TP54	13
MEMA_MD16	L28	MAA_15	C25	MEMA_BA1	MEMA_BA1	13
MEMA_MD17	M28	DOMAb_0	H31	MEMA_DOM0#	MEMA_DOM0#	13
MEMA_MD18	L25	DOMAb_1	J29	MEMA_DOM1#	MEMA_DOM1#	13
MEMA_MD19	L25	DOMAb_2	J26	MEMA_DOM2#	MEMA_DOM2#	13
MEMA_MD20	J25	DOMAb_3	G23	MEMA_DOM3#	MEMA_DOM3#	13
MEMA_MD21	L27	DOMAb_4	E21	MEMA_DOM4#	MEMA_DOM4#	13
MEMA_MD22	G28	DOMAb_5	B15	MEMA_DOM5#	MEMA_DOM5#	13
MEMA_MD23	H27	DOMAb_6	D14	MEMA_DOM6#	MEMA_DOM6#	13
MEMA_MD24	H27	DOMAb_7	J17	MEMA_DOM7#	MEMA_DOM7#	13
MEMA_MD25	H26	QSA_0	J31	MEMA_QS0	MEMA_QS0	13
MEMA_MD26	G26	QSA_1	K29	MEMA_QS1	MEMA_QS1	13
MEMA_MD27	H24	QSA_2	K25	MEMA_QS2	MEMA_QS2	13
MEMA_MD28	H24	QSA_3	F23	MEMA_QS3	MEMA_QS3	13
MEMA_MD29	H22	QSA_4	D20	MEMA_QS4	MEMA_QS4	13
MEMA_MD30	J23	QSA_5	B16	MEMA_QS5	MEMA_QS5	13
MEMA_MD31	J22	QSA_6	D16	MEMA_QS6	MEMA_QS6	13
MEMA_MD32	E23	QSA_7	H15	MEMA_QS7	MEMA_QS7	13
MEMA_MD33	D22	QSA_0B	K31	MEMA_QS0#	MEMA_QS0#	13
MEMA_MD34	D23	QSA_1B	K28	MEMA_QS1#	MEMA_QS1#	13
MEMA_MD35	D24	QSA_2B	K26	MEMA_QS2#	MEMA_QS2#	13
MEMA_MD36	E22	QSA_3B	G24	MEMA_QS3#	MEMA_QS3#	13
MEMA_MD37	F20	QSA_4B	D21	MEMA_QS4#	MEMA_QS4#	13
MEMA_MD38	F20	QSA_5B	C16	MEMA_QS5#	MEMA_QS5#	13
MEMA_MD39	D19	QSA_6B	D15	MEMA_QS6#	MEMA_QS6#	13
MEMA_MD40	B19	QSA_7B	J15	MEMA_QS7#	MEMA_QS7#	13
MEMA_MD41	C17	ODTA0	F29	MEMA_ODTA0	MEMA_ODTA0	13
MEMA_MD42	B18	ODTA1	D24	MEMA_ODTA1	MEMA_ODTA1	13
MEMA_MD43	C17	CLKA0	D31	MEMA_CLK0	MEMA_CLK0	13
MEMA_MD44	C14	CLKA0b	E31	MEMA_CLK0#	MEMA_CLK0#	13
MEMA_MD45	B14	CKEA0	B30	MEMA_CKE0	MEMA_CKE0	13
MEMA_MD46	C13	RASAb	C28	MEMA_RAS0#	MEMA_RAS0#	13
MEMA_MD47	B13	CASAb	B29	MEMA_CAS0#	MEMA_CAS0#	13
MEMA_MD48	D17	WEAb	B31	MEMA_WE0#	MEMA_WE0#	13
MEMA_MD49	D18	CSA0b_0	B29	MEMA_CS0#	MEMA_CS0#	13
MEMA_MD50	E17	CSA0b_1	C28			
MEMA_MD51	F17	CLKA1	B20	MEMA_CLK1	MEMA_CLK1	13
MEMA_MD52	E15	CLKA1b	C19	MEMA_CLK1#	MEMA_CLK1#	13
MEMA_MD53	E14	CKEA1	C22	MEMA_CKE1	MEMA_CKE1	13
MEMA_MD54	F14	RASA1b	B24	MEMA_RAS1#	MEMA_RAS1#	13
MEMA_MD55	H18	CASA1b	B22	MEMA_CAS1#	MEMA_CAS1#	13
MEMA_MD56	H18	WEA1b	B21	MEMA_WE1#	MEMA_WE1#	13
MEMA_MD57	H17	CSA1b_0	B23	MEMA_CS1#	MEMA_CS1#	13
MEMA_MD58	G18	CSA1b_1	C23			
MEMA_MD59	G18					
MEMA_MD60	G15					
MEMA_MD61	G14					
MEMA_MD62	H14					
MEMA_MD63	J14					

U511D						
MEMB_MD0	B12	MAB_0	G4	MEMB_MAO	MEMB_MAO	14
MEMB_MD1	C12	MAB_1	E6	MEMB_MAI	MEMB_MAI	14
MEMB_MD2	B11	MAB_2	E4	MEMB_MAJ	MEMB_MAJ	14
MEMB_MD3	C11	MAB_3	H4	MEMB_MAK	MEMB_MAK	14
MEMB_MD4	C7	MAB_4	J5	MEMB_MAL	MEMB_MAL	14
MEMB_MD5	C8	MAB_5	G5	MEMB_MAM	MEMB_MAM	14
MEMB_MD6	B12	MAB_6	F4	MEMB_MAN	MEMB_MAN	14
MEMB_MD7	B6	MAB_7	H6	MEMB_MAO	MEMB_MAO	14
MEMB_MD8	D12	MAB_8	G2	MEMB_MAI	MEMB_MAI	14
MEMB_MD9	F11	MAB_9	F2	MEMB_MAJ	MEMB_MAJ	14
MEMB_MD10	F11	MAB_10	D4	MEMB_MAK	MEMB_MAK	14
MEMB_MD11	F9	MAB_11	F2	MEMB_MAL	MEMB_MAL	14
MEMB_MD12	F9	MAB_12	H2	MEMB_MAM	MEMB_MAM	14
MEMB_MD13	D8	MAB_13	D5	MEMB_MAN	MEMB_MAN	14
MEMB_MD14	D7	MAB_14	H2	MEMB_BA0	TP36	14
MEMB_MD15	E7	MAB_15	H3	MEMB_BA1	MEMB_BA1	14
MEMB_MD16	G11	DOMBb_0	B8	MEMB_DOM0#	MEMB_DOM0#	14
MEMB_MD17	G11	DOMBb_1	G9	MEMB_DOM1#	MEMB_DOM1#	14
MEMB_MD18	H12	DOMBb_2	D9	MEMB_DOM2#	MEMB_DOM2#	14
MEMB_MD19	H9	DOMBb_3	K7	MEMB_DOM3#	MEMB_DOM3#	14
MEMB_MD20	E8	DOMBb_4	M6	MEMB_DOM4#	MEMB_DOM4#	14
MEMB_MD21	F8	DOMBb_5	V2	MEMB_DOM5#	MEMB_DOM5#	14
MEMB_MD22	G8	DOMBb_6	W4	MEMB_DOM6#	MEMB_DOM6#	14
MEMB_MD23	G6	DOMBb_7	T9	MEMB_DOM7#	MEMB_DOM7#	14
MEMB_MD24	G7	OSB_0	B9	MEMB_QS0	MEMB_QS0	14
MEMB_MD25	G6	OSB_1	D10	MEMB_QS1	MEMB_QS1	14
MEMB_MD26	H8	OSB_2	H10	MEMB_QS2	MEMB_QS2	14
MEMB_MD27	K8	OSB_3	K6	MEMB_QS3	MEMB_QS3	14
MEMB_MD28	K8	OSB_4	L2	MEMB_QS4	MEMB_QS4	14
MEMB_MD29	L8	OSB_5	N4	MEMB_QS5	MEMB_QS5	14
MEMB_MD30	L9	OSB_6	U4	MEMB_QS6	MEMB_QS6	14
MEMB_MD31	L8	OSB_7	V8	MEMB_QS7	MEMB_QS7	14
MEMB_MD32	K5	OSB_0B	B10	MEMB_QS0#	MEMB_QS0#	14
MEMB_MD33	K4	OSB_1B	E10	MEMB_QS1#	MEMB_QS1#	14
MEMB_MD34	K5	OSB_2B	G10	MEMB_QS2#	MEMB_QS2#	14
MEMB_MD35	K4	OSB_3B	J7	MEMB_QS3#	MEMB_QS3#	14
MEMB_MD36	K4	OSB_4B	M4	MEMB_QS4#	MEMB_QS4#	14
MEMB_MD37	K5	OSB_5B	V4	MEMB_QS5#	MEMB_QS5#	14
MEMB_MD38	K4	OSB_6B	J7	MEMB_QS6#	MEMB_QS6#	14
MEMB_MD39	P4	OSB_7B	V9	MEMB_QS7#	MEMB_QS7#	14
MEMB_MD40	P4	ODTB0	D6	MEMB_ODTA0	MEMB_ODTA0	14
MEMB_MD41	P2	ODTB1	J4	MEMB_ODTA1	MEMB_ODTA1	14
MEMB_MD42	R2	CLKB0	B4	MEMB_CLK0	MEMB_CLK0	14
MEMB_MD43	R2	CLKB0b	B5	MEMB_CLK0#	MEMB_CLK0#	14
MEMB_MD44	R2	CKEB0	C2	MEMB_CKE0	MEMB_CKE0	14
MEMB_MD45	W3	RASB0b	E2	MEMB_RAS0#	MEMB_RAS0#	14
MEMB_MD46	W2	CASB0b	D3	MEMB_CAS0#	MEMB_CAS0#	14
MEMB_MD47	W2	WE0b	B2	MEMB_WE0#	MEMB_WE0#	14
MEMB_MD48	W3	CSB0b_0	D3	MEMB_CS0#	MEMB_CS0#	14
MEMB_MD49	W2	CSB0b_1	E2			
MEMB_MD50	R5	CLKB1	N2	MEMB_CLK1	MEMB_CLK1	14
MEMB_MD51	R5	CLKB1b	P3	MEMB_CLK1#	MEMB_CLK1#	14
MEMB_MD52	W5	CKEB1	L3	MEMB_CKE1	MEMB_CKE1	14
MEMB_MD53	W6	RASB1b	J2	MEMB_RAS1#	MEMB_RAS1#	14
MEMB_MD54	W6	CASB1b	L2	MEMB_CAS1#	MEMB_CAS1#	14
MEMB_MD55	W6	WE1b	M2	MEMB_WE1#	MEMB_WE1#	14
MEMB_MD56	W6	CSB1b_0	K2	MEMB_CS1#	MEMB_CS1#	14
MEMB_MD57	W8	CSB1b_1	K3			
MEMB_MD58	W7					
MEMB_MD59	W7					
MEMB_MD60	W7					
MEMB_MD61	W7					
MEMB_MD62	W7					
MEMB_MD63	W9					

Close to M56-P

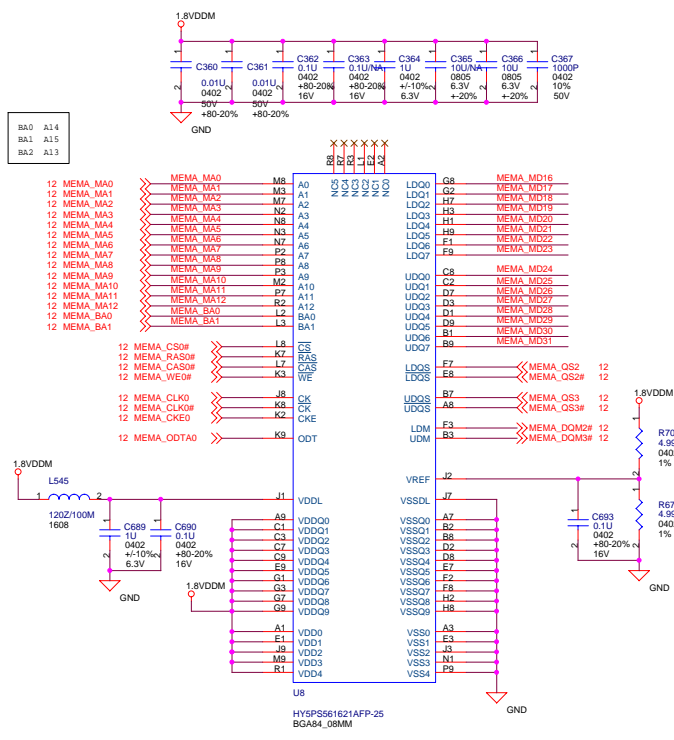
Close to M56-P



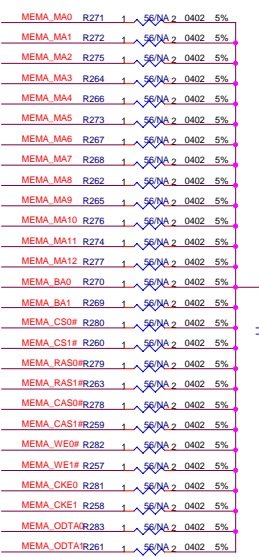
MITAC

File: ATI M56-P(3/3)

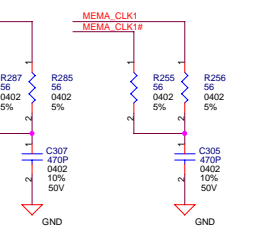
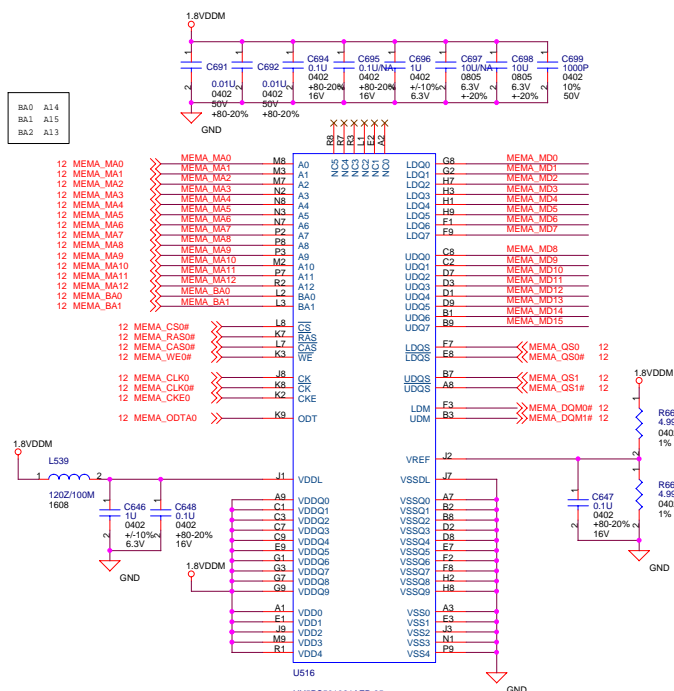
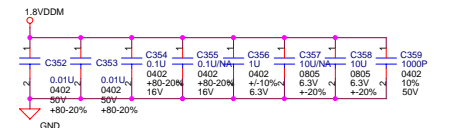
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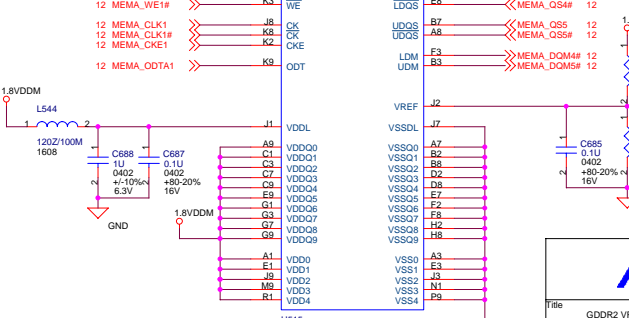
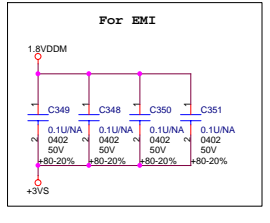
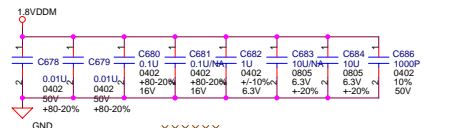
MEMA_MD0[63] MEMA_MD0[63] 12

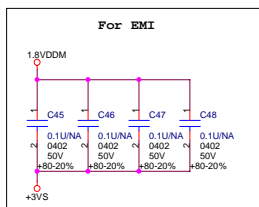
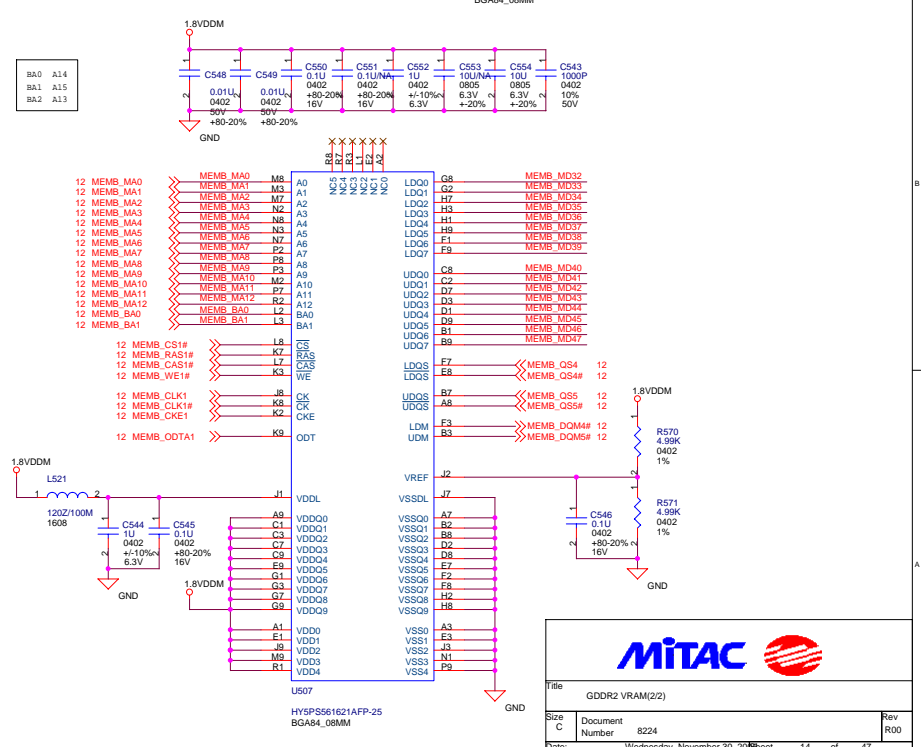
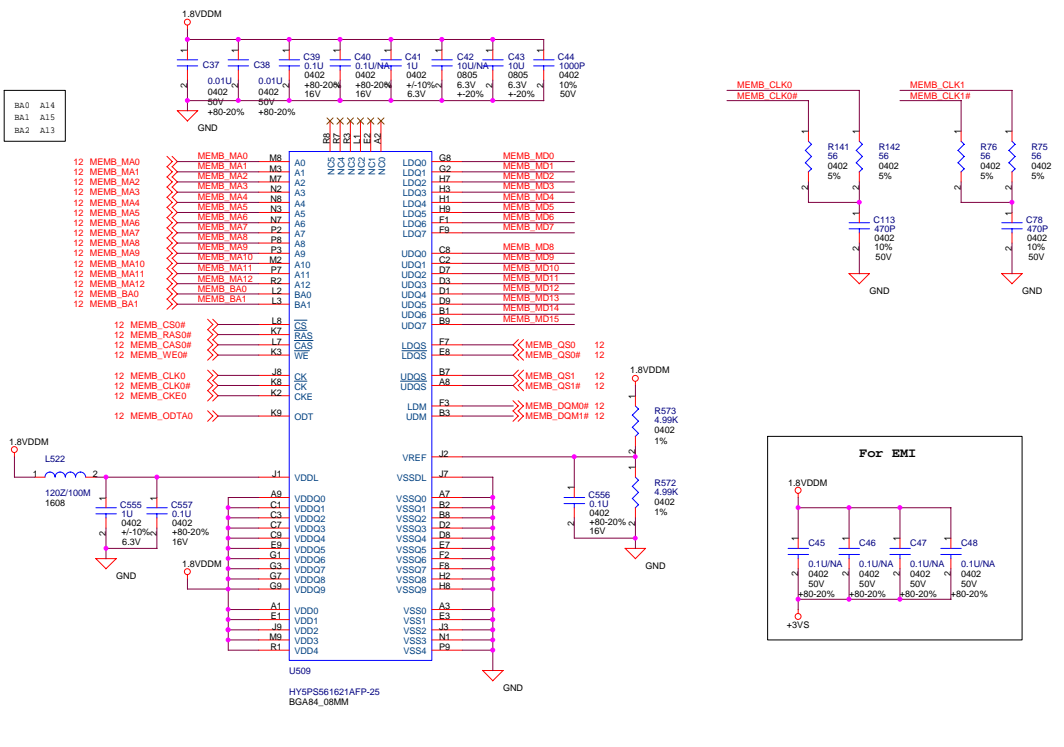
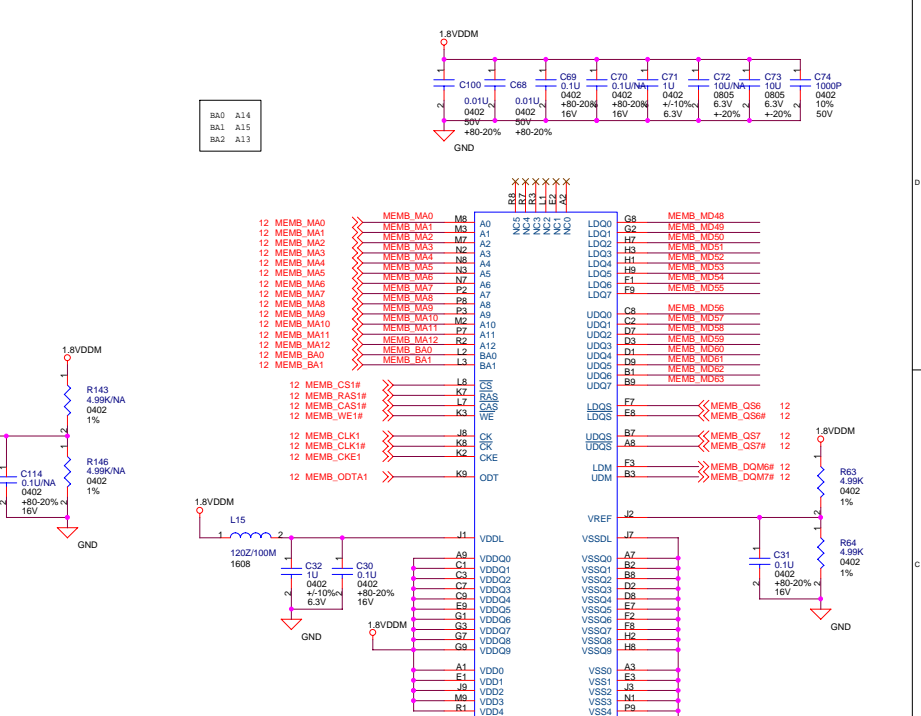
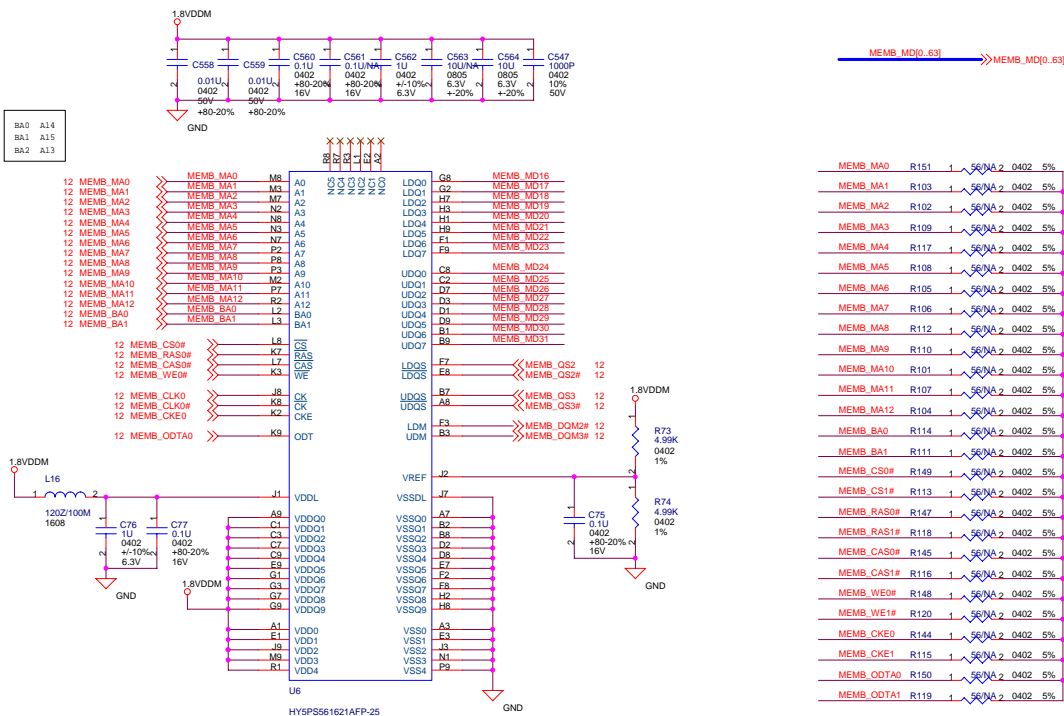


BA0 A14
BA1 A15
BA2 A13

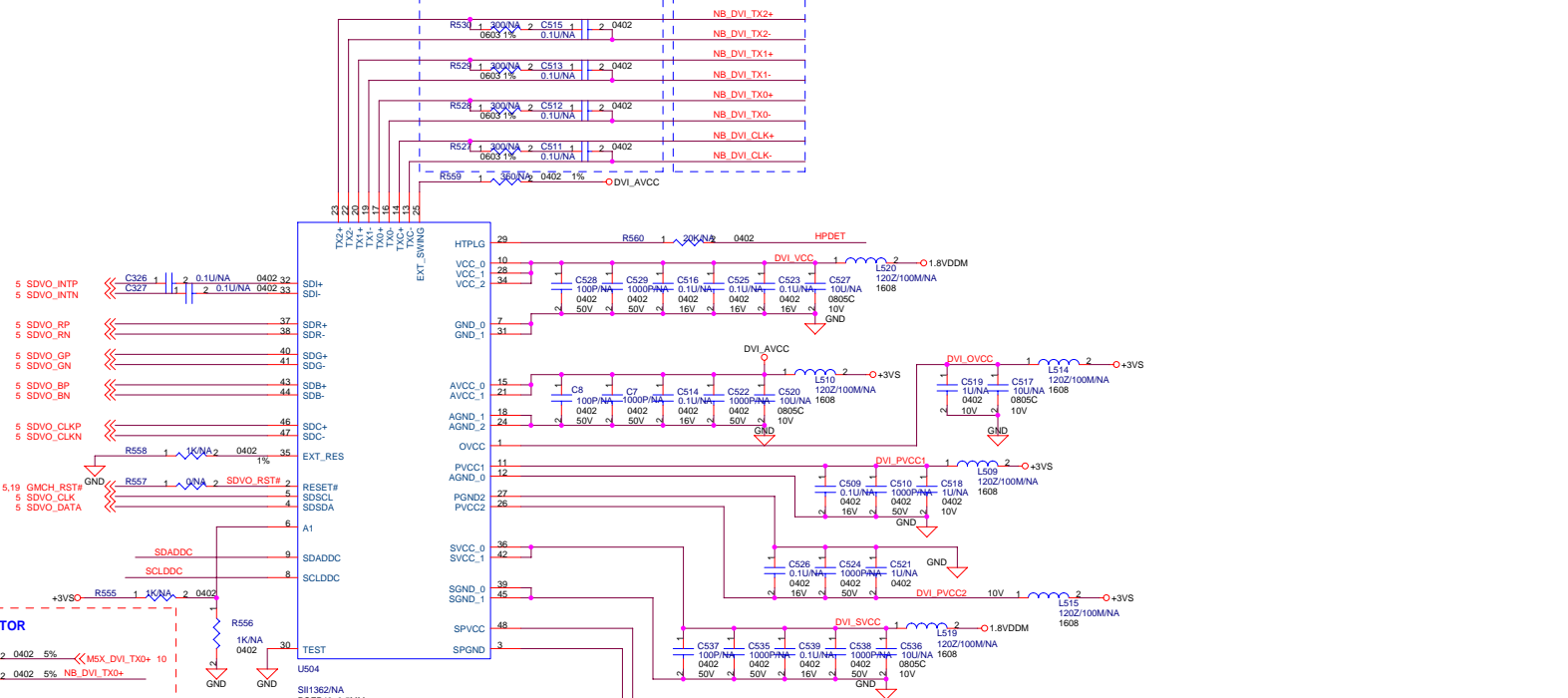


BA0 A14
BA1 A15
BA2 A13

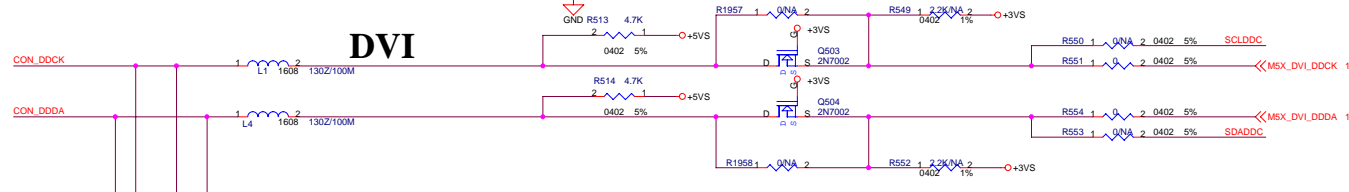
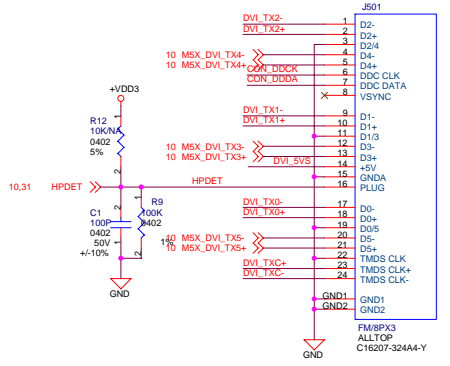
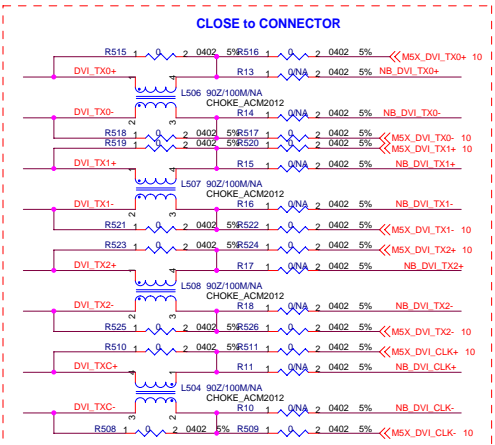




as CLOSE as possible to Sii1362 route trace with 100ohm differential impedance



DVI

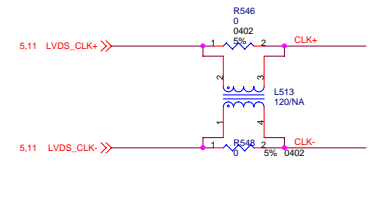
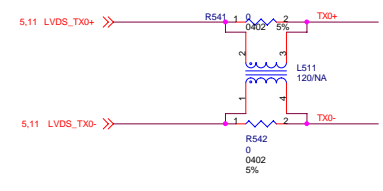
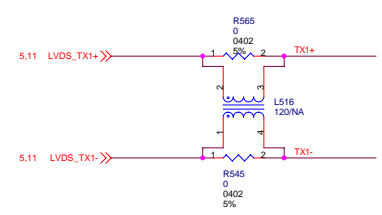
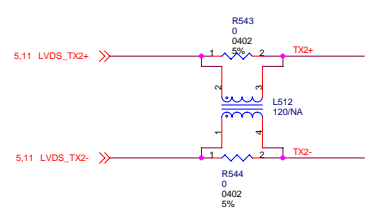
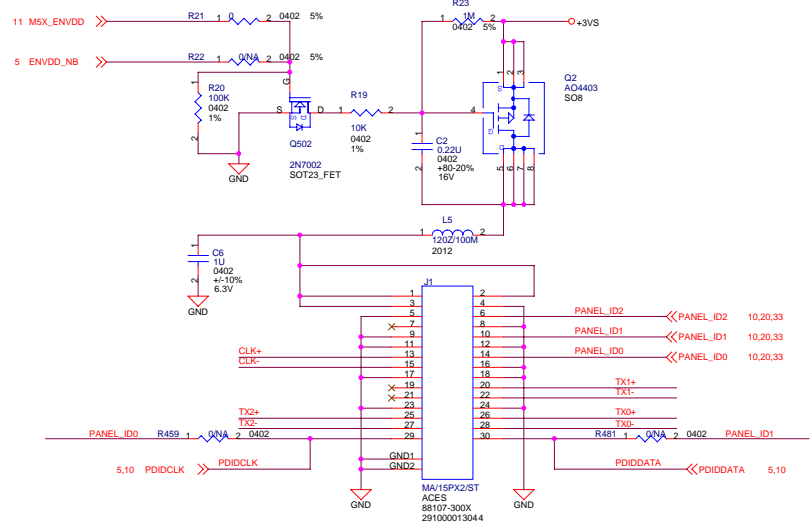
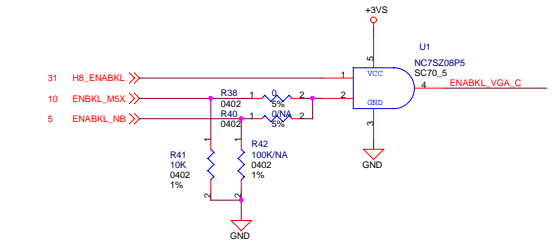
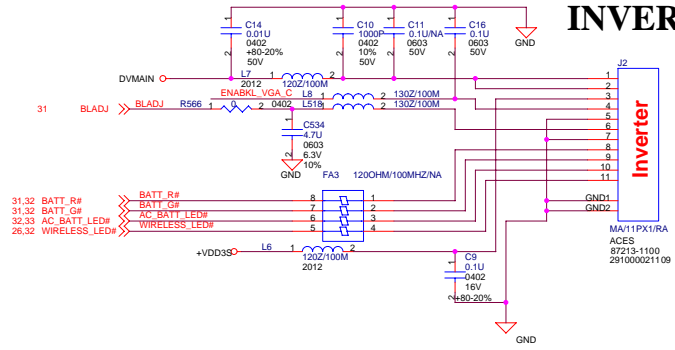


MITAC		
File: DVI-D CONNECTOR		
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Display (LCD)

Pannel ID			PANEL TYPE
LCD_ID0	LCD_ID1	LCD_ID2	
0	0	0	AU
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	CHIMEI

INVERTER



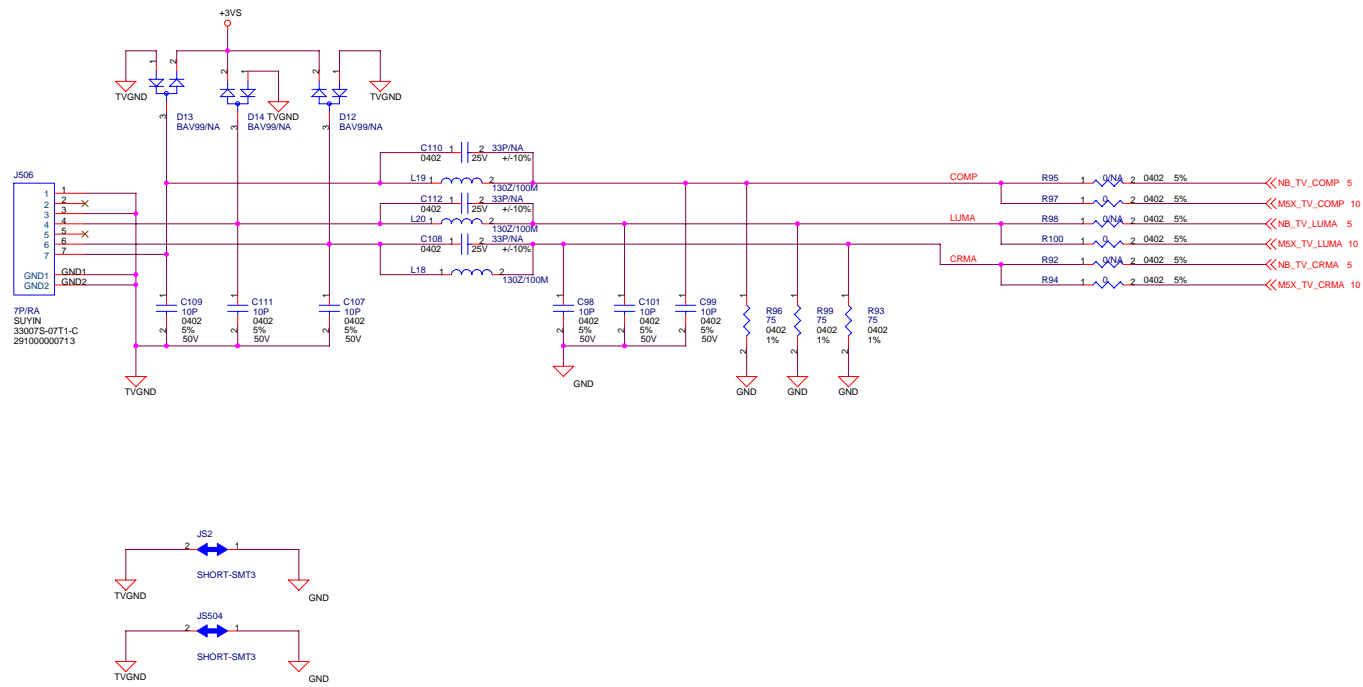
MITAC

File: LCD CONNECTOR

Size: C Document Number: 8224 Rev: R00

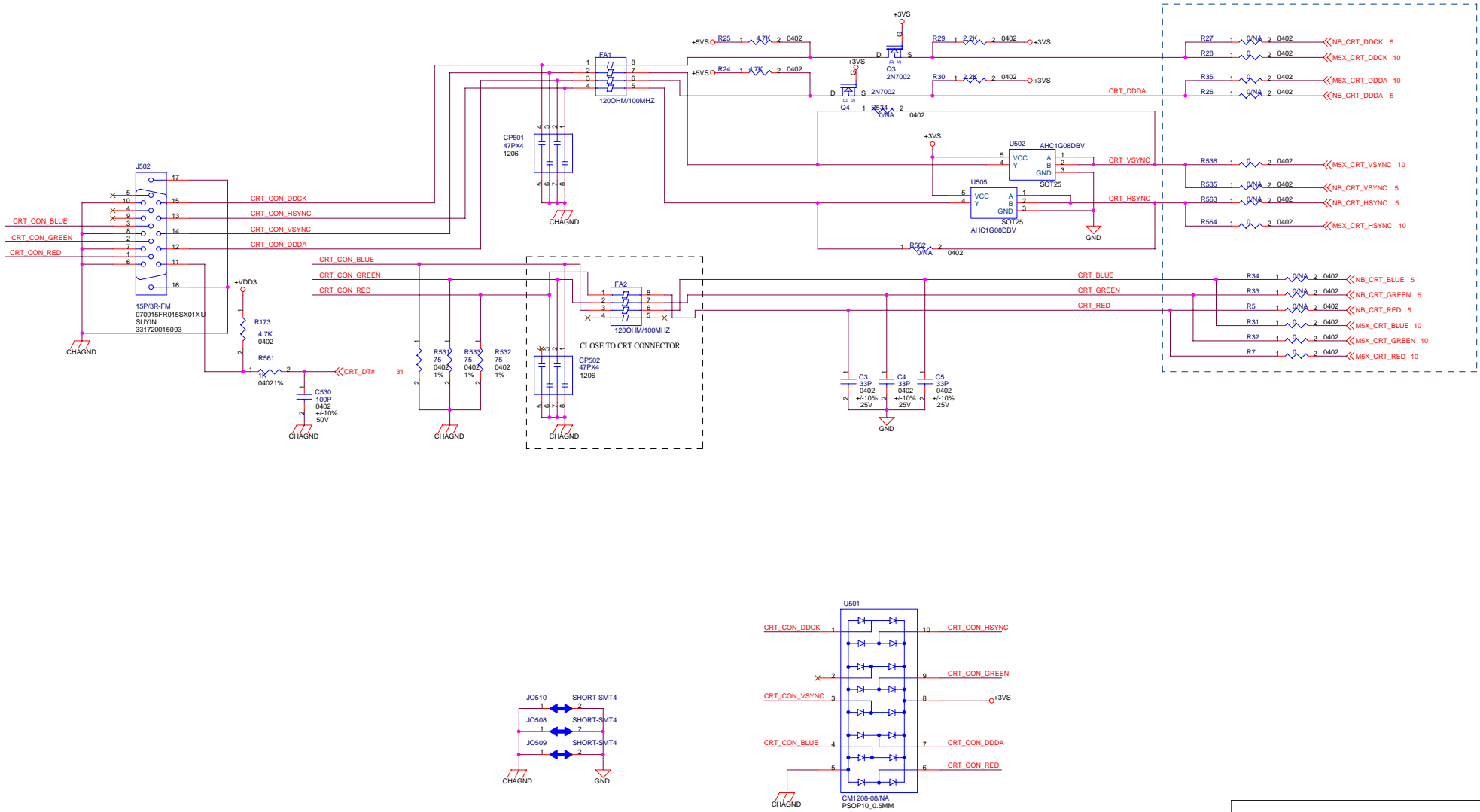
Date: Wednesday, November 30, 2005 Sheet: 16 of 41

TV CONNECTOR

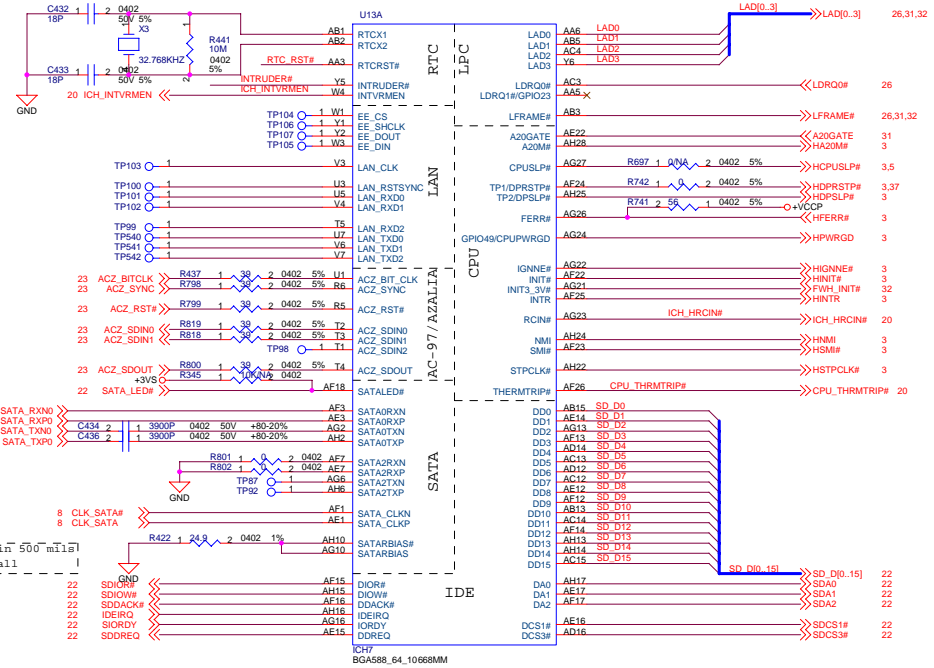
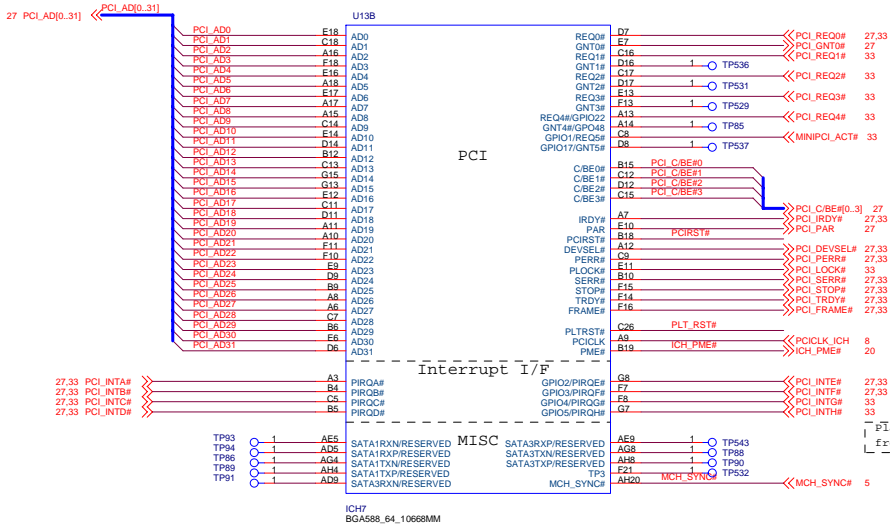
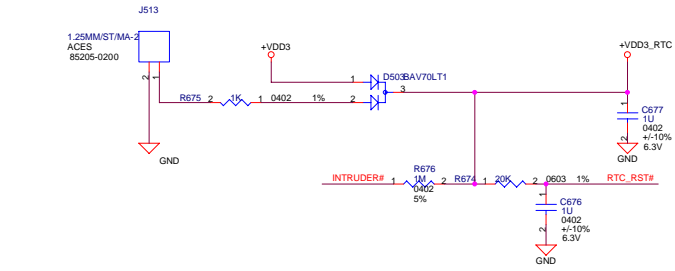
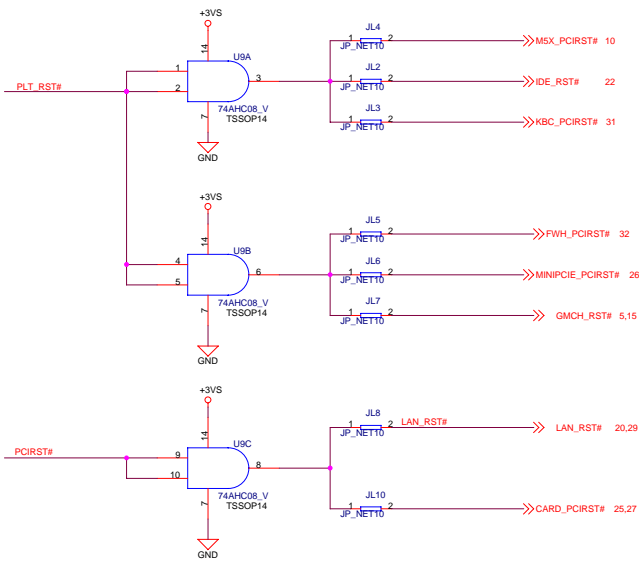


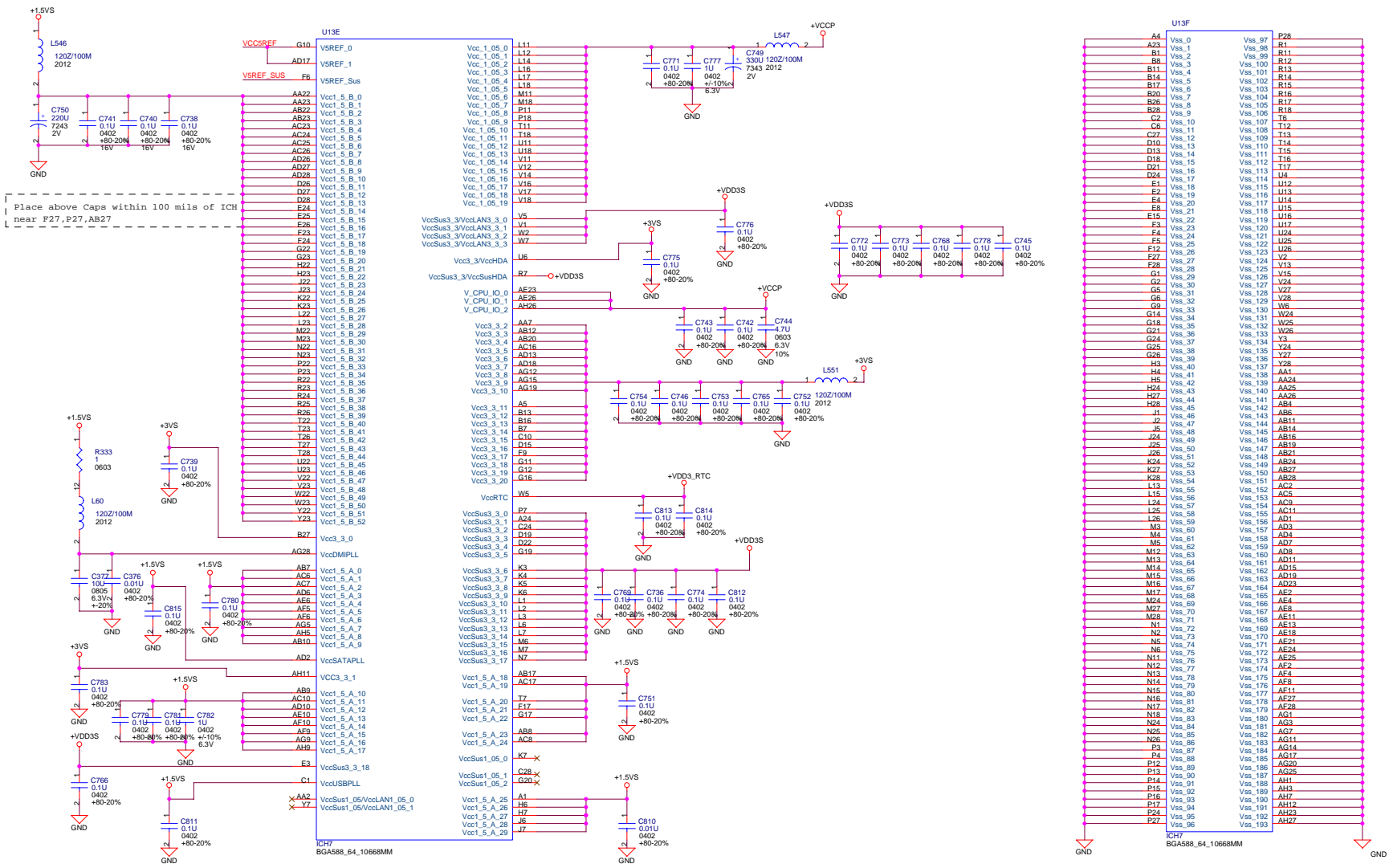
File TV-OUT CONNECTOR		
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CRT




File CRT CONNECTOR		
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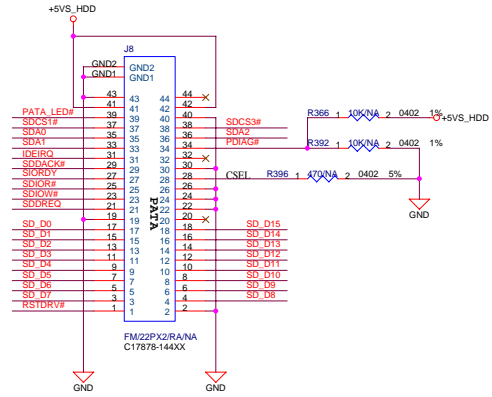
Place above Caps within 100 mils of ICH near P27, P27, AB27



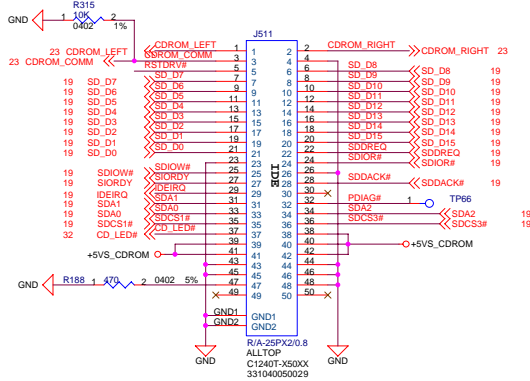
File ICH7-M(3/3)
 Size C Document Number 8224 Rev R00
 Date Wednesday, November 30, 2005 Sheet 21 of 41

CDROM- SECONDARY IDE CONNECTOR

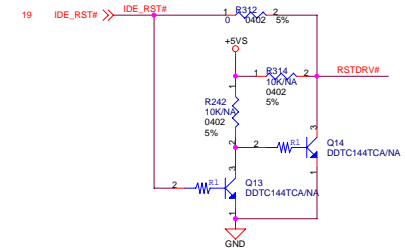
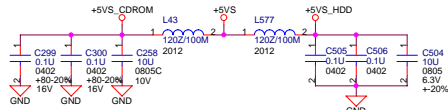
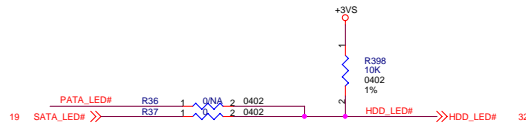
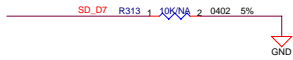
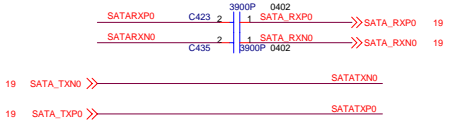
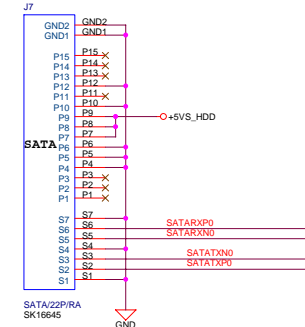
PATA HDD



CD-ROM

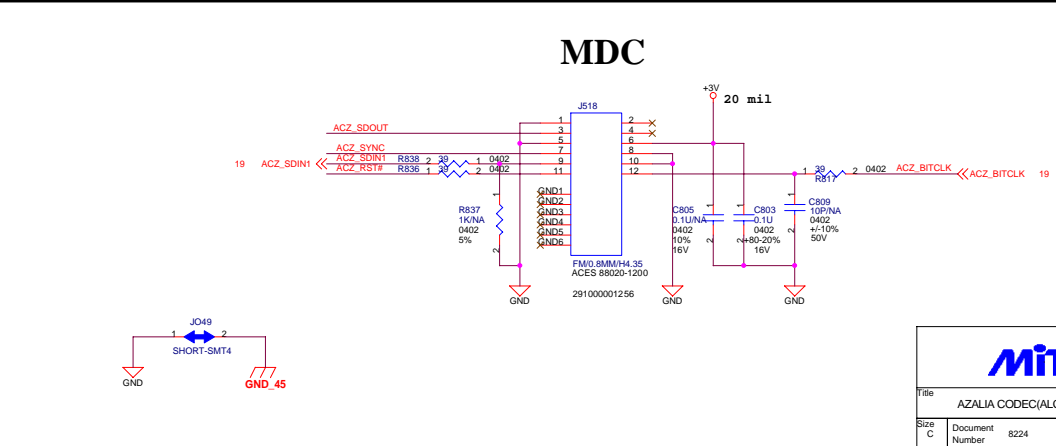
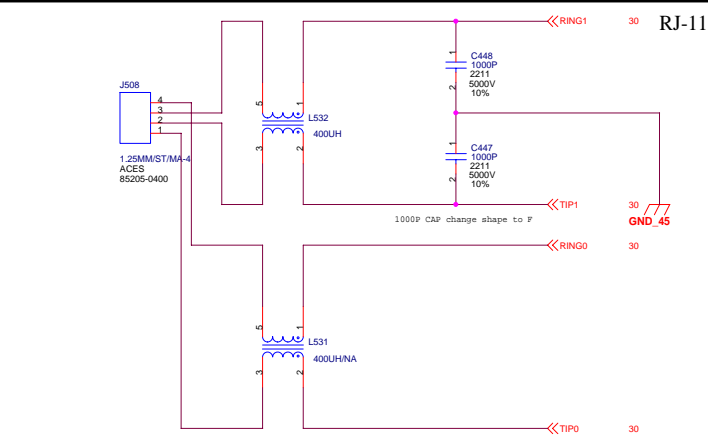
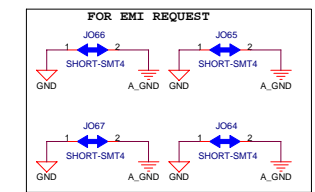
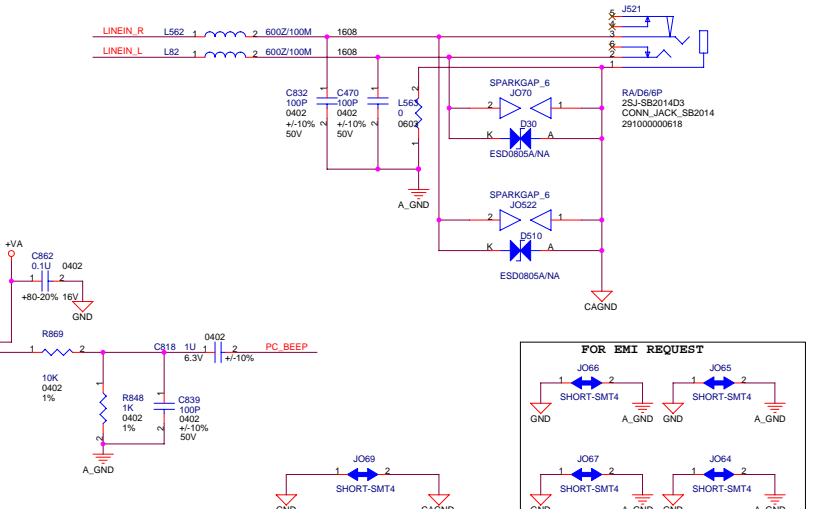
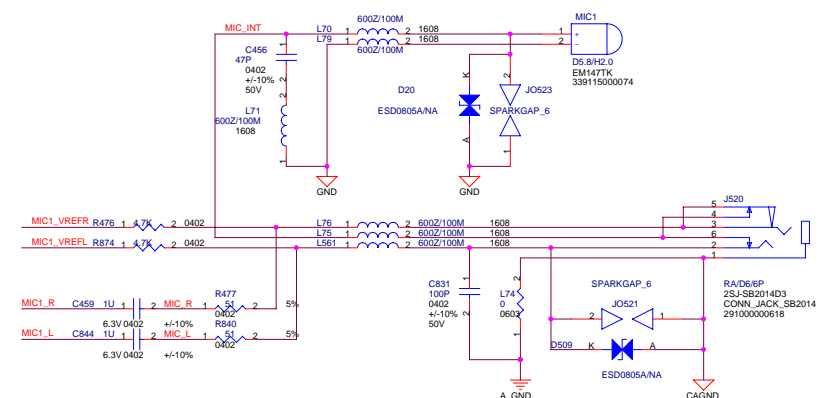
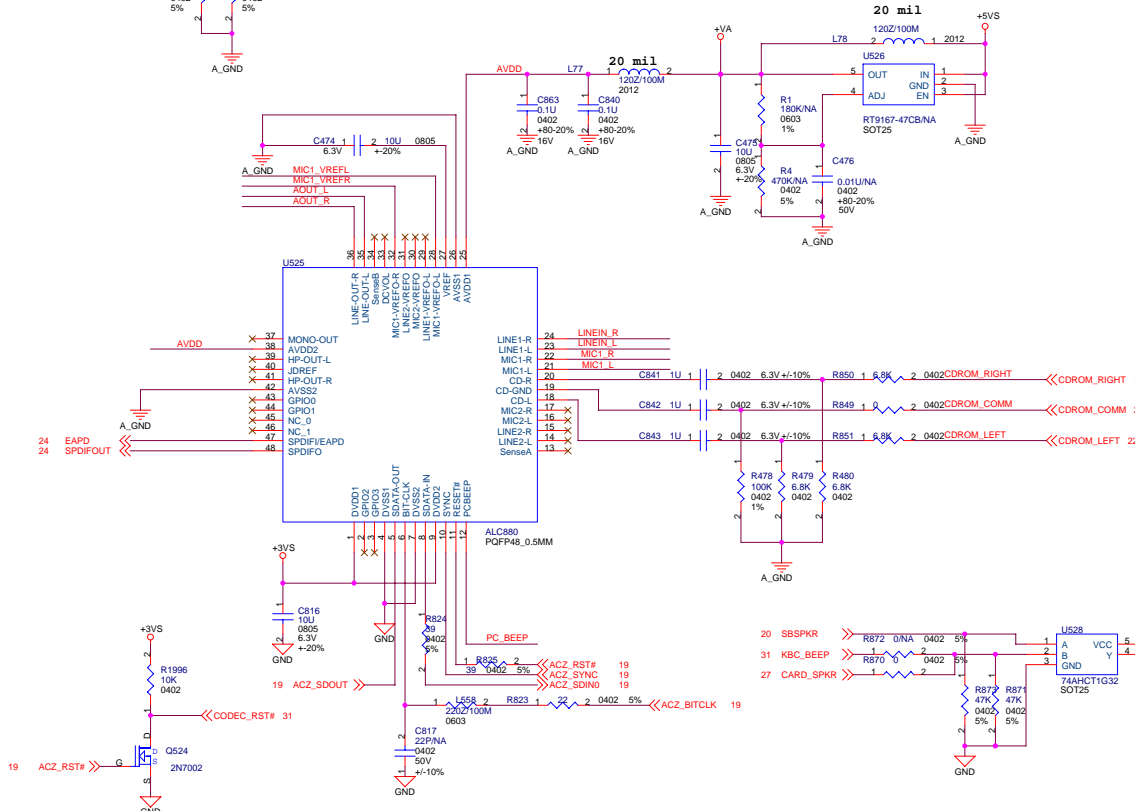
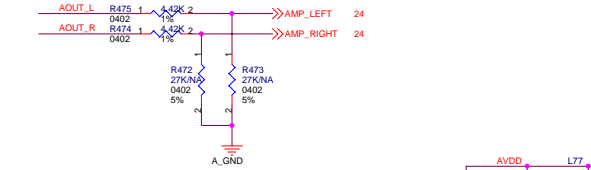


SATA HDD

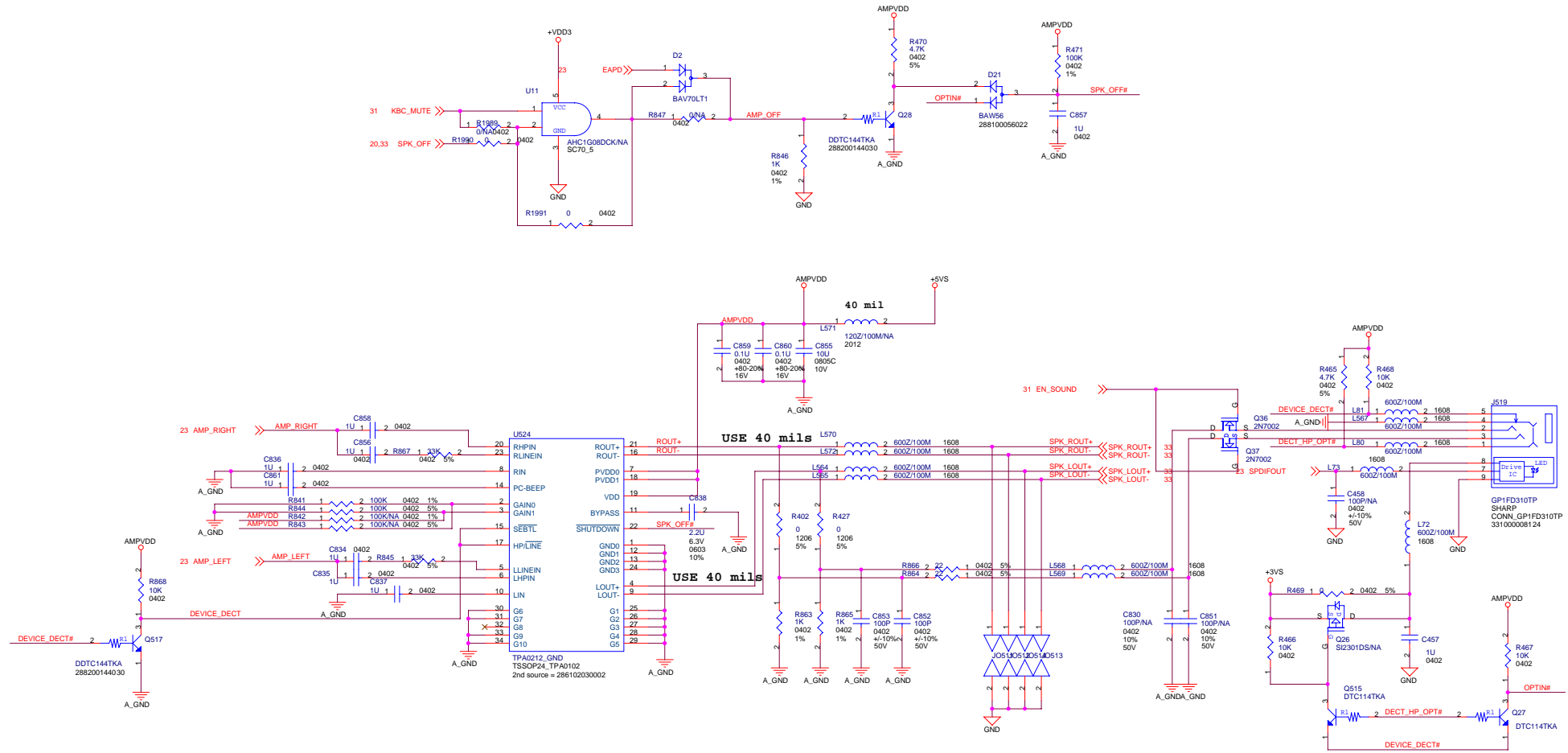


File CDROM/HDD CONNECTOR		
Size C	Document Number 8224	Rev R00
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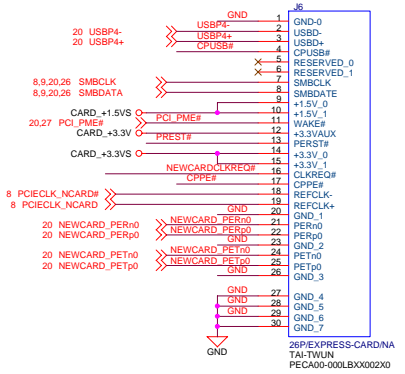
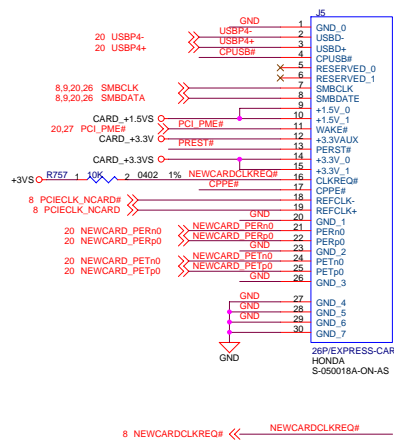
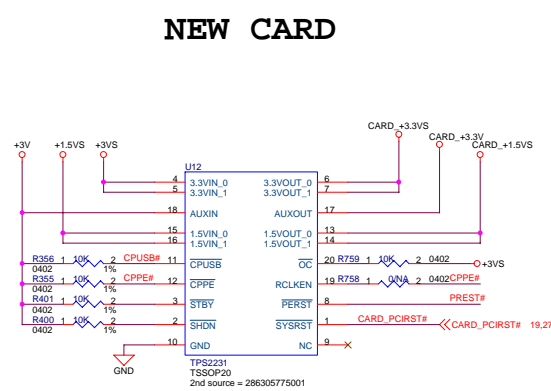
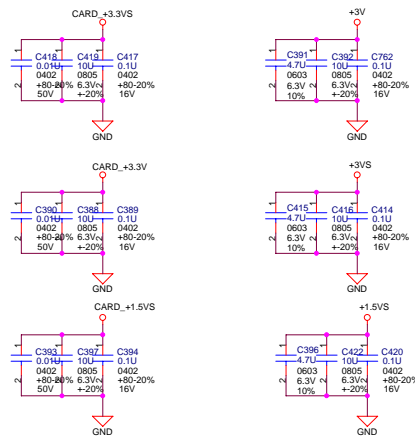
AZALIA CODEC(ALC880)



AUDIO AMPLIFIER



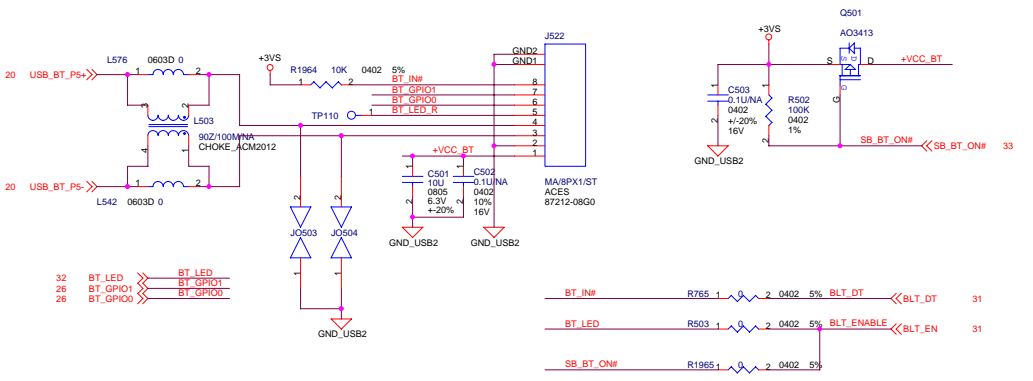
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AUDIO AMPLIFIER		
Size	Document	Rev
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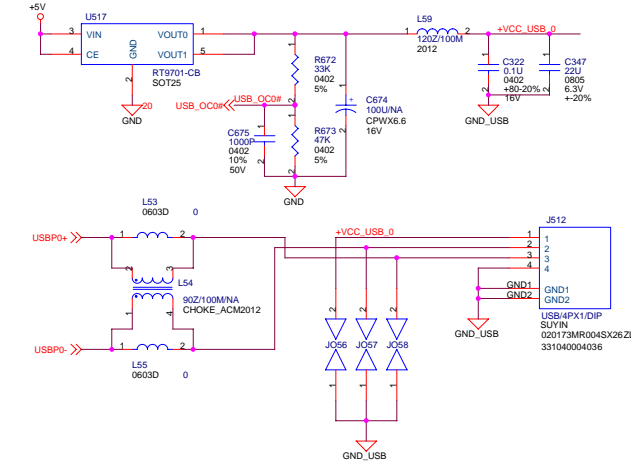
USB

GPIO0=> BLUETOOTH ACTIVITE
GPIO1=> WIRELESS ACTIVITE

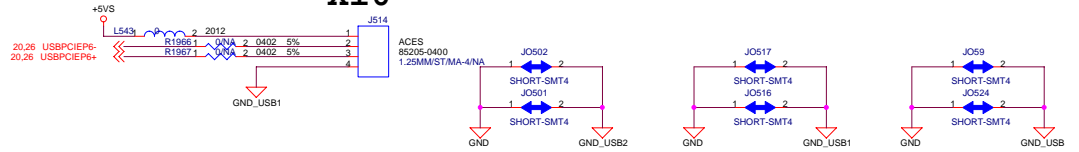
BLUE TOOTH



USB CONNECTOR

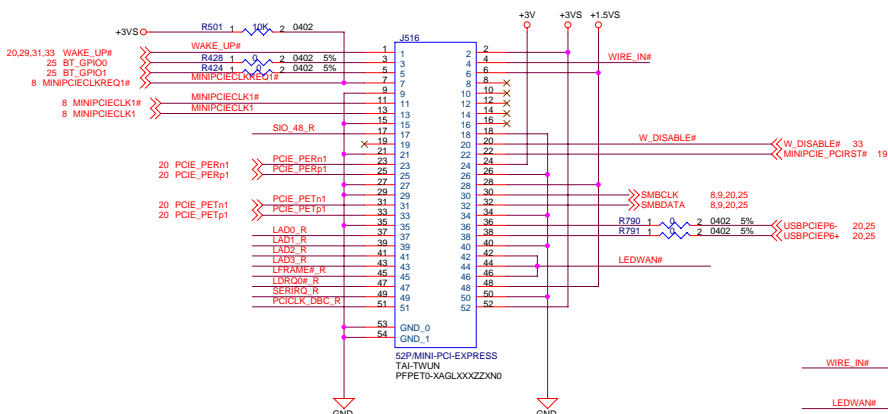


X10

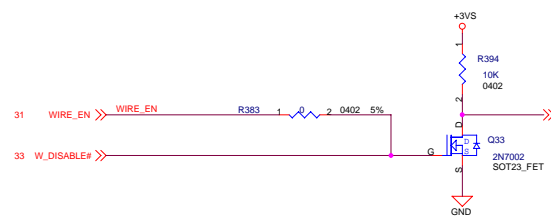


File			NEW CARD/BLUE TOOTH/USB CONNECTOR		
Size	Document	8224	Rev	R00	
C	Number		Date	Wednesday, November 30, 2005 Sheet 26 of 47	

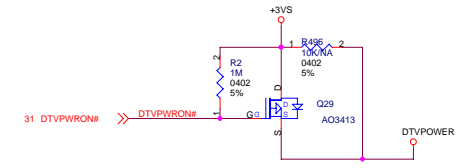
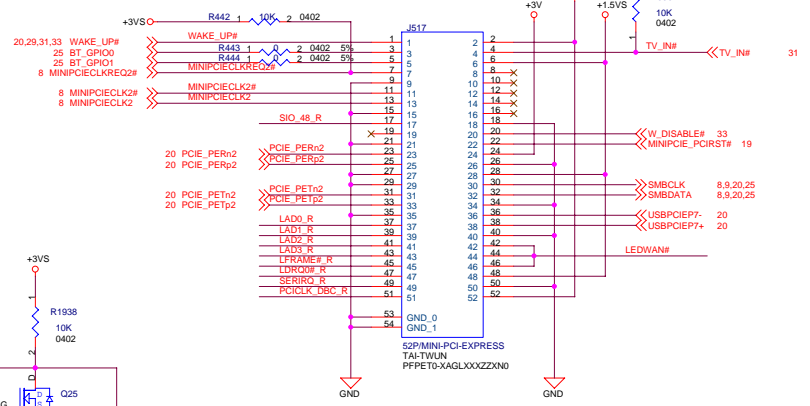
WIRELESS LAN CARD



8,27	SIO_48M	>>	SIO_48M	>>	SIO_48_R
19,31,32	LAD0	>>	LAD0	>>	LAD0_R
19,31,32	LAD1	>>	LAD1	>>	LAD1_R
19,31,32	LAD2	>>	LAD2	>>	LAD2_R
19,31,32	LAD3	>>	LAD3	>>	LAD3_R
19,31,32	LFRAME#	>>	LFRAME#	>>	LFRAME#_R
19	LDRQ#	>>	LDRQ#	>>	LDRQ#_R
20,27,31,33	SERIRQ	>>	SERIRQ	>>	SERIRQ_R
8	PCICLK_DBC	>>	PCICLK_DBC	>>	PCICLK_DBC_R

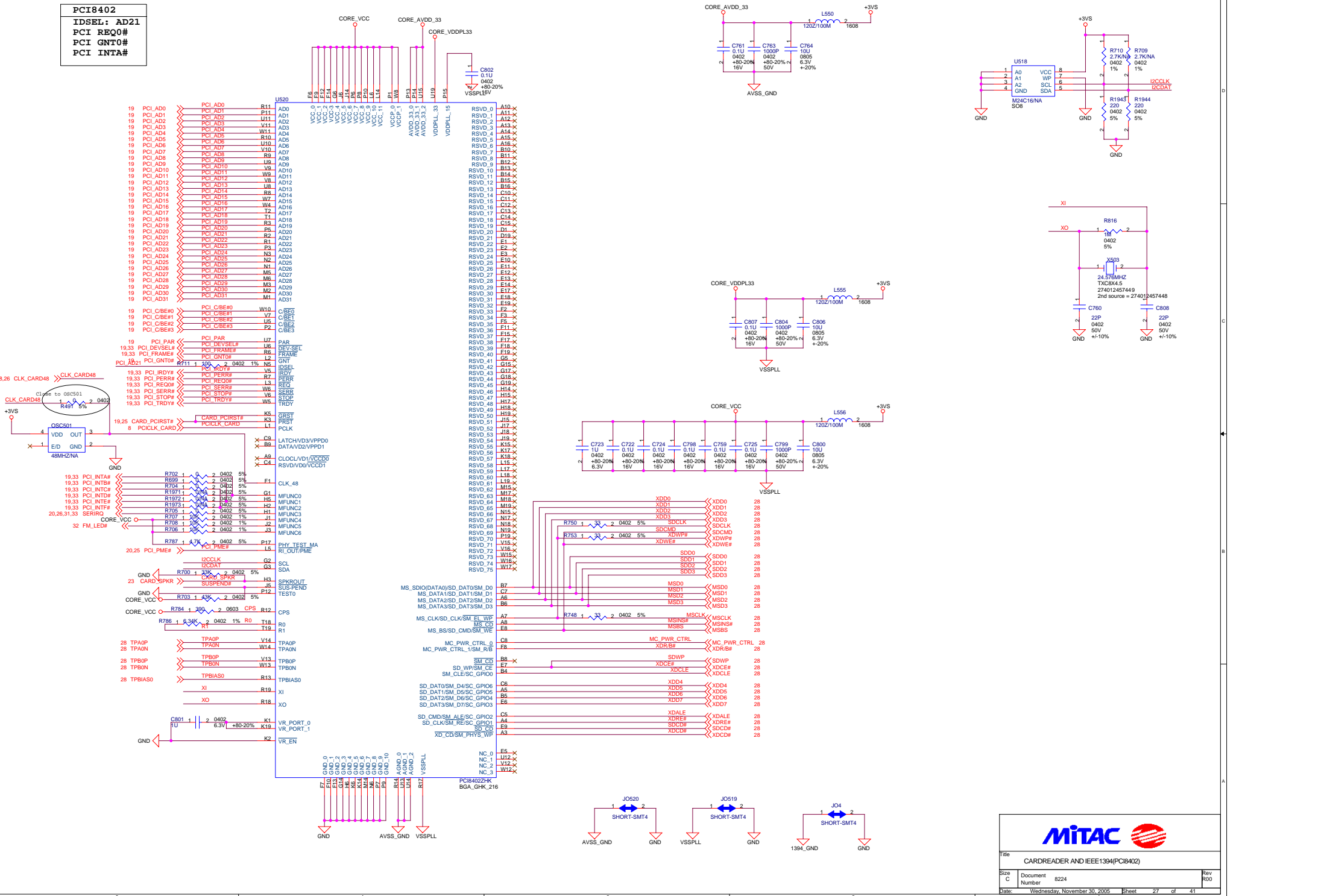


TV CARD



File		
MINI PCI-E (WIRELESS LAN/TV CARD)		
Size	Document	Rev
C	8224	R00
Date	Wednesday, November 30, 2005 Sheet 26 of 41	

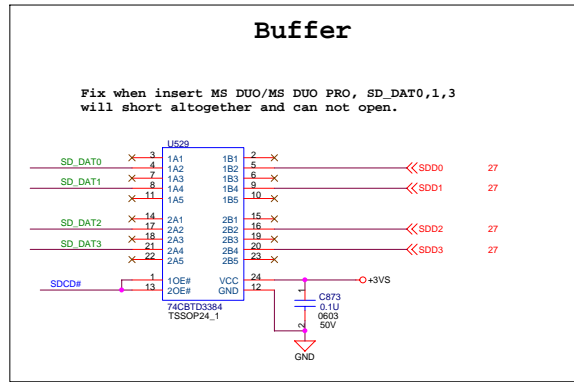
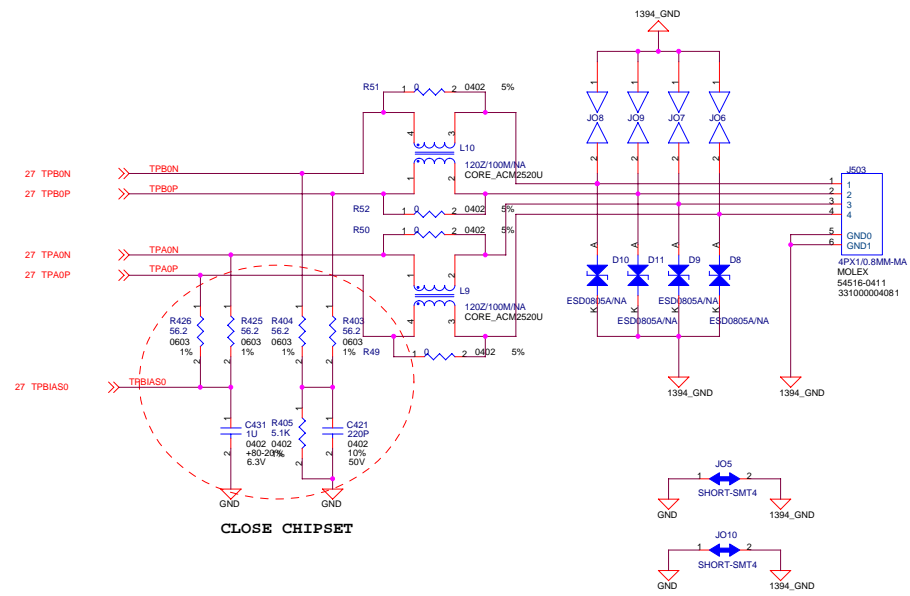
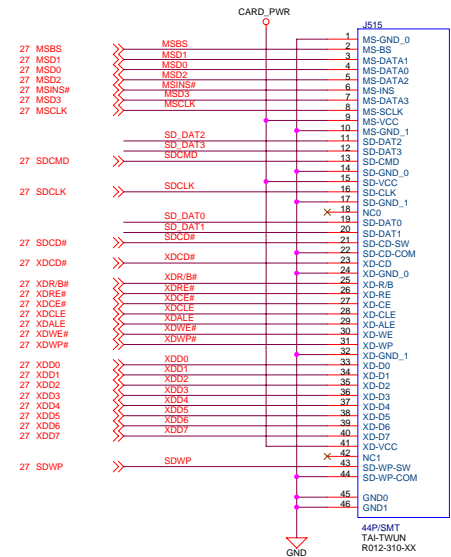
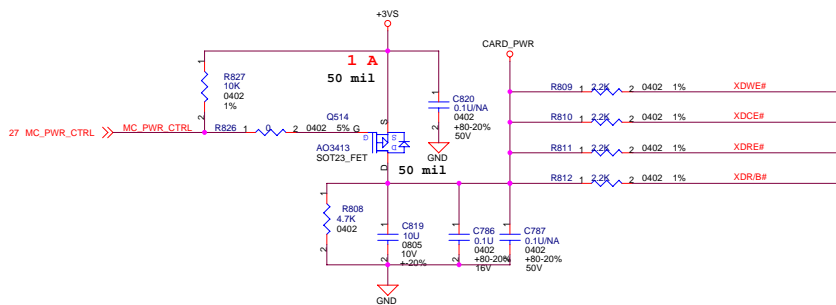
PCI8402
 IDSEL: AD21
 PCI REQ0#
 PCI GNT0#
 PCI INTA#

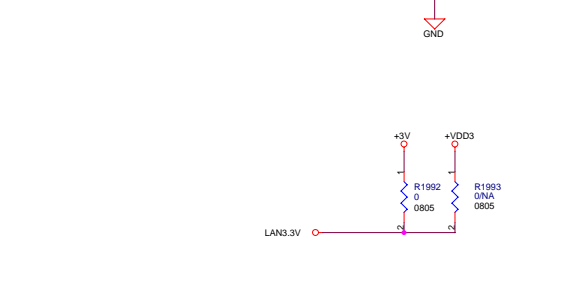
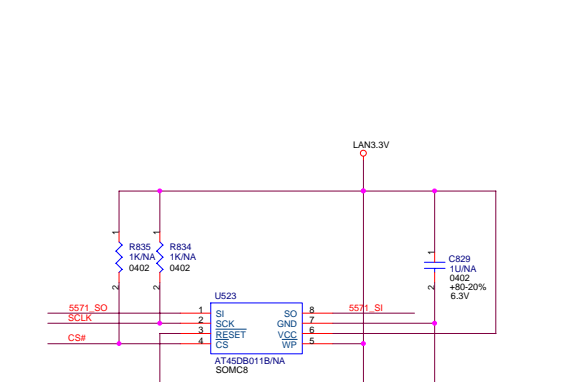
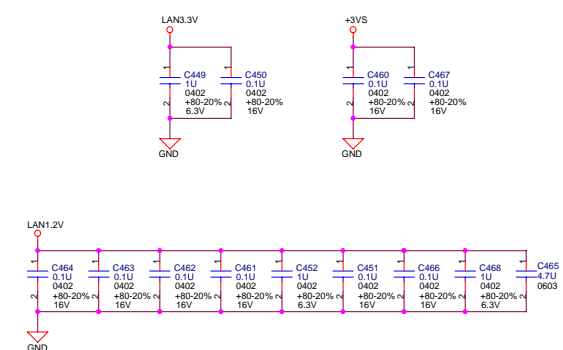
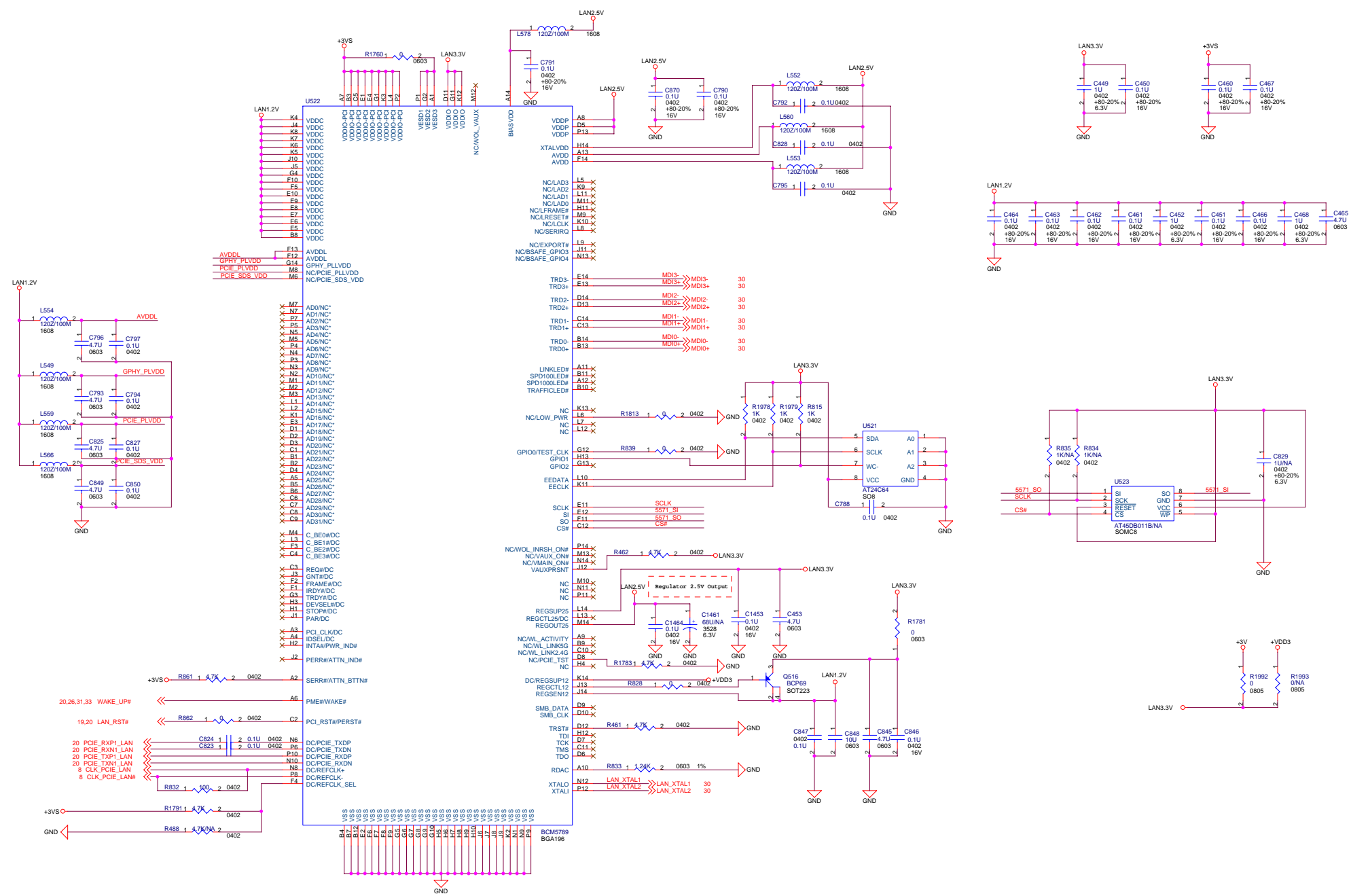


MITAC

File: CARDREADER AND IEEE1394(PCI8402)

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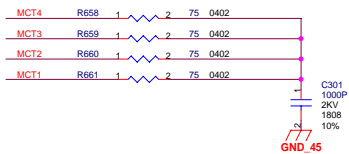
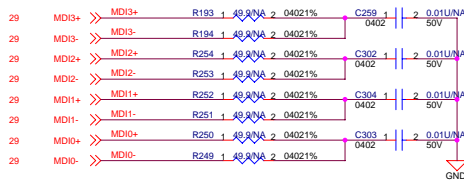
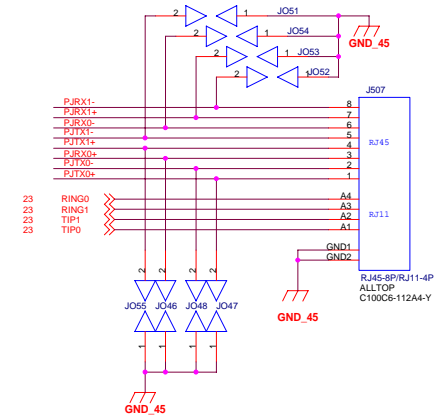
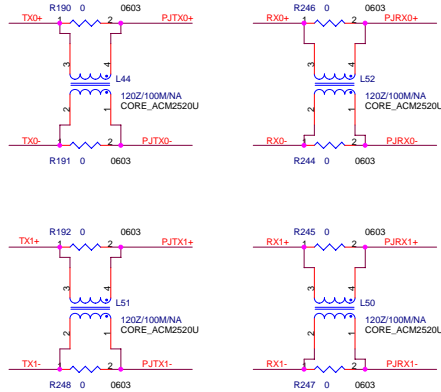
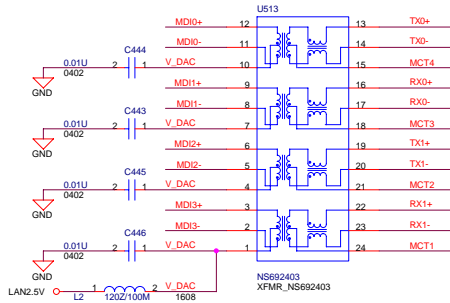


MITAC

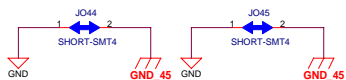
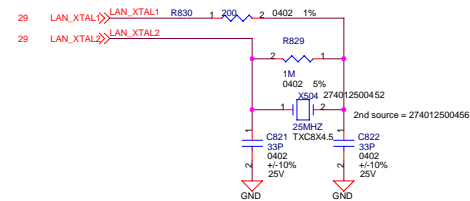
File: GIGA LAN(BCM5789)

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Please place these bead close to RJ45 connector

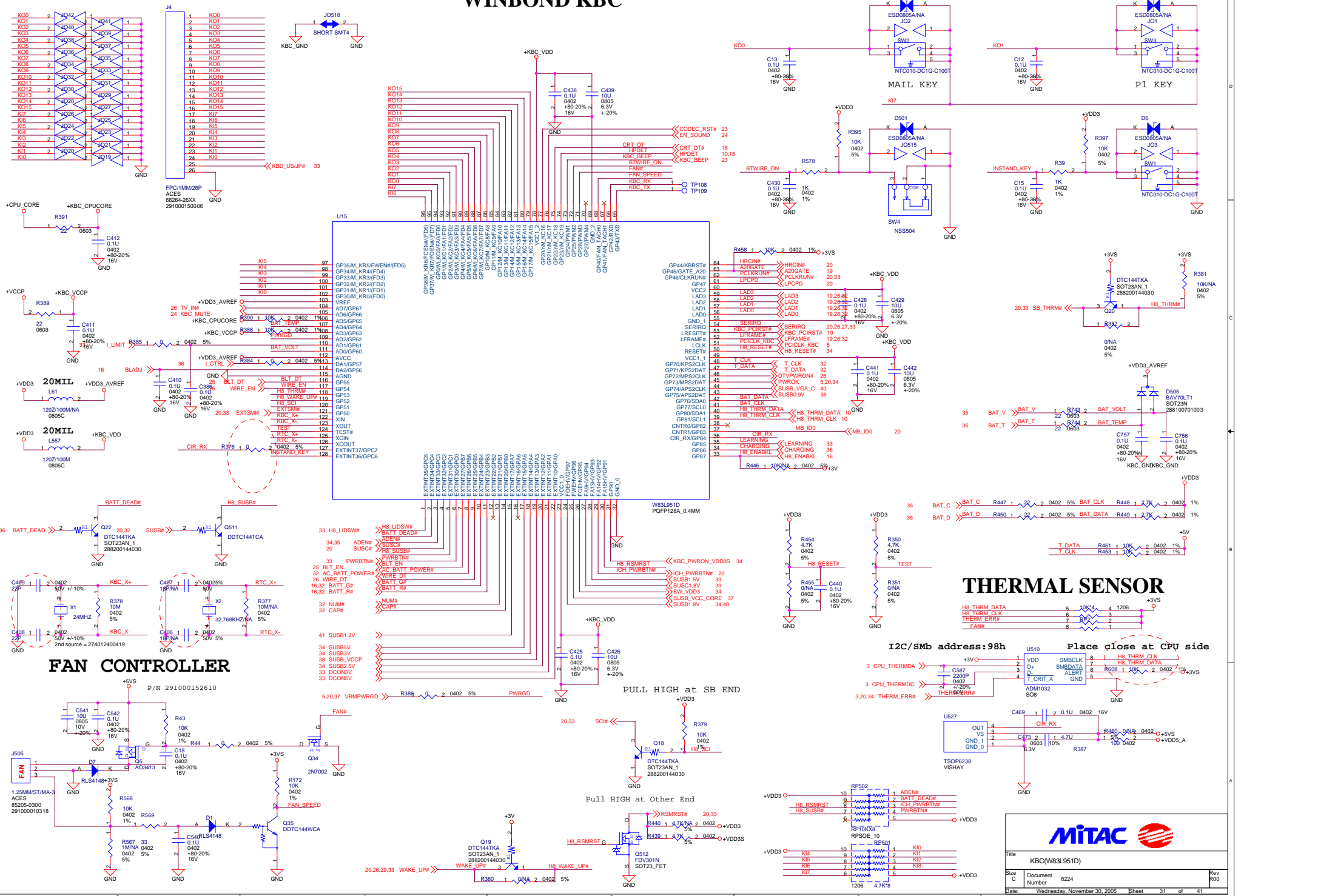


Crystal should be placed far away from I/O port and Tx, Rx, power, magnetics.



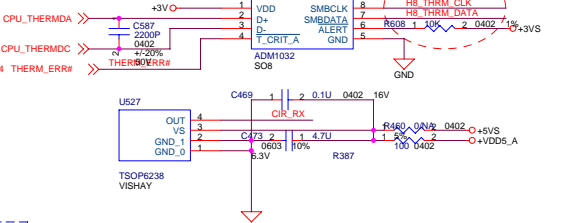
File		
LAN CONNECTOR		
Size	Document	Rev
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WINBOND KBC



THERMAL SENSOR

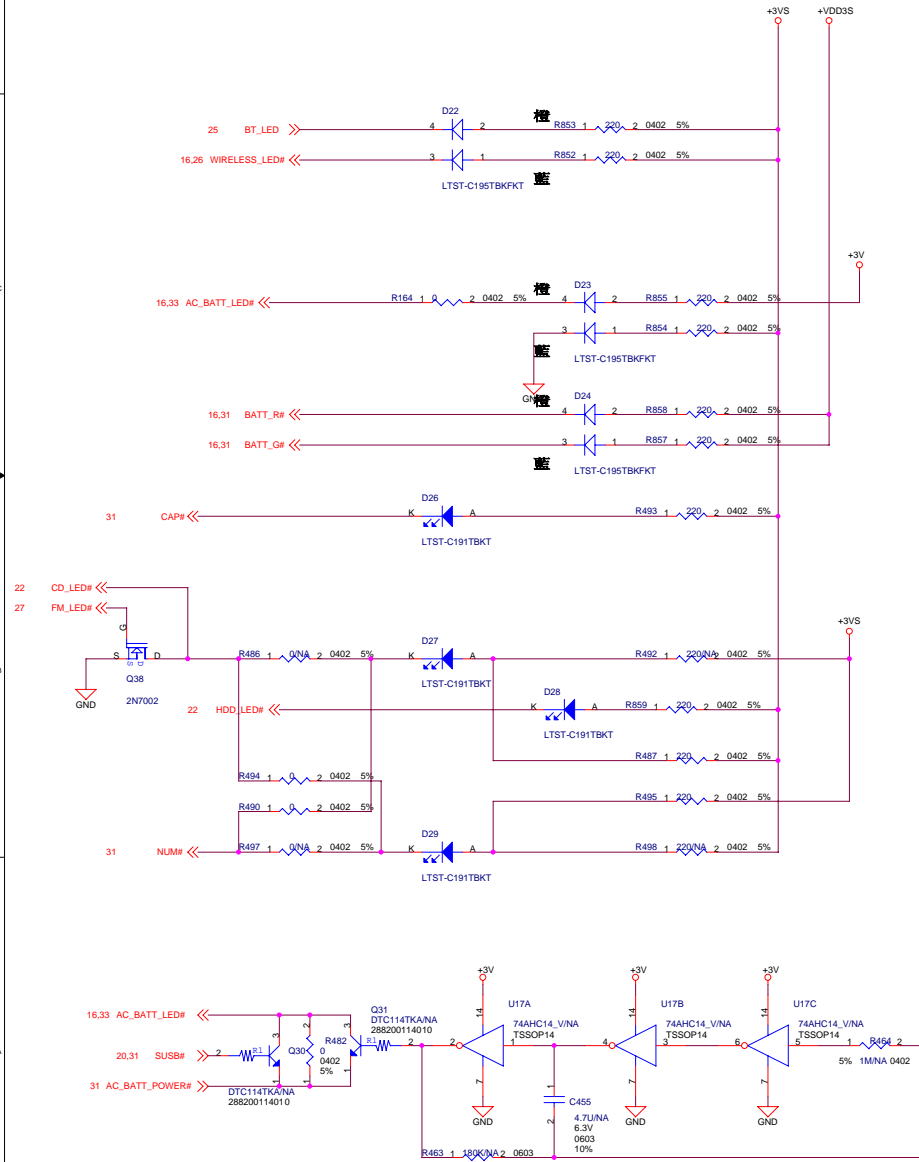
I2C/SMB address: 98h



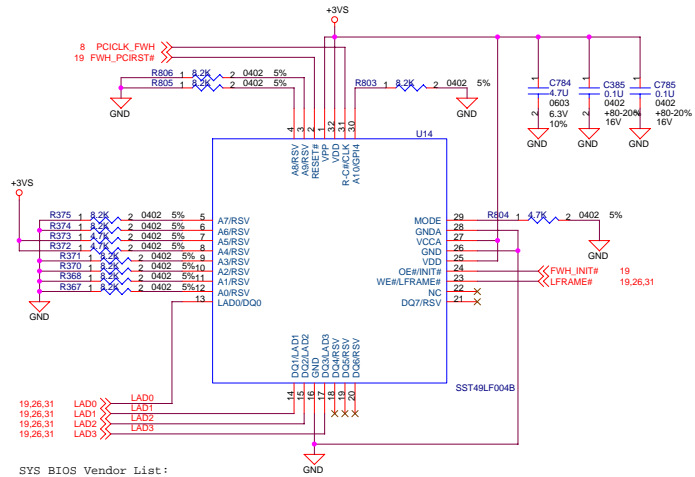
File		KBC(W83L951D)	
Size	Document	8224	
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- 1.WLAN + BT
- 2.AC+Battery
- 3.Charger
- 4.Caps Lock
- 5.MEMERY CARD IN
- 6.HDD + ODD
- 7.Num Lock

LED

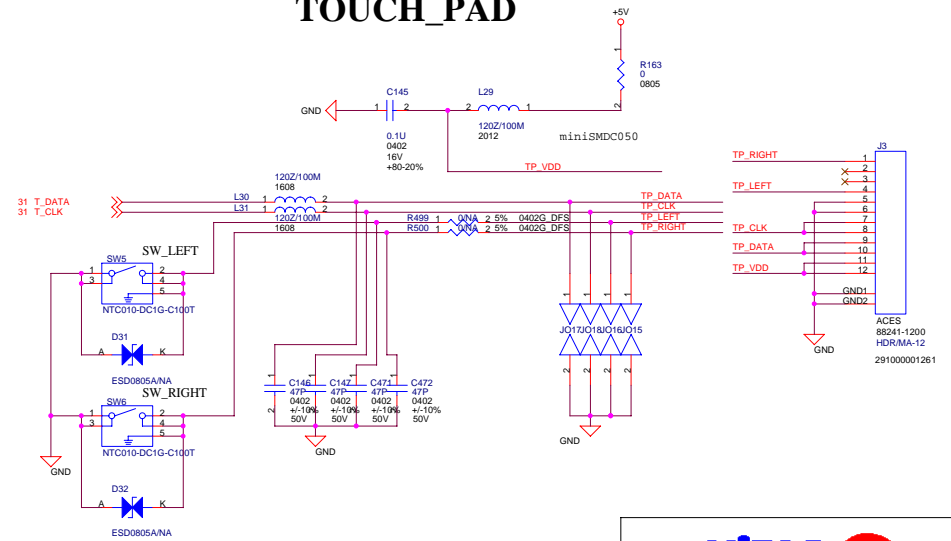


FWH



SYS BIOS Vendor List:
 S5T49LF004B : 283468470005
TF041-TH-IC;FLASH,512K*8,LPC & FWH,S5T49LF004B,PLCC32

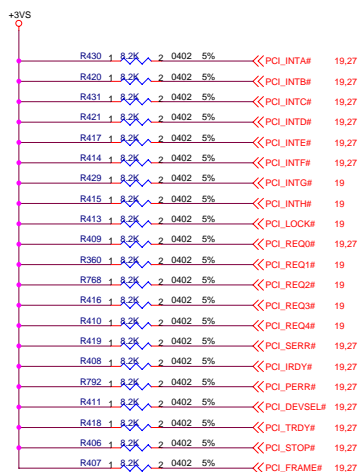
TOUCH_PAD



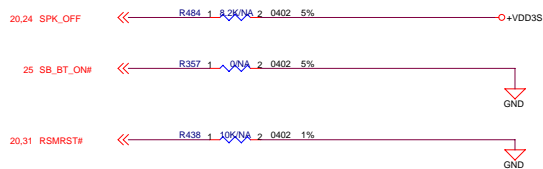
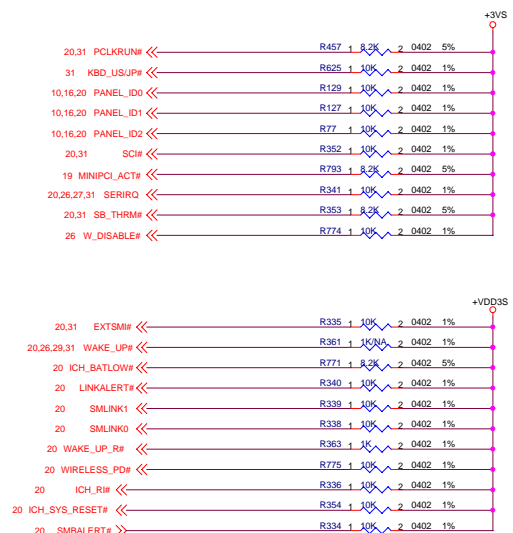
File: FWH/LED/TOUCH PAD		
Size: C	Document Number: 8224	Rev: R00
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PULL -HIGH

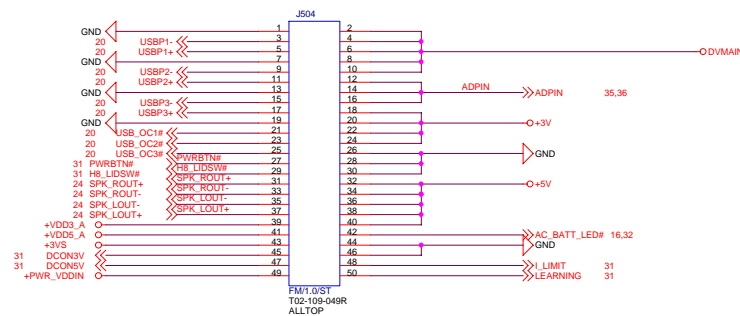
PCI PULL HIGH



GPIO PULL HIGH

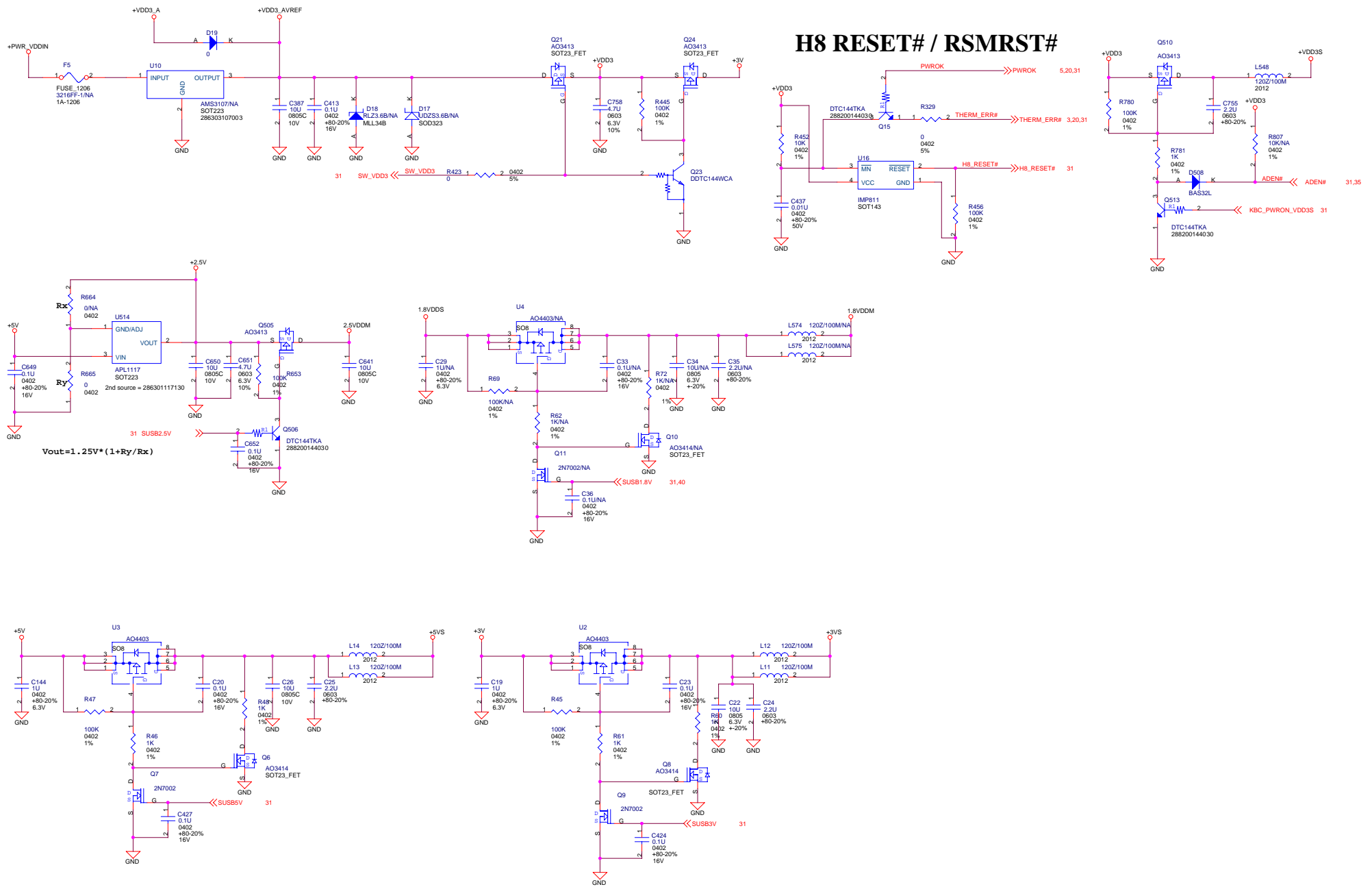


BOARD TO BOARD CNN



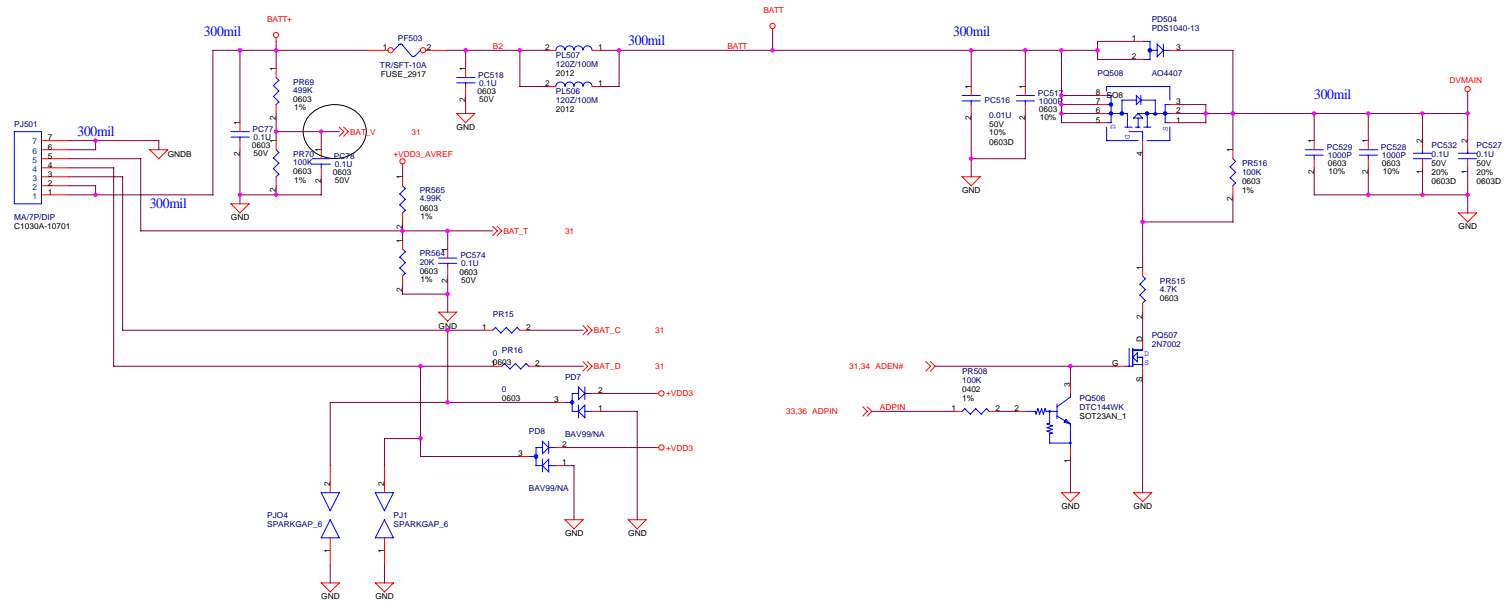
File PULL HI/DAUGHTER BOARD CONNECTOR		
Size C	Document Number 8224	Rev R00
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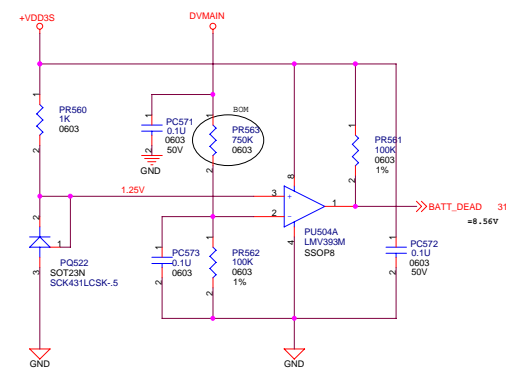
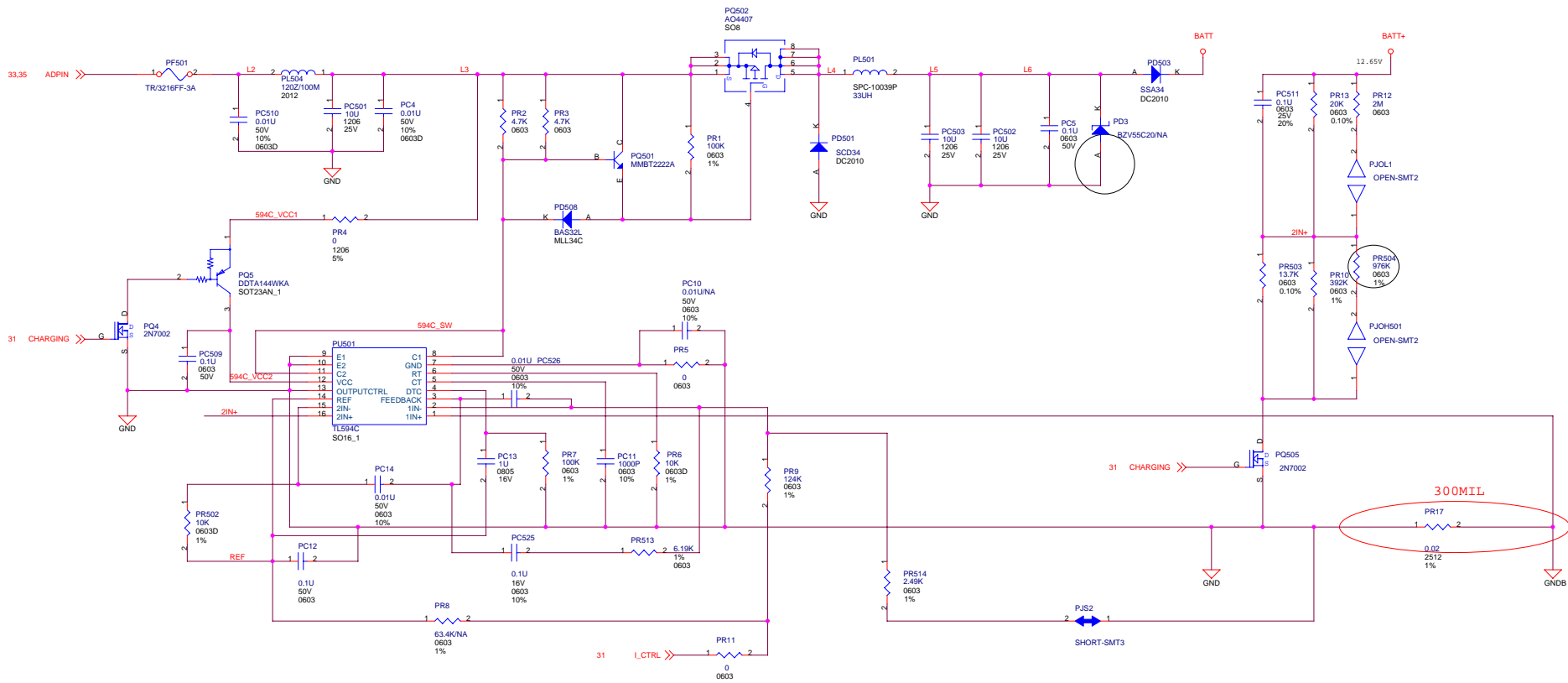
POWER ON PERIPHERAL CIRCUIT



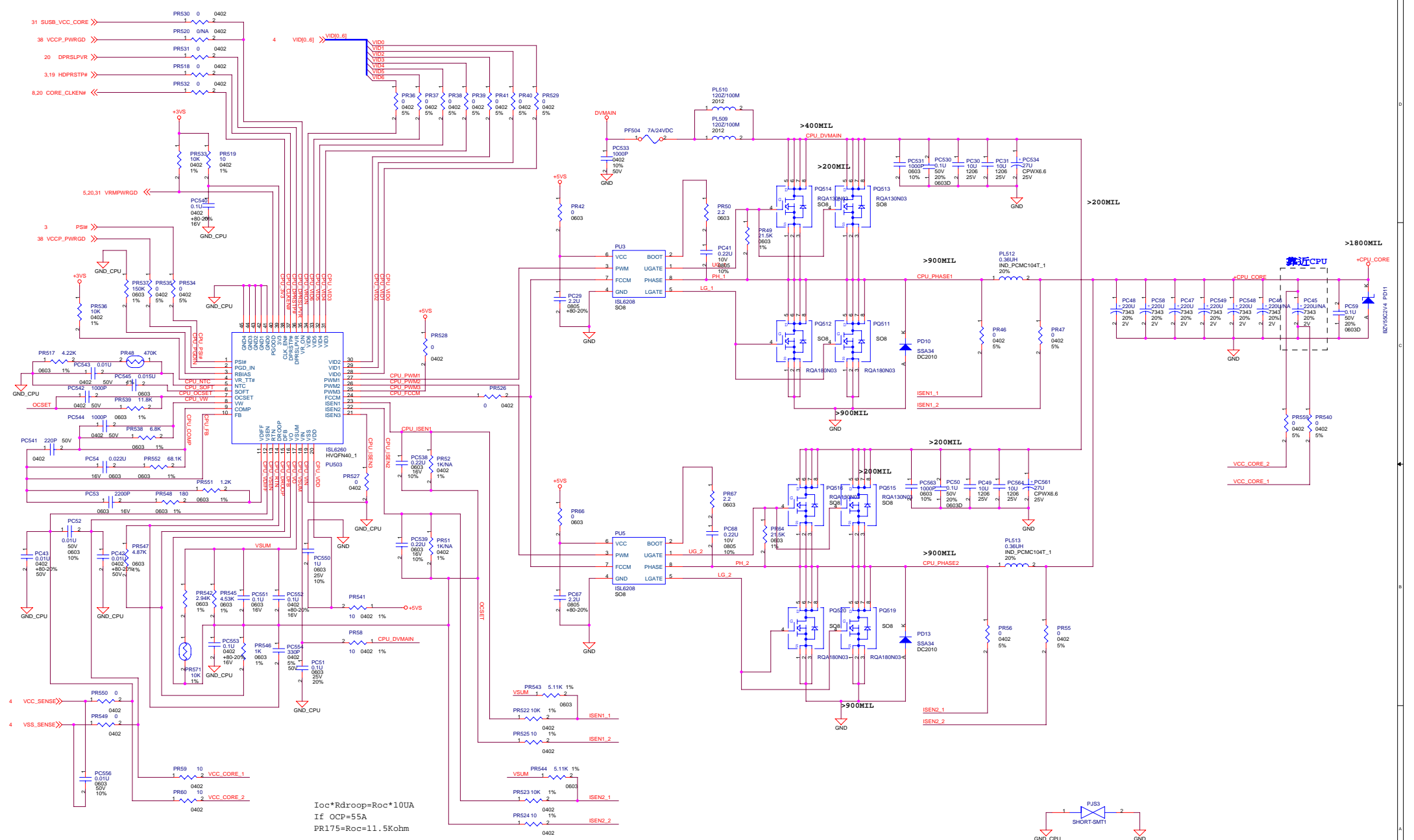
File			PERIPHERAL
Size	Document	Number	8224
C			
Date			Wednesday, November 30, 2005
Sheet		34	of 41
Rev			000

DISCHARGE

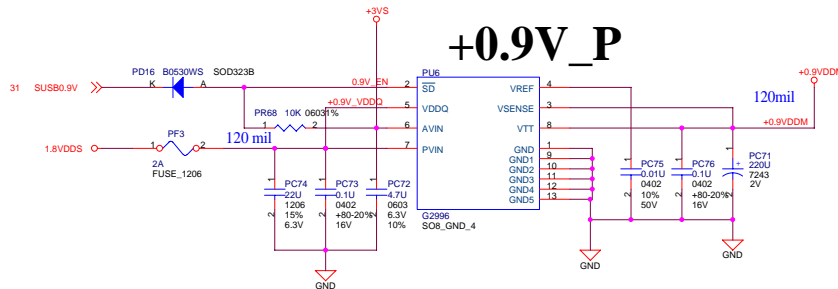
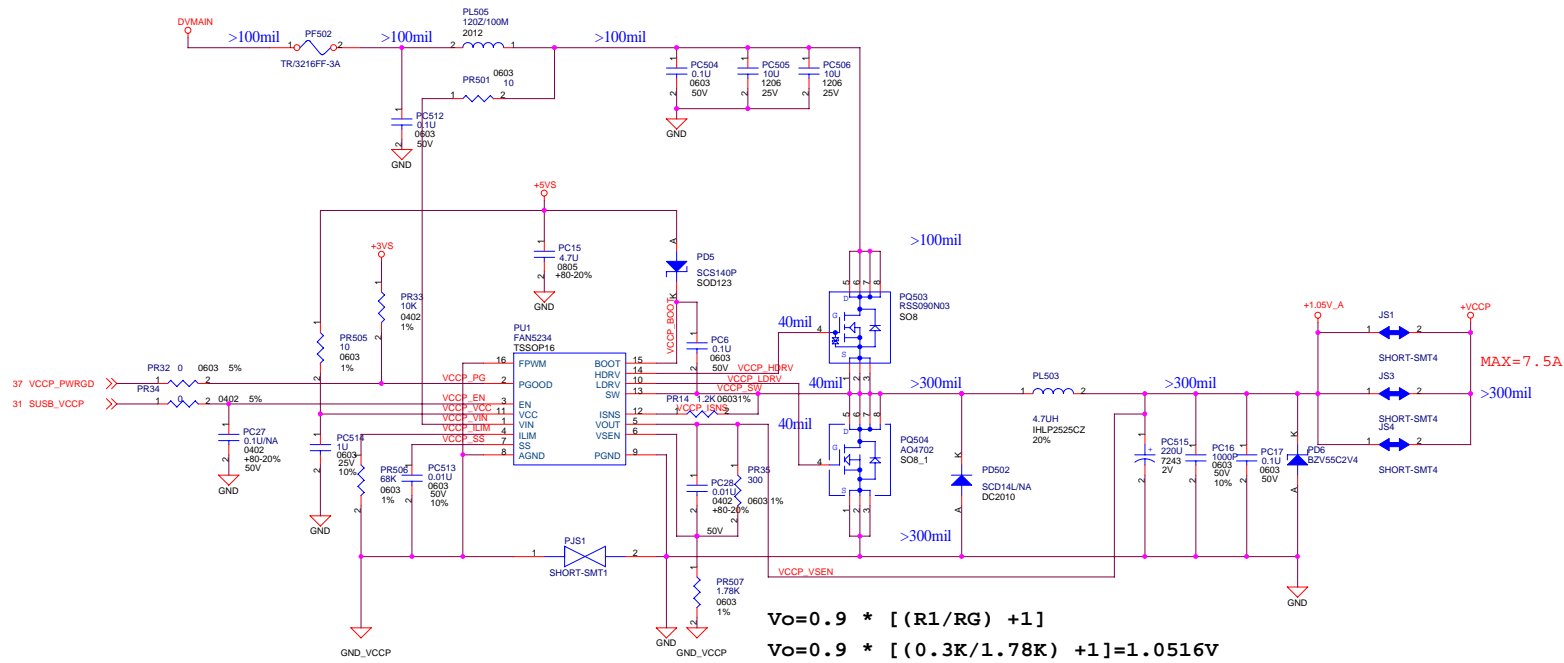




File CHARGER (TL594C)		
Size C	Document Number 8224	Rev R00
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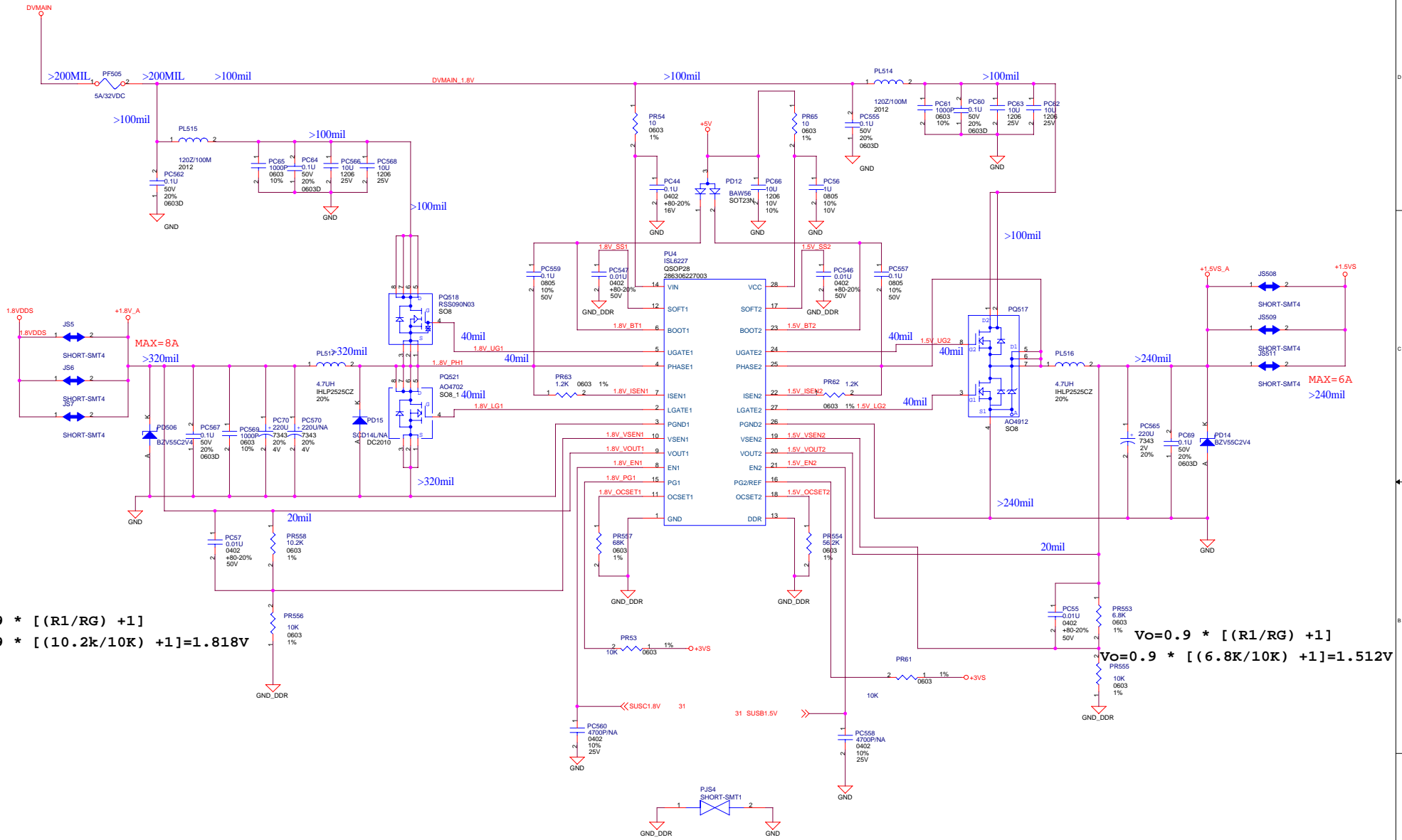


$I_{oc} * R_{droop} = R_{oc} * 10\mu A$
 If OCP = 55A
 $PR175 = R_{oc} = 11.5K\Omega$



File VCCP(FAN5234) / 0.9V(G2996)		
Size C	Document Number 8224	Rev R00
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+1.8V_P / +1.05V_P



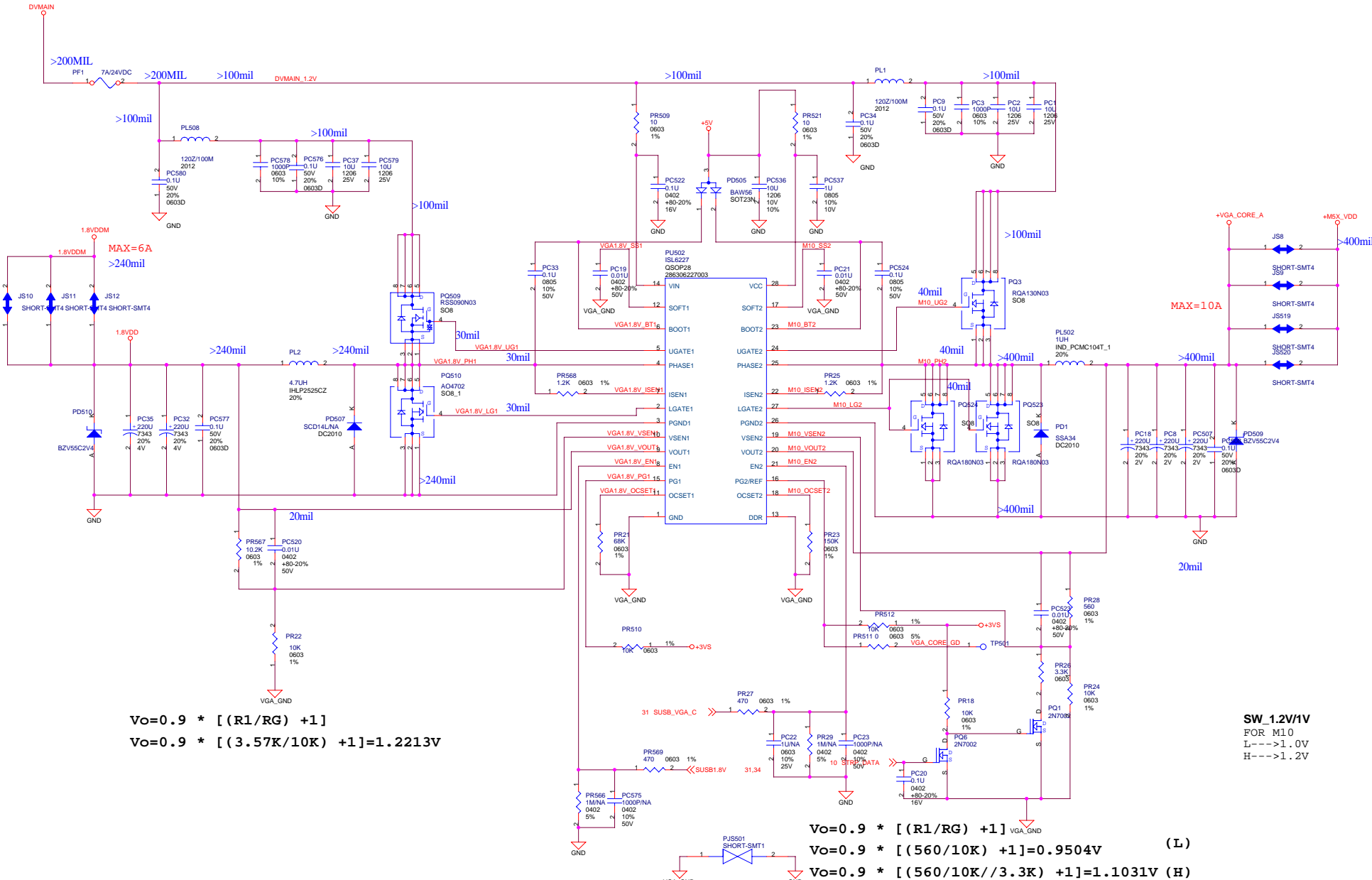
$V_o = 0.9 * [(R1/RG) + 1]$
 $V_o = 0.9 * [(10.2k/10K) + 1] = 1.818V$

$V_o = 0.9 * [(R1/RG) + 1]$
 $V_o = 0.9 * [(6.8K/10K) + 1] = 1.512V$



File: +1.8V/+1.5V(ISL6227)		
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VGA_CORE / +1.2V_P



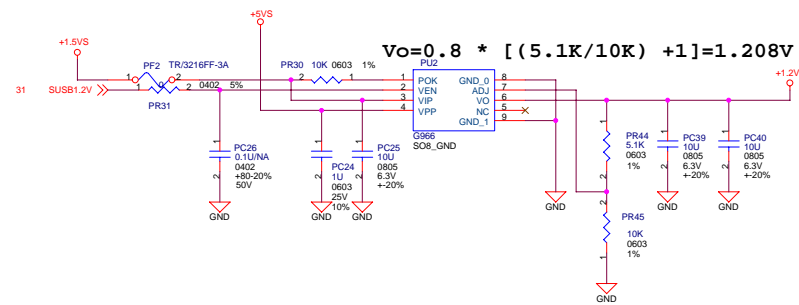
$V_o = 0.9 * [(R1/RG) + 1]$
 $V_o = 0.9 * [(3.57K/10K) + 1] = 1.2213V$

$V_o = 0.9 * [(R1/RG) + 1]$
 $V_o = 0.9 * [(560/10K) + 1] = 0.9504V \quad (L)$
 $V_o = 0.9 * [(560/10K / 3.3K) + 1] = 1.1031V \quad (H)$

SW_1.2V/1V
 FOR M10
 L ---> 1.0V
 H ---> 1.2V



File VGA_CORE (1.2V/1.0V) ISL6227		
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File		
VGA(1.8V) FANS234		
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Date: Wednesday, November 30, 2011 11:41 AM Page 41 of 47		

8224 Daughter Board R00

PROJECT CODE- GXXX
PRODUCT CODE- XXXX

PCB P/N:XXXXXXXXXXXX
ASSY P/N:XXXXXXXXXXXX

PAGE 1 TITLE
PAGE 2 CONNECTER
PAGE 3 USB CONN
PAGE 4 +3VS/+5VS(ISL6232)

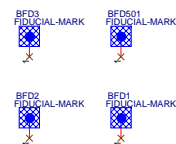
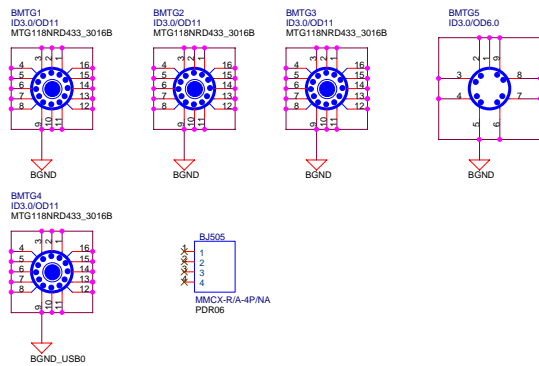
REVISION	TAPEOUT DAY	HISTORY
R00	2004/09/13	Initial Release.
R0A		
R01		


PCB STACK 1.2mm

4 mil	Component side	Layer 1: 1/2 oz
5 mil	Ground 1	Layer 2: 1 oz
21 mil	Signal layer(IN1)	Layer 3: 1 oz
5 mil	Signal layer(IN2)	Layer 4: 1 oz
4 mil	Power layer	Layer 5: 1 oz
	Solder side	Layer 6: 1/2 oz

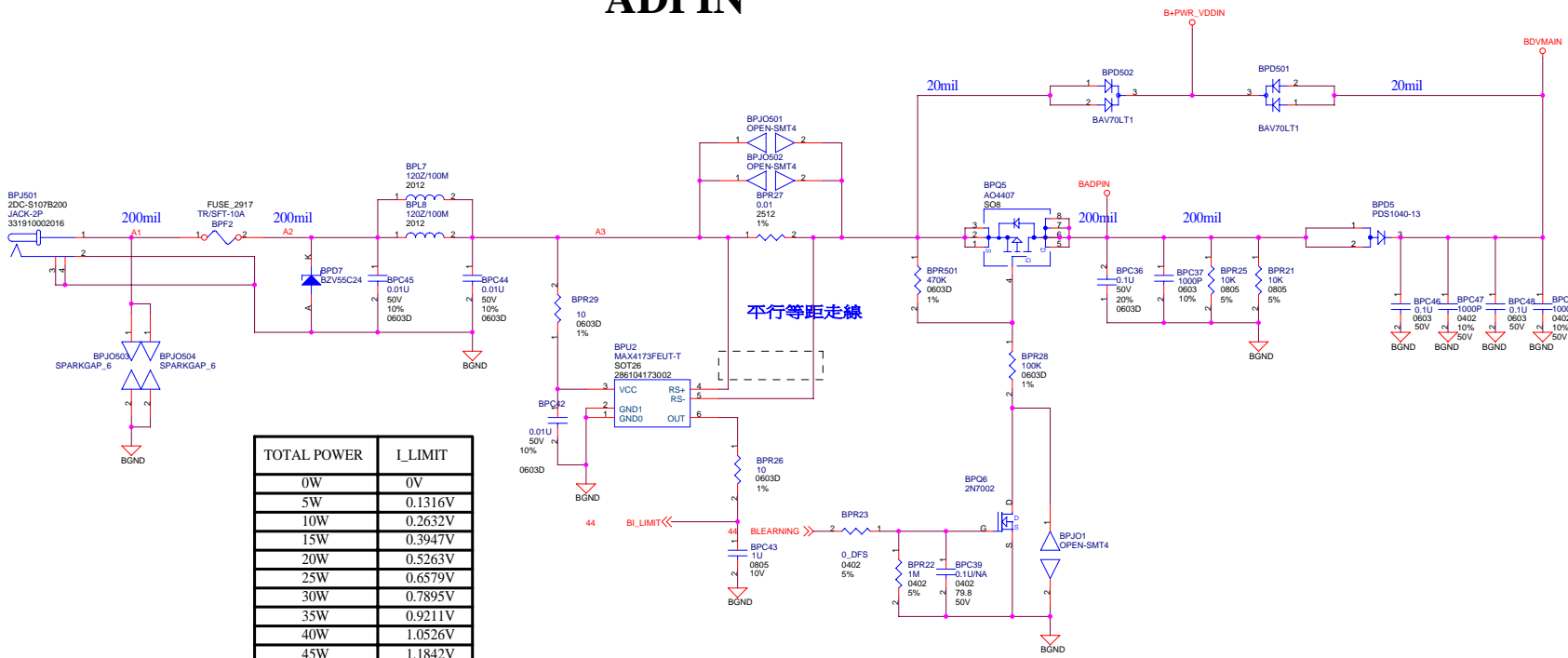
Differential Pair :

USB -->6/6 Z(diff) = 90 ohm



DRAWN	DESIGN	CHECK	ISSUES			
				File DAUGHTER BOARD TITTLE		
				Size C	Document Number 8224	Rev R00
				Date: Wednesday, November 30, 2005	Sheet 42 of 47	

ADPIN

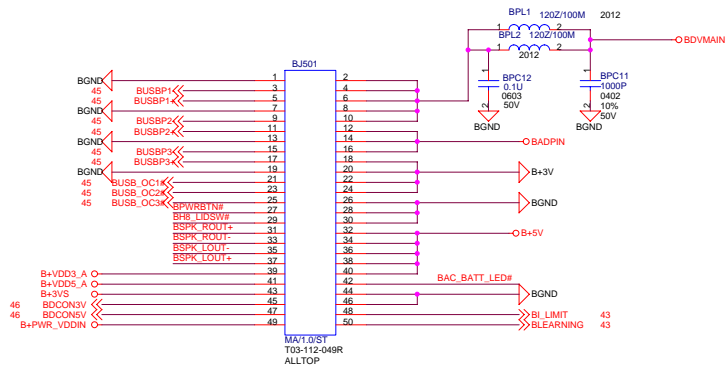


TOTAL POWER	I_LIMIT
0W	0V
5W	0.1316V
10W	0.2632V
15W	0.3947V
20W	0.5263V
25W	0.6579V
30W	0.7895V
35W	0.9211V
40W	1.0526V
45W	1.1842V
50W	1.3158V
55W	1.4474V
60W	1.5789V
65W	1.7105V
70W	1.8421V
75W	1.9737V
80W	2.1052V
85W	2.2368V
90W	2.3684V



File ADAPTOR/ VMAIN		
Size C	Document Number 8224	Rev R00
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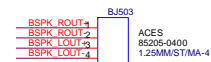
BOARD TO BOARD CNN



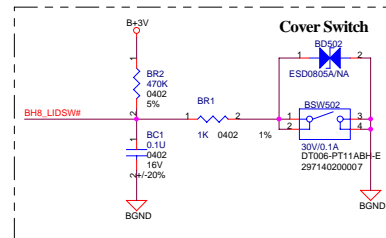
DVMAIN	6 PIN
+5V	6 PIN
+3V	4 PIN
+PWR_VDDIN	1 PIN
+VDD3_A	1 PIN
+VDD5_A	1 PIN
GND	12 PIN

PWR : GND=19 : 12

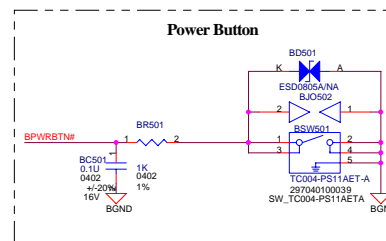
SPEAKER



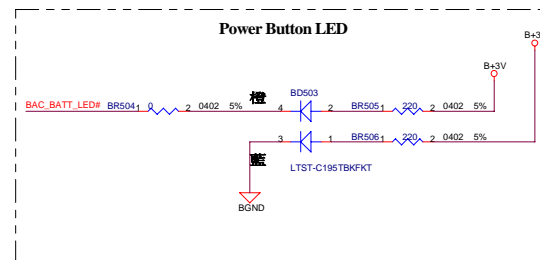
Cover Switch



Power Button

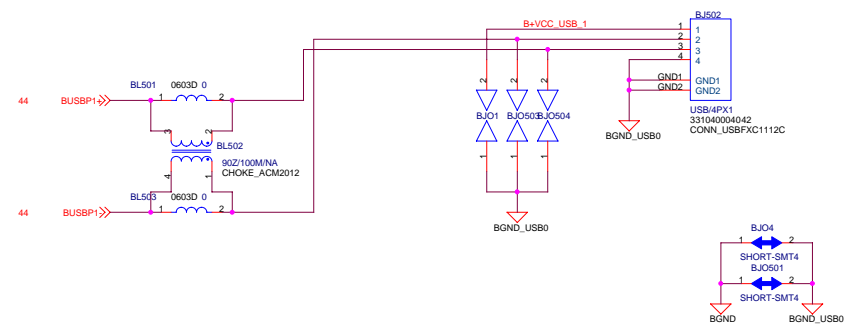
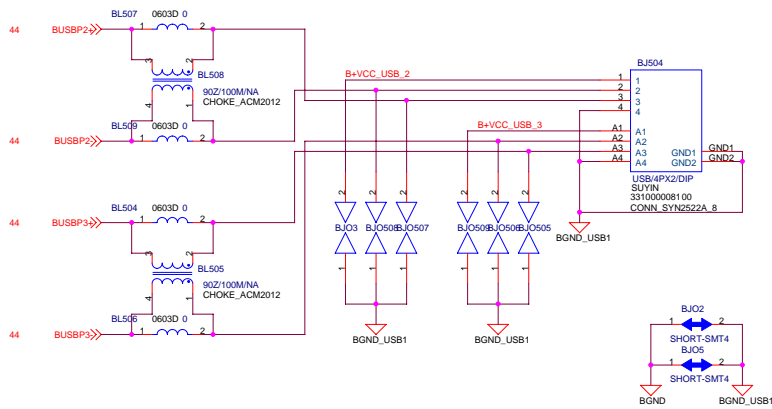
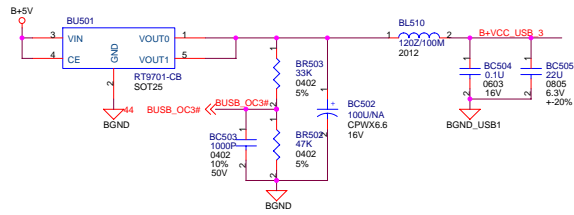
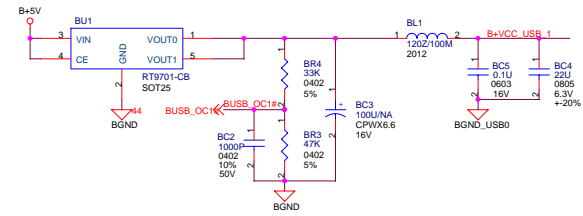
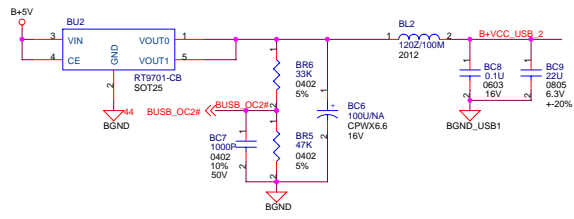


Power Button LED

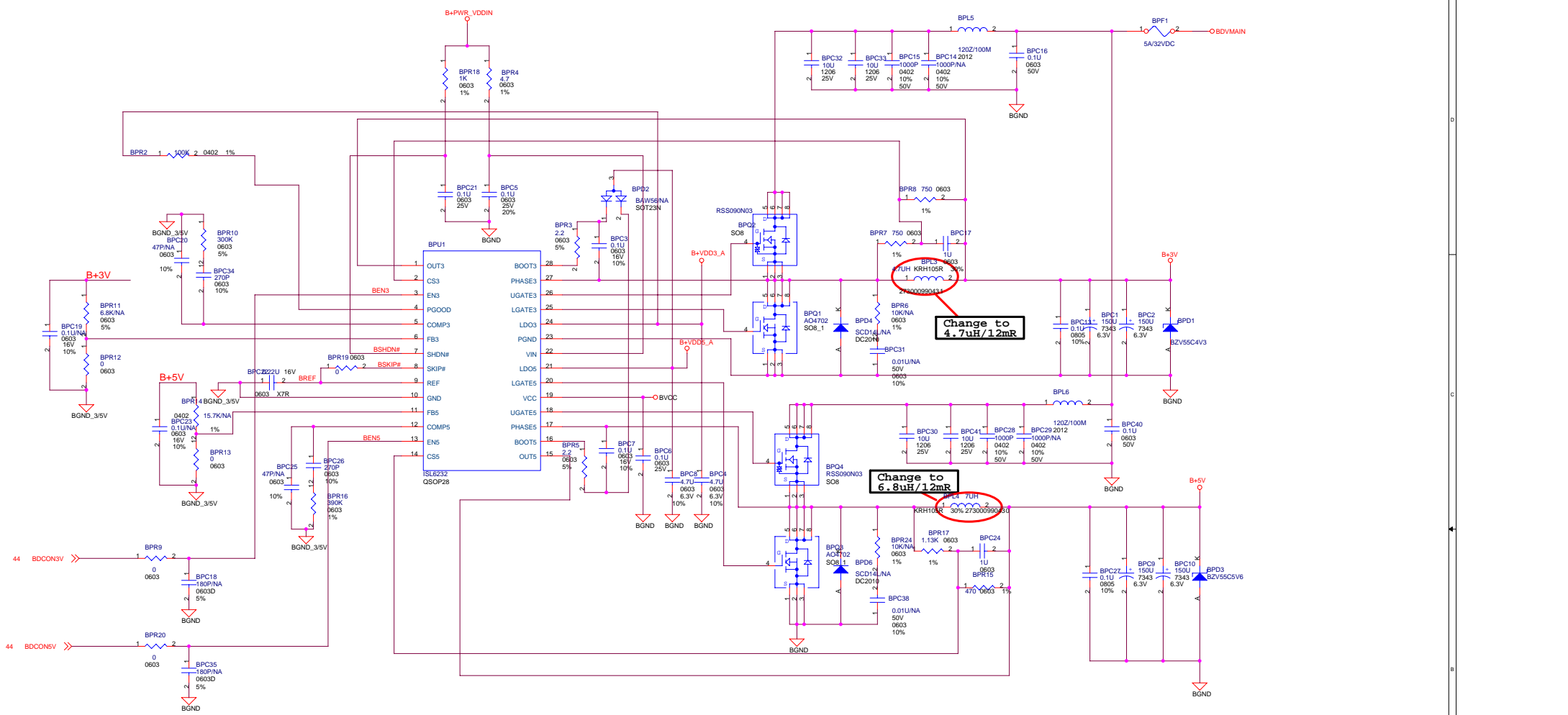


File		
DAUGHTER CONNECTOR		
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USB CONNECTOR



File		
DAUGHTER BOARD USB CONNECTOR		
Size	Document	Rev
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SKIP#	Operate Mode
VCC	PWM
REF	Ultrasonic
GND	Pluse Skip

SHDN#	EN3	EN5	LDO3	LDO5	3.3V Buck	5V Buck
LOW	X	X	OFF	OFF	OFF	OFF
High	LOW	LOW	ON	ON	OFF	OFF
High	LOW	High	ON	ON	OFF	ON
High	High	LOW	ON	ON	ON	OFF
High	High	High	ON	ON	ON	ON
High	High	REF	ON	ON	ON	ON after 3.3V up
High	REF	High	ON	ON	ON after 3.3V up	ON

MITAC

File: +3VS/+5VS(ISL6232)

Size C	Document Number 8224	Rev R00
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R00

- 1.Modify CLK differential signal from 33 ohm to 22 ohm
- 2.Modify R637 from 100 ohm to 470 ohm .ATI M56p clk must be under 1.2V
- 3.DNS VRAM pull hi resistor with over 350MHZ R271 ,R272 ,R275 ,R264 ,R266 ,R273 ,R267 ,R268 ,R262 ,R265 ,R276 ,R274 ,R277 ,R270 ,R269 ,R280 ,R260 ,R279 ,R263 ,R278 ,R259 ,R282 ,R257 ,R281 ,R258 ,R283 ,R261 ,R286 ,R284 ,C306 ,R151 ,R103 ,R102 ,R109 ,R117 ,R108 ,R105 ,R106 ,R112 ,R110 ,R101 ,R107 ,R104 ,R114 ,R111 ,R149 ,R113 ,R147 ,R118 ,R145 ,R116 ,R148 ,R120 ,R144 ,R115 ,R150 ,R119 ,R143 ,R146 ,C114.
- 4.Add panel EDID pin on connector J1
- 5.Add CRT detect pin pull hi
- 6.Add TI card reade IRQ#,prevent all device use the same IRQ#
- 7.Add 2 buffer 2n7002 with ICH_PTN# and EXTSMI# prevent KBC power lose.
- 7.Add 2 buffer 2n7002 with ICH_PTN# and EXTSMI# prevent KBC power lose.



File		<Title>
Size	Document	Rev
C	Number	ROA
Date	Wednesday, November 30, 2005 Sheet 47 of 47	