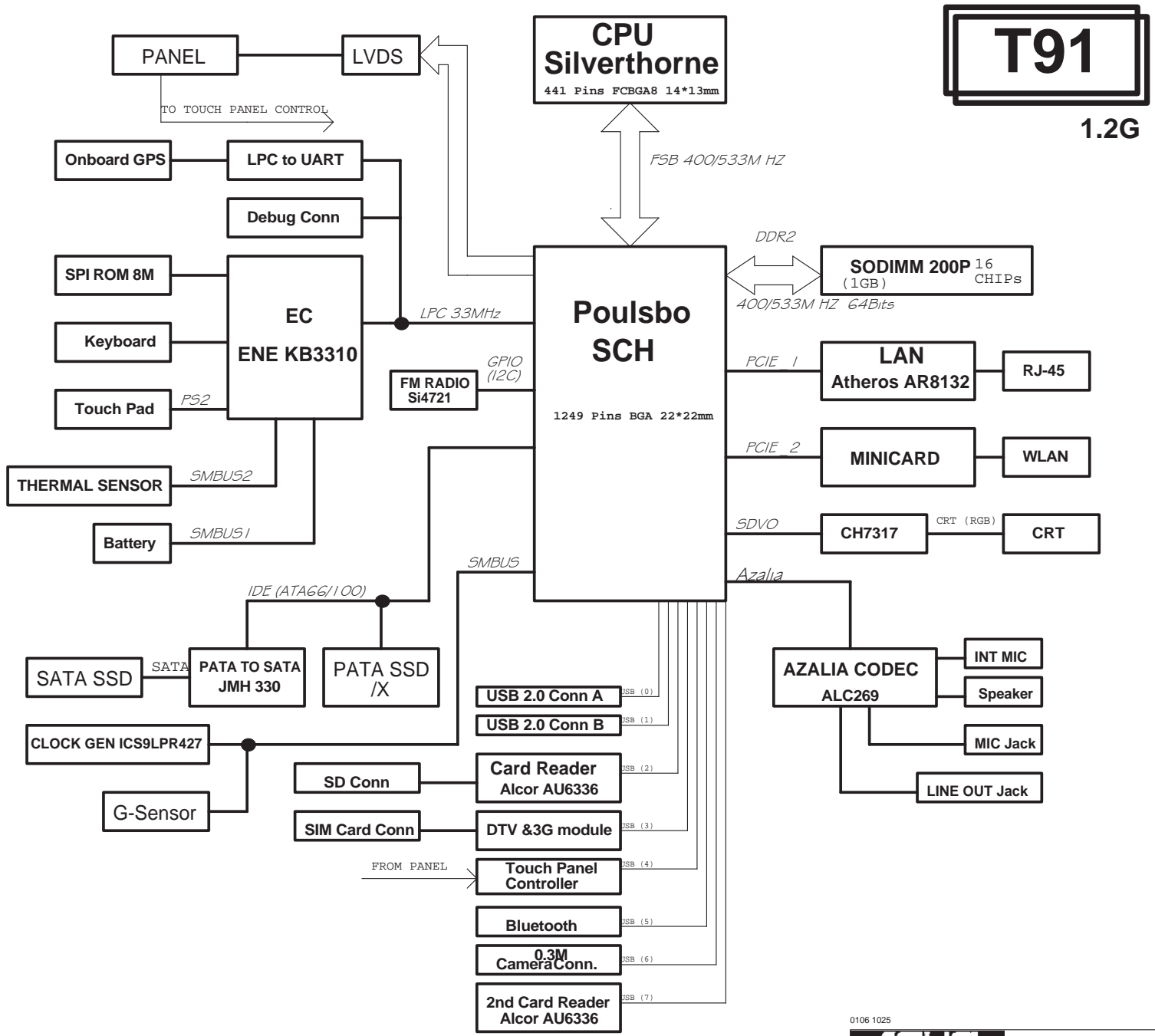



- 01\_BLOCK DIAGRAM
- 02\_SCH GPIO Setting
- 03\_EC Pin Define
- 04\_Power Sequrnse DC
- 05\_Power Sequence AC
- 06\_Power Sequence Description
- 07\_Clock Gen\_ICS9LPR427
- 08\_CPU-SILVERTHORNE (1)
- 09\_CPU-SILVERTHORNE (2)
- 10\_CPU-SILVERTHORNE (3)
- 11\_SCH Poulsbo\_HOST (1)
- 12\_SCH Poulsbo\_DDR2 (2)
- 13\_SCH Poulsbo\_LVDS/SDVO (3)
- 14\_SCH Poulsbo\_PM/USB/IDE/AZ (4)
- 15\_SCH Poulsbo\_STRAP(5)
- 16\_SCH Poulsbo\_POWER (6)
- 17\_SCH Poulsbo\_GND (7)
- 18\_DDR2\_SODIMM
- 19\_DDR2\_Termination
- 20\_CH7317\_SDVO\_CRT
- 21\_Onboard VGA
- 22\_LCD Conn\_LID
- 23\_PCIEx 3.5G & Ext. Antenna
- 24\_Mini WIFI / BT
- 25\_Bluetooth\_BT253
- 26\_FM\_RADIO\_Si4721
- 27\_Onboard GPS
- 28\_LAN\_Atheros AR8113/AR8132
- 29\_RJ45
- 30\_Flash Conn
- 31\_PATA\_TO\_SATA
- 32\_USB Port
- 33\_Card Reader\_AU6336C52
- 34\_Camera Conn
- 35\_Codec\_ALC269
- 36\_Audio Amp Jack
- 37\_EC\_ENE KB3310
- 38\_EC\_UART Contoller
- 39\_SPI ROM\_Debug Conn
- 40\_Reset Map
- 41\_KB\_Touch Pad
- 42\_Thermal Sensor
- 43\_Small\_Board\_Conn
- 44\_G-Sensor
- 45\_Discharge
- 46\_PWR Jack
- 47\_SCREW HOLE
- 48\_EMI
- 49\_Power Flow
- 50\_Vcore
- 51\_Power System
- 52\_Power\_+1.8V & VTDDR
- 53\_Power\_VCCP
- 54\_Power\_+1.5VS & +2.5VS
- 55\_Power\_Charger
- 56\_Power\_Load Switch
- 57\_Power Latch



**SCH GPIO SETTING**

Pin	Pin Name	Connect to	Type	Power Well	S3	S4/ S5	Input/Output Set
U41	GPIO0	PM_LEVELDOWN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N43	GPIO1	CPU_LEVELDOWN	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
N45	GPIO2	PM_PWRBTN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
R41	GPIO3/ USBCC	Test Point	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
G29	GPIO4	Strap CMC/ BT_Disable	I/O CMOS3.3	Core	OFF	OFF	Input
K30	GPIO5	PCB ID	I/O CMOS3.3	Core	OFF	OFF	Input
F34	GPIO6	GPS_EN	I/O CMOS3.3	Core	OFF	OFF	Output
G33	GPIO7	Strap CMC	I/O CMOS3.3	Core	OFF	OFF	Input
K36	GPIO8	3GLAN_OFF	I/O CMOS3.3	Core	OFF	OFF	Output
H36	GPIO9	MINICARD_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F36	GPIO10	DDR_MEM_CONFIG	I/O CMOS3.3	Core	OFF	OFF	Input
J31	GPIO11/SLPIOVR#	SLPIOVR#	I/O CMOS3.3	Core	OFF	OFF	Output
H34	GPIO12/PROCHOT#	CAMERA_EN	I/O CMOS3.3/ OD	Core	OFF	OFF	Output
K28	GPIO13/EXTTS1#	WLAN_LED	I/O CMOS3.3	Core	OFF	OFF	Output

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		<b>Title : SCH GPIO Setting</b>	
ASUSTek Computer INC.		<b>Engineer: Jerry Liu</b>	
Size	Project Name		Rev
A3	<b>T91</b>		1.2G
Date: Tuesday, January 06, 2009		Sheet	2 of 57

## EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO0/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO4	HOTKEY_SW0#	I	Internal pull high
13	GPIO05/PCIRST#	HOT_RST#	I	
14	GPIO07	BUF_KEY_SW1#	I	Battery over temperature
15	GPIO08	EXT_SM#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	Reserved for GPIO extender
18	GPIO0C/ESB_DAT	NC	O	Reserved for GPIO extender
19	GPIO0D	LID_EC_R#	I	Internal pull high
20	GPIO0E/SC#	KBC_SC#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL#	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN1_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN0_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	PS-ON	O	latch power
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	LPC_CLKRUN#	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_A	I	
64	GPI39/AD1	BAT_B	I	
65	GPIO3A/AD2	BAT_C	I	
66	GPIO3B/AD3	BAT_D	I	
68	GPO3C/DA0	CHG_EN#	O	battery charger enabled

<http://hobi-elektronika.net>

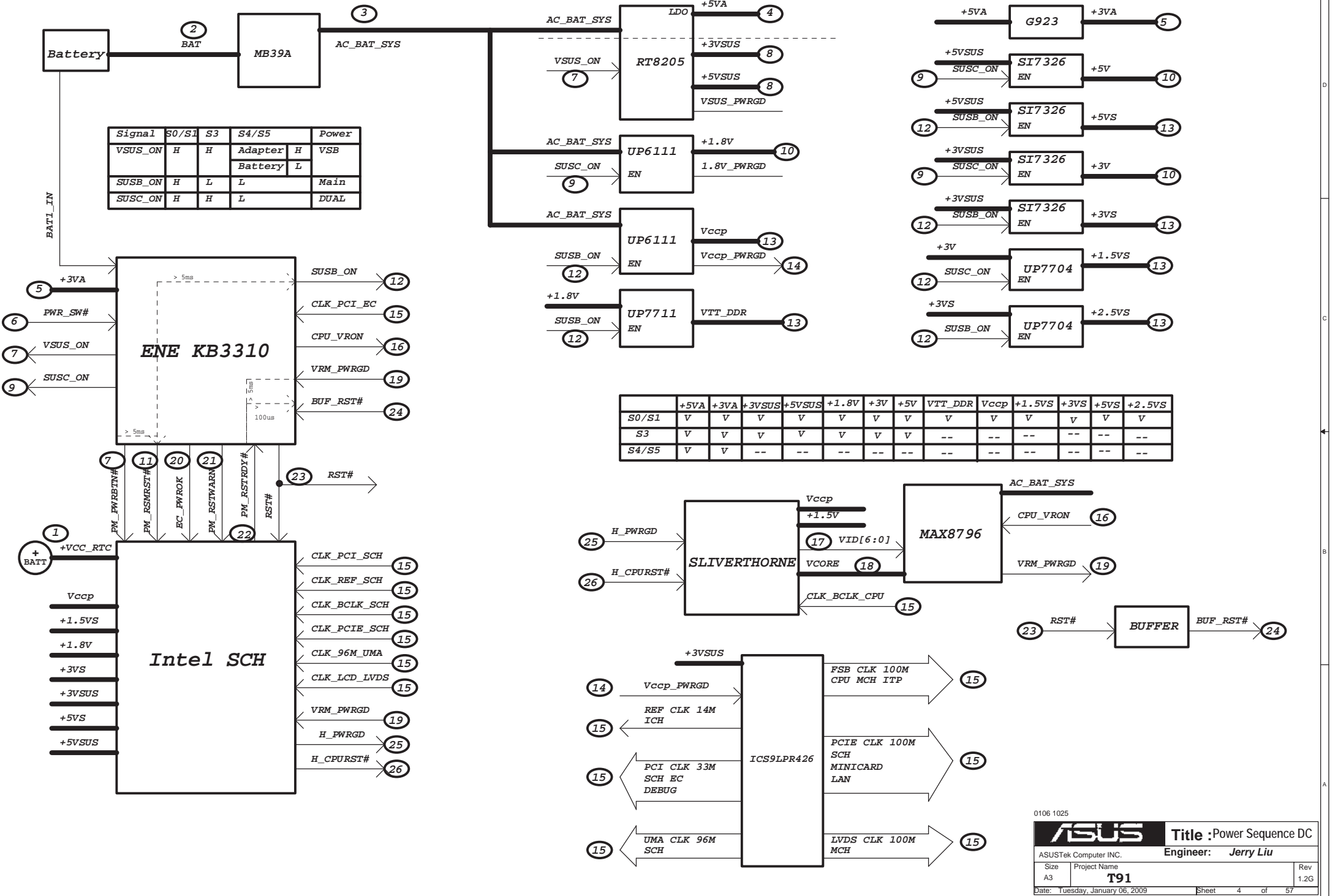
Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	THRO_CPU_VOLT#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	Batt1 (Small/Internal): 1-present, 0-absent
76	GPI43	BAT2_IN	I	Batt2 (Small/Internal): 1-present, 0-absent
77	GPIO44/SCL1	SMB0_CLK	I/O	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/O	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/O	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/O	10K pull high to +3V
81	GPIO48/KSO16	KB_ID0	I	for KB type detection
82	GPIO49/KSO17	KB_ID1	I	for KB type detection
83	GPIO4A/PSCLK1	N.C.	O	
84	GPIO4B/PSDAT1	N.C.	O	
85	GPIO4C/PSCLK2	N.C.	O	
86	GPIO4D/PSDAT2	GS2_INT2	O	
87	GPIO4E/PSCLK3	TP_CLK	I/O	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/O	10K pull high to +3V
89	GPIO50/SELIO#	CHG_LED_GREEN#	O	Green charger LED
90	GPIO52/E51_CS#	CHG_LED_UP#	O	Orange charger LED
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRLED_LED#	O	
95	GPIO56	GS1_INT1	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	CNT1_CHG#	O	batt1 (Big/External) charging enabled. Batt1 is discharging priority in AC mode.
103	GPXOA06	CNT1_DIS#	O	batt1 discharging enabled
104	GPXOA07	CNT2_CHG#	O	batt2 (Small/Internal) charging enabled. Batt2 is charging priority in AC mode.
105	GPXOA08	CNT2_DIS#	O	batt2 discharging enabled
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	PM_PWROK	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	RST#	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	PM_SLPRDY#	I	SLPRDY#, 100K pull down to GND
115	GPXID4	SLPMODE	I	SUSC#, 100K pull down to GND
116	GPXID5	VRM_PWRGD	I	Pull high to +3V
117	GPXID6	PM_RSTRDY#	I	
118	GPXID7	RSTWARN	O	
121	GPIO57	GS1_INT2	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	GS2_INT1	O	

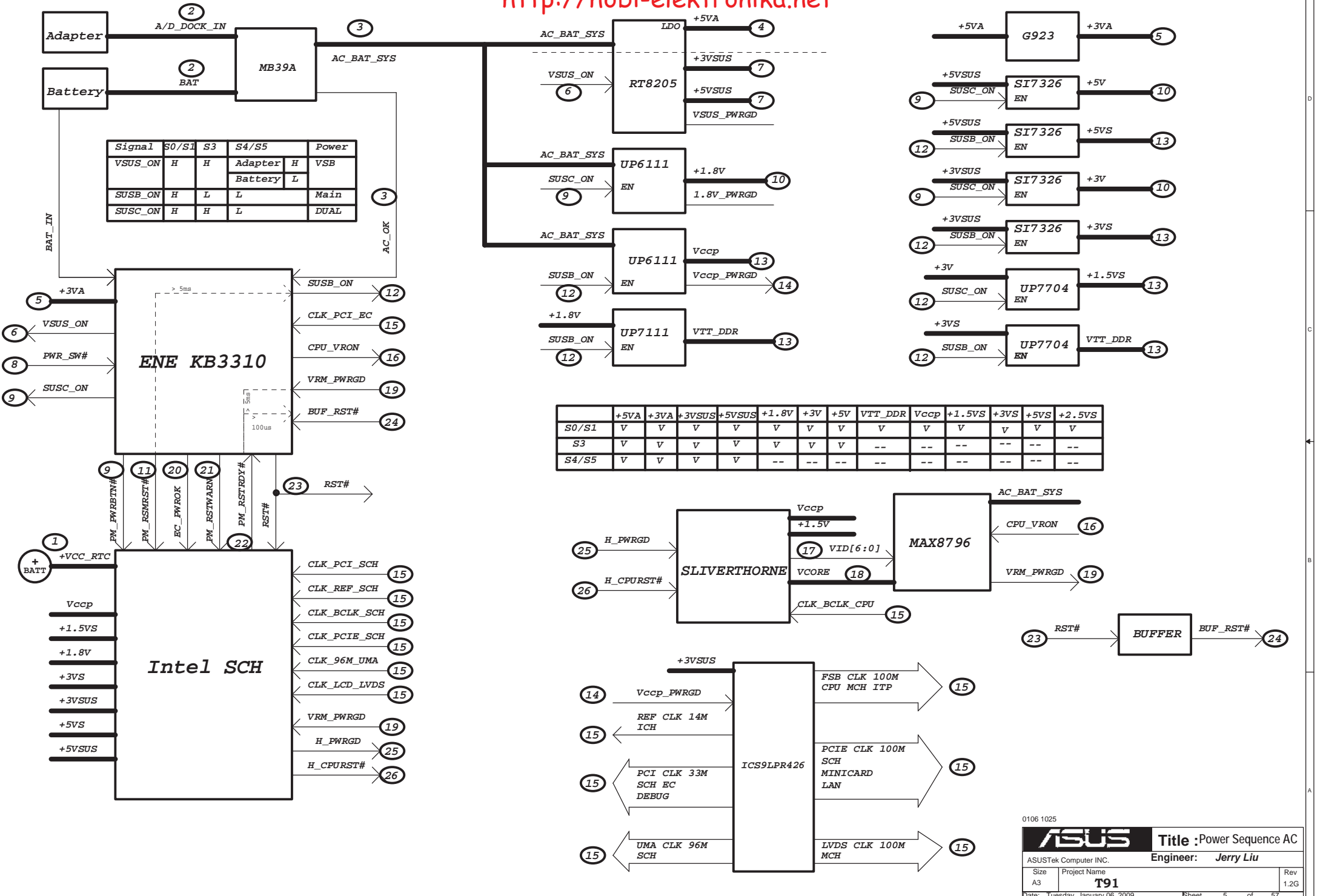
## EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/O	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA	P	
24	GND	GND	P	
33	VCC	+3VA	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VA_AEC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA	P	
111	VCC	+3VA	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
122	XCLKI	K_XCLKI	I	
123	XCLKO	K_XCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA	P	
128	SPICS#/SELMEM#	SPI_CS#	O	

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<b>ASUS</b>		Title : EC Pin Define	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size	Project Name	Rev	
A3	<b>T91</b>	1.2G	
Date: Tuesday, January 06, 2009		Sheet	3 of 57





### S4/S5 to S0(Adapter Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS\_ON=0, SUSB\_ON=0, SUSC\_ON=0, A20GA=X, KBRST=X, CPU\_VRON=0, ICH\_PWROK=0, RSTWARN=0, and PM\_RSMRST#=0, RESET#=0.

- 1.Waiting for AC\_OK until adaptor power is good, then
- 2.At least **5ms** after AC\_OK is asserted, EC asserts VSUS\_ON to enable VSUS power.
- 3.At least **20ms** after VSUS power is stable, waiting for PWR\_SW# until user is pressed. (Or waiting for SCH deasserted SLPRDY#, too?)
- 4.EC asserts RSTWARN.
- 5.SUSC\_ON is asserted at least 20ms (de-bounce) after receiving PWR\_SW#.
- 6.PM\_RSMRST# is deasserted at least **5ms** after SUSC power is stable.
- 7.At least **5ms** after PM\_RSMRST# is deasserted, SUSB\_ON is enabled.
- 8.CPU\_VRON is deasserted at least **100ms** after SUSB power is stable.
- 9.Waiting for CPUPWR\_GD (VRM\_PWRGD) until CPU\_VRON power is stable.
- 10.At least **10ms** after receiving CPUPWR\_GD, PM\_PWROK is asserted, and then deasserts RSTWARN.
- 11.Waiting for RSTRDY# until deasserted by SCH.
- 12.RESET# can be deasserted at lease **100us** after PM\_PWROK is asserted.

### S4/S5 to S0(Battery Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS\_ON=0, SUSB\_ON=0, SUSC\_ON=0, A20GA=X, KBRST=X, CPU\_VRON=0, ICH\_PWROK=0, RSTWARN=0, and PM\_RSMRST#=0, RESET#=0.

- 1.Waiting for BAT\_IN until battery power is good, then
- 2.Waiting for PWR\_SW# until user is pressed.
- 3.EC asserts VSUS\_ON to enable VSUS power.
- 4.At least **20ms** after VSUS power is stable.
- 5.EC asserts RSTWARN.
- 6.SUSC\_ON is asserted at least 20ms (de-bounce) after receiving PWR\_SW#.
- 7.PM\_RSMRST# is deasserted at least 5ms after SUSC power is stable.
- 8.At least 5ms after PM\_RSMRST# is deasserted, SUSB\_ON is enabled.
- 9.CPU\_VRON is deasserted at least 10ms after SUSB power is stable.
- 10.Waiting for CPUPWR\_GD (VRM\_PWRGD) until CPU\_VRON power is stable.
- 11.At least 10ms after receiving CPUPWR\_GD, PM\_PWROK is asserted, and then deasserts RSTWARN.
- 12.Waiting for RSTRDY# until deasserted by SCH.
- 13.RESET# can be deasserted at lease 100us after ICH\_PWROK is asserted.

### S0 to S3/S4/S5

This sequence will occur when system entry to sleep states, or all power planes are shut down.

Initial EC state: VSUS\_ON=1, SUSB\_ON=1, SUSC\_ON=1, CPU\_VRON=1, ICH\_PWROK=1, and PM\_RSMRST#=1, RESET#=1, RSTWARN=0, PM\_PWRBTN#=1.

- 1.Waiting for PWR\_SW# until user is pressed (go to 2), or waiting for SLPRDY# is asserted (go to 3).
- 2.At least 20ms after PWR\_SW# is asserted, EC asserts PM\_PWRBTN# (50ms width) to SCH.
- 3.Waiting for SLPRDY# until has been asserted.
- 4.EC asserts RSTWARN to SCH to begin internal sequence.
- 5.SCH asserts RSTRDY# to EC to indicate all outstanding transactions are completed.
- 6.EC asserts RESET# after detecting RSTRDY# asserted.
- 7.EC deasserts ICH\_PWROK.
- 8.EC deasserts SUSB\_ON and CPU\_VRON to turn off power planes.

#### This completes the entry to S3 (SLPMODE=1).

If SLPMODE=0, this indicates S4/S5 was the desired state, EC takes additional actions:

- 9.EC asserts PM\_RSMRST#.
- 10.EC deasserts SUSC\_ON to turn off the other power planes.
- 11.EC deasserts VSUS\_ON if in battery mode.
- 12.EC deasserts RSTWARN to save more power.

### Power Sequence Description: S3 to S0

This sequence will occur in S3, and wake event is detected by EC or SCH.

Initial EC state: SUSB\_ON=0, CPU\_VRON=0, ICH\_PWROK=0, PM\_RSMRST#=1, PM\_PWRBTN#=1, and VSUS\_ON=1, RSTWARN=1, SUSC\_ON=1, RESET#=0.

- 1.For internal wake event, SCH deasserts SLPRDY# to EC, than 4.
- 2.For external wake event (PWR\_SW#, keyboard wake up), then
- 3.EC asserts PM\_PWRBTN# at least 50ms to wake SCH, and waiting for SLPRDY# until SCH deasserted.
- 4.EC asserts SUSB\_ON to enable SUSB power.
- 5.CPU\_VRON is deasserted at least **100ms** after SUSB power is stable.
- 6.Waiting for CPUPWR\_GD (VRM\_PWRGD) until CPU\_VRON power is stable.
- 7.At least **5ms** after receiving CPUPWR\_GD, ICH\_PWROK is asserted.
- 8.Deasserts RSTWARN after ICH\_PWROK is asserted.
- 9.RESET# can be deasserted **100us** after RSTWARN is deasserted.

### Warm Reset (SLPMODE=1)

The warm reset sequence results in reset without remove any power supplies.

Initial EC state: SUSB\_ON=1, CPU\_VRON=1, ICH\_PWROK=1, PM\_RSMRST#=1, PM\_PWRBTN#=1, and VSUS\_ON=1, RSTWARN=1, SUSC\_ON=1, RESET#=1.

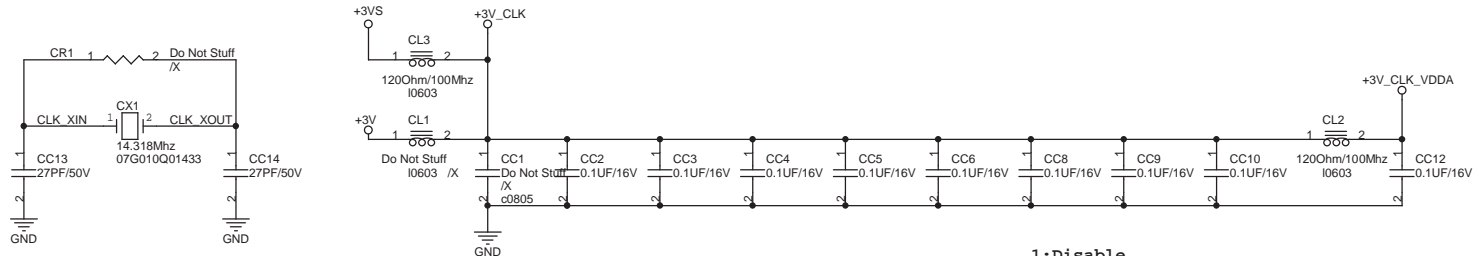
- 1.SCH asserts RSTRDY# at the same time as driving SLPMODE=1 to EC.
- 2.EC asserts RSTWARN to SCH.
- 3.EC asserts RESET# for **1200ms** to SCH after asserts RSTWARN.
- 4.EC deasserts RSTWARN.
- 5.EC deasserts RESET# after at least **100us** delay from RSTWARN.

### Cold Reset (SLPMODE=0)

The cold reset sequence results in a power cycling of all but the RTC power well.

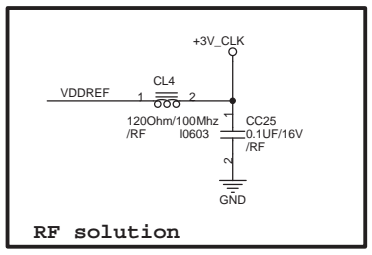
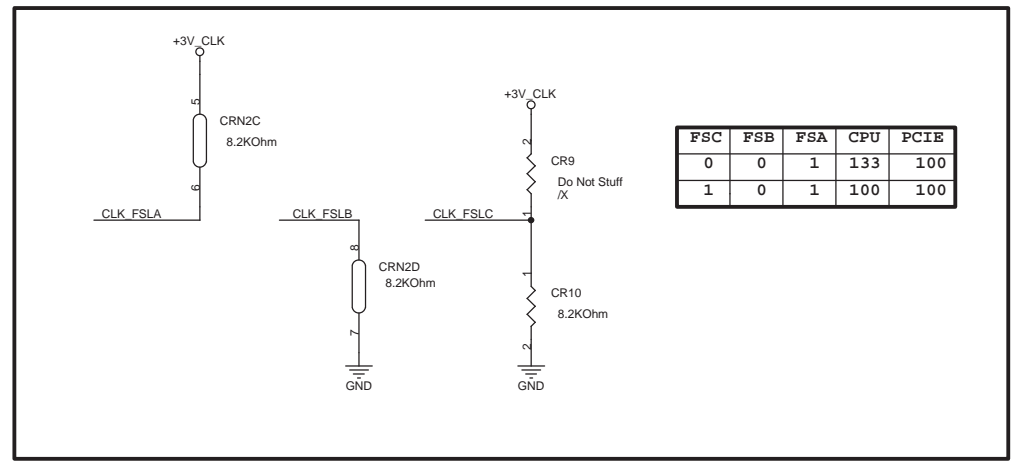
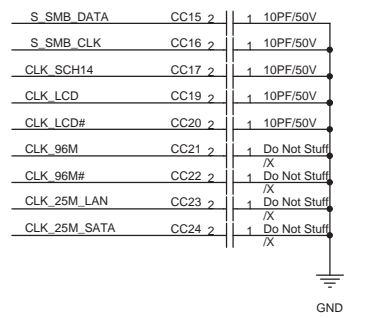
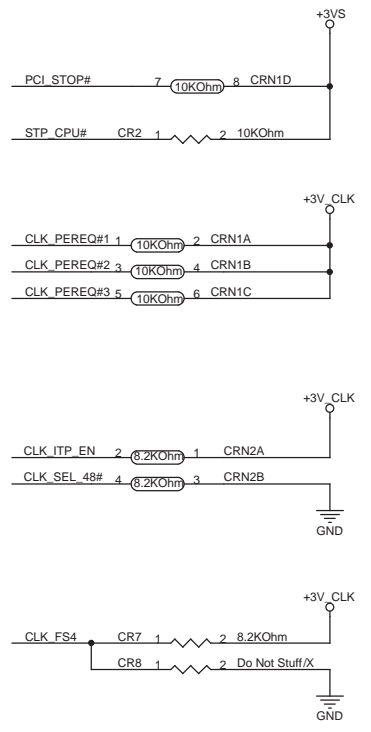
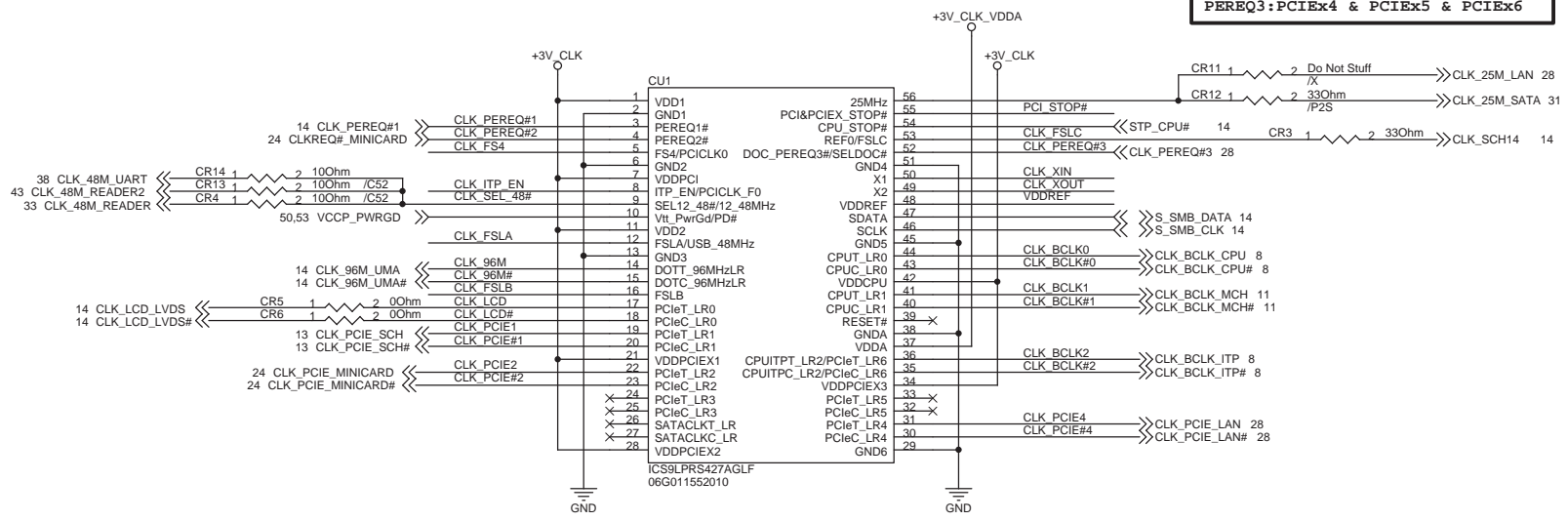
Initial EC state: SUSB\_ON=1, CPU\_VRON=1, ICH\_PWROK=1, PM\_RSMRST#=1, PM\_PWRBTN#=1, and VSUS\_ON=1, RSTWARN=1, SUSC\_ON=1, RESET#=1.

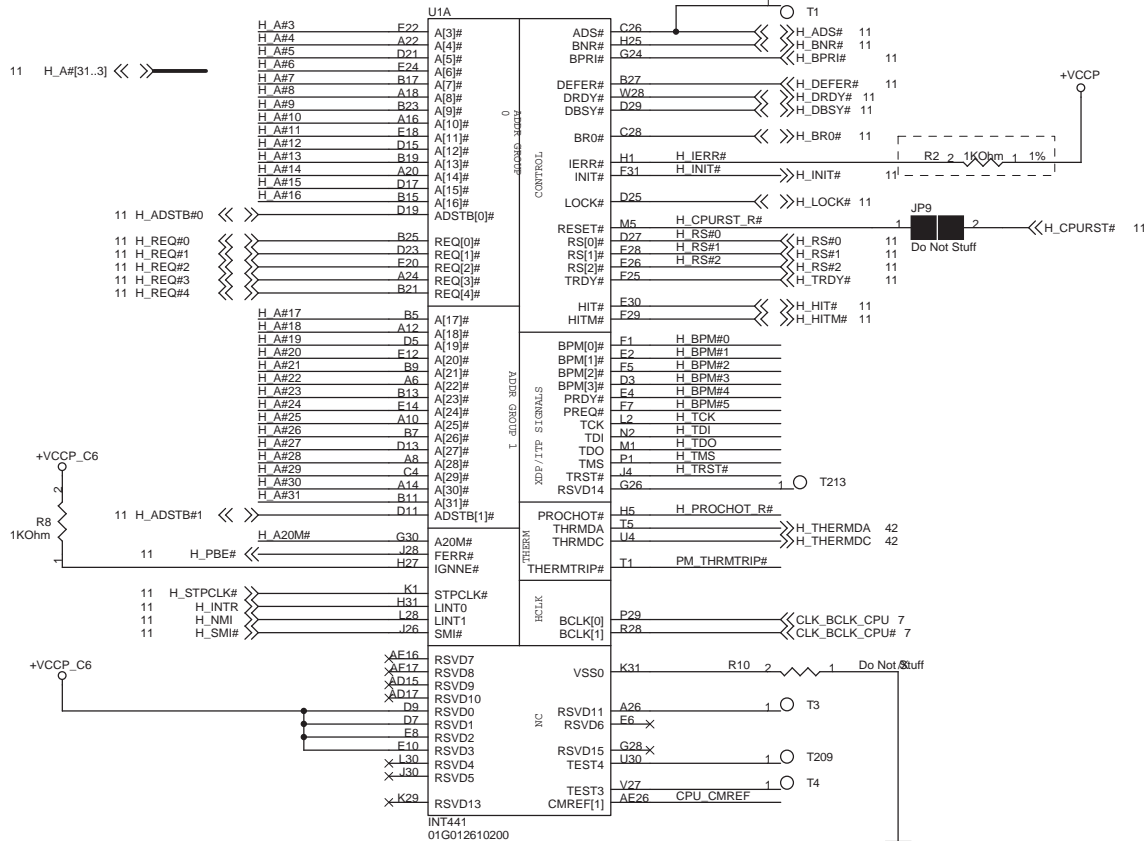
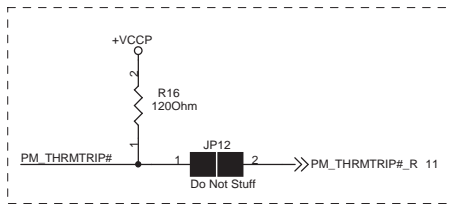
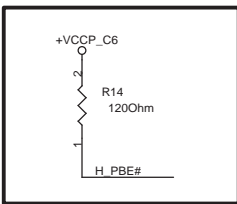
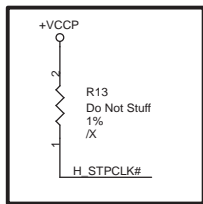
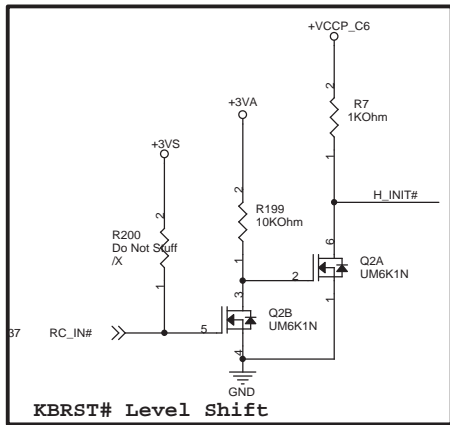
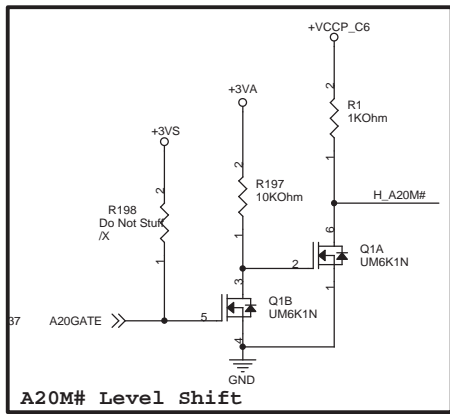
- 1.SCH asserts RSTRDY# at the same time as driving SLPMODE=0 to EC.
- 2.EC asserts RSTWARN to SCH.
- 3.EC asserts RESET# to SCH after asserts RSTWARN.
- 4.EC deasserts PM\_PWROK and disables SUSB\_ON and CPU\_VRON power.
- 5.EC asserts PM\_RSMRST# after CPU\_VRON power is off.
- 6.EC disables SUSC\_ON power for 3-5 seconds.
- 7.S4/S5 to S0 sequence is automatically followed to bring the system back to S0 when SUSC\_ON power is enable.



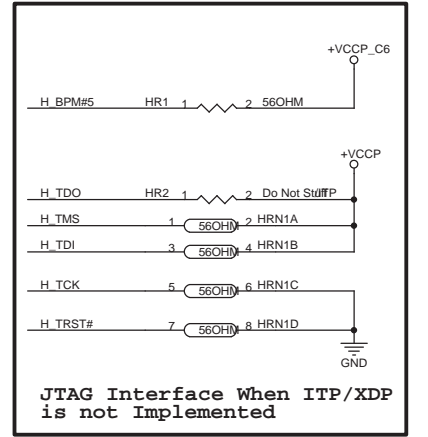
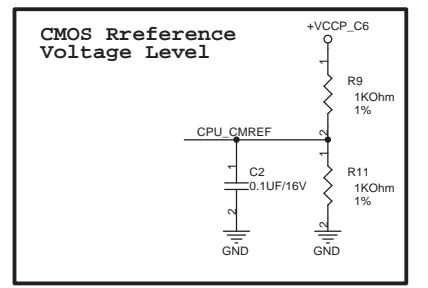
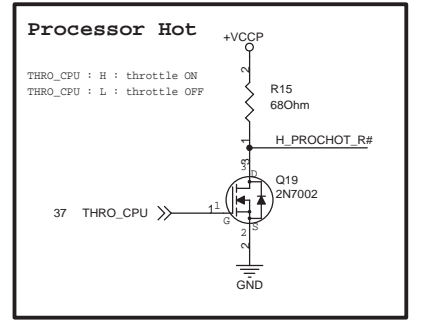
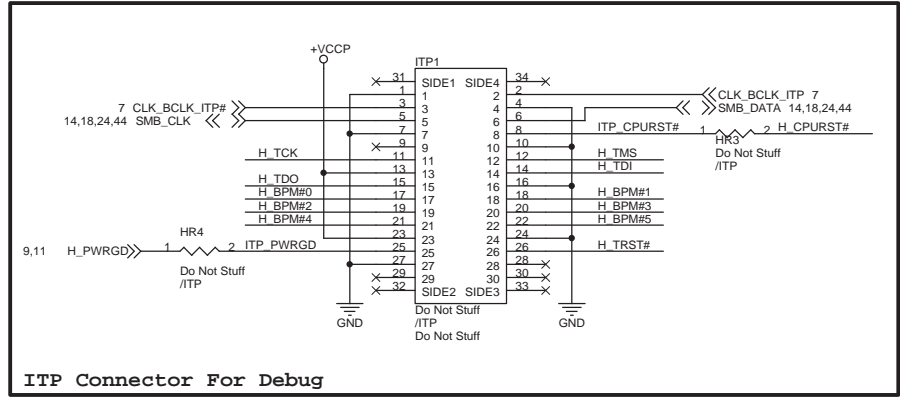
1:Disable  
0:Enable

PEREQ1:PCIEx0 & PCIEx1  
PEREQ2:PCIEx2 & PCIEx3 & SATA  
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

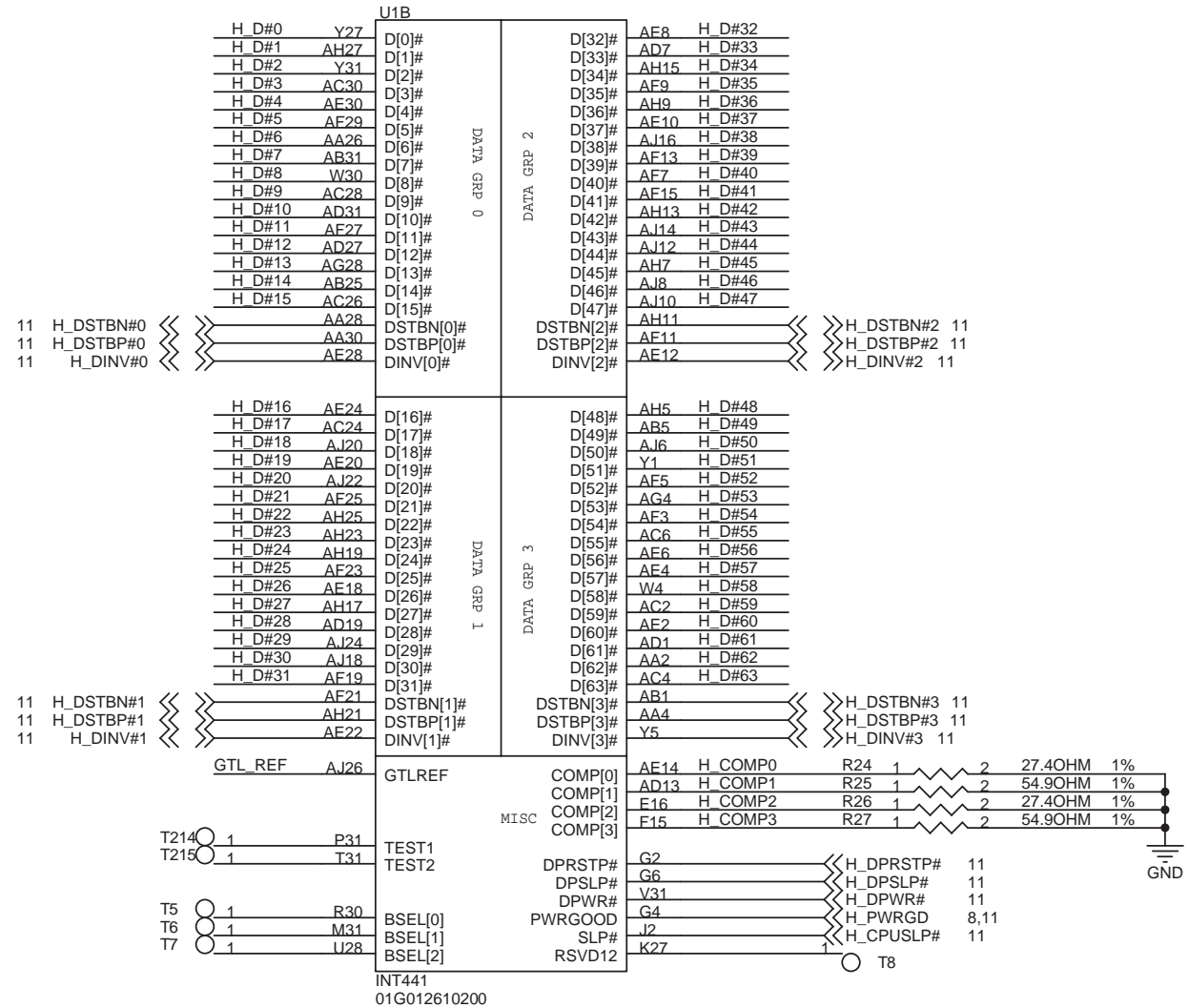




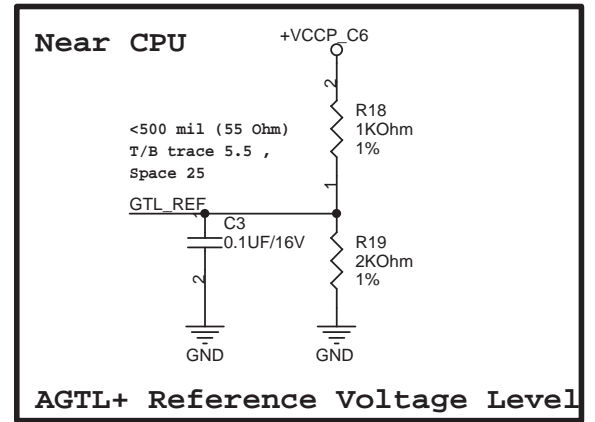
Z530 : 01G011980000  
 Z520 C0 stage : 01G012610200







H\_D#[63:0] << >> H\_D#[63:0] 11



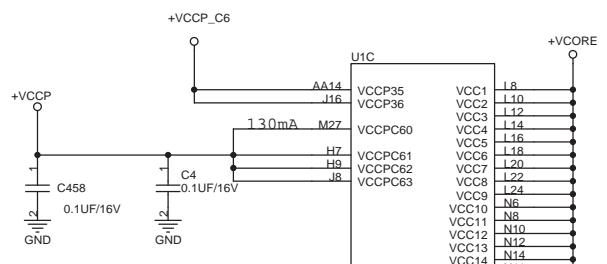
**Layout Note**

COMP 0 2 connect with Z0=27.4 ohm,L<0.5"

COMP 1 3 connect with Z0=55 ohm,L<0.5"

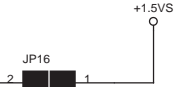
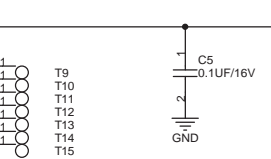
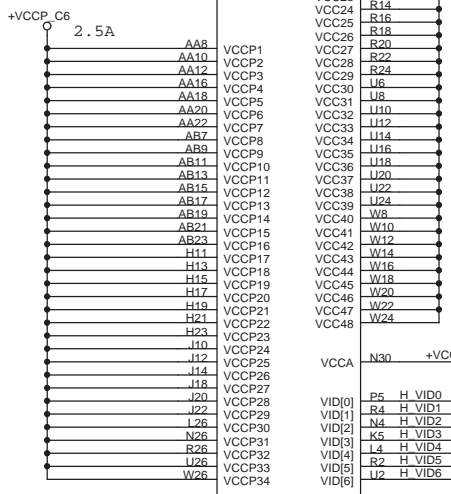
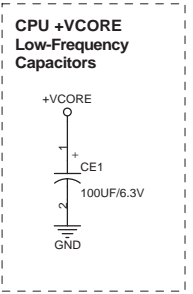
0106 1025

<b>ASUS</b>		<b>Title :</b> CPU-SLIVERTHORNE(1)	
ASUSTeK COMPUTER INC		<b>Engineer:</b> Jerry Liu	
Size A4	Project Name <b>T91</b>	Rev 1.2G	
Date: Tuesday, January 06, 2009		Sheet	9 of 57

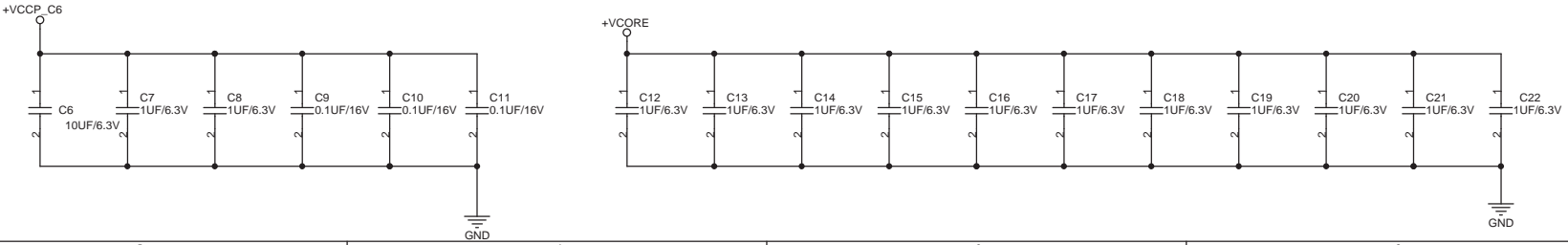
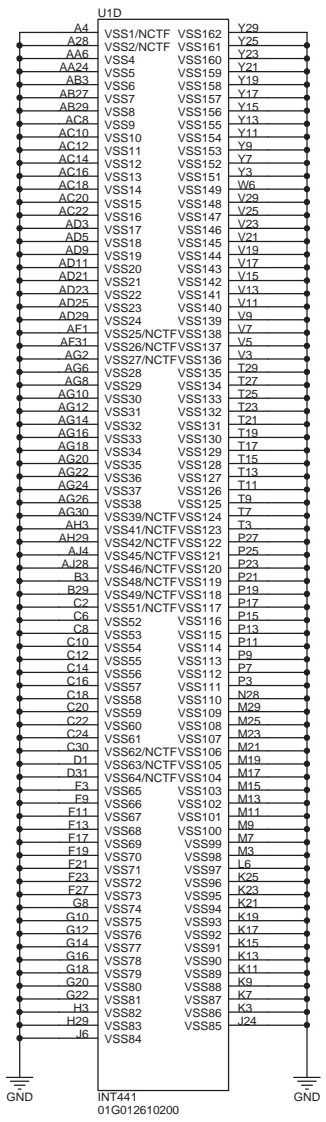


CPU TYPE	Vcore	Freq
Silverthorne Standard Voltage	0.98V @HFM TBD @LFM	TBD
Processors Medium Voltage	0.8V @HFM TBD @LFM	TBD
Processors Low Voltage	0.76V @HFM TBD @LFM	TBD

Processor



Layout Note:  
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 18mil trace, 7mil vccsense to vssense spacing. 25 mil spacing from others. Place PU and PD within 1 inch of CPU.



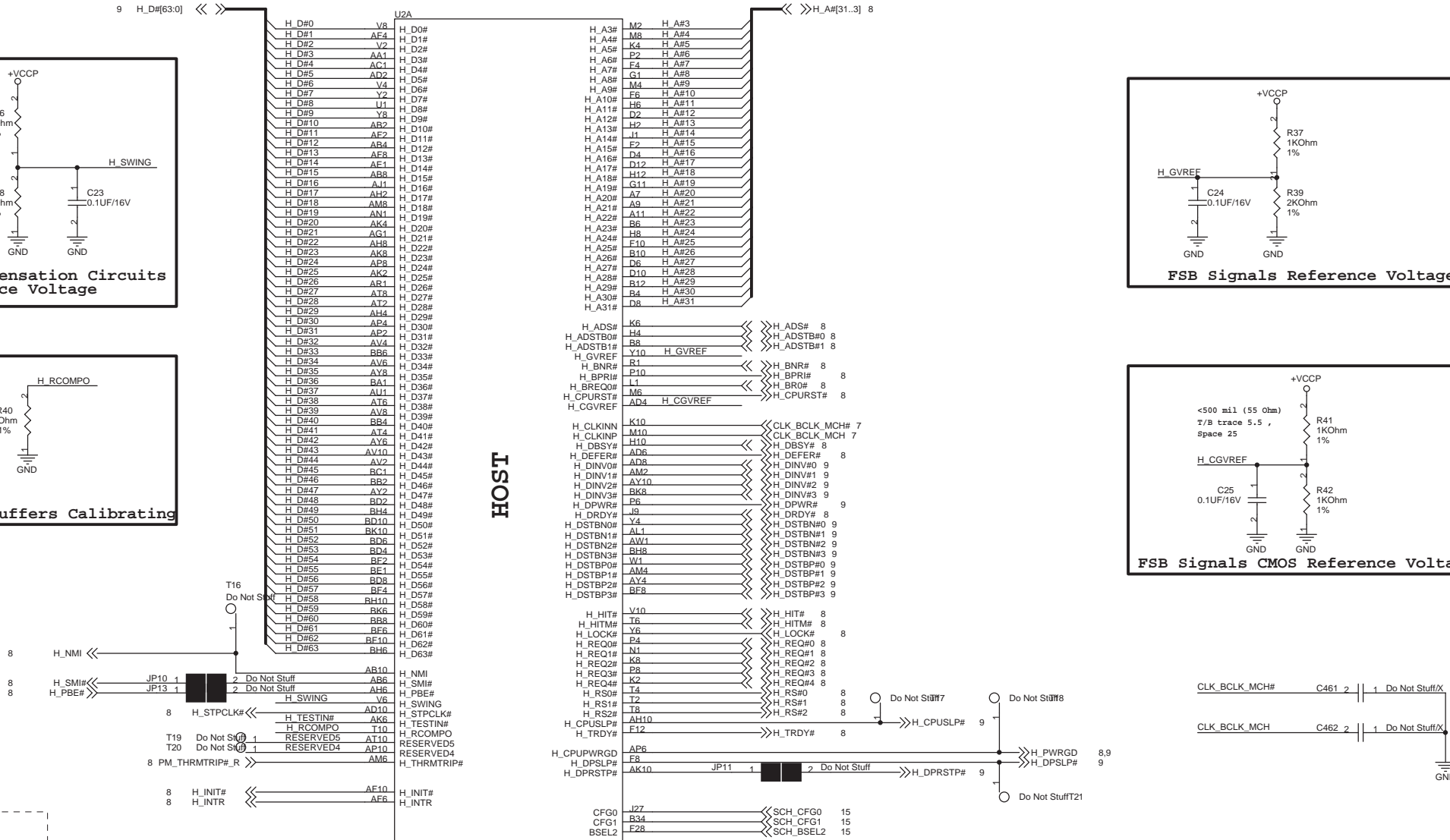
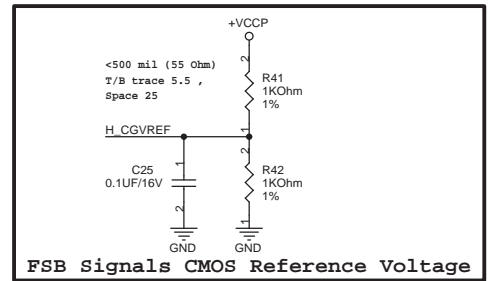
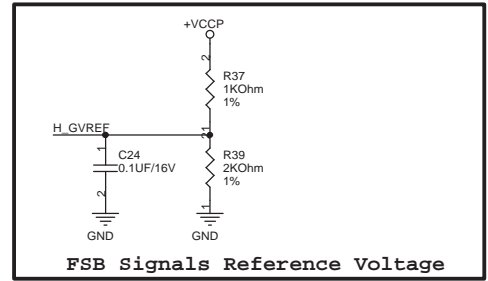
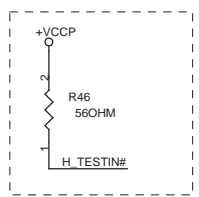
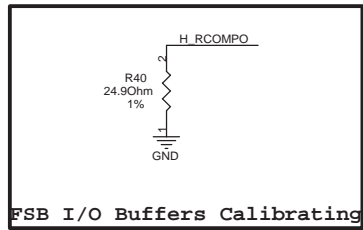
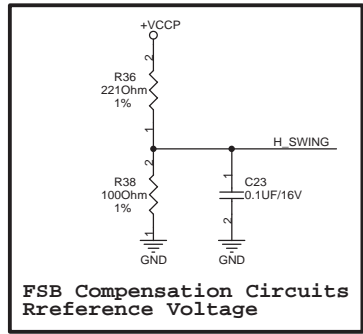
1016 1025

**ASUS** Title :CPU-SILVERTHORNE (2)

ASUSTeK COMPUTER INC Engineer: Jerry Liu

Size	Project Name	Rev
Custom	<b>T91</b>	1.2G

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02G010018704

**US15W D2 stage : 02G010018704**

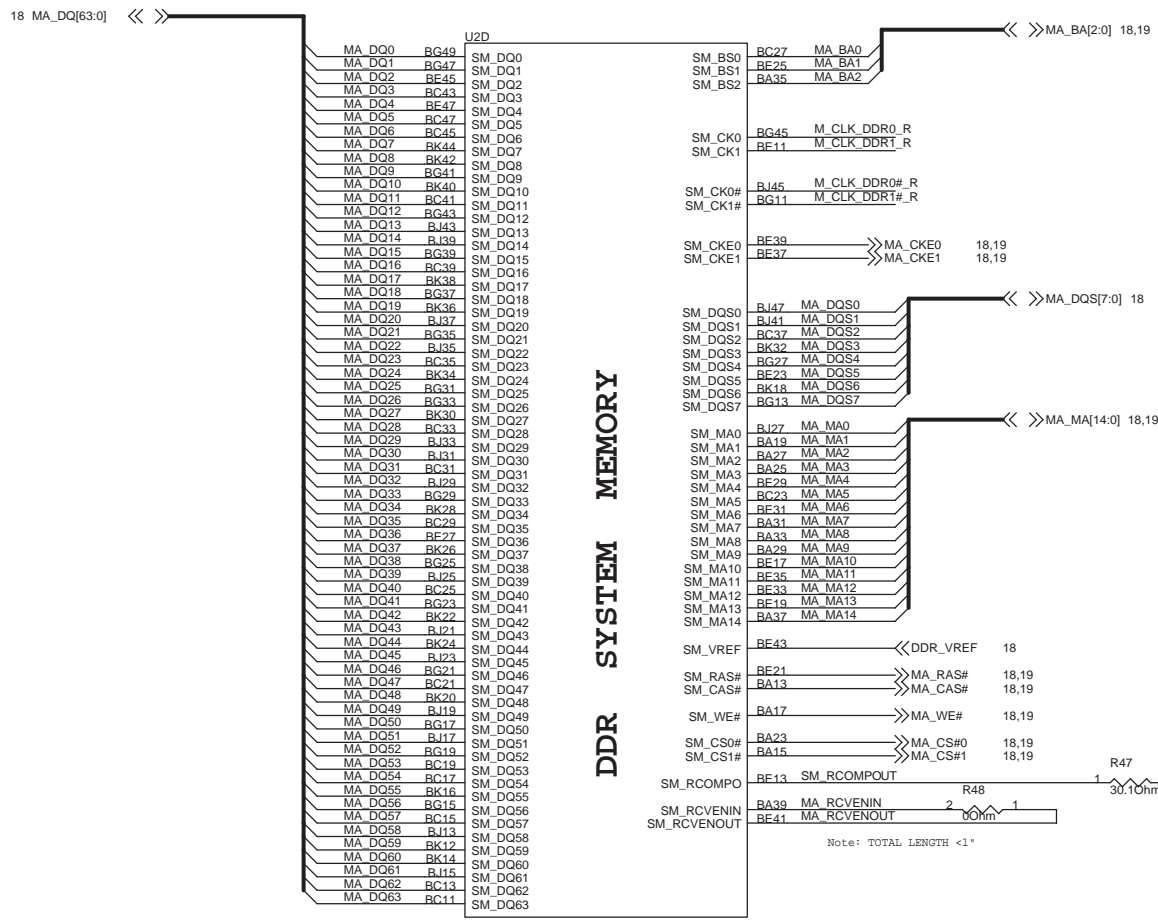
1016 1025

**ASUS** Title : Poulsobo\_HOST (1)

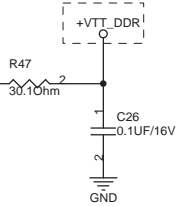
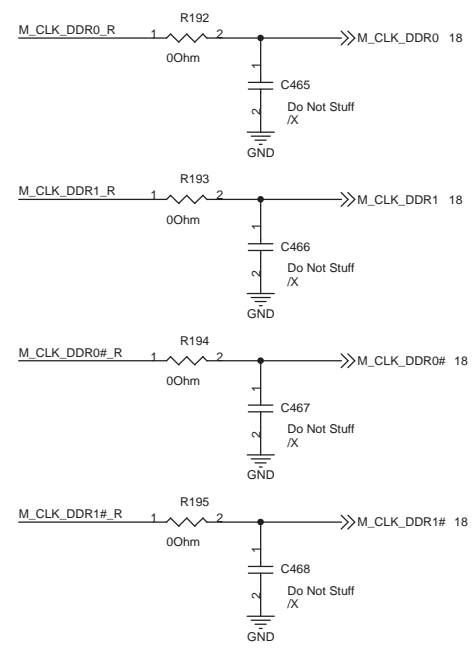
ASUSTeK COMPUTER INC Engineer: Jerry Liu

Size	Project Name	Rev
Custom	<b>T91</b>	1.2G

Date: Tuesday, January 06, 2009 Sheet 11 of 57

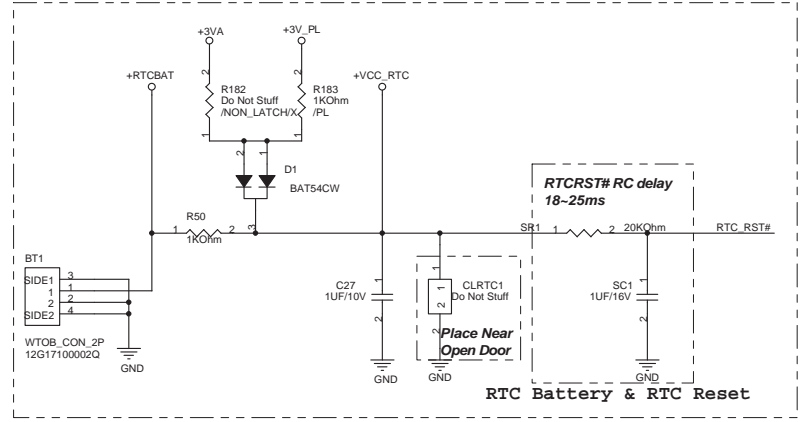
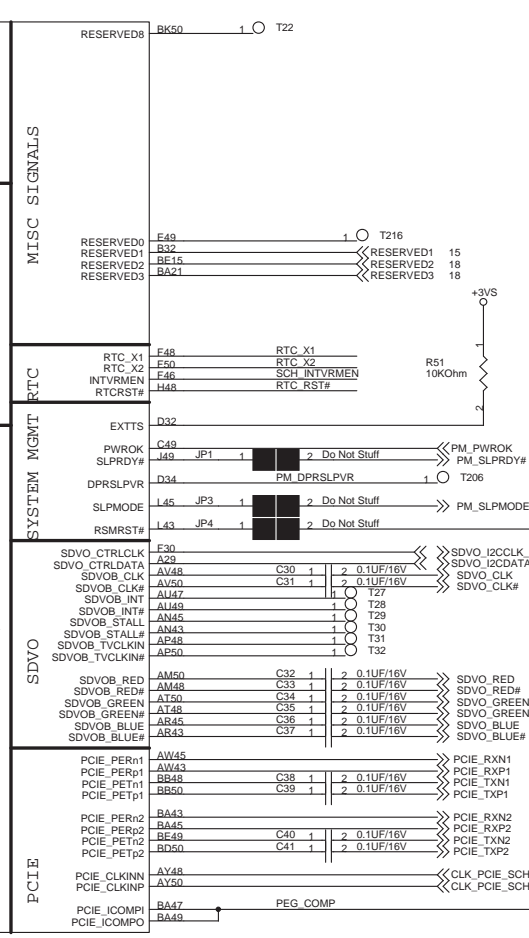
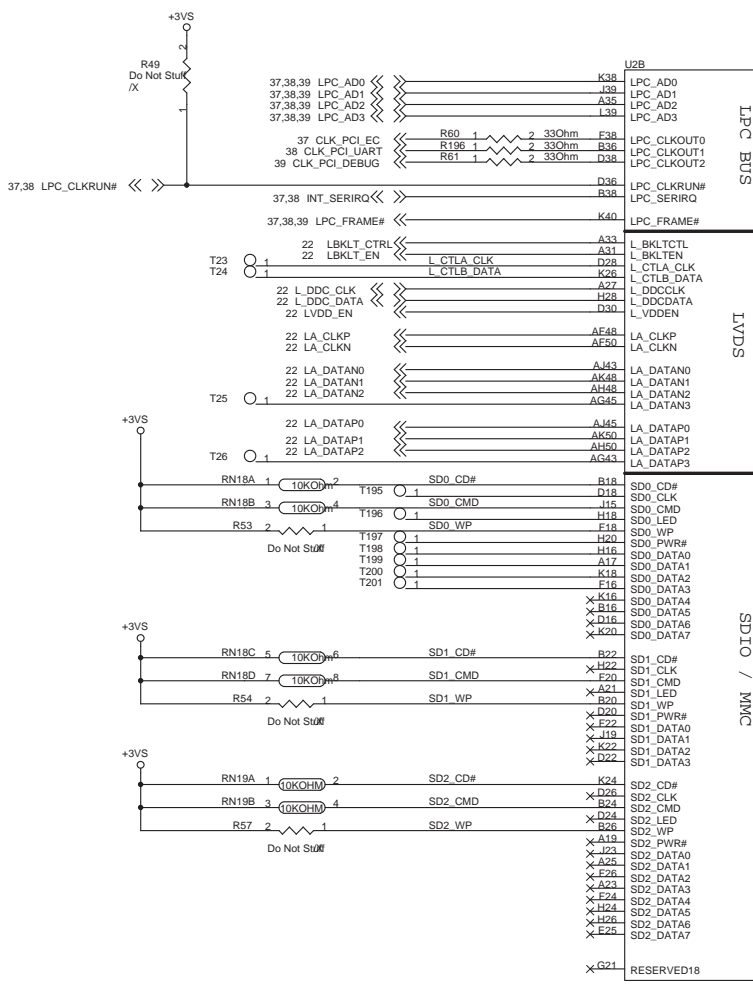


02G010018704

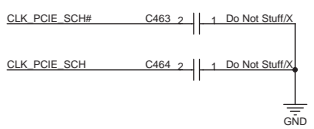
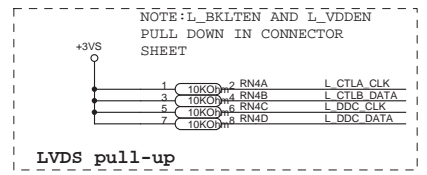
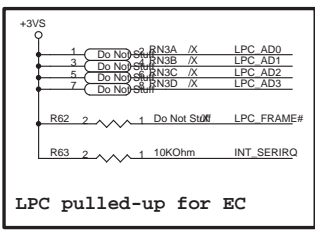
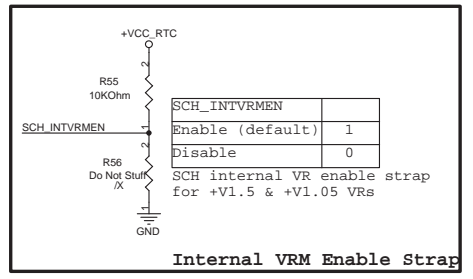
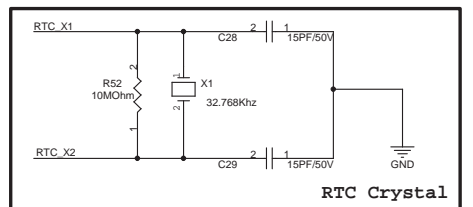


0106 1025

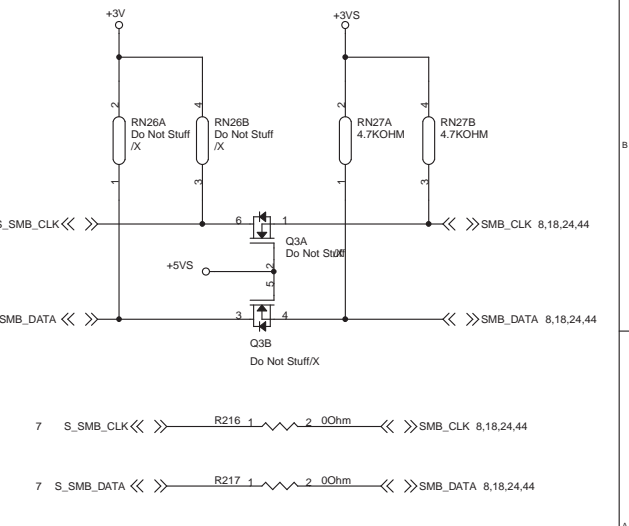
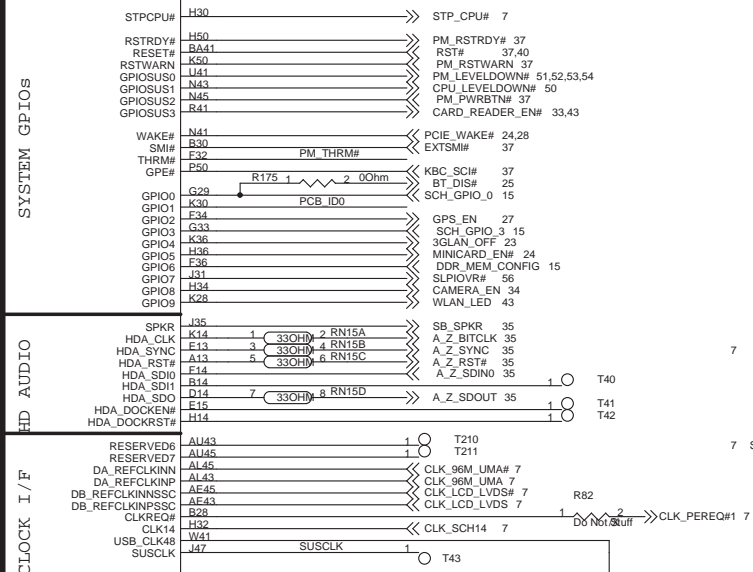
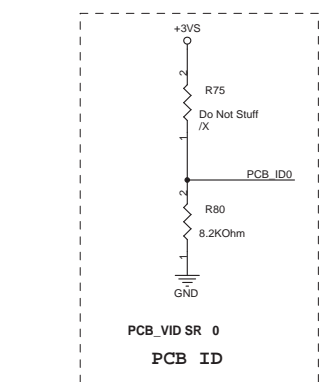
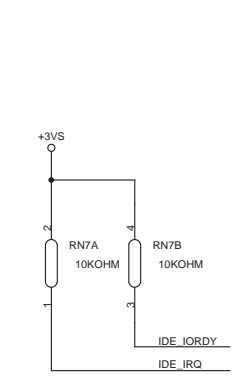
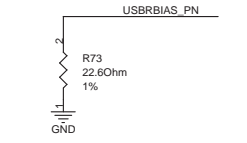
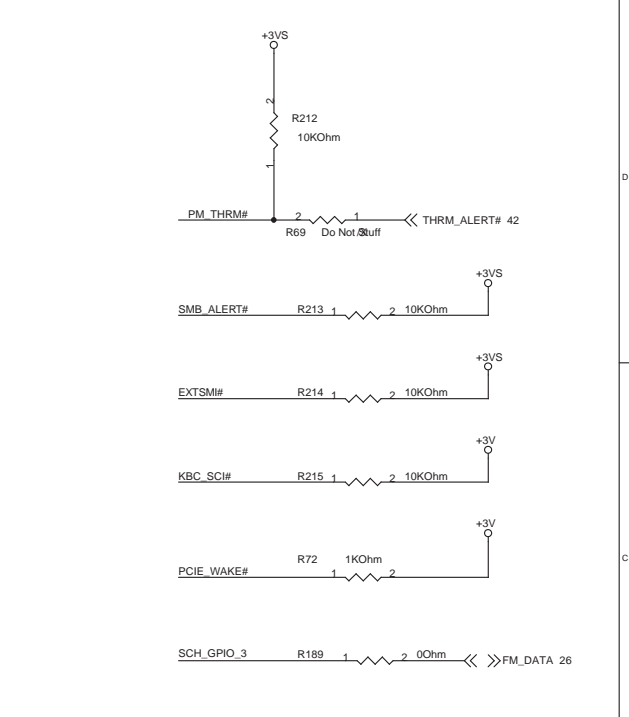
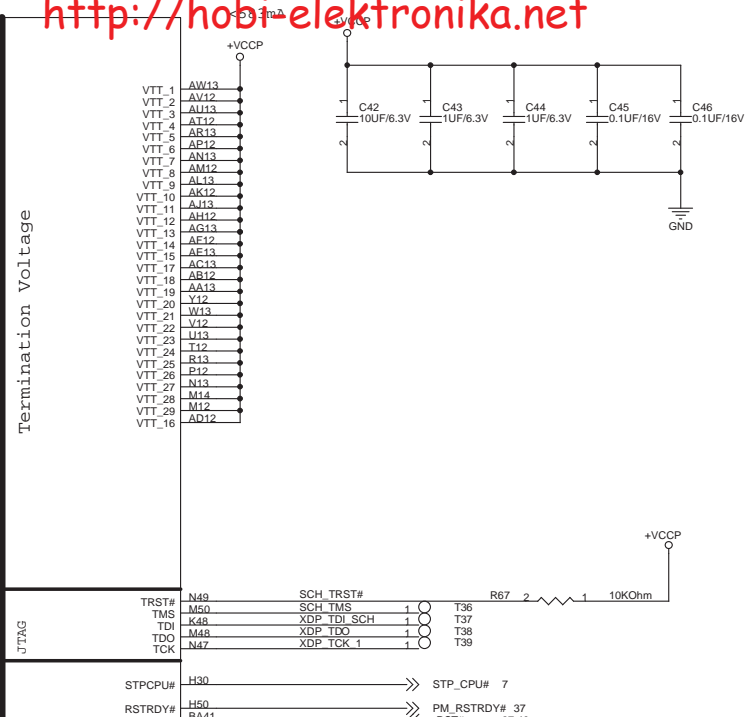
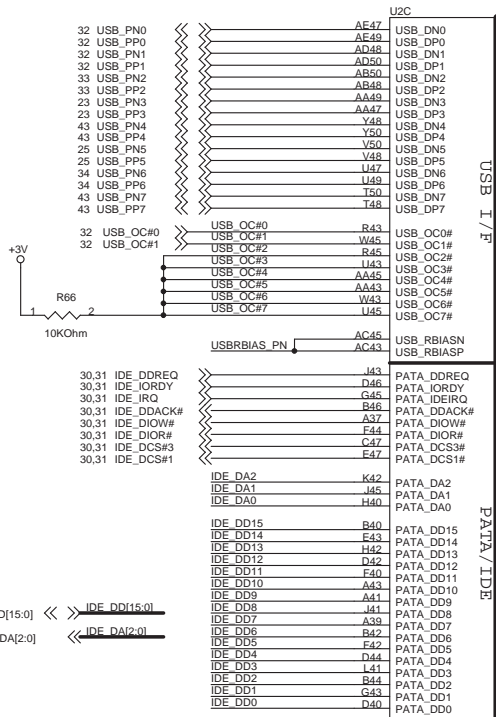
<b>ASUS</b>		Title : Poulisbo_DDR2 (2)	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size Custom	Project Name <b>T91</b>	Rev 1.2G	
Date: Tuesday, January 06, 2009		Sheet 12 of 57	



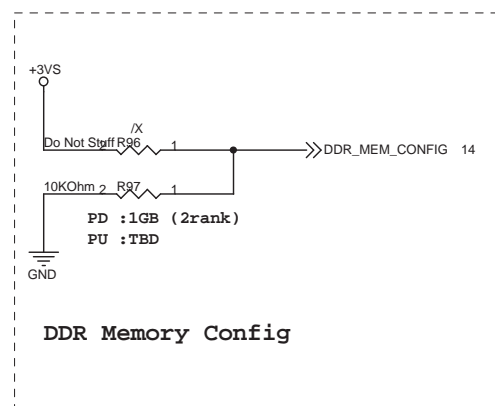
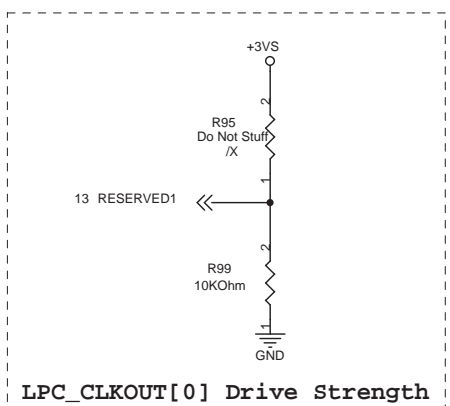
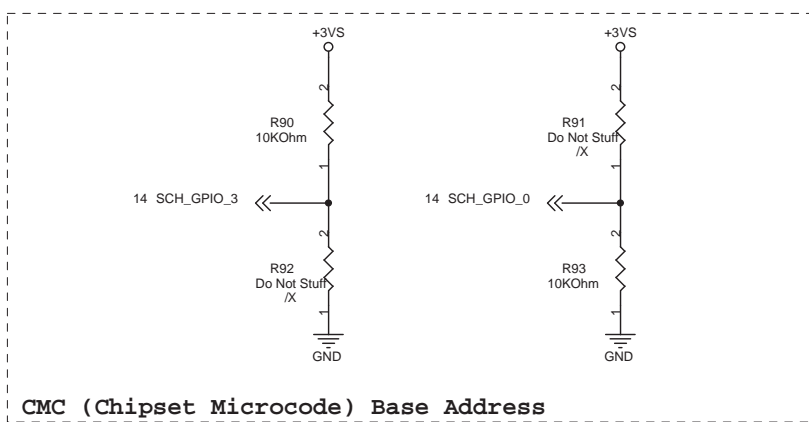
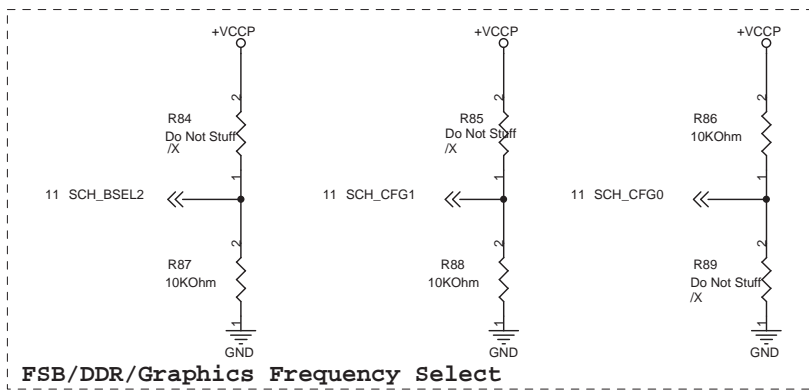
PM_SLPDRY#	PM_SLPMODE	System Behavior
0	1	SCH ready to enter S3
0	0	SCH ready to enter S4/S5



USB 0	USB PORT
USB 1	USB PORT
USB 2	Card Reader
USB 3	3.5G
USB 4	Touch Panel
USB 5	Bluetooth
USB 6	Camera
USB 7	2'nd Card Reader



02G010018704



Strap Function	Signal Name			Strap		Comment
<b>FSB/DDR Frequency Select</b>	SCH_BSEL2	SCH_CFG1	SCH_CFG0	Gfx_Freq	FSB	Note: Clock Frequencies are in Mhz Default Frequency determined by FSB speed
	0	0	0	200	400	
<b>Graphics Frequency Select</b>	0	0	1	200	533	
	GPIO3		GPIO0	Address		
<b>CMC (Chipset Microcode) Base Address</b>	0	0	0xFFFF0000			
	0	1	0xFFFC0000			
	1	0	0xFFFD0000 (default)			
	1	1	0xFFFE0000			
<b>LPC_CLKOUT[0] Buffer Strength</b>	RESERVED1		Value			Selects the drive strength of the LPC_CLKOUT[0] clock.
	0	Reserved				
	0	1 Load (Default)				
	1	Reserved				
	1	2 Loads				

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**ASUS** Title : POULSBO\_STRAP(5)  
 ASUSTek Computer INC. Engineer: Jerry Liu

Size	Project Name	Rev
B	<b>T91</b>	1.2G
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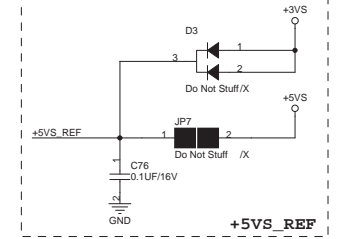
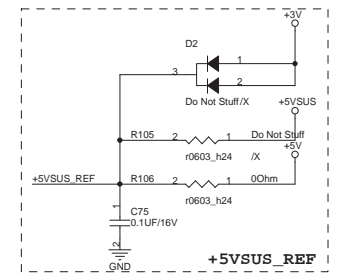
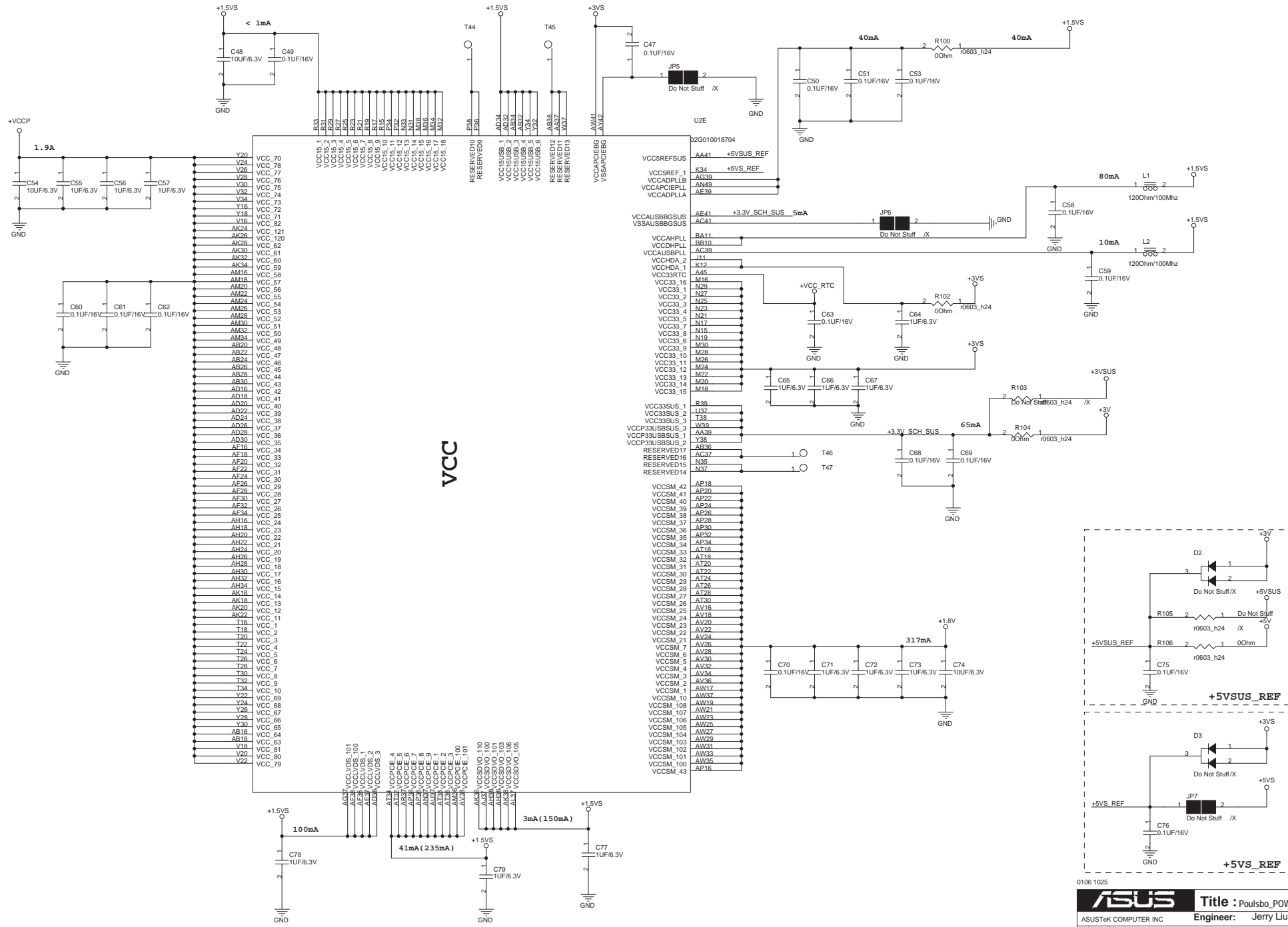




Table listing various components and their VSS connections, including U2G, U2F, and numerous VSS points.

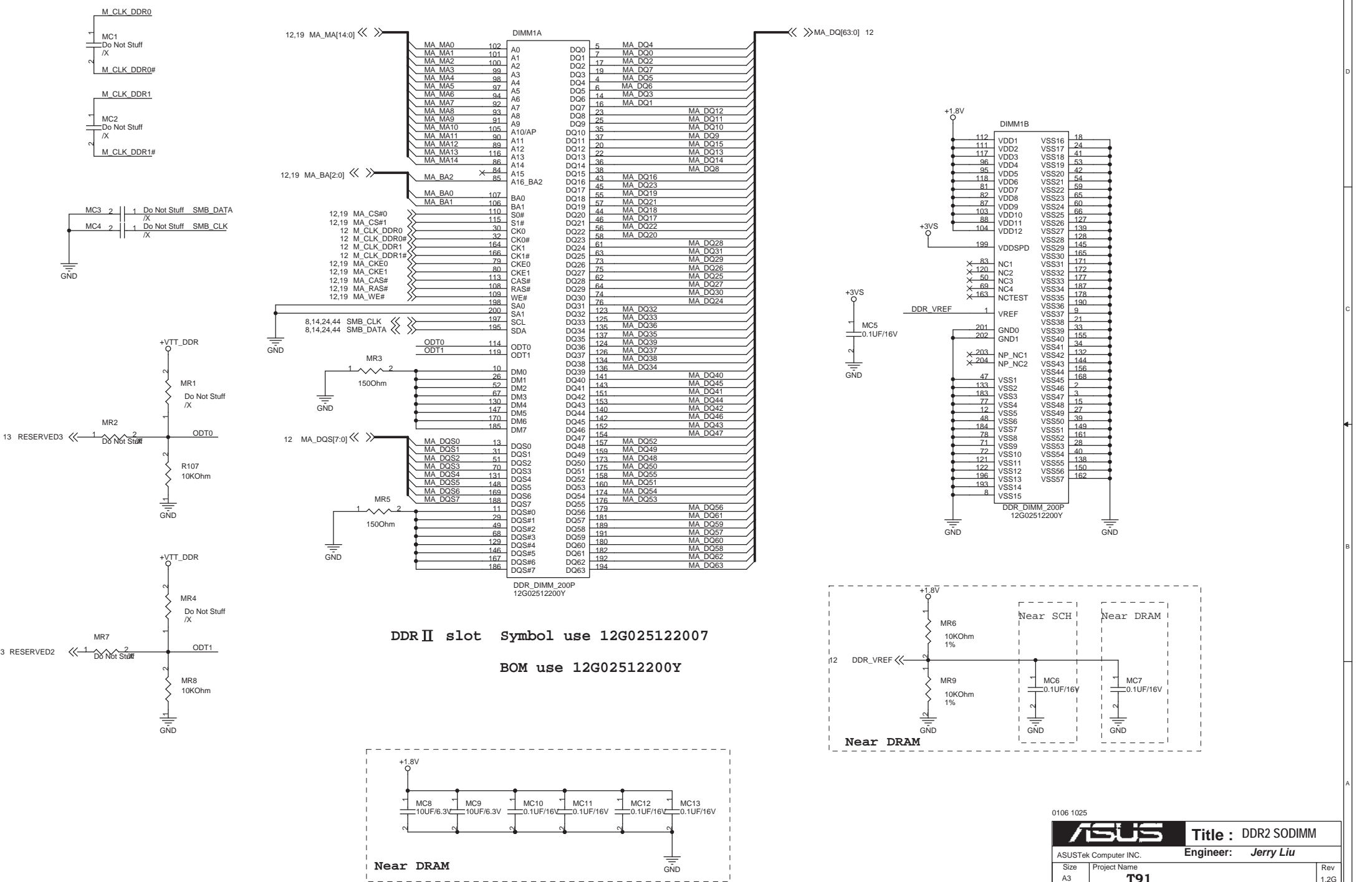
Table listing various components and their VSS connections, including BH30, BH40, BH50, and numerous VSS points.

Table listing various components and their VSS connections, including BH20, BH30, BH40, BH50, and numerous VSS points.

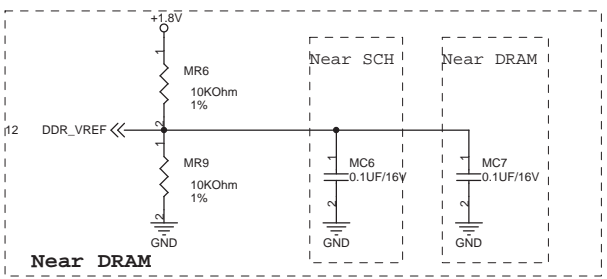
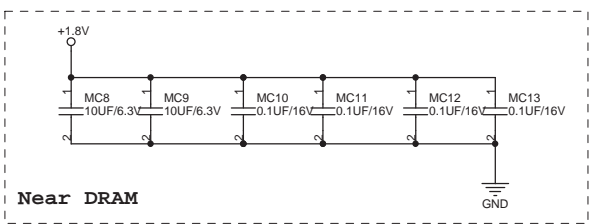
Table listing various components and their VSS connections, including BH50, BH60, BH70, and numerous VSS points.

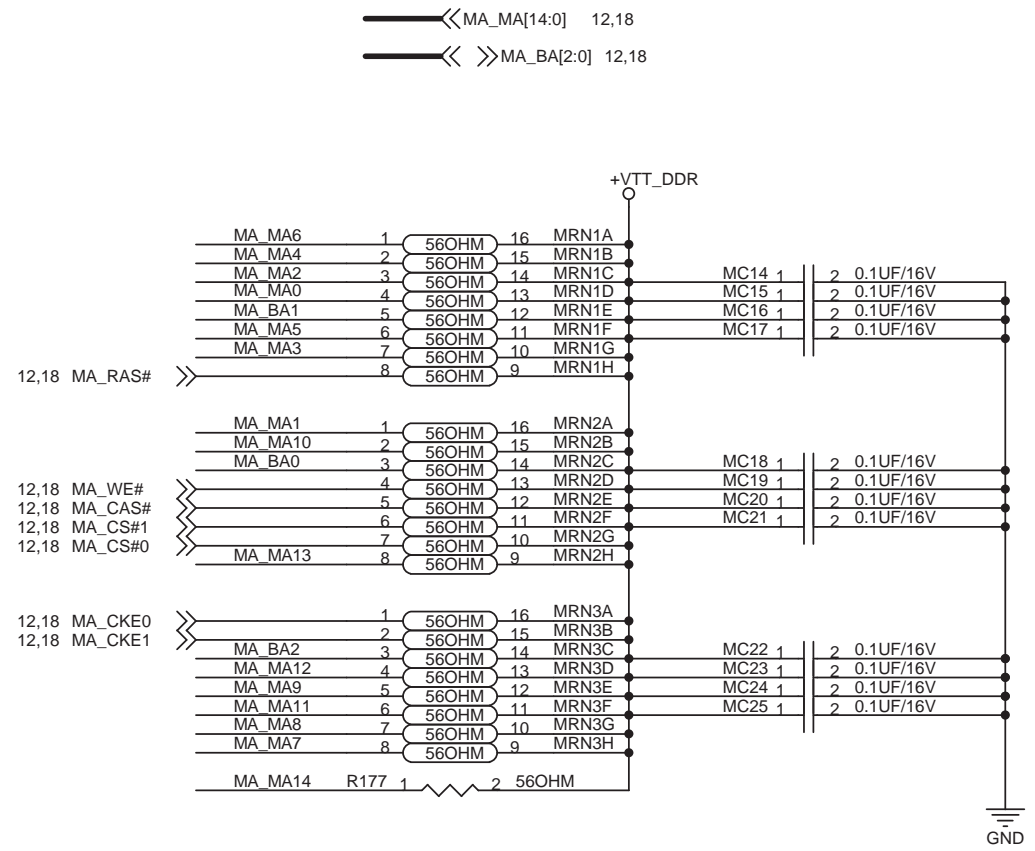
Table listing various components and their VSS connections, including BH80, BH90, BH100, and numerous VSS points.

Table listing various components and their VSS connections, including BH110, BH120, BH130, and numerous VSS points.



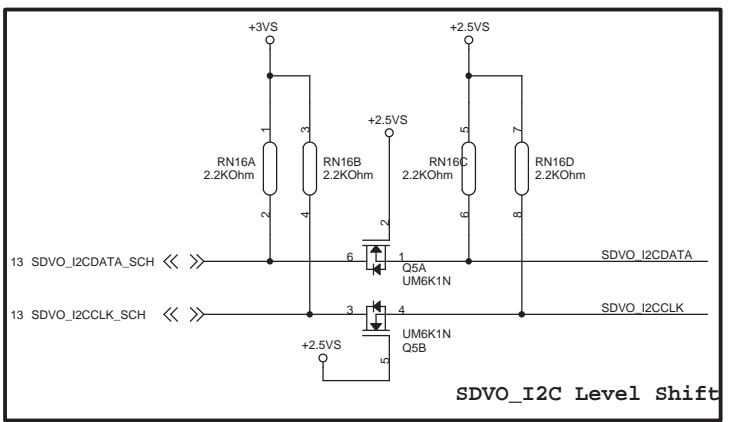
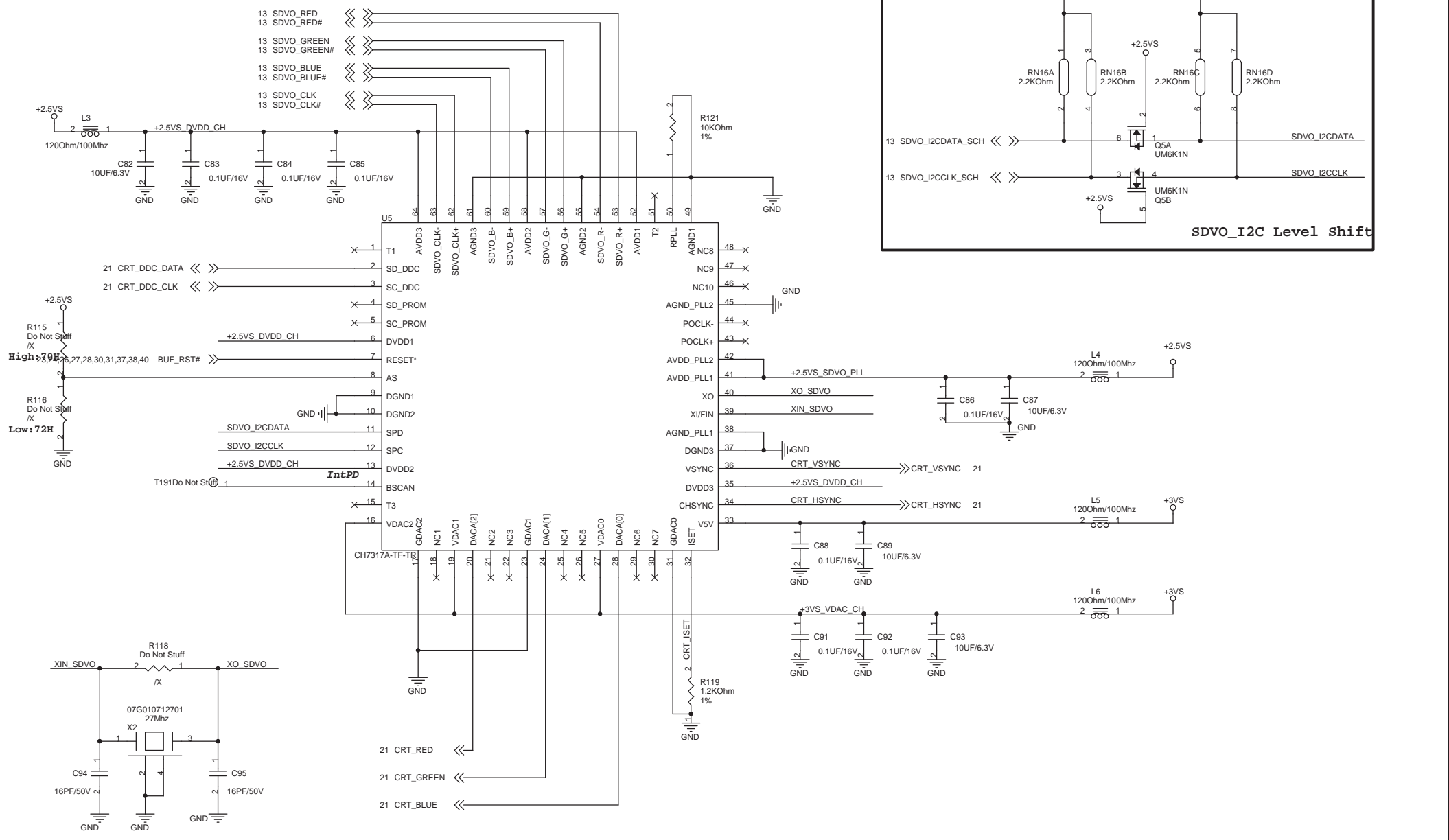
DDR II slot Symbol use 12G025122007  
 BOM use 12G02512200Y





0106 1025

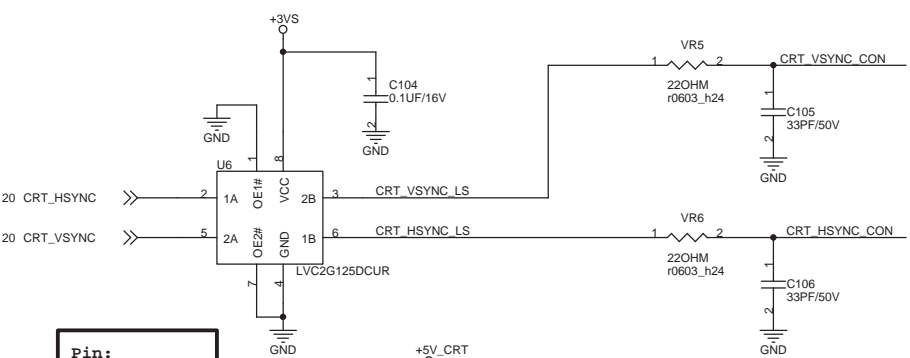
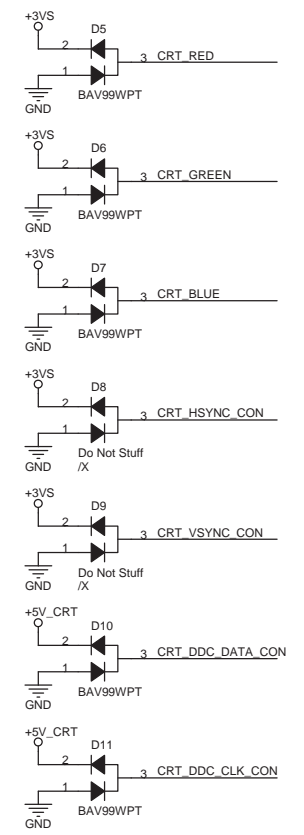
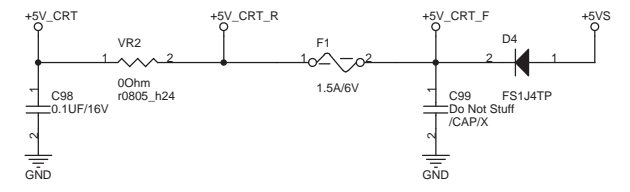
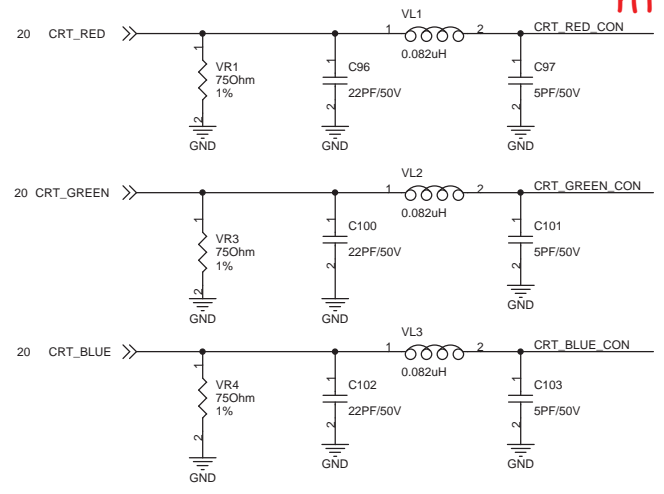
<b>ASUS</b>		<b>Title : DDR2_Termination</b>	
ASUSTek Computer INC.		<b>Engineer: Jerry Liu</b>	
Size A4	Project Name <b>T91</b>	Rev 1.2G	
Date: Tuesday, January 06, 2009		Sheet	19 of 57



SDVO\_I2C Level Shift

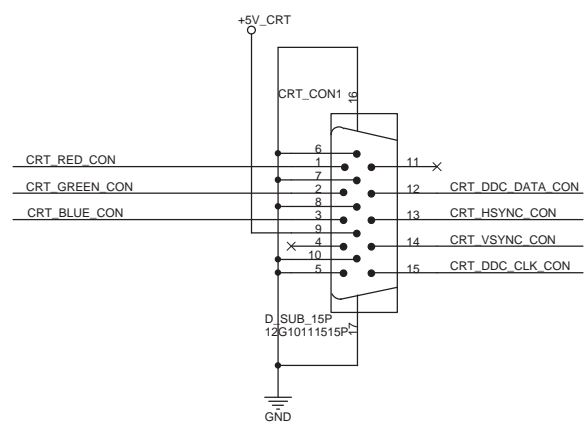
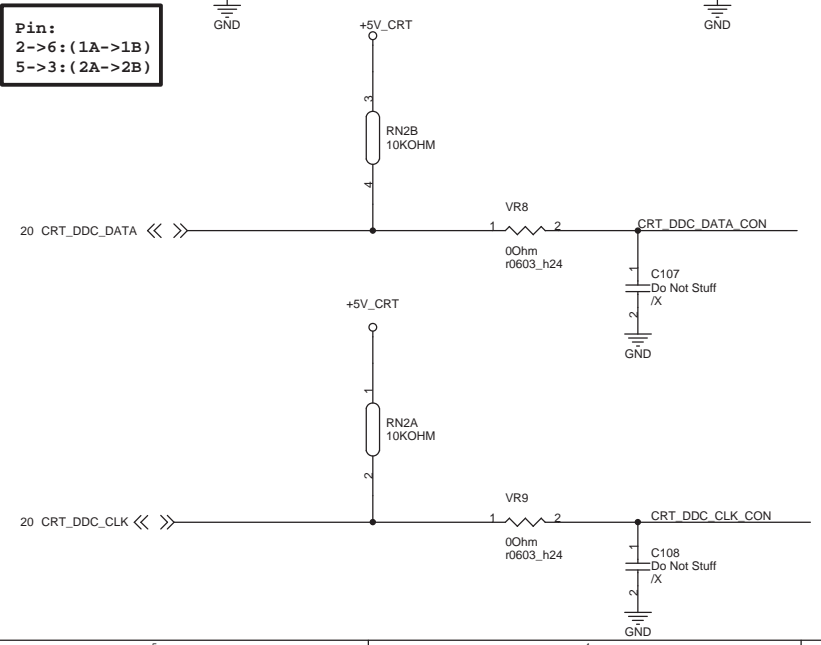
XTAL Height 1mm

0106 1025		Title :CH7317_SDVO_CRT	
ASUSTek COMPUTER INC		Engineer: Leon_Sun	
Size A3	Project Name <b>T91</b>	Rev 1.2G	
Date: Tuesday, January 06, 2009		Sheet	20 of 57

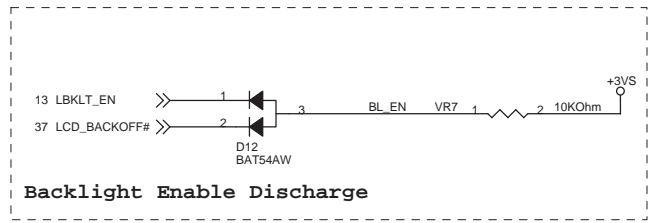
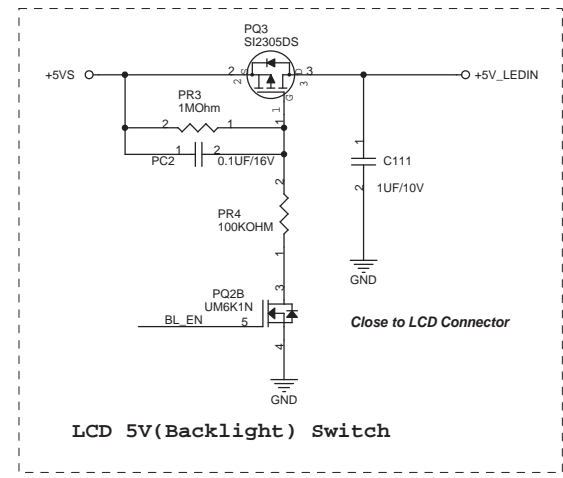
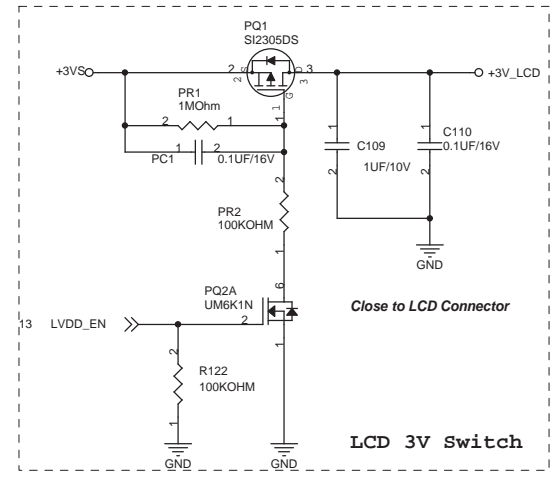
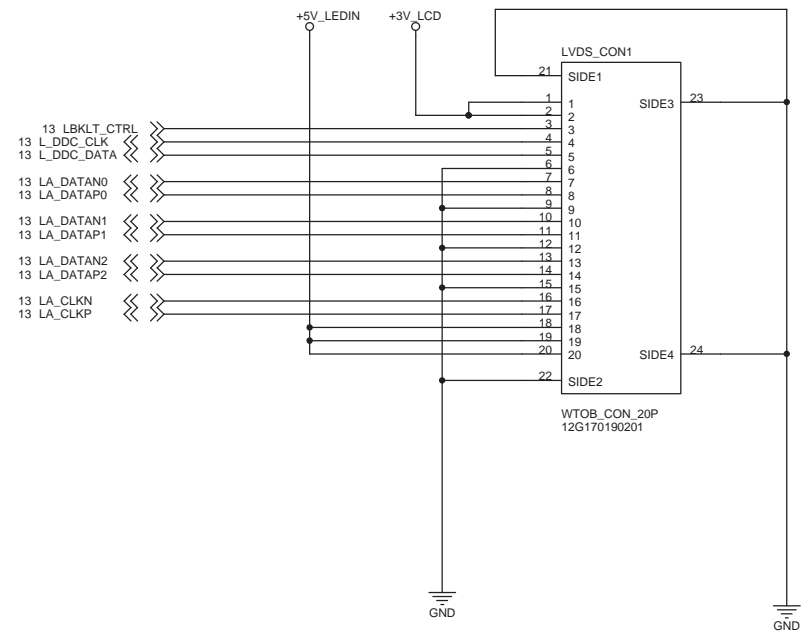
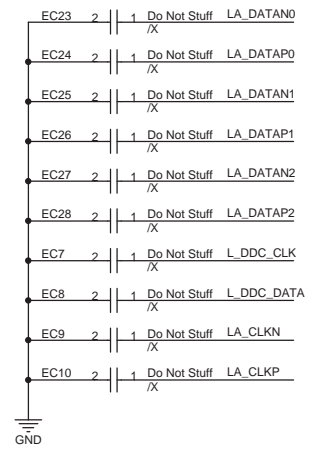


**C105 C106 for EA measurement**  
**U6 ↑: VR5 & VR6 --> 22 OHM**  
**U6 /X : VR5 & VR6 --> 0 OHM**

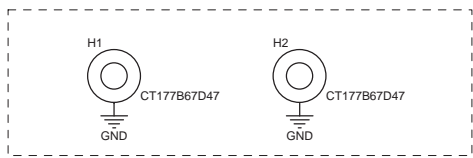
**BUS BUFFER:**  
 Unidirectional buffers (high impedance buffers) are required on both HSYNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.



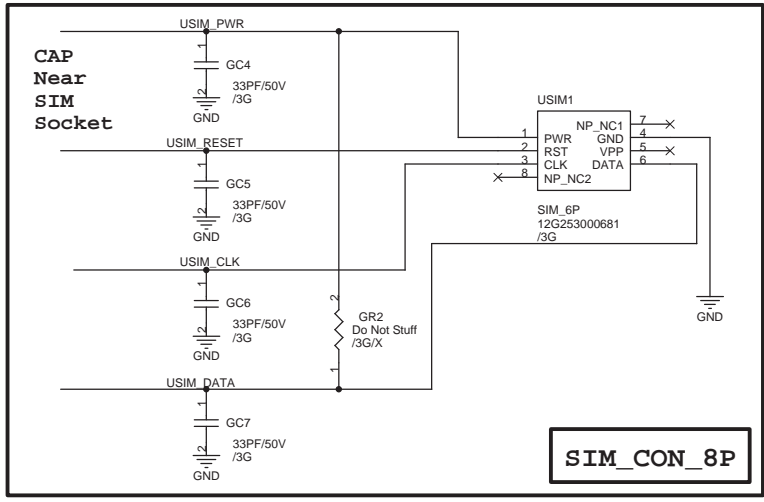
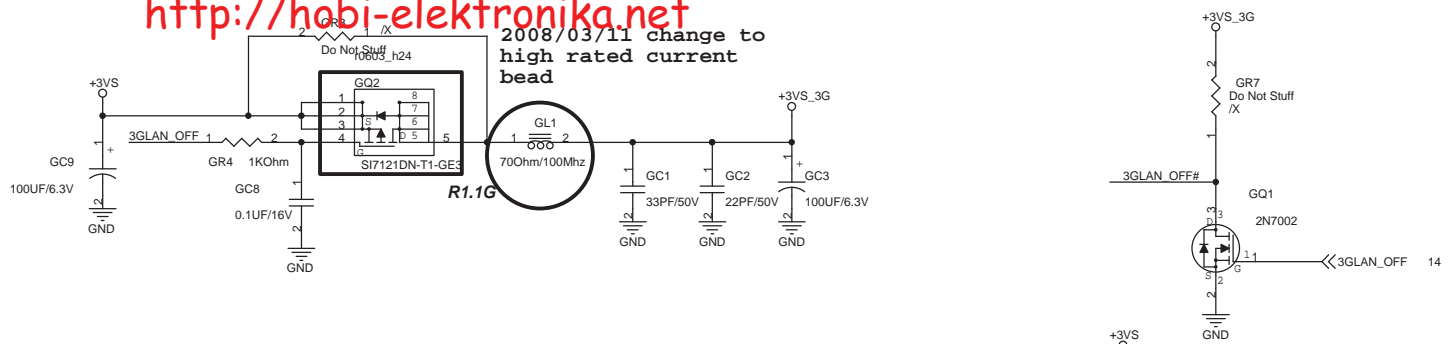
**Pin:**  
**2->6: (1A->1B)**  
**5->3: (2A->2B)**



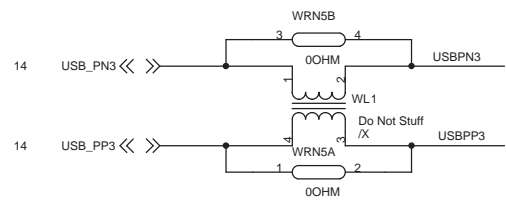
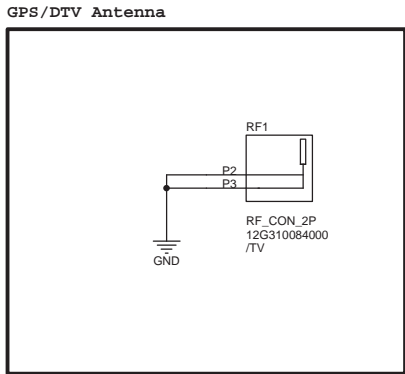
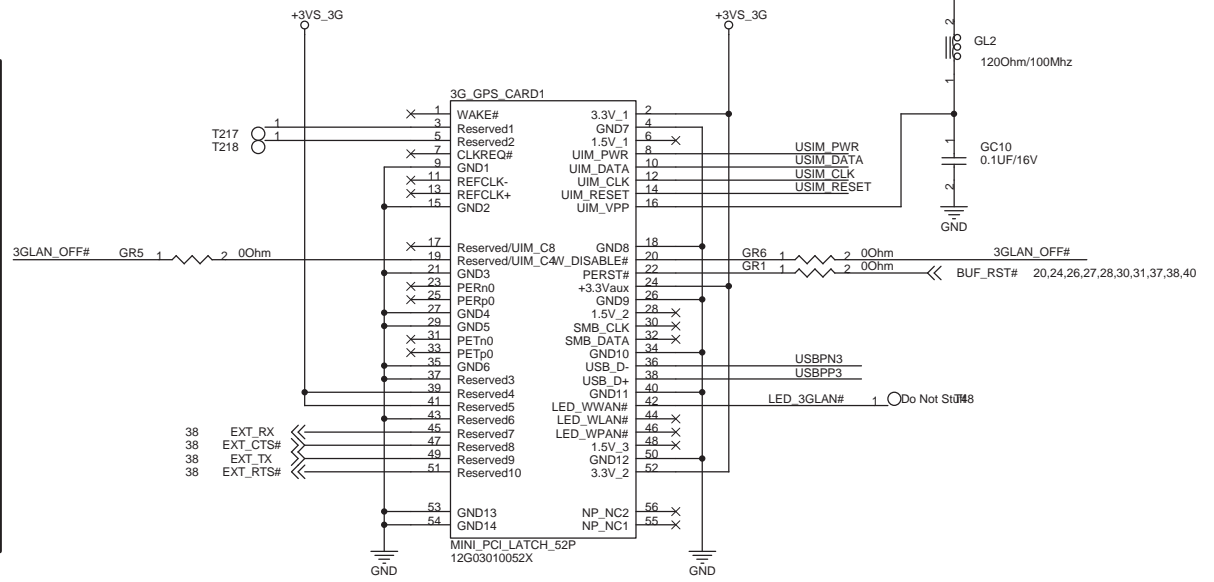
2008/03/11 change to high rated current bead

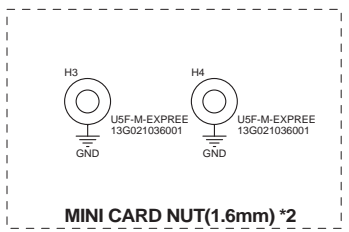
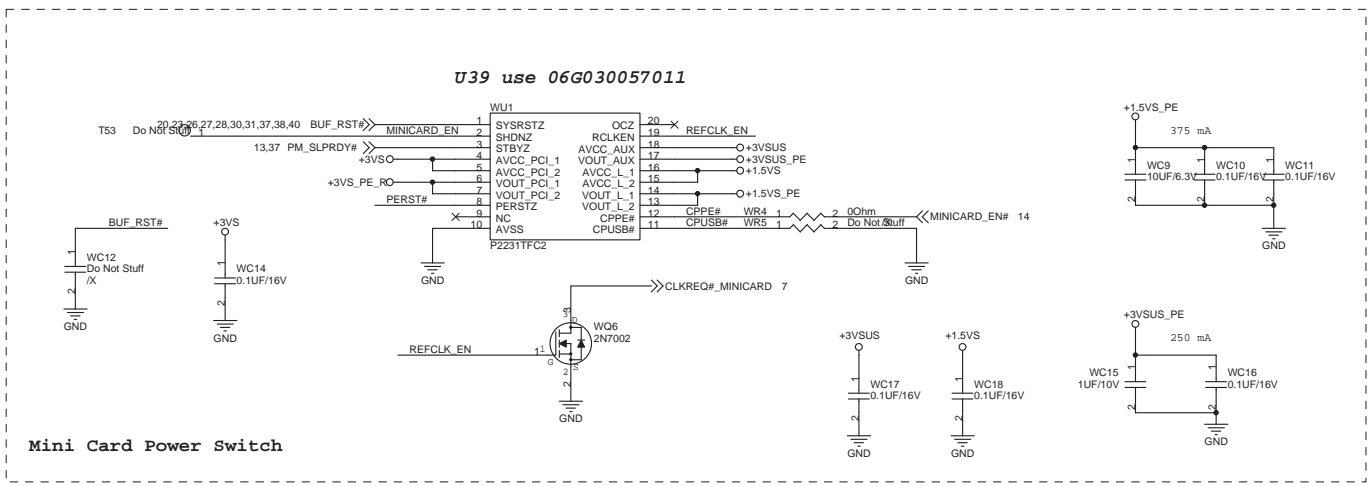
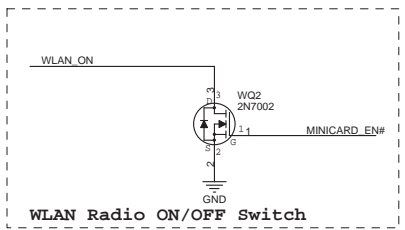
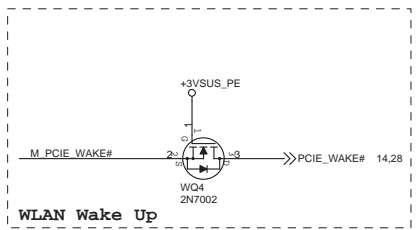
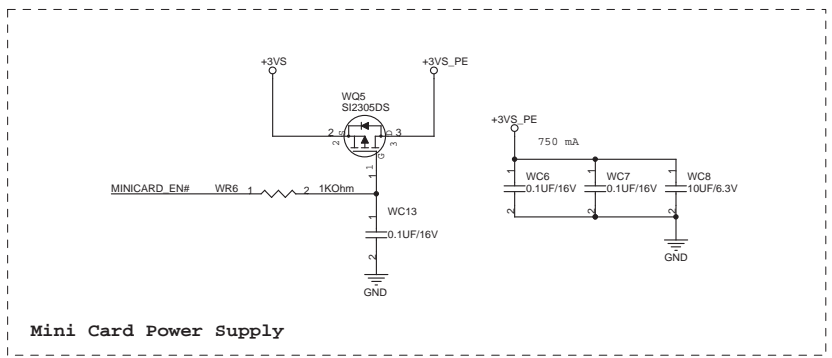
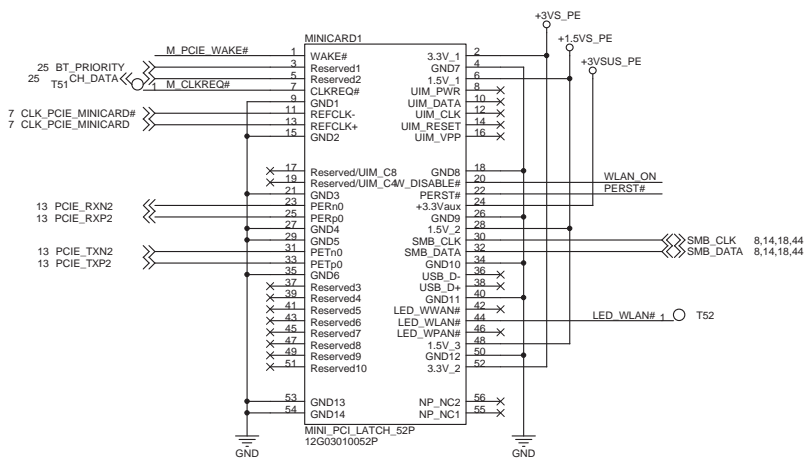


MINI CARD NUT(2.8mm) \*2

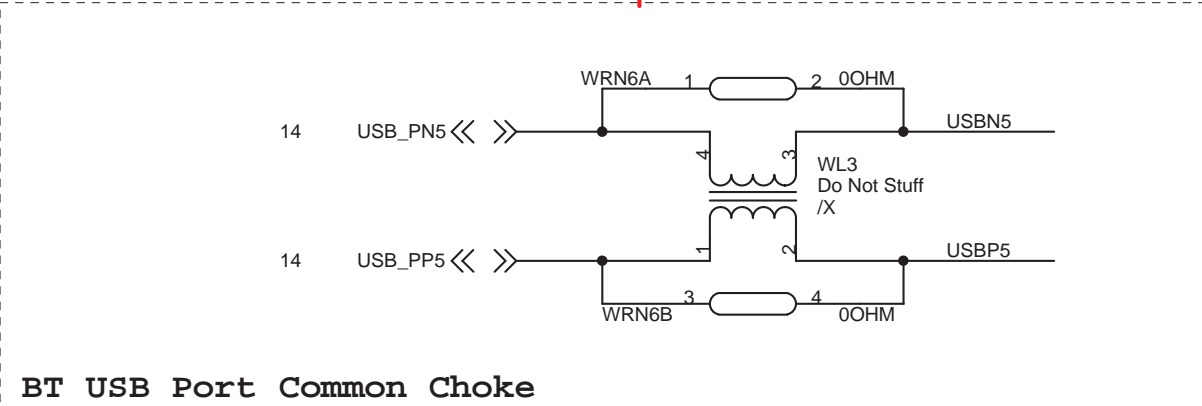


SIM\_CON\_8P

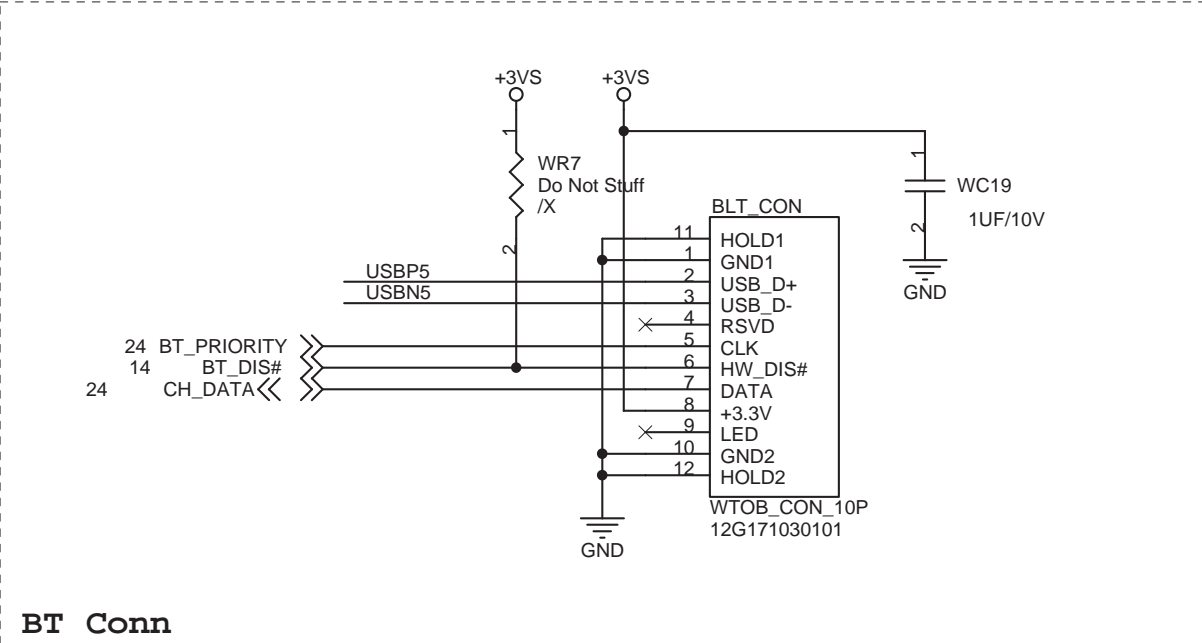








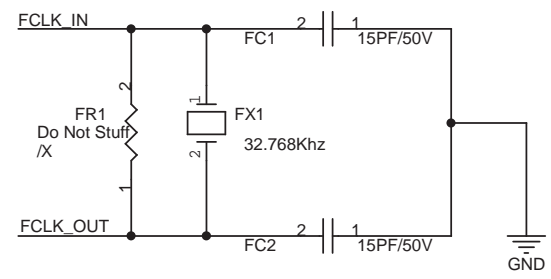
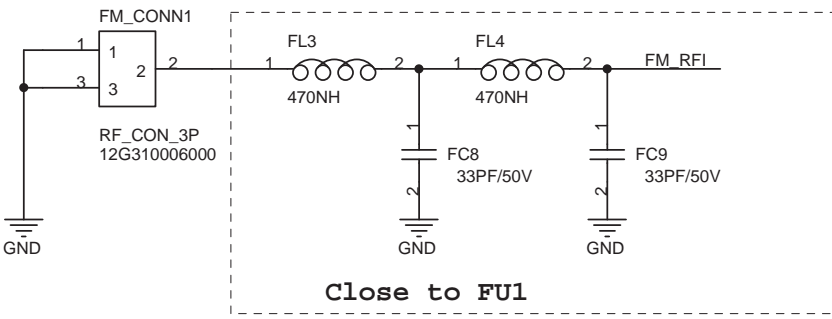
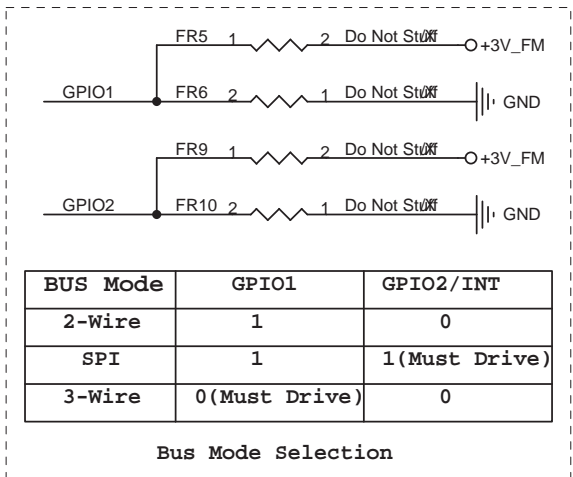
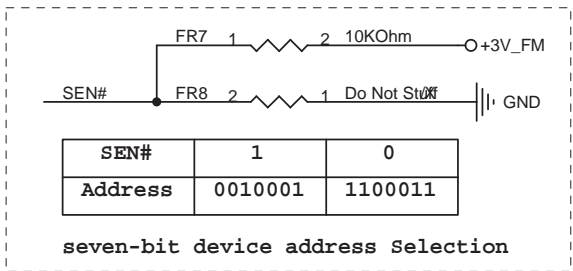
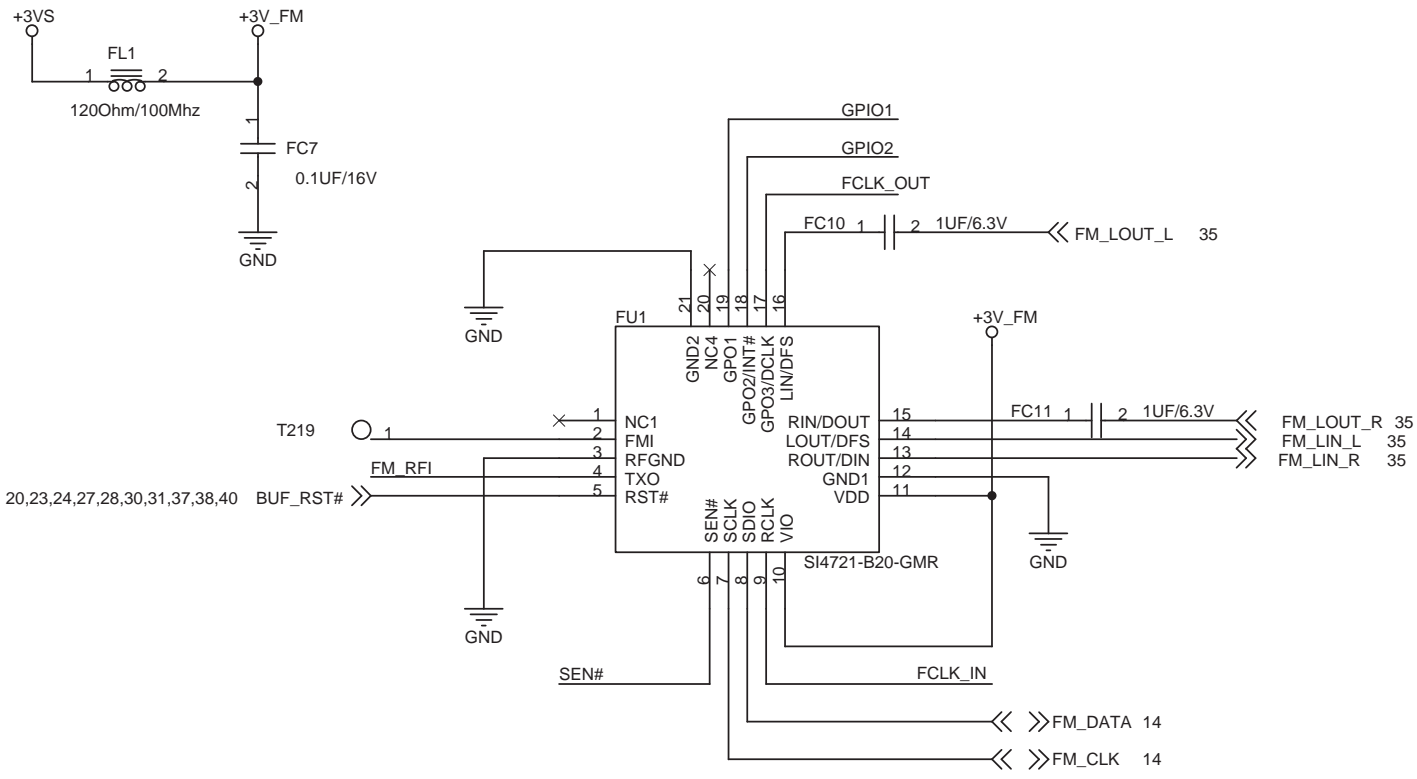
**BT USB Port Common Choke**



**BT Conn**

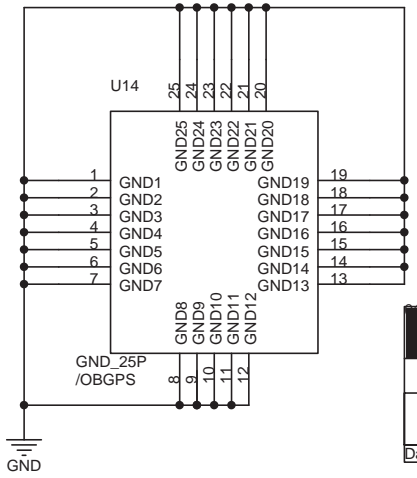
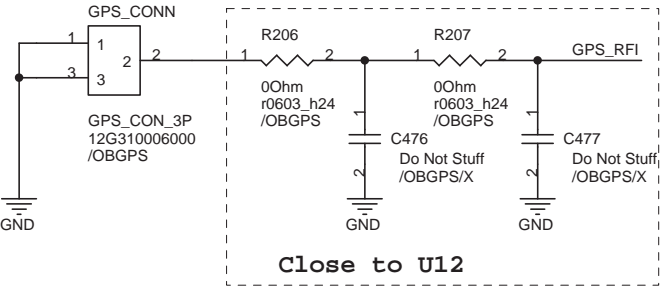
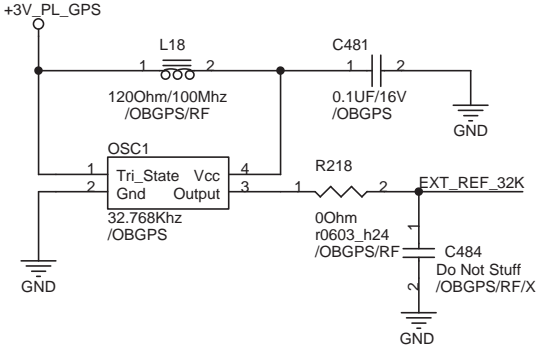
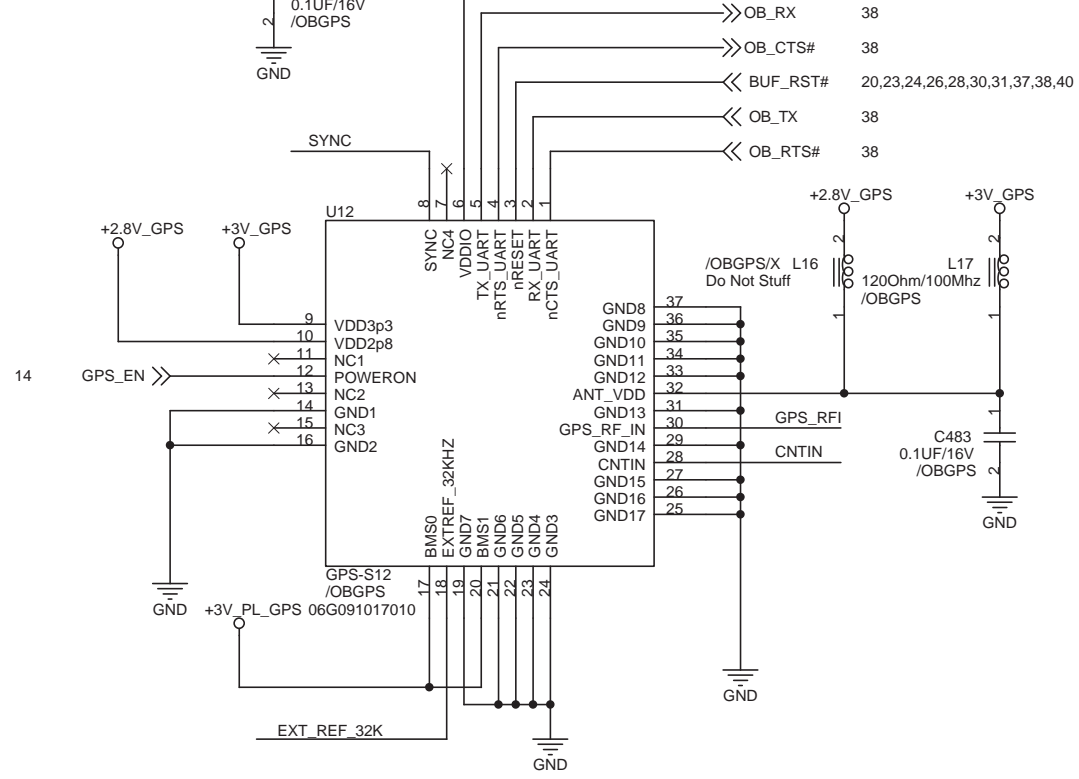
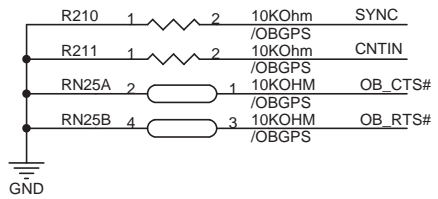
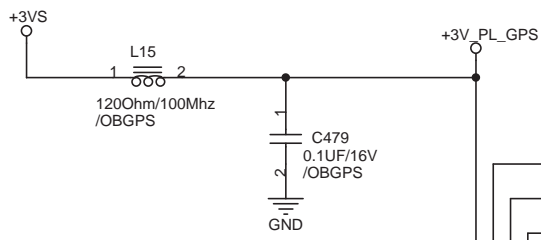
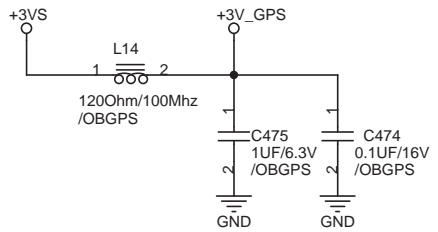
0106 1025

<b>ASUS</b>		<b>Title : Bluetooth</b>	
ASUSTek Computer INC.		<b>Engineer: Jerry Liu</b>	
Size A	Project Name <b>T91</b>		Rev 1.2G
Date: Tuesday, January 06, 2009		Sheet 25 of 57	

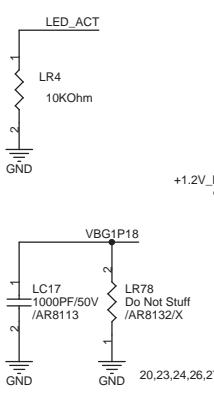
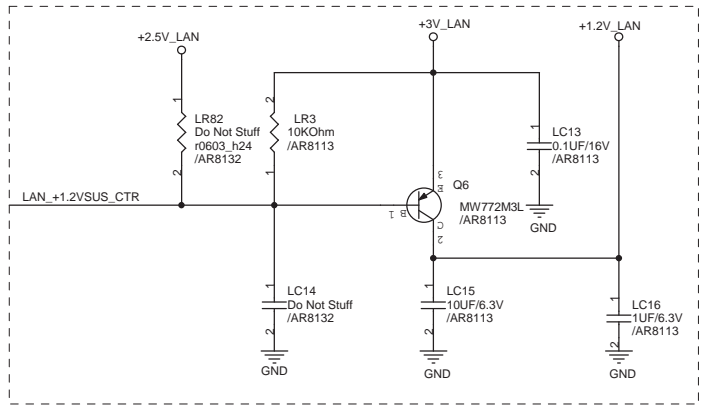
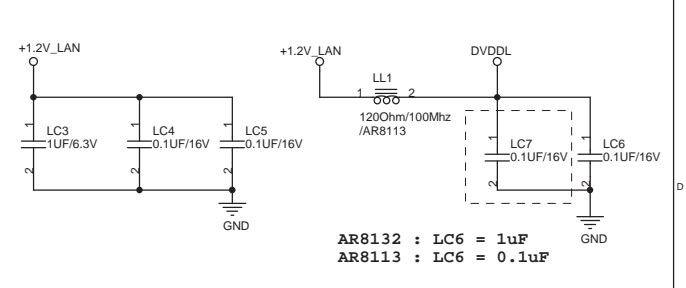
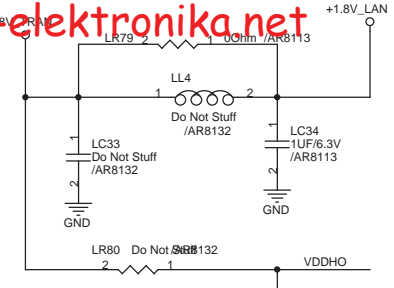
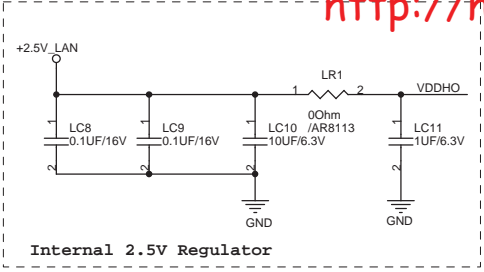
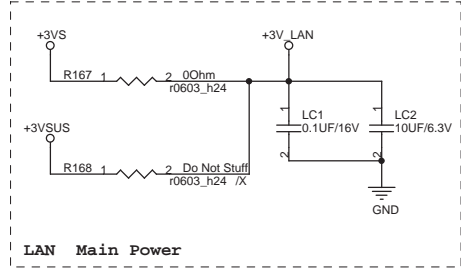


0106 1025

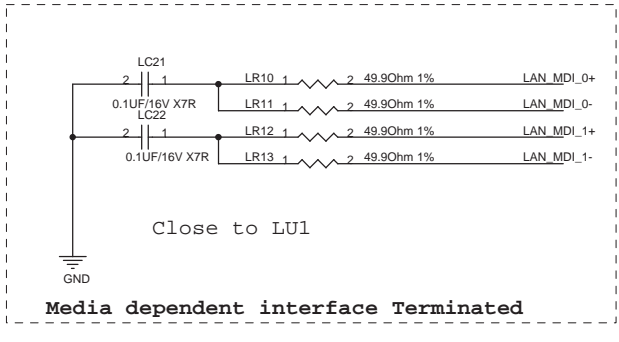
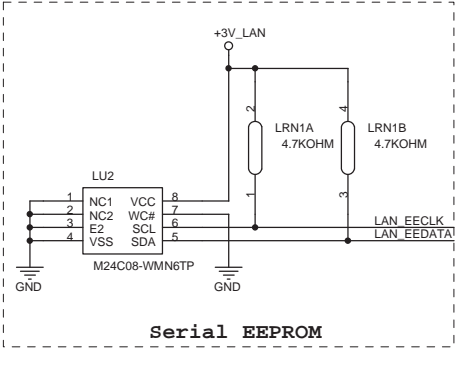
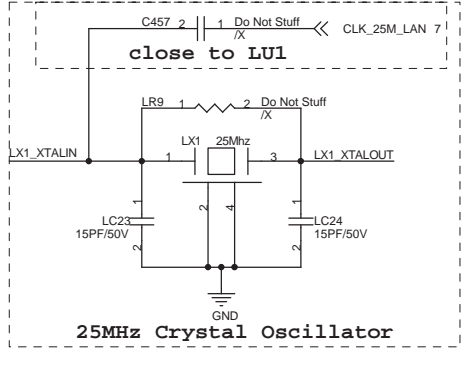
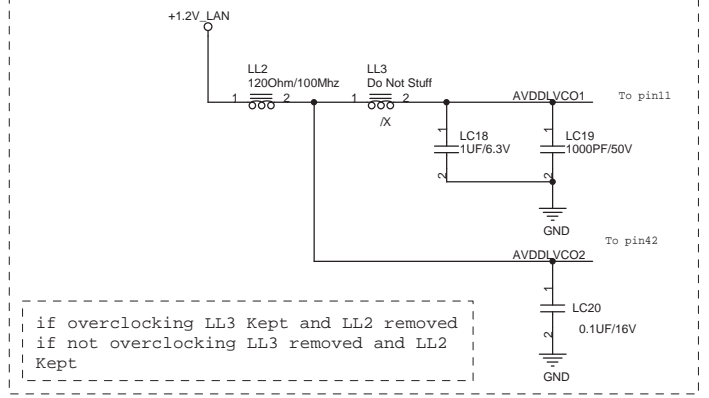
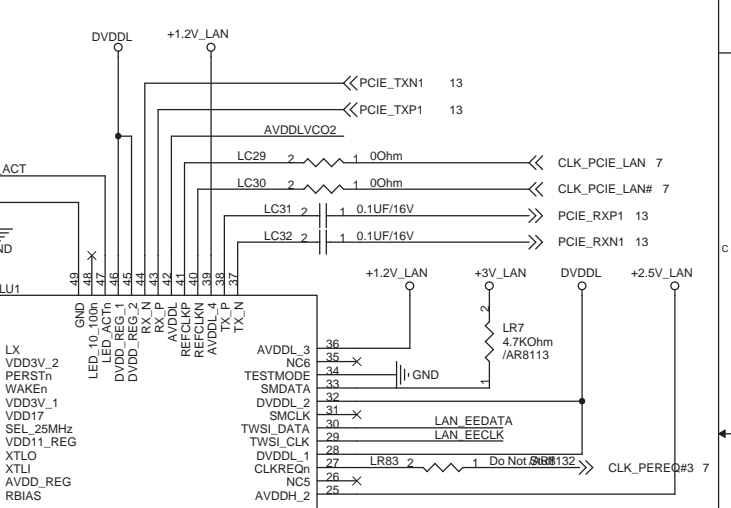
<b>ASUS</b>		<b>Title : FM RADIO</b>	
ASUSTek Computer INC.		<b>Engineer: Jerry Liu</b>	
Size A4	Project Name <b>T91</b>	Rev 1.2G	
Date: Tuesday, January 06, 2009		Sheet 26 of 57	



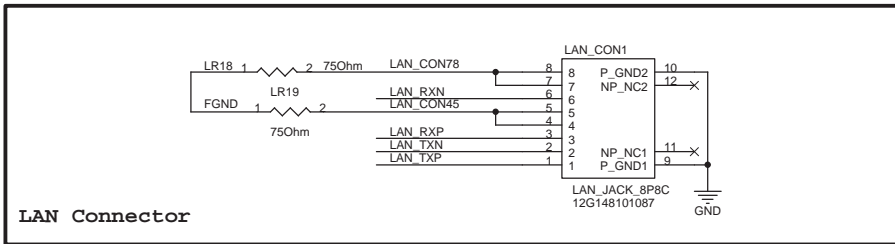
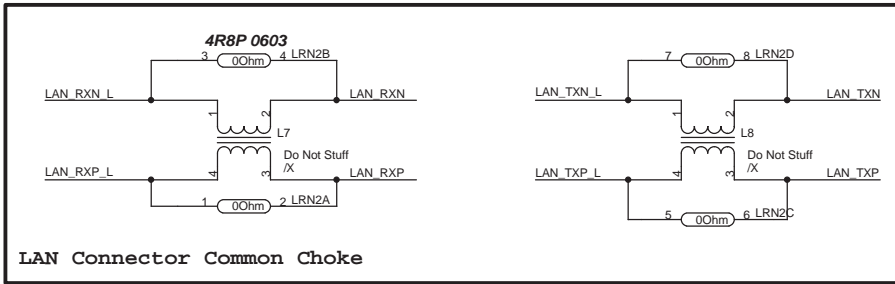
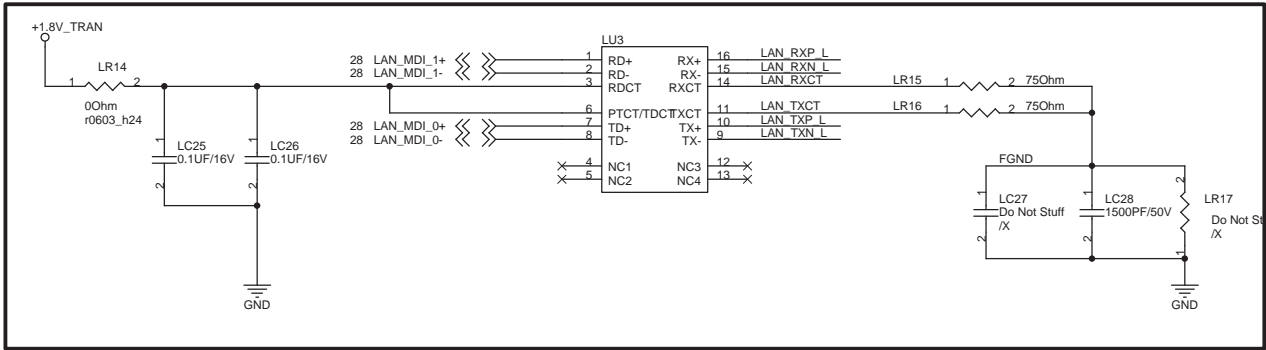
**ASUS** Title : Onboard GPS  
 ASUSTek Computer INC. Engineer: Jerry Liu  
 Size Project Name  
 Custom T91 Rev 1.2G  
 Date: Tuesday, January 06, 2009 Sheet 27 of 57

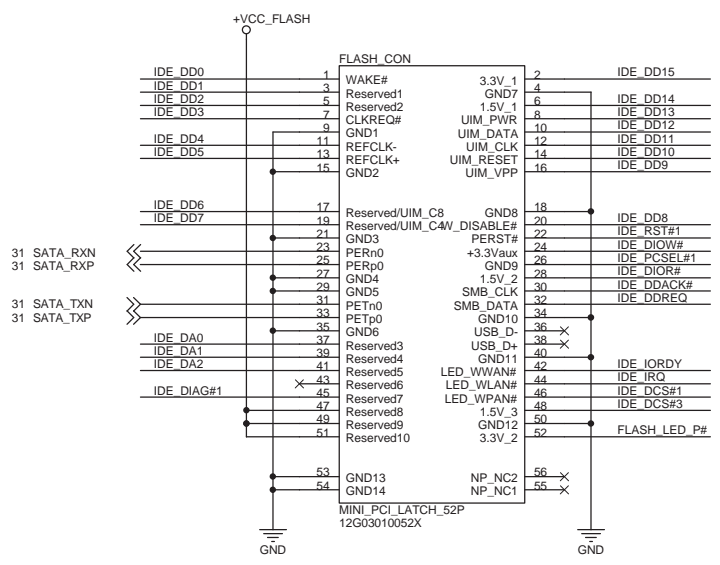
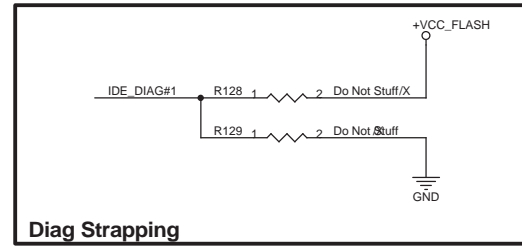
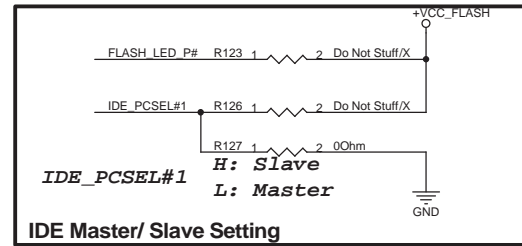
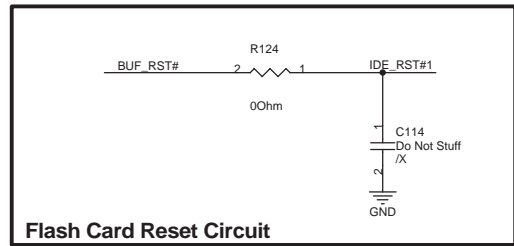
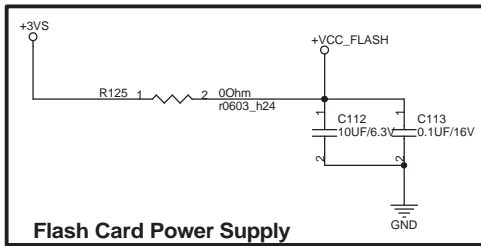


**AR8132 : LC35 = 0.1uF**  
**AR8113 : LC35 = 1uF**

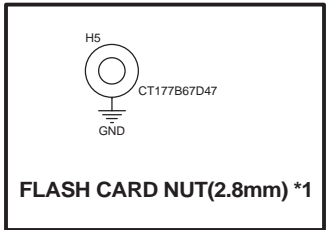


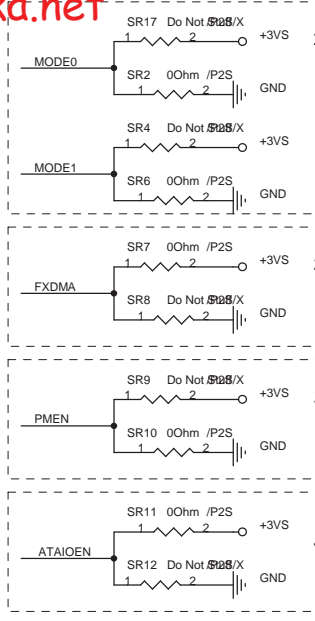
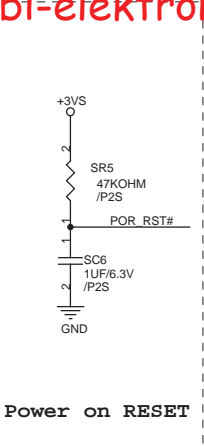
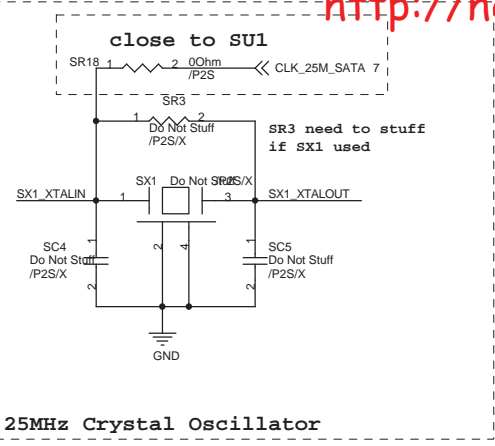
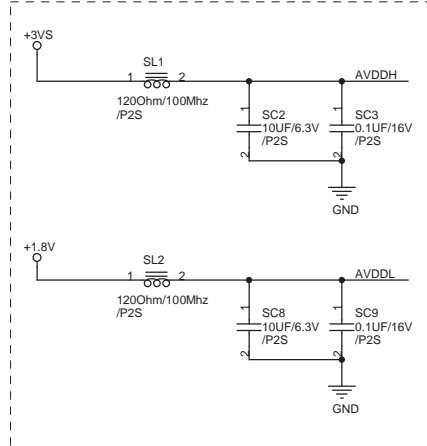
**AR8113 : 02G911002100**  
**AR8132 : 02G911002600 (Default)**





- ◀◀ IDE\_DD[15:0] 14,31
- ▶▶ IDE\_DA[2:0] 14,31
- ◀◀ IDE\_DACK# 14,31
- ▶▶ IDE\_DDREQ 14,31
- ◀◀ IDE\_DIOR# 14,31
- ▶▶ IDE\_IORDY 14,31
- ◀◀ IDE\_DCS#1 14,31
- ▶▶ IDE\_DCS#3 14,31
- ◀◀ IDE\_IRQ 14,31
- ◀◀ BUF\_RST# 20,23,24,26,27,28,31,37,38,40
- ▶▶ FLASH\_LED\_P# 31,43
- ▶▶ IDE\_DIAG#1 31





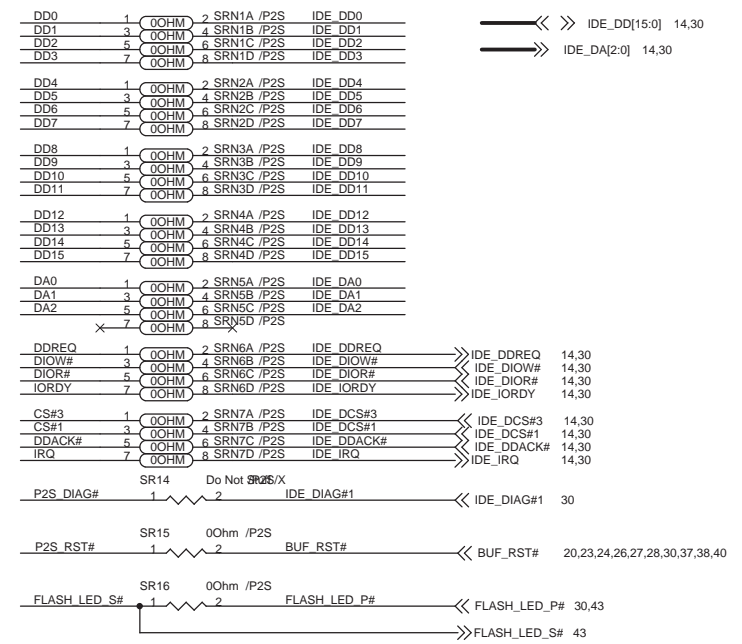
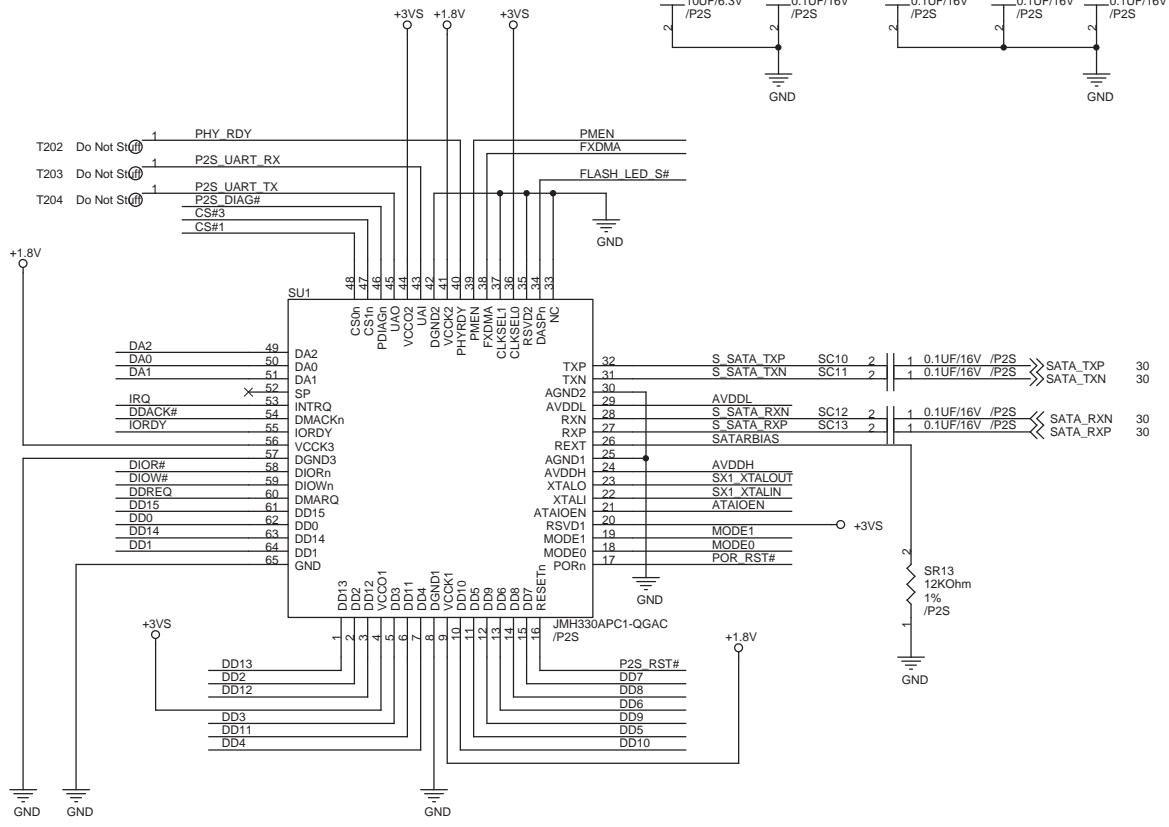
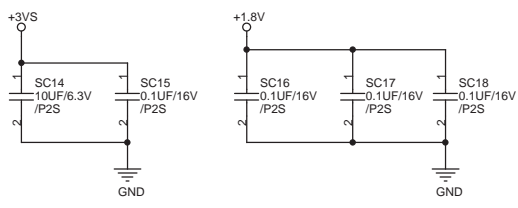
1. MODE[1:0]=Select UDMA speed when FXDMA is set  
 00:100MB/s ; 01:133MB/s  
 10:150MB/s ; 11:Reserved

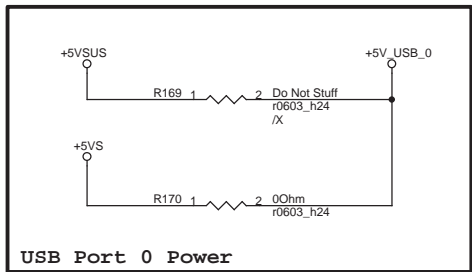
2. FXDMA=0, Auto adjustable speed rate according set Feature Command  
 FXDMA=1, speed rate depend on Mode[1:0] setting

3. PMEN=0 power management function Disable  
 PMEN=1 power management function Enable

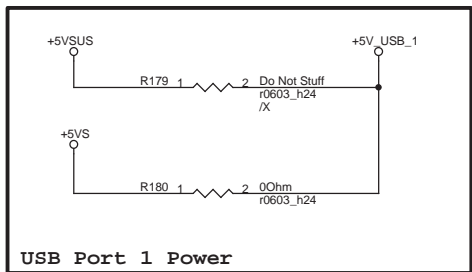
4. ATAIOEN=0, Disable the ATA output pins, ATA I/O output pins are Hi-Z.  
 ATAIOEN=1, Enable ATA output

JMH330 only simulate PATA as Device 0

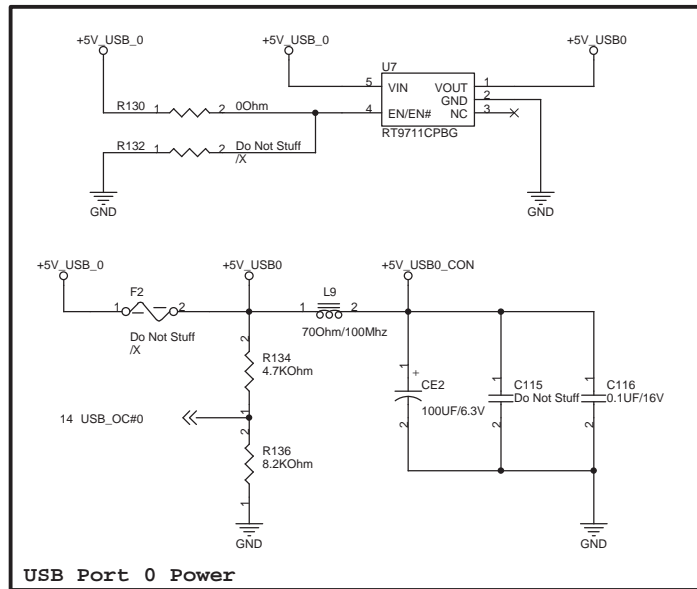




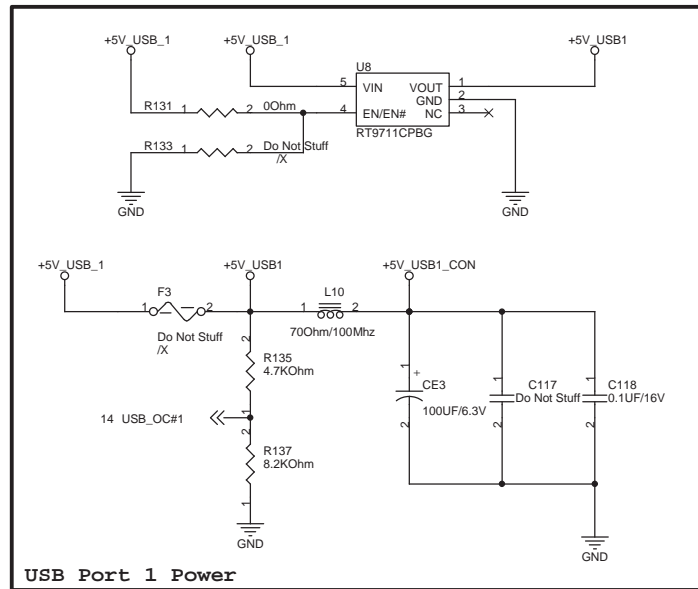
USB Port 0 Power



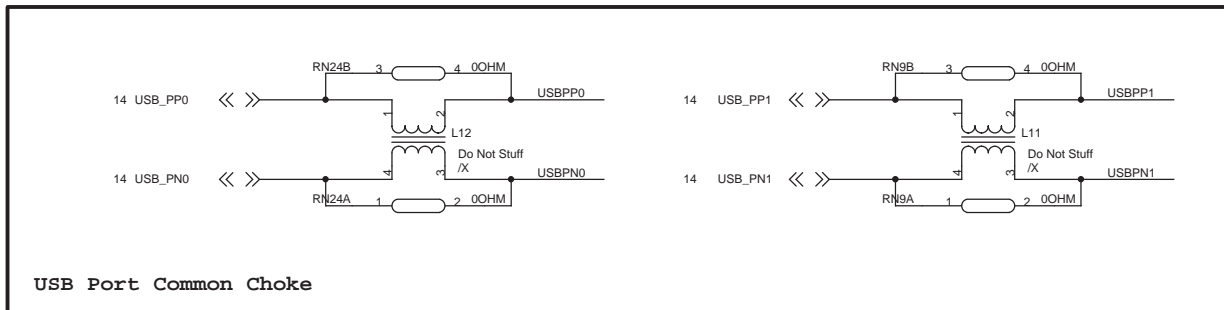
USB Port 1 Power



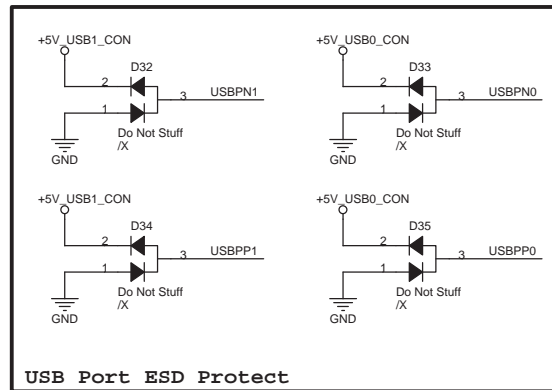
USB Port 0 Power



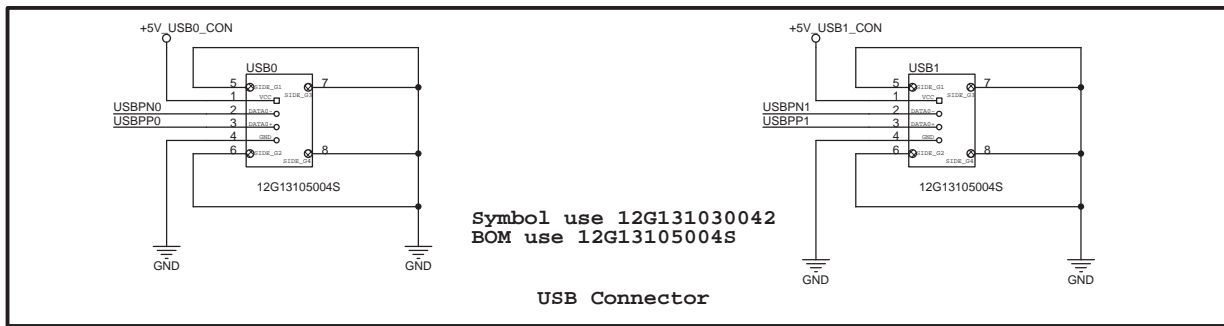
USB Port 1 Power



USB Port Common Choke



USB Port ESD Protect



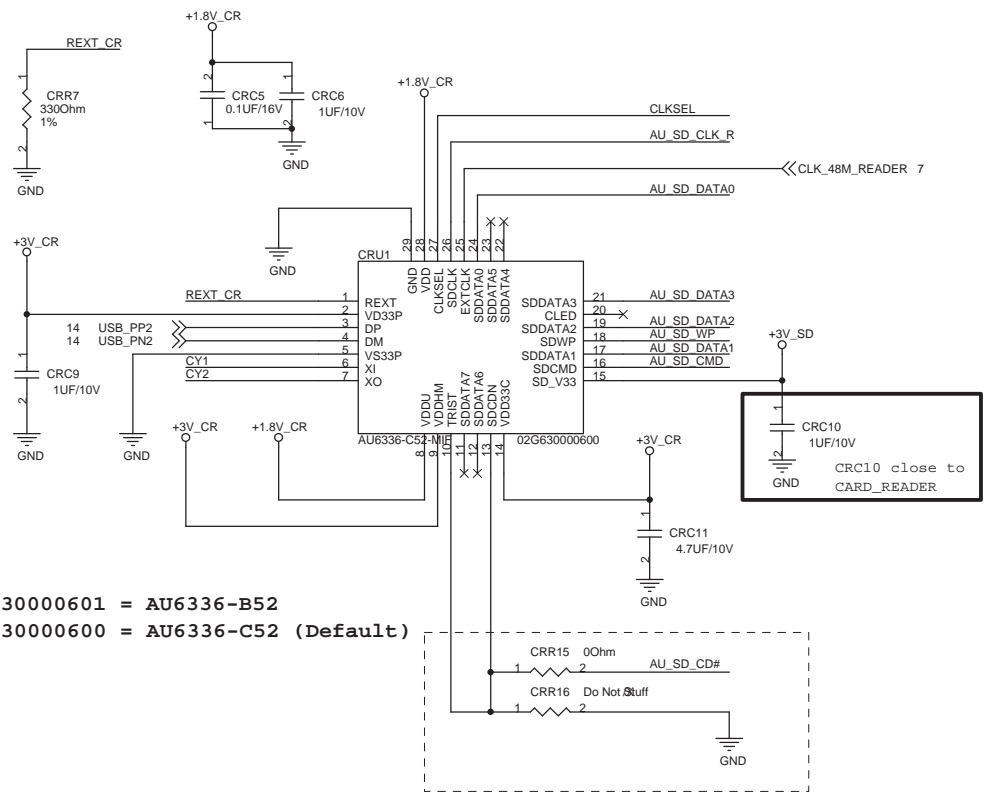
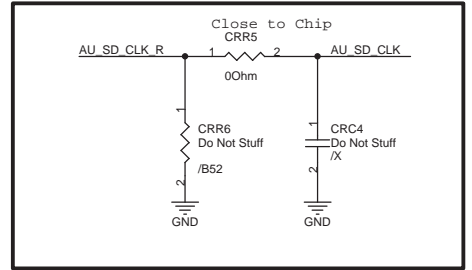
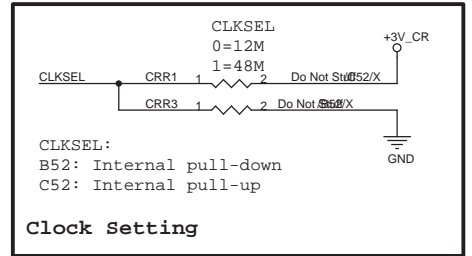
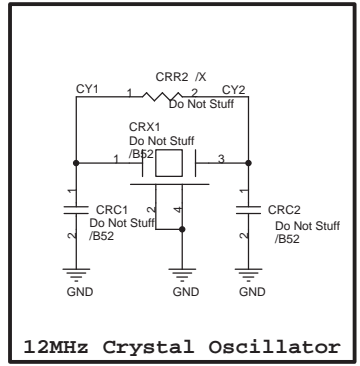
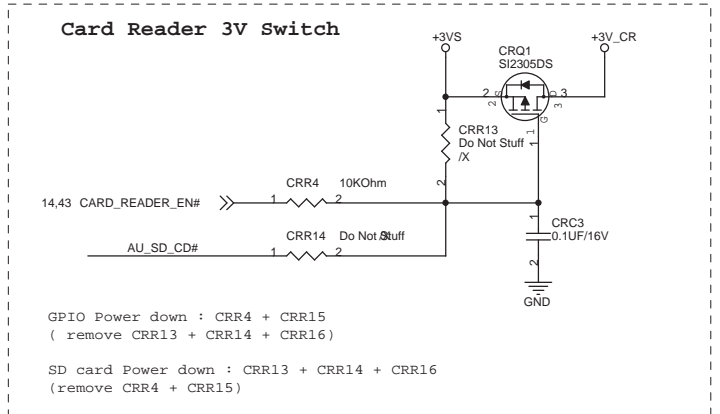
Symbol use 12G131030042  
BOM use 12G13105004S

USB Connector

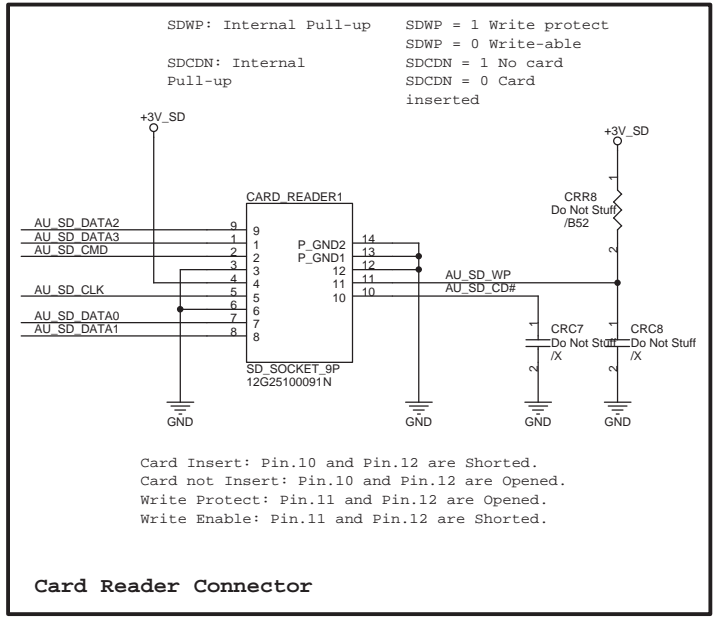
0106 1025

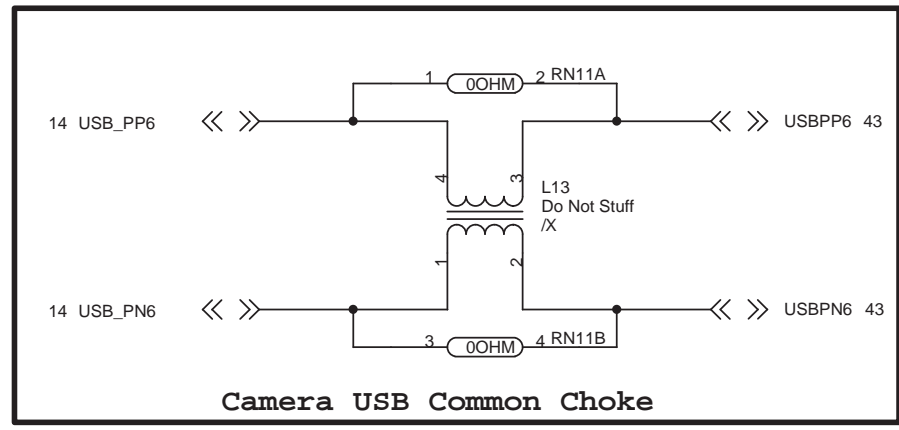
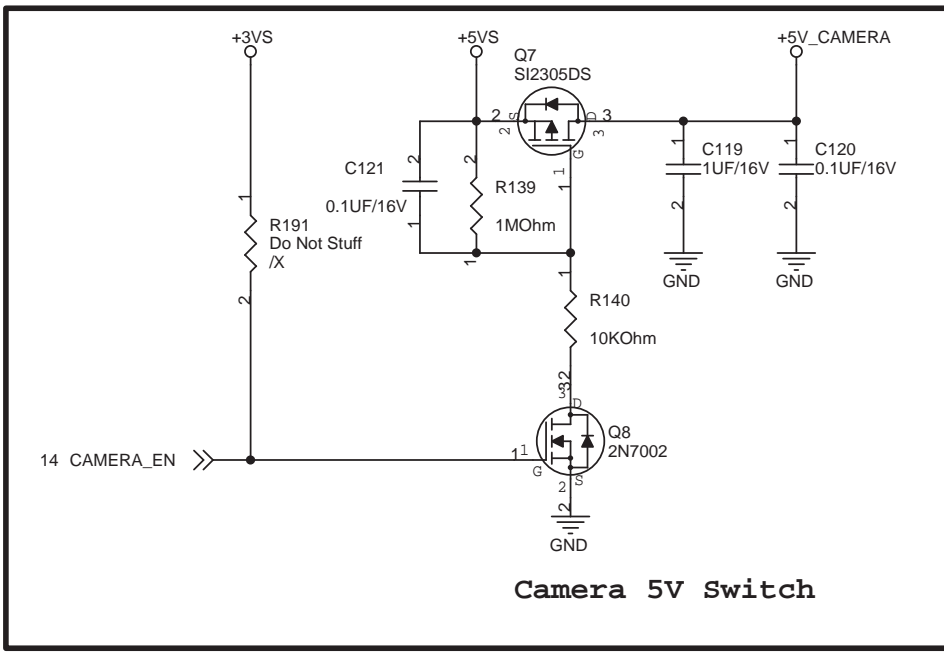
<b>ASUS</b>		<b>Title : USB Port</b>	
ASUSTek Computer INC.		<b>Engineer: Jerry Liu</b>	
Size	Project Name		Rev
A3	<b>T91</b>		1.2G
Date: Tuesday, January 06, 2009	Sheet	32 of 57	





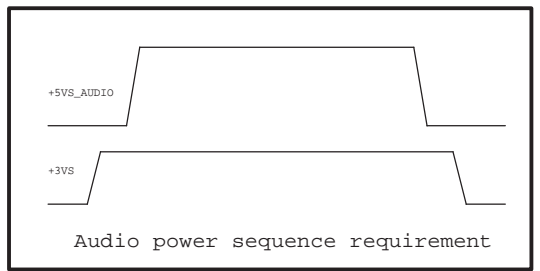
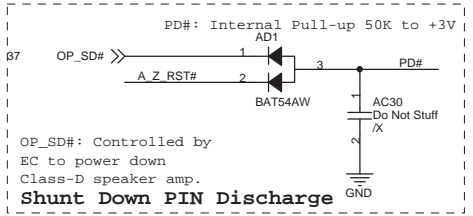
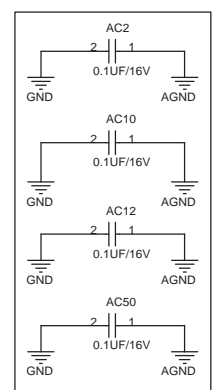
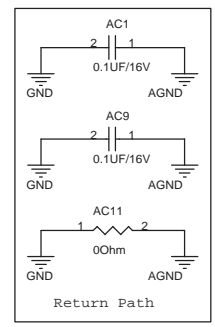
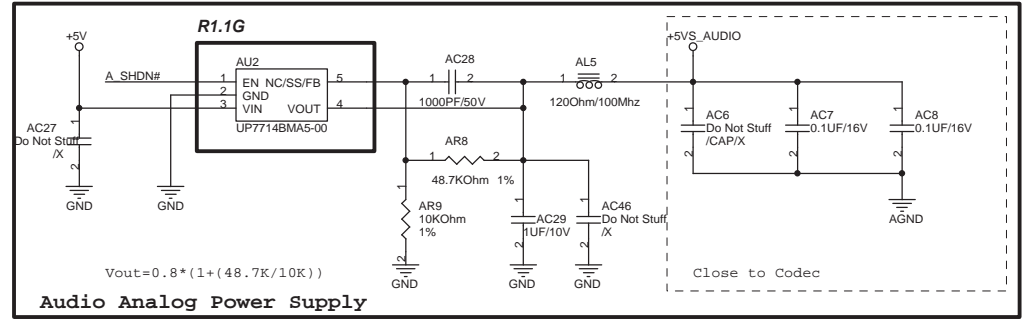
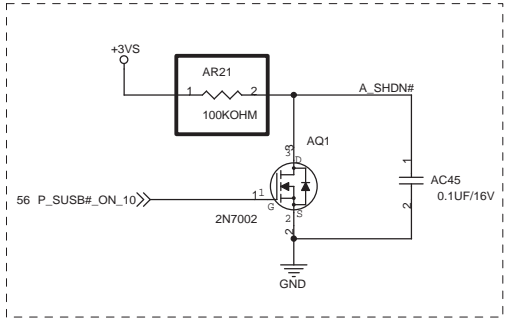
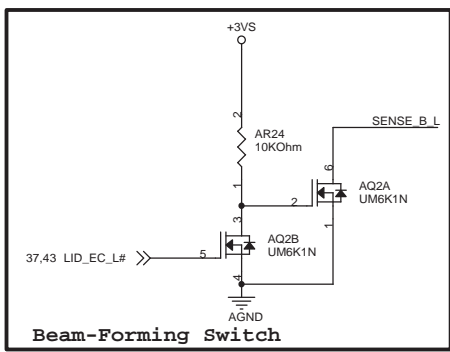
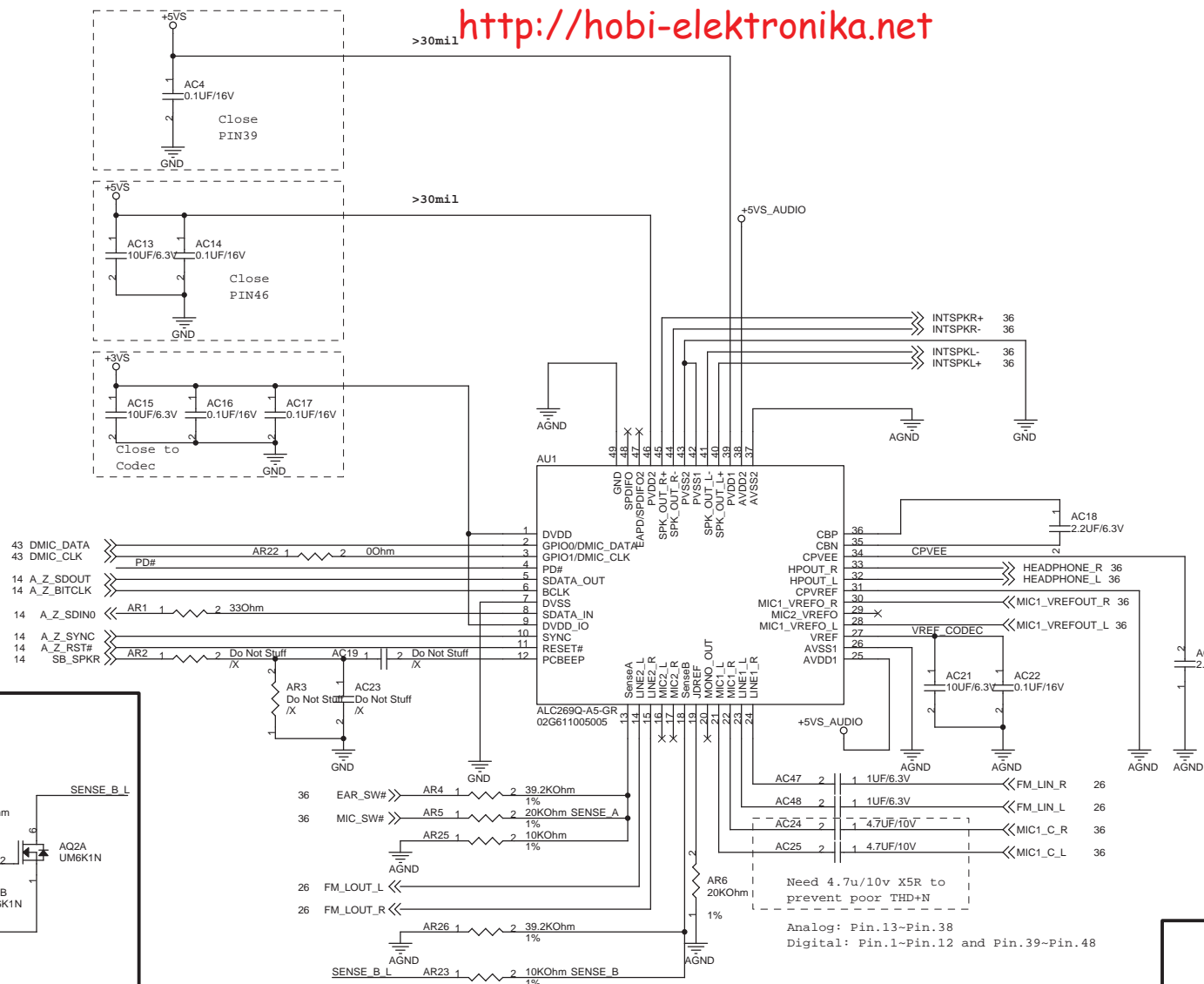
02G63000601 = AU6336-B52  
02G63000600 = AU6336-C52 (Default)

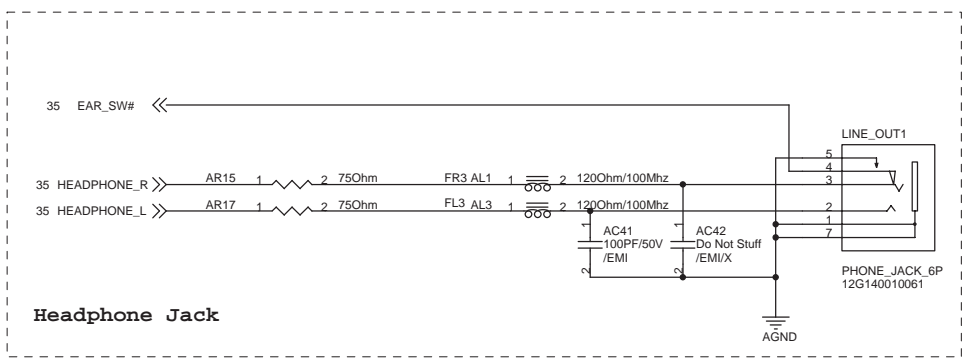
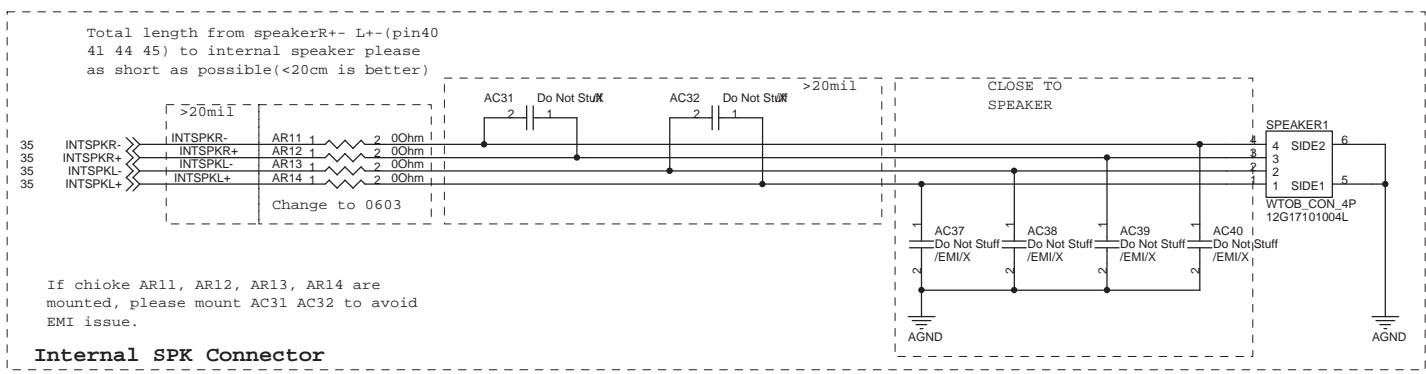




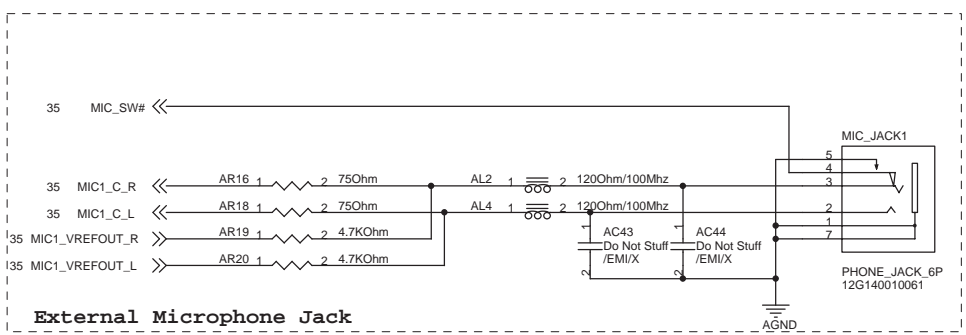
0106 1025

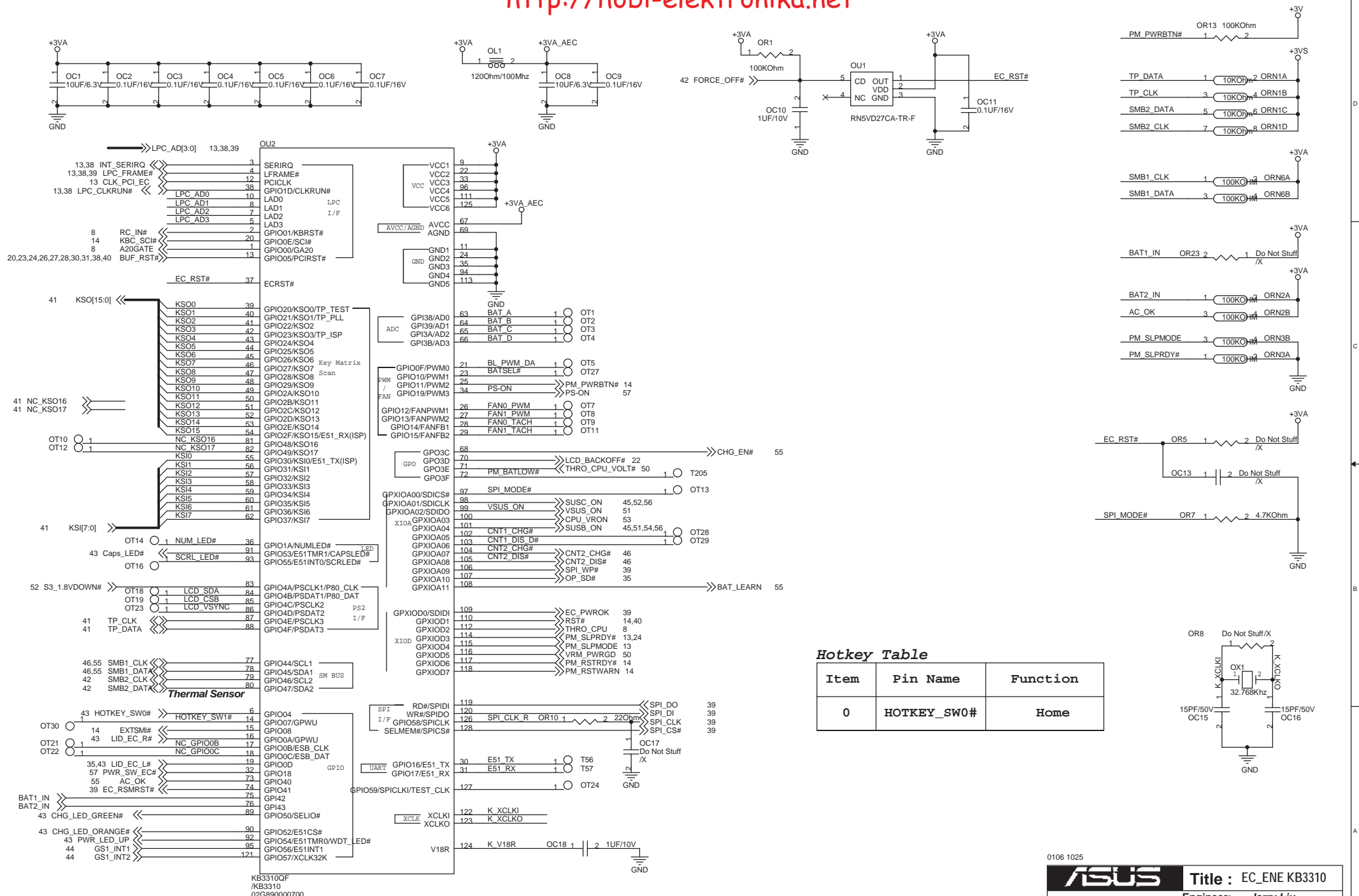
<b>ASUS</b>		<b>Title : Camera Conn</b>	
ASUSTek Computer INC.		<b>Engineer: Jerry Liu</b>	
Size A4	Project Name <b>T91</b>	Date: Tuesday, January 06, 2009	Rev 1.2G
Date: Tuesday, January 06, 2009		Sheet 34	of 57





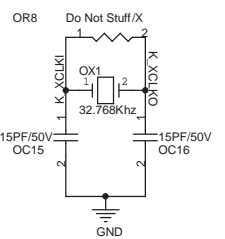
Symbol use 12G140010060  
 BOM use 12G140010061





Hotkey Table

Item	Pin Name	Function
0	HOTKEY_SW0#	Home



HOTKEY\_SW0# - HOTKEY\_SW3# internal PU

0106 1025

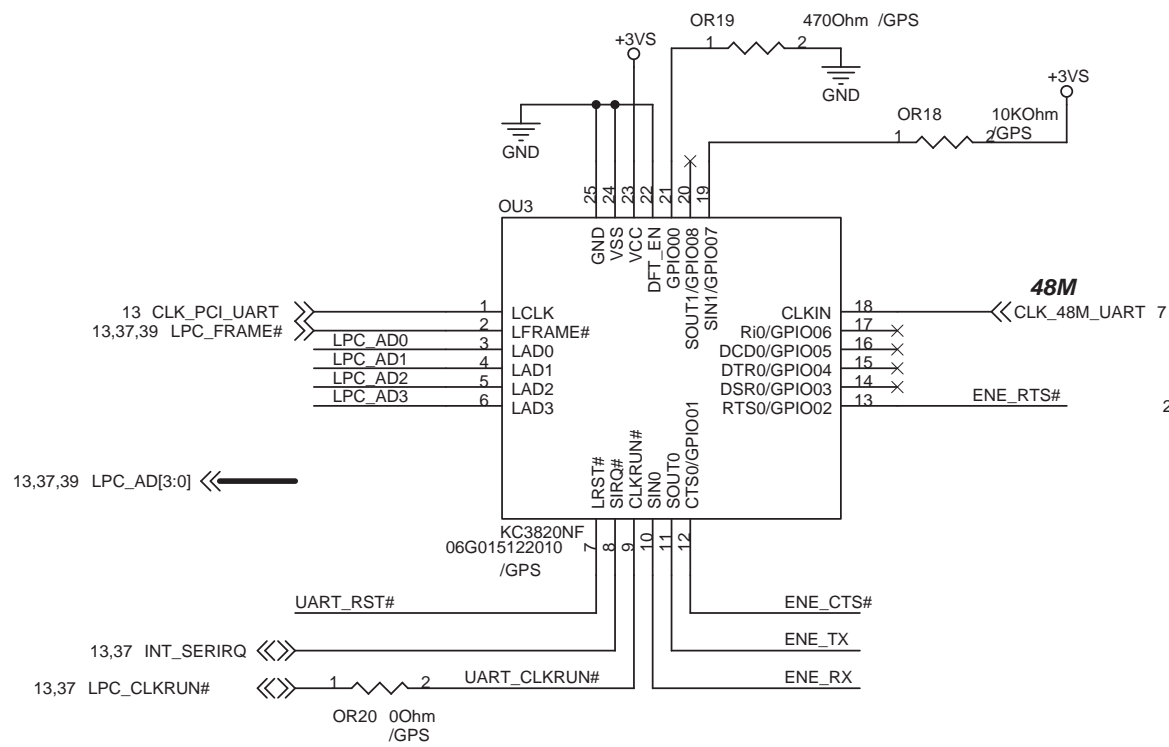
**ASUS** Title : EC\_ENE KB3310

ASUSTek Computer INC. Engineer: Jerry Liu

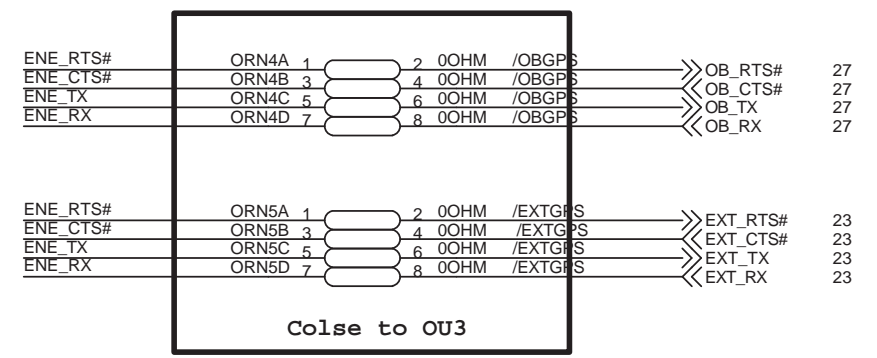
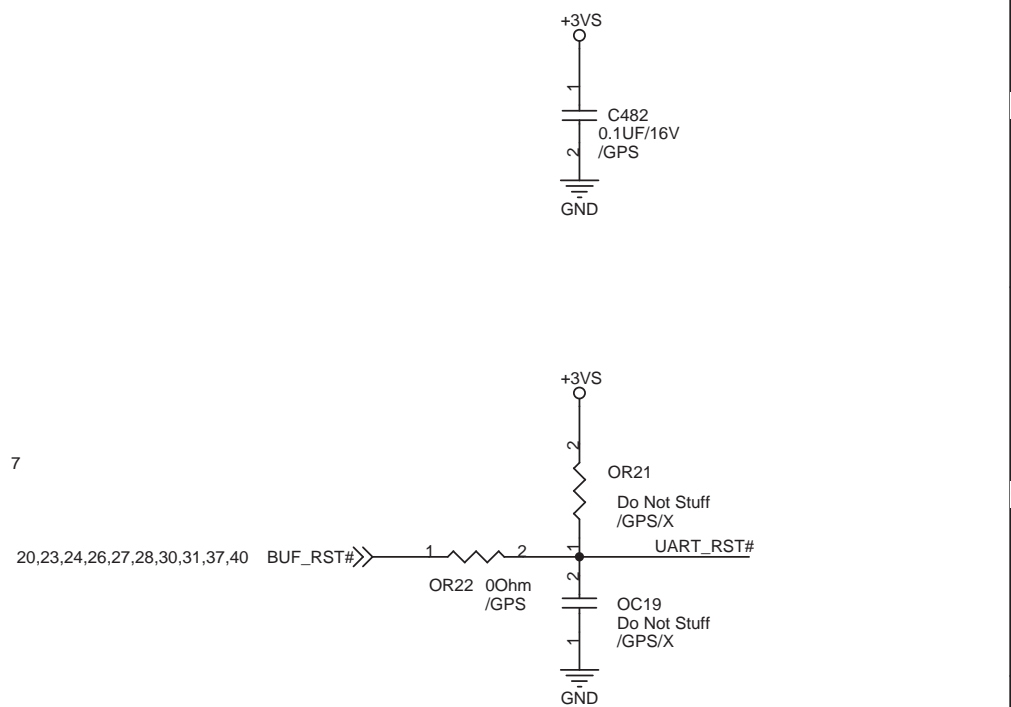
Size	Project Name	Rev
A3	T91	1.2G

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**GPIO00**  
**Hardware strap(internal pull-high)**  
**Low:4E 4F**  
**High:2E 2F**



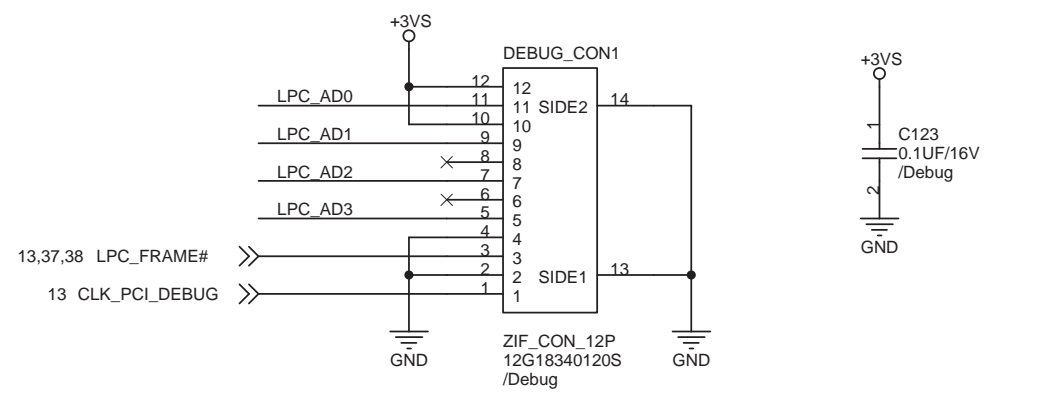
**UART Control IC for using GPS module  
 due to no UART on ENE EC**



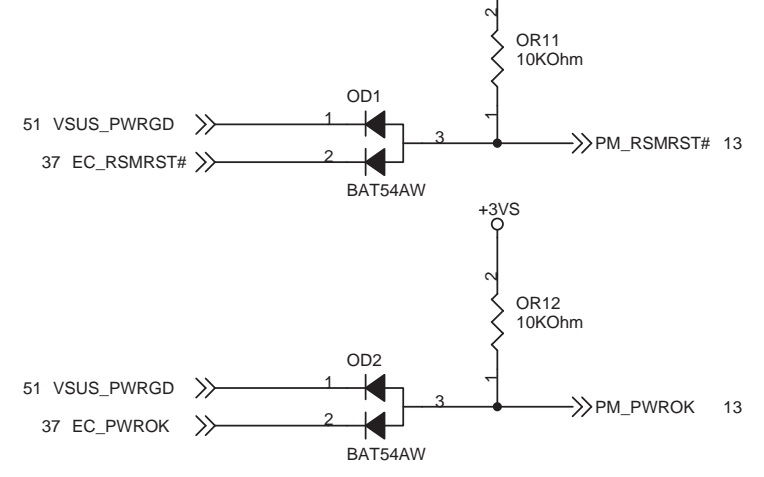
0106 1025

<b>ASUS</b>		<b>Title : EC_UART_KC3820</b>	
ASUSTek Computer INC.		<b>Engineer: Jerry_Liu</b>	
Size A4	Project Name <b>T91</b>	Rev 1.2G	
Date: Tuesday, January 06, 2009		Sheet 38 of 57	

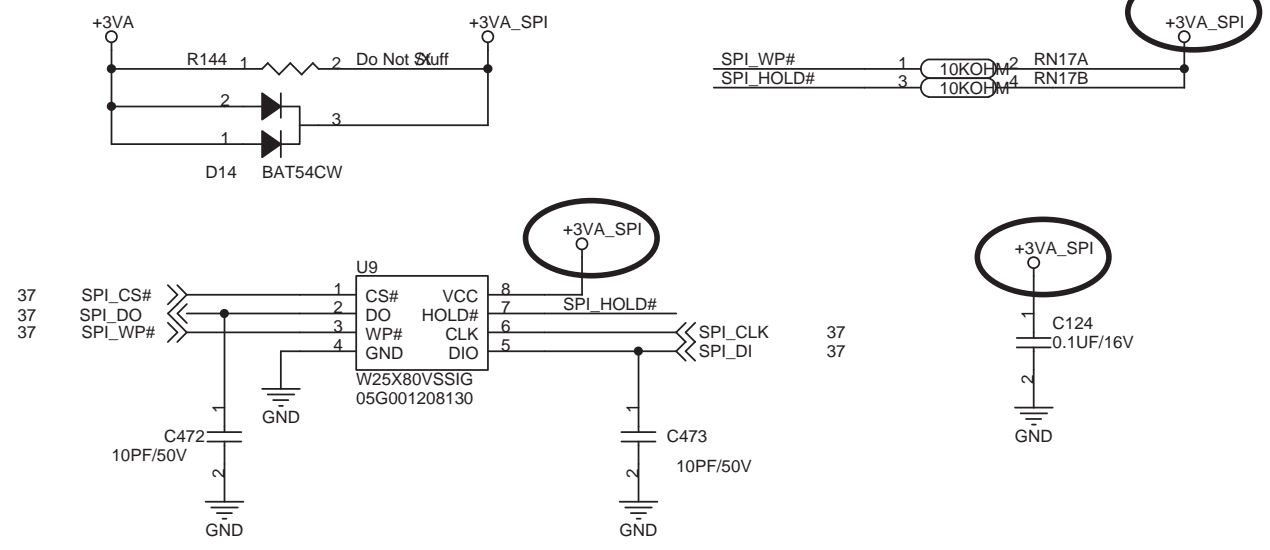
**For Debug**



**Resolve auto-boot issue**

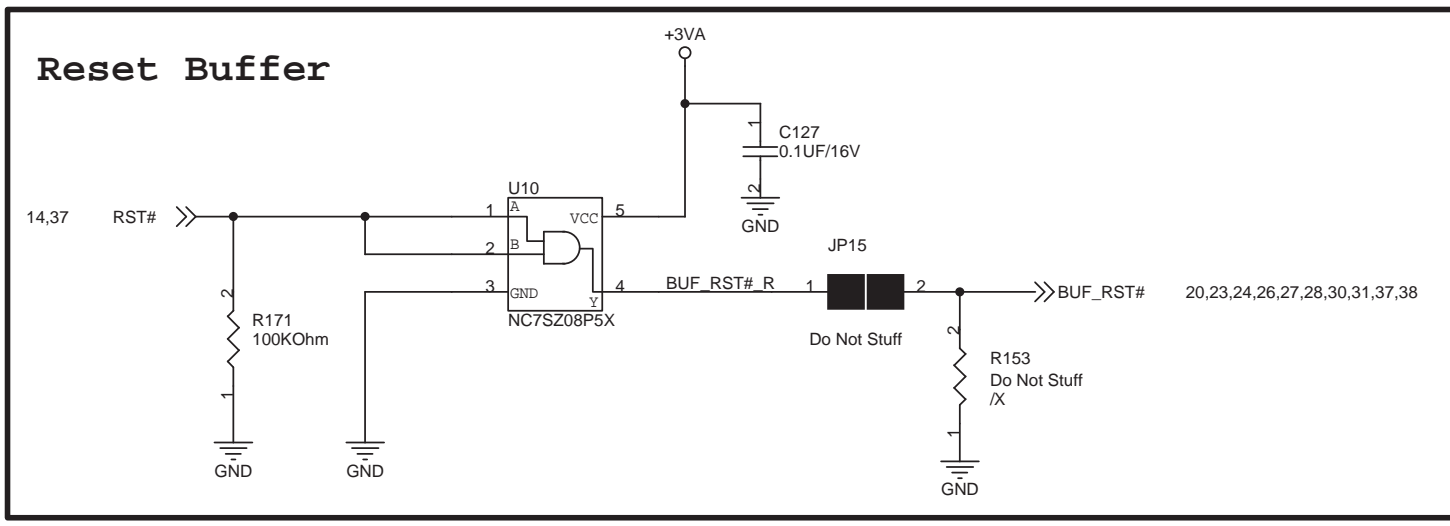
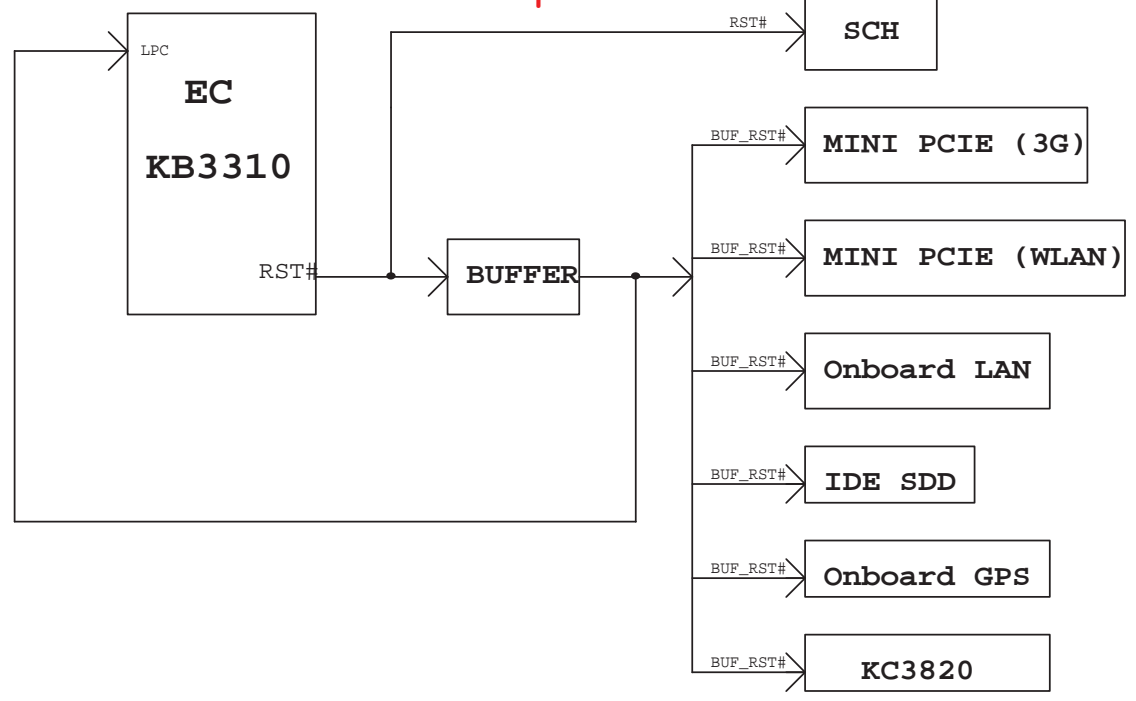


**SPI ROM**



0106 1025

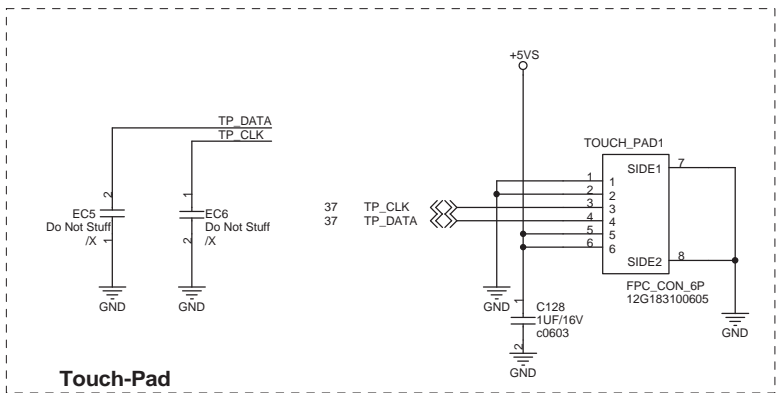
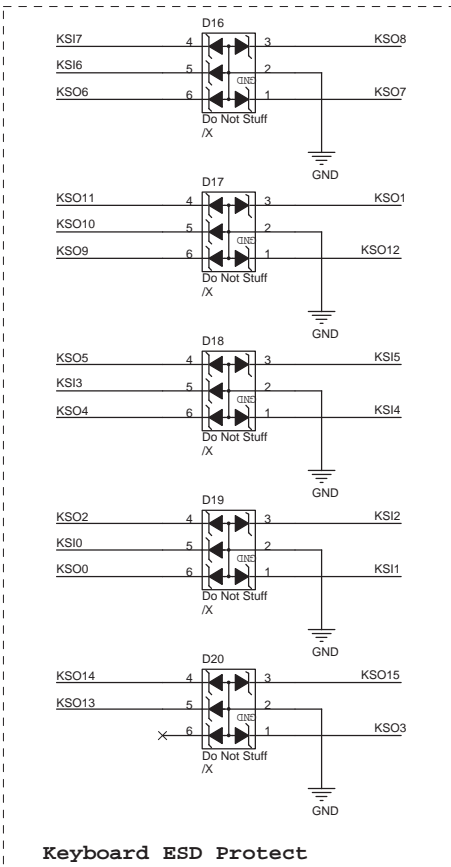
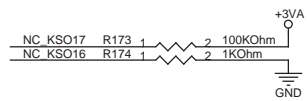
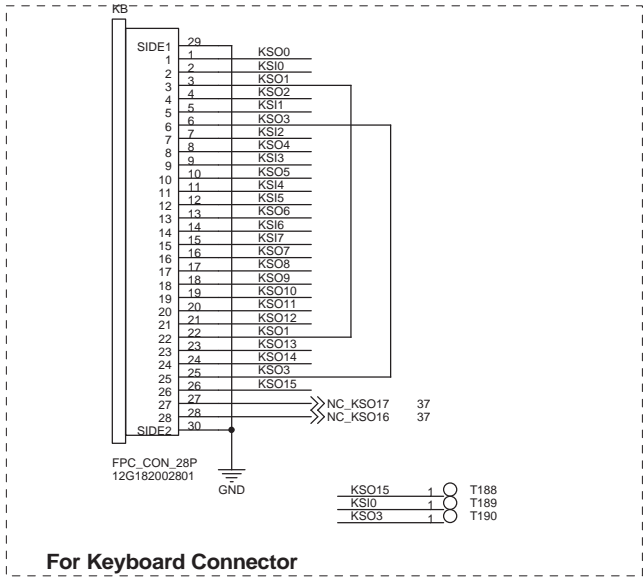
<b>ASUS</b>		<b>Title : SPI ROM/ Debug</b>	
ASUSTek Computer INC.		<b>Engineer: Jerry Liu</b>	
Size A4	Project Name <b>T91</b>	Rev 1.2G	
Date: Tuesday, January 06, 2009		Sheet 39 of 57	

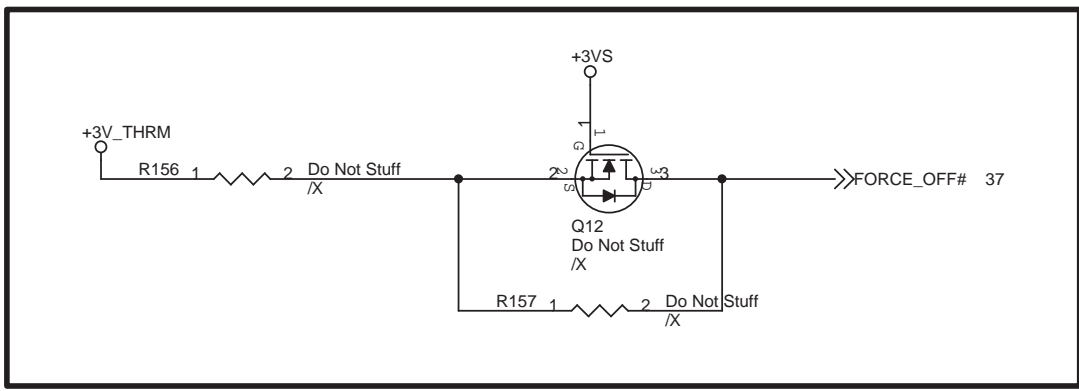
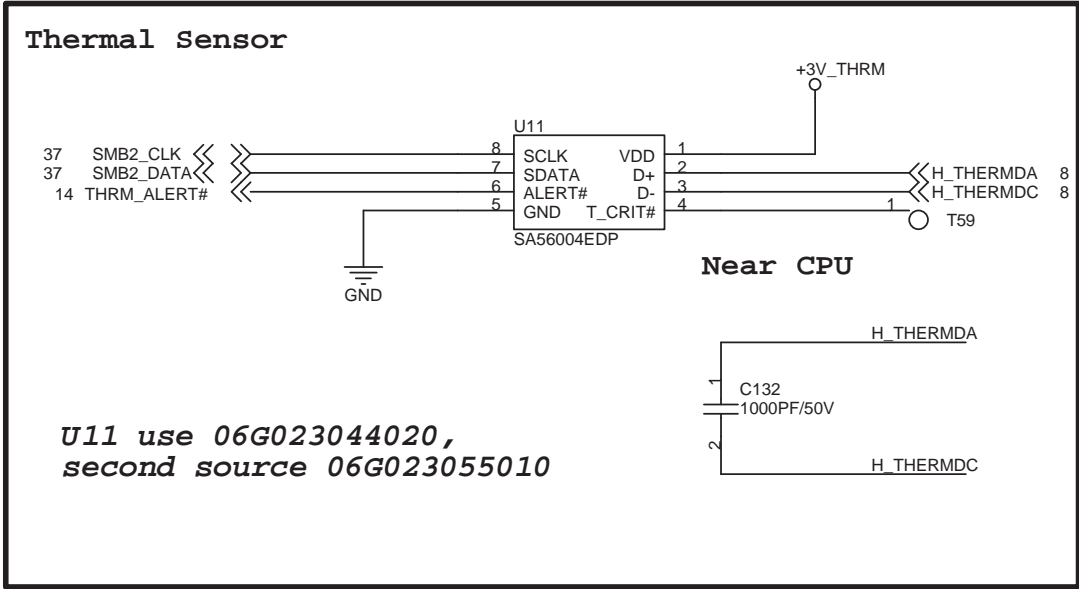
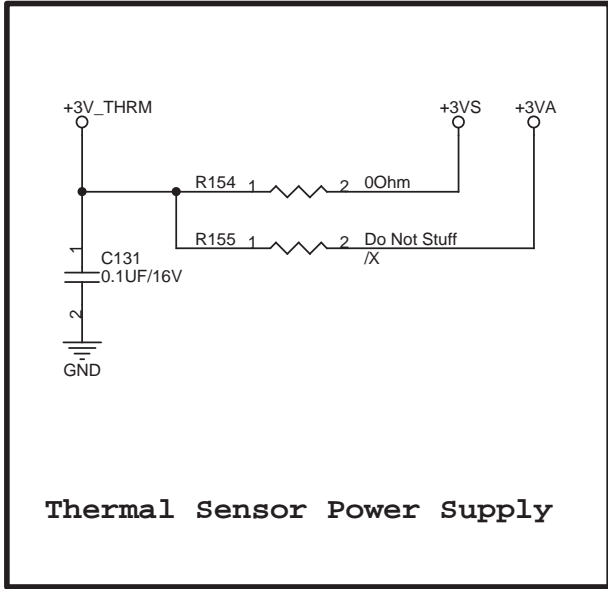


0106 1025

<b>ASUS</b>		<b>Title : Reset Map</b>	
ASUSTeK COMPUTER INC		<b>Engineer: Jerry Liu</b>	
Size A4	Project Name <b>T91</b>	Rev 1.2G	
Date: Tuesday, January 06, 2009		Sheet 40 of 57	

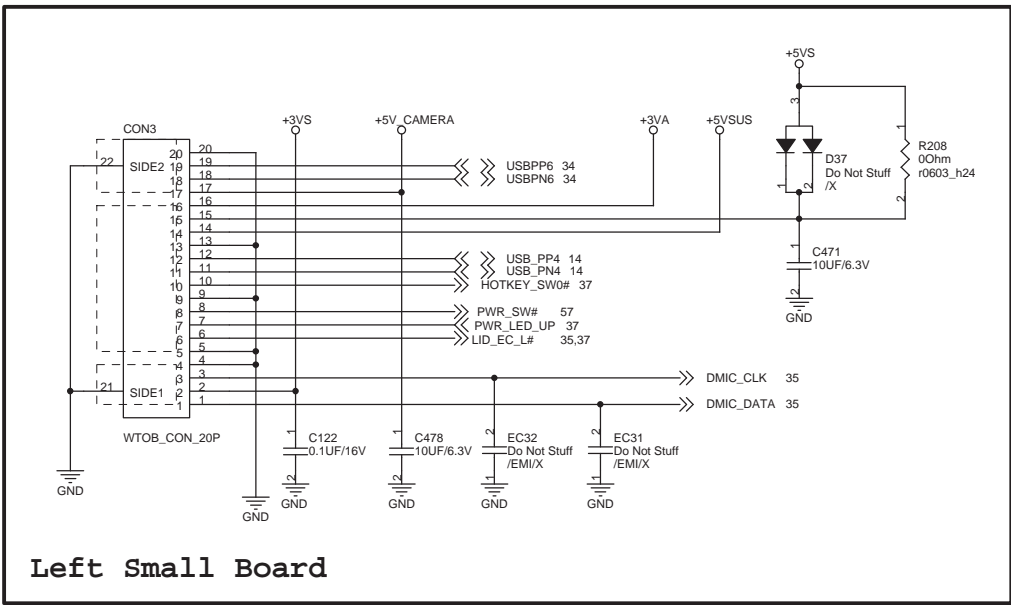




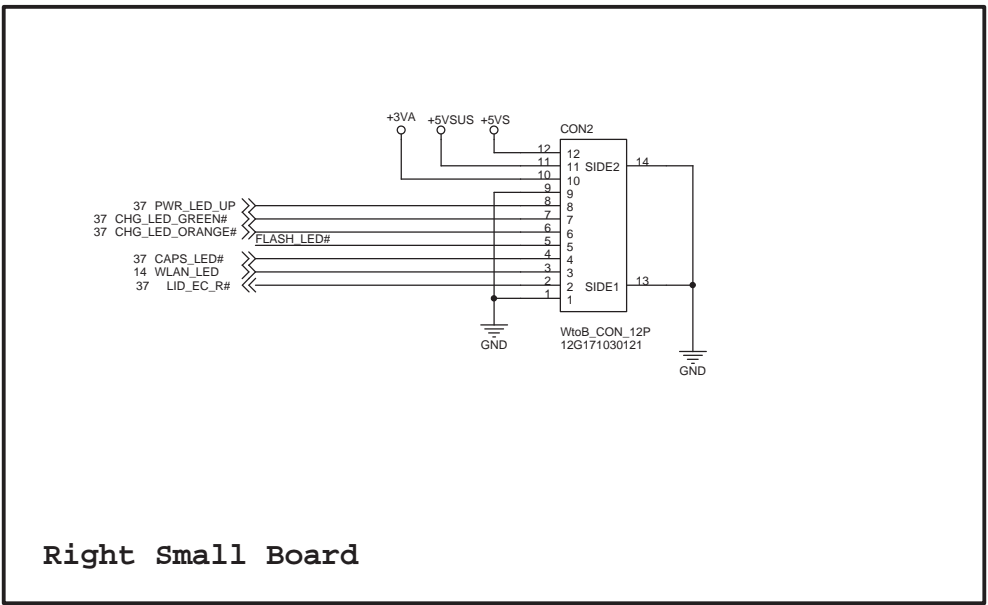


0106 1025

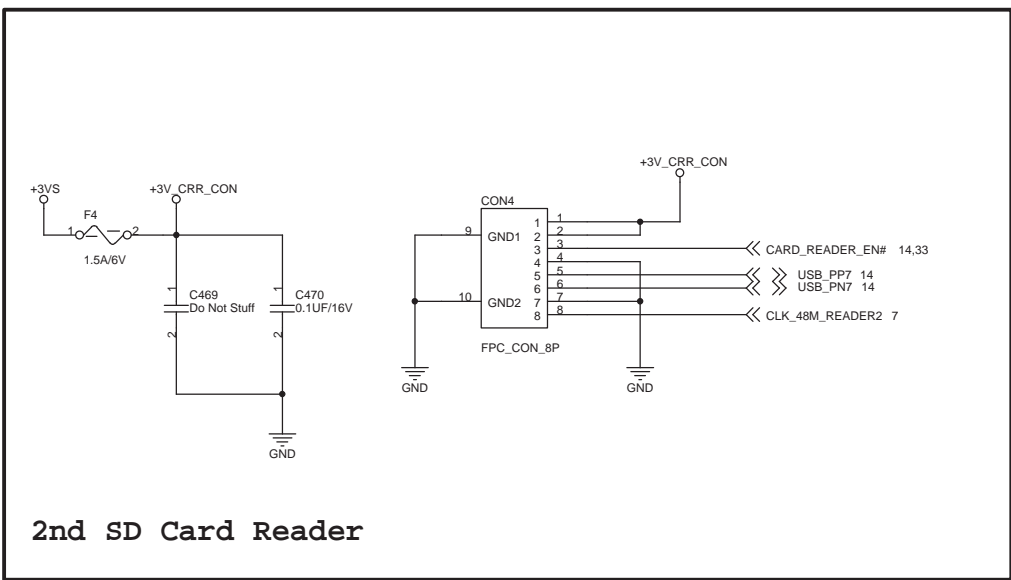
<b>ASUS</b>		<b>Title : Thermal Sensor</b>	
ASUSTek Computer INC.		<b>Engineer: Jerry Liu</b>	
Size A4	Project Name <b>T91</b>	Date: Tuesday, January 06, 2009	Rev 1.2G
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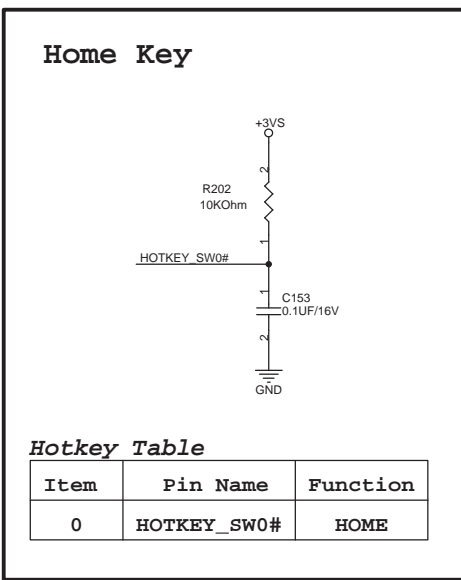
Left Small Board



Right Small Board

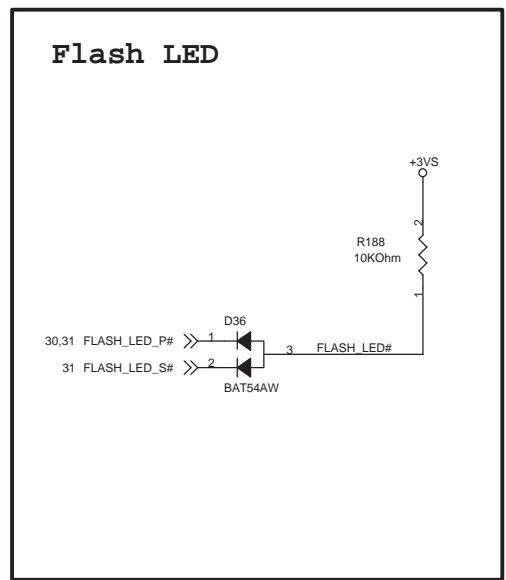


2nd SD Card Reader

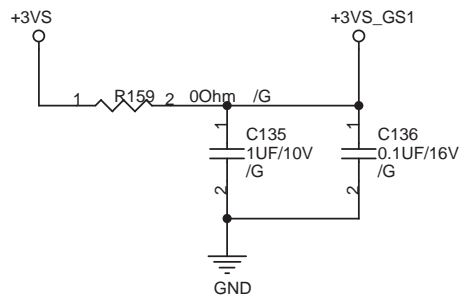


Hotkey Table

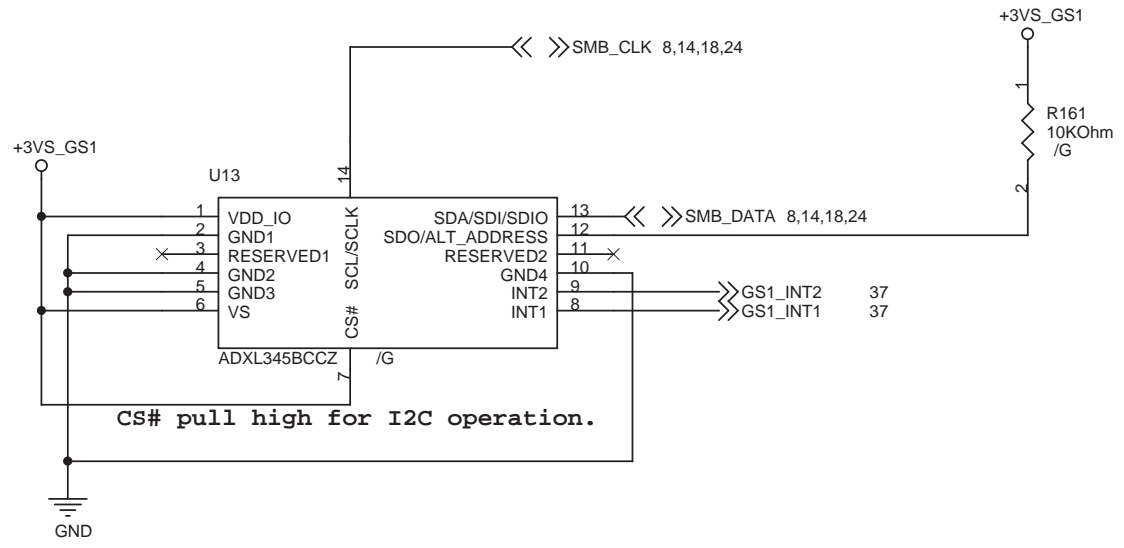
Item	Pin Name	Function
0	HOTKEY_SW0#	HOME



Flash LED

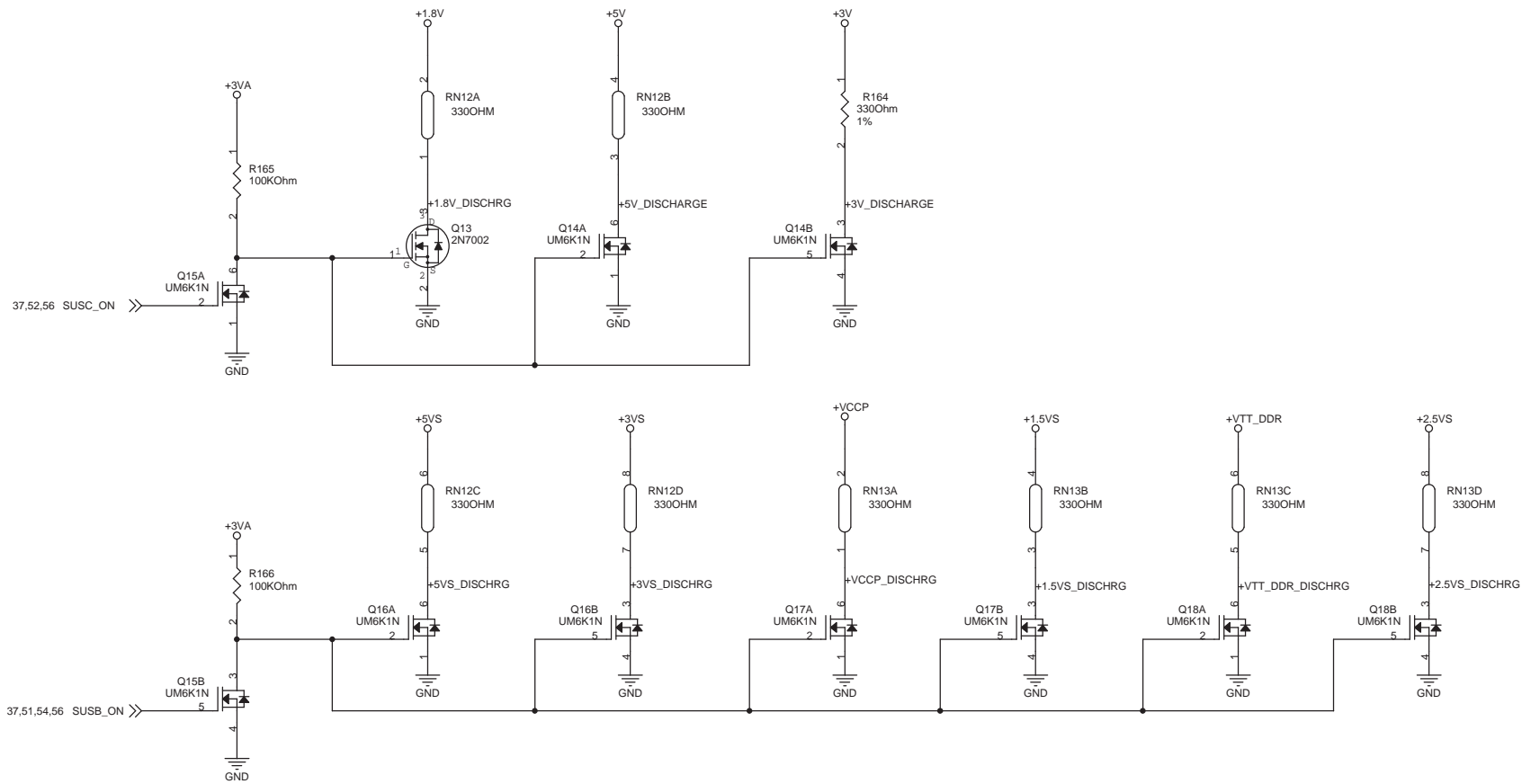


SMBUS Address: 0X1D



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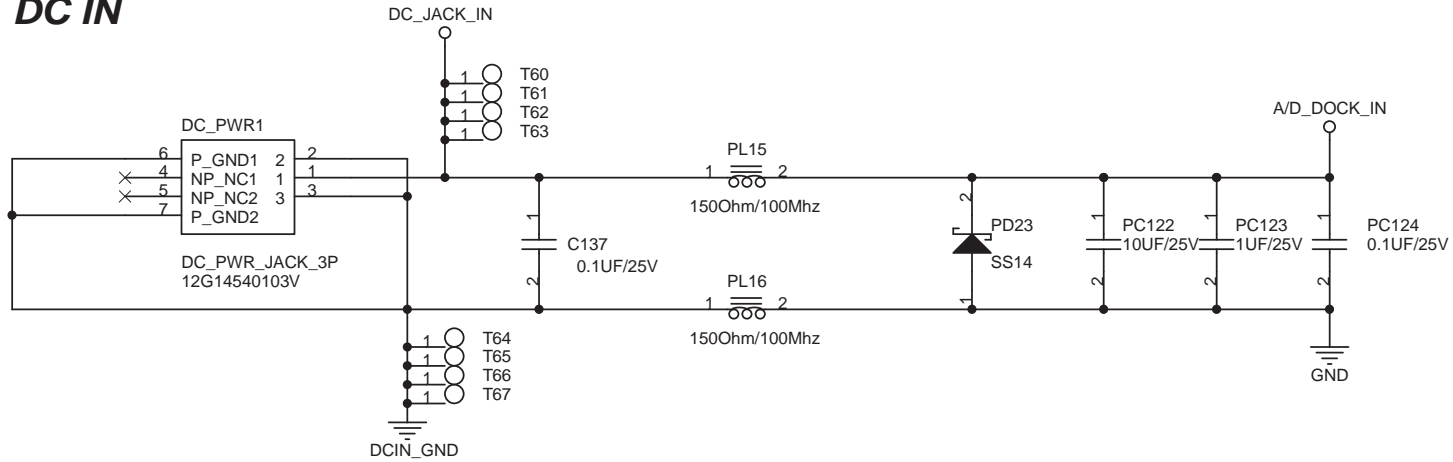
<b>ASUS</b>		<b>Title : G-Sensor</b>	
ASUSTek Computer INC.		<b>Engineer: Jerry Liu</b>	
Size A4	Project Name <b>T91</b>	Rev 1.2G	
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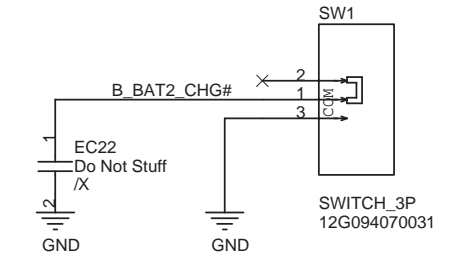
0106 1025

<b>ASUS</b>		<b>Title : Discharge</b>	
ASUSTek Computer INC.		<b>Engineer: Jerry Liu</b>	
Size	Project Name		Rev
A3	<b>T91</b>		1.2G
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### DC IN

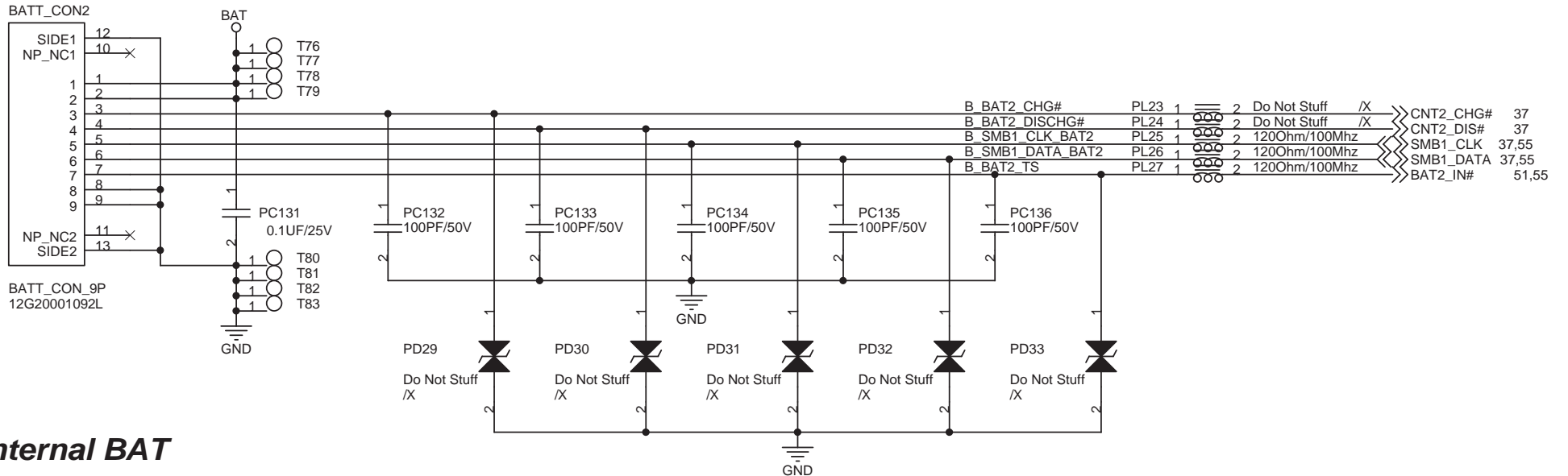


### Battery Switch



CNT2\_CHG# : Low : Battery ON  
 CNT2\_CHG# : open : Battery OFF

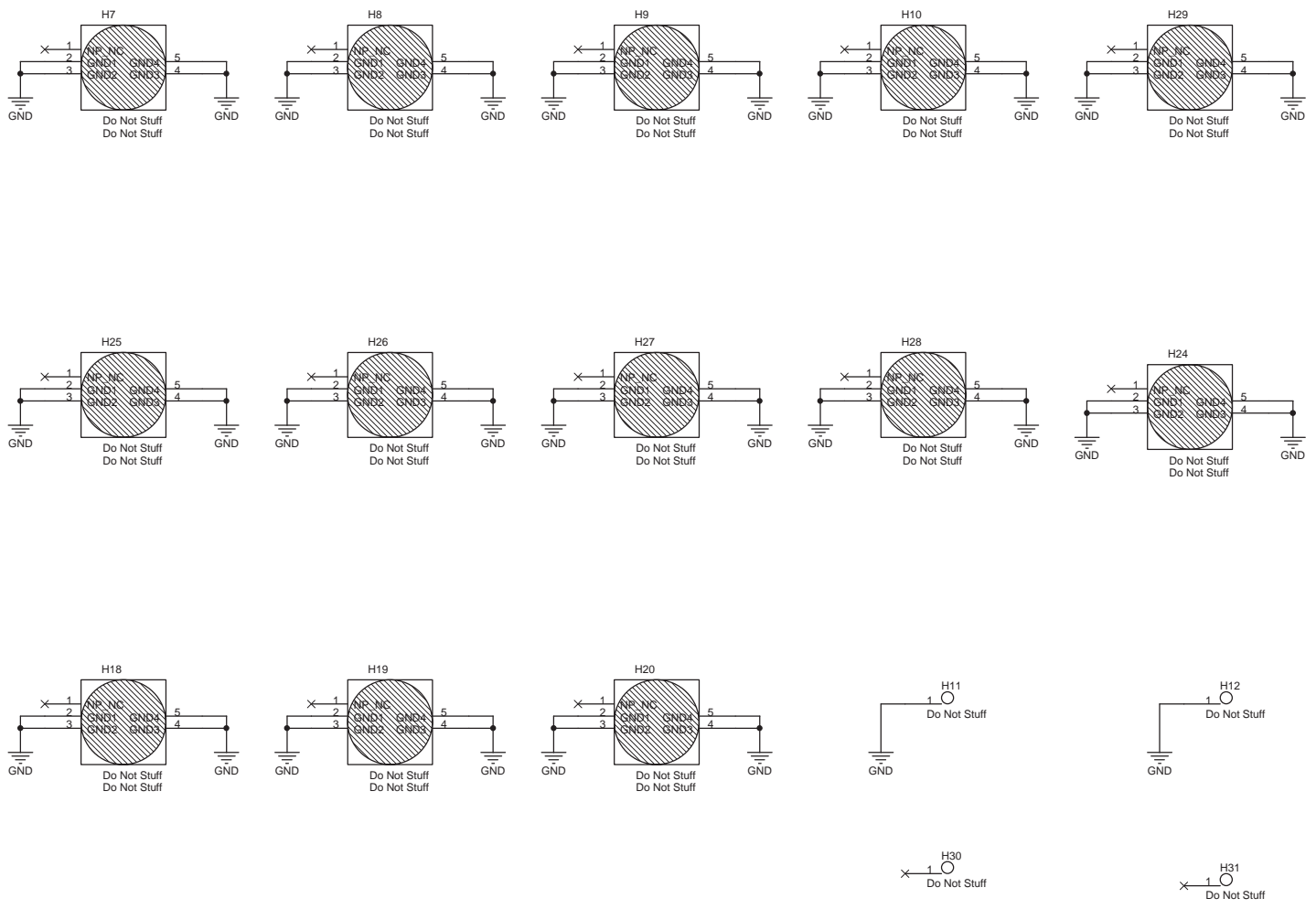
### BATT\_CON2



### Internal BAT

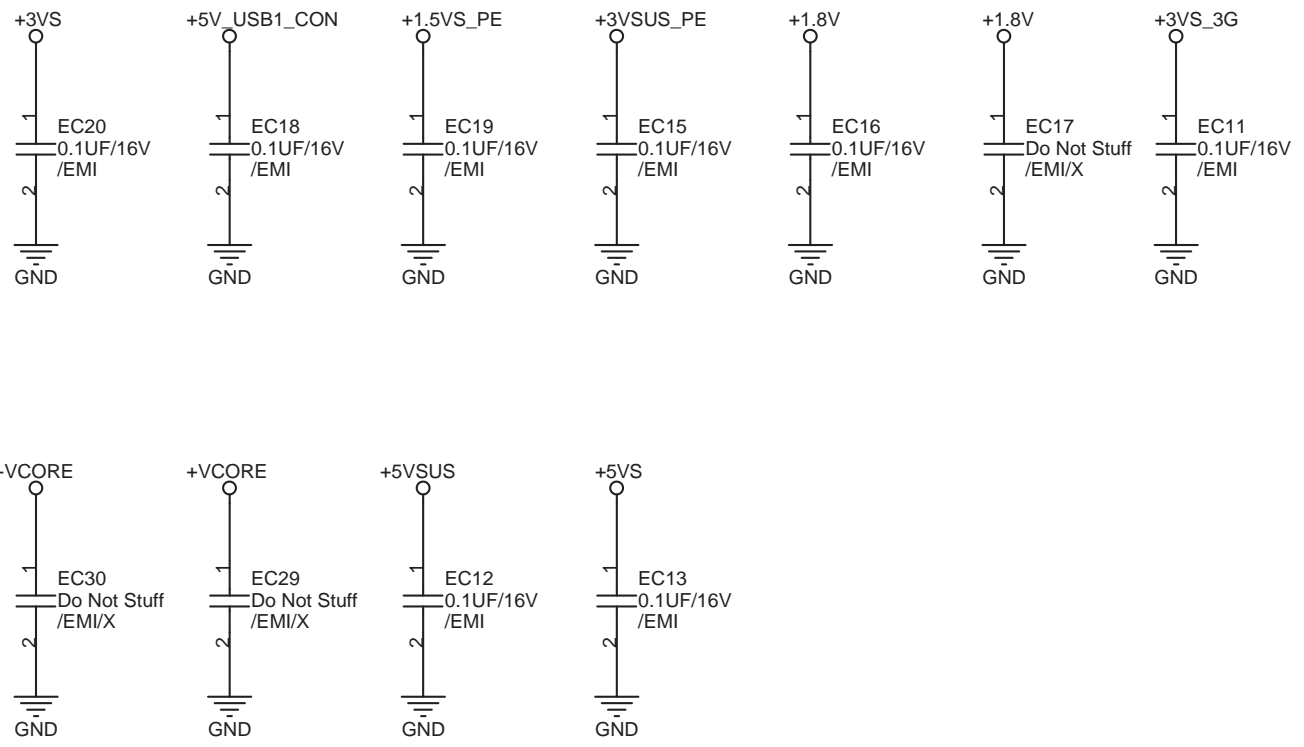
0106 1025

<b>ASUS</b>		<b>Title : PWR Jack</b>	
ASUSTek Computer INC.		<b>Engineer: Jerry Liu</b>	
Size A4	Project Name <b>T91</b>	Date: Tuesday, January 06, 2009	Rev 1.2G
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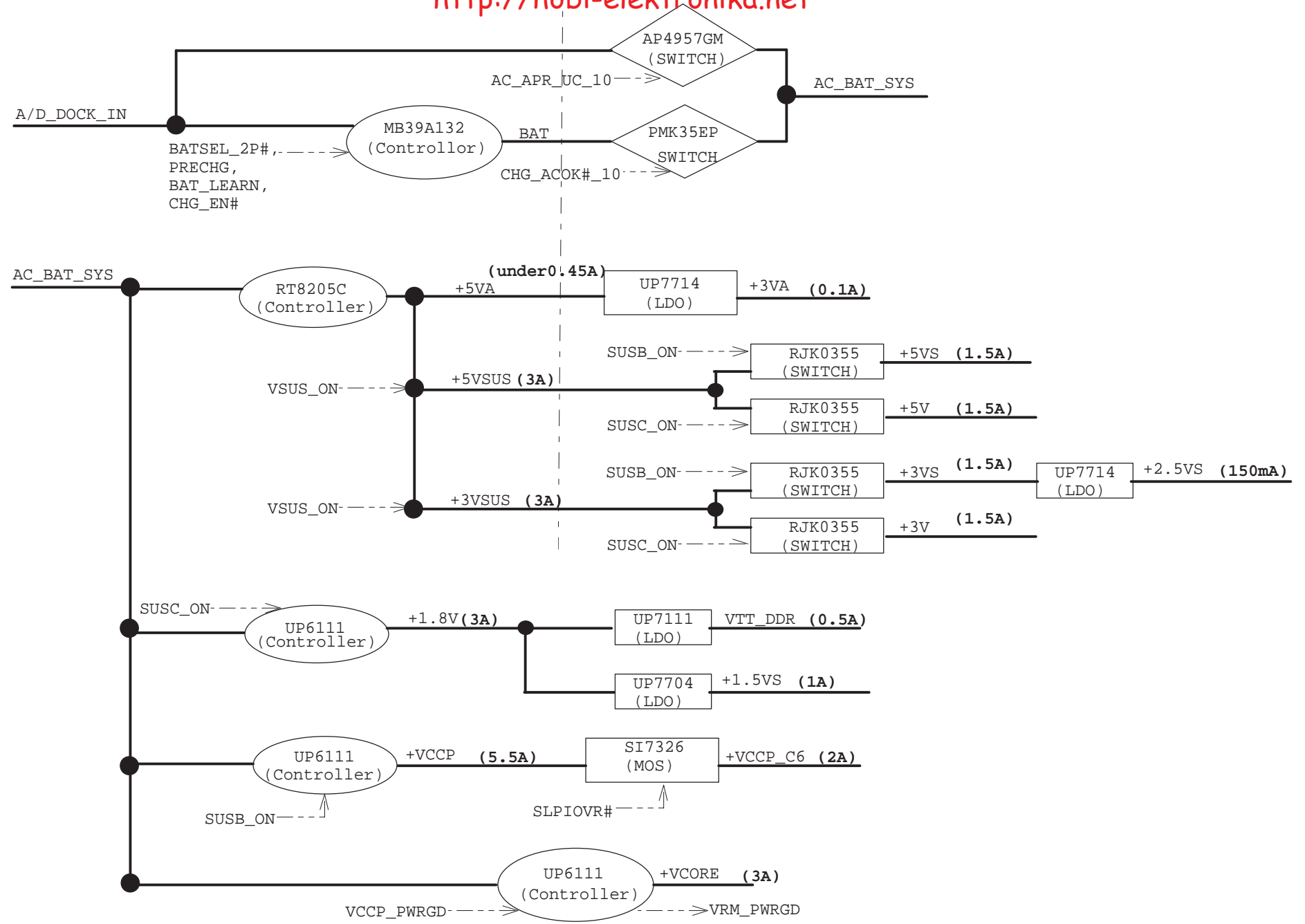
<b>ASUS</b>		<b>Title : Screw Hole</b>	
ASUSTek Computer INC.		<b>Engineer: Jerry Liu</b>	
Size	Project Name		Rev
A3	<b>T91</b>		1.2G
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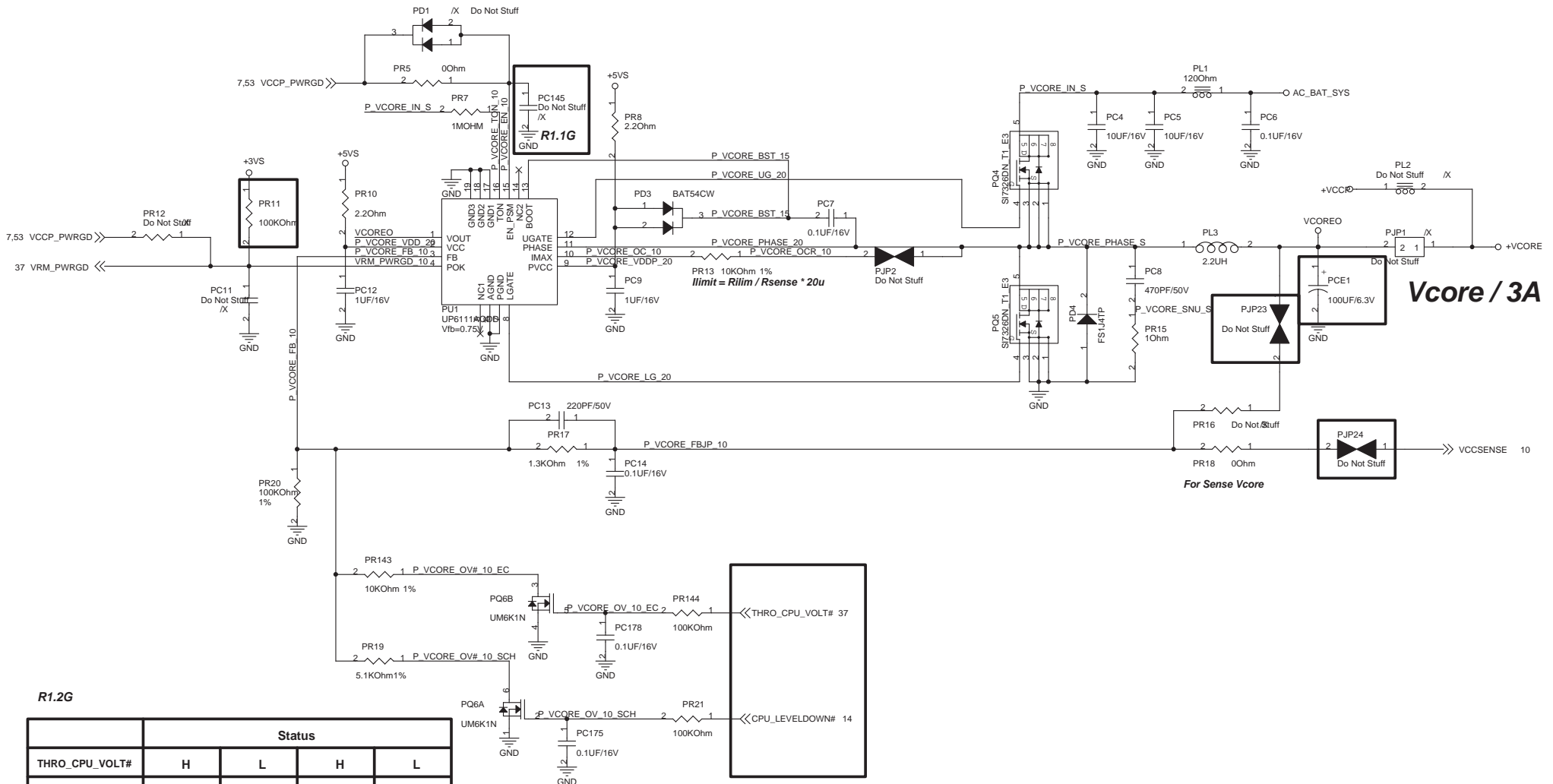


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		Title : EMI	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size A	Project Name <b>T91</b>	Rev 1.2G	
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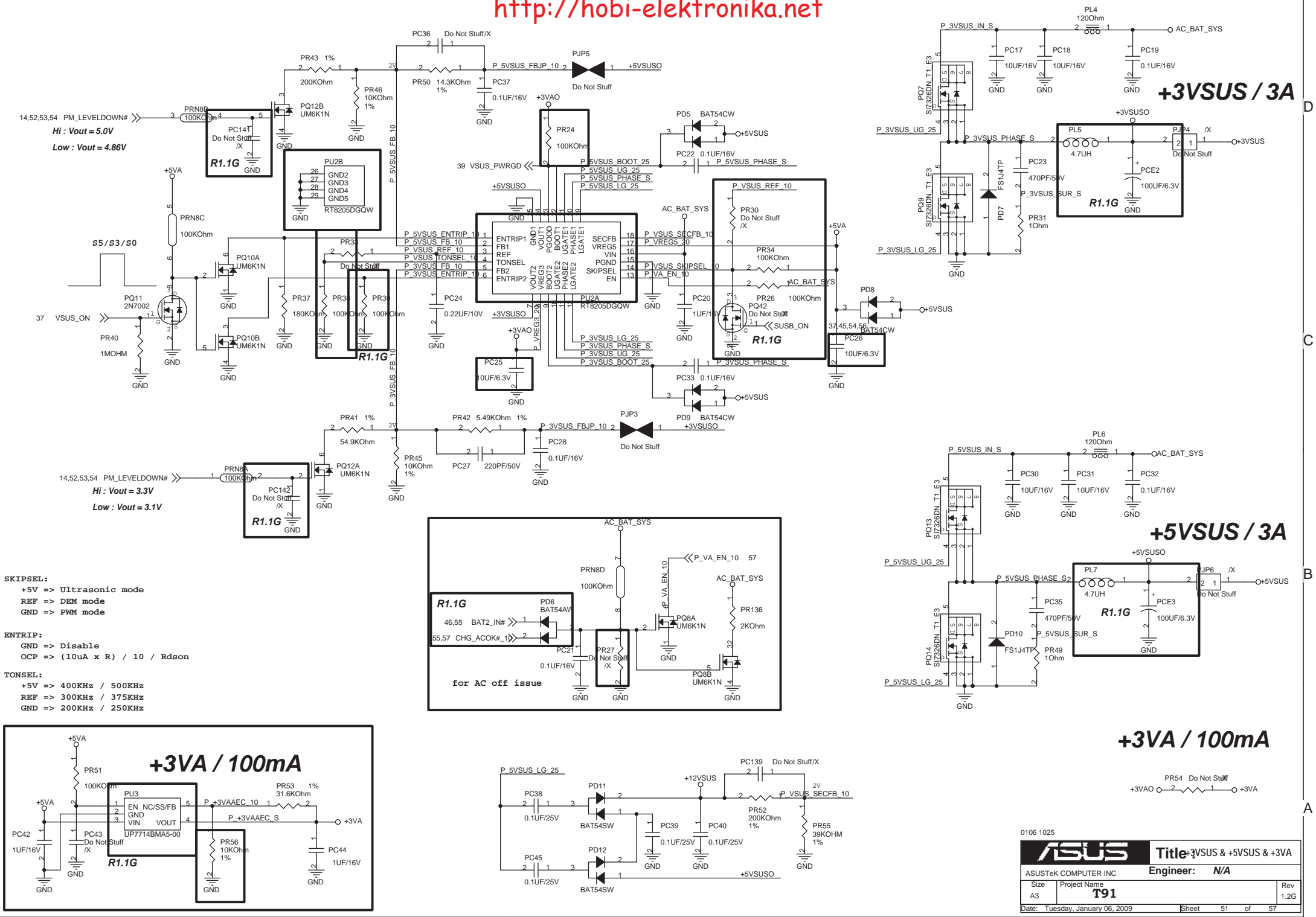


R1.2G

		Status			
THRO_CPU_VOLT#		H	L	H	L
CPU_LEVELDOWN#		H	H	L	L
Voltage		1.0484V	0.9509V	0.8573V	0.7598V
		Normal	Normal + Throttle	Power Saving	Power Saving + Throttle

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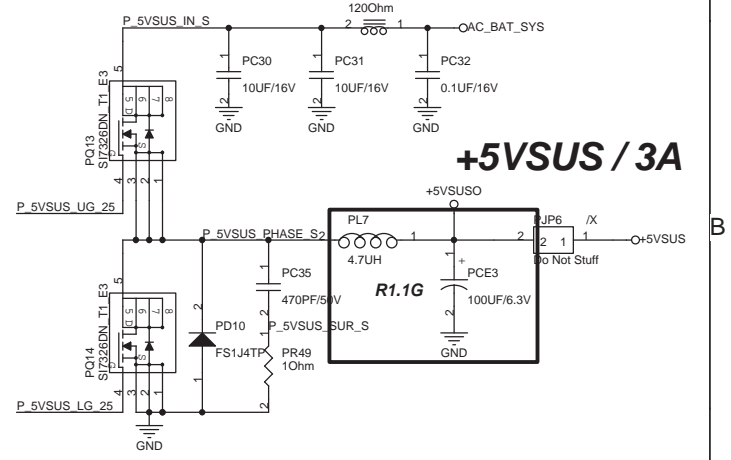
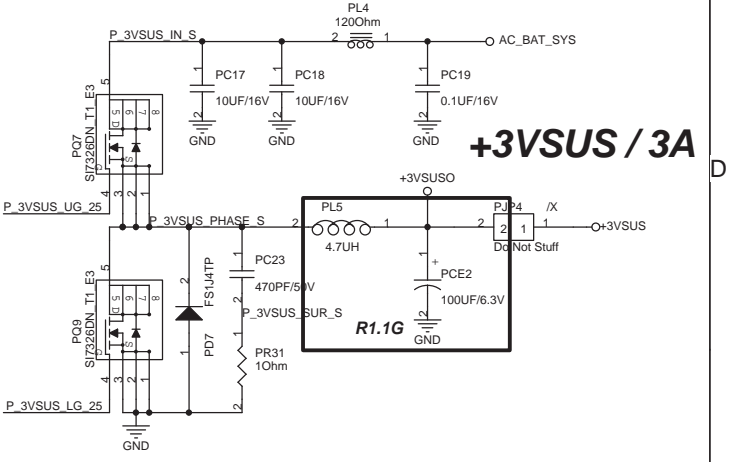
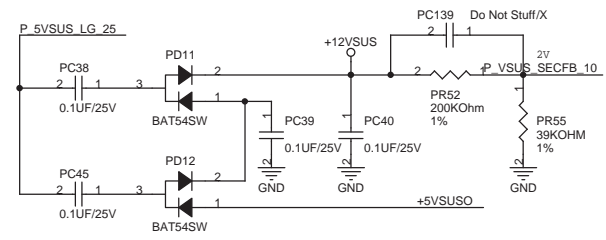
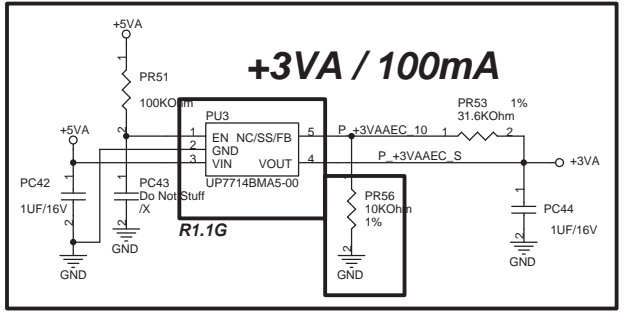
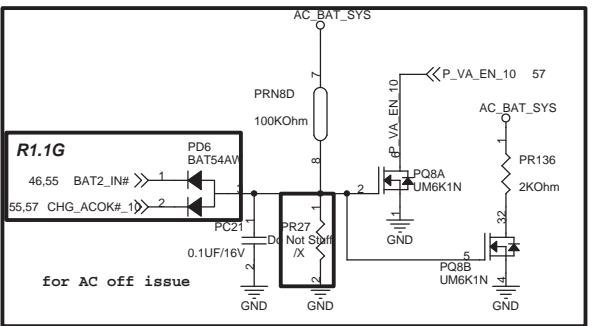
<b>ASUS</b>		Title : Vcore	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size	Project Name	Rev	
Custom	<b>T91</b>	1.2G	
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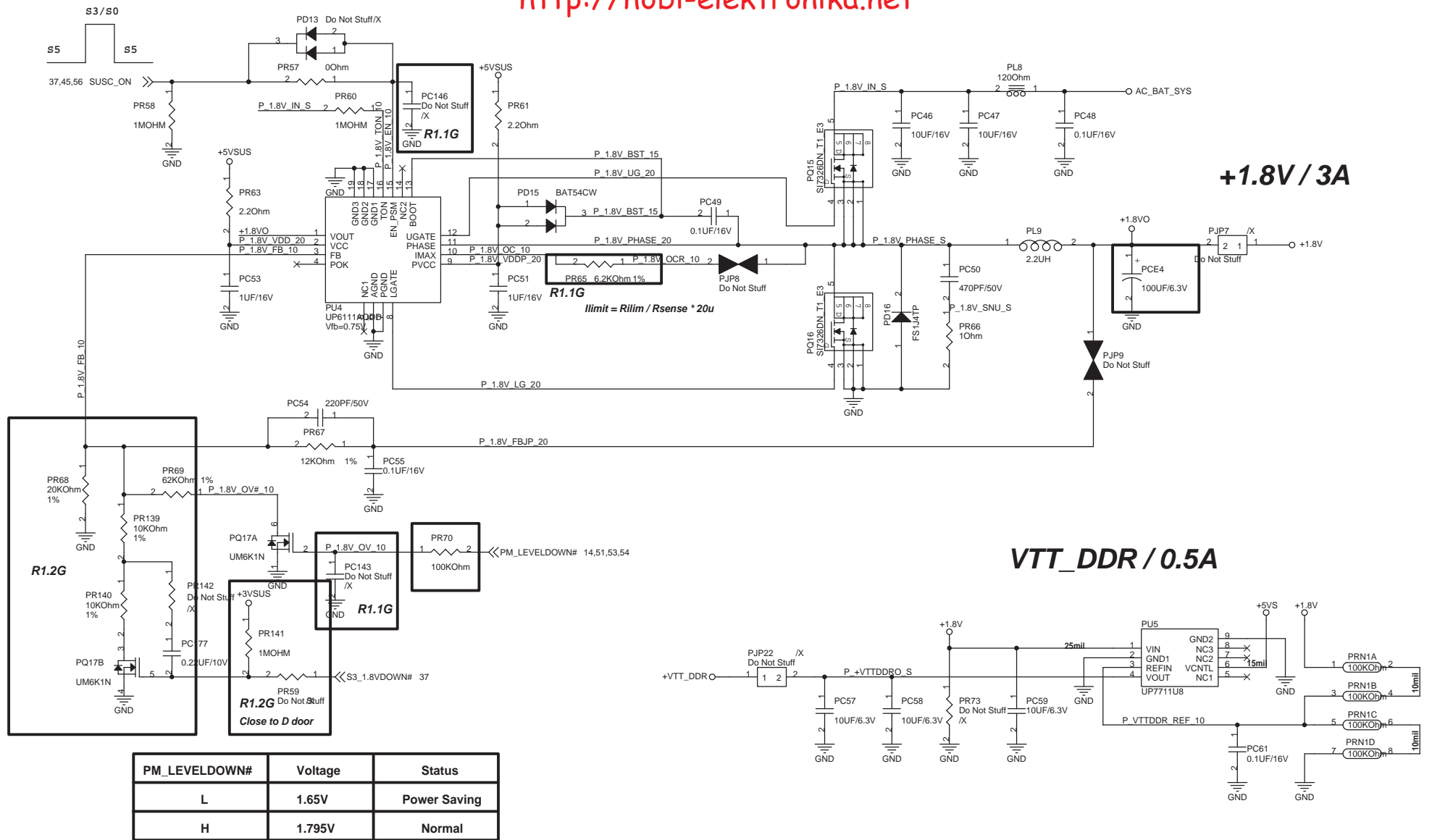


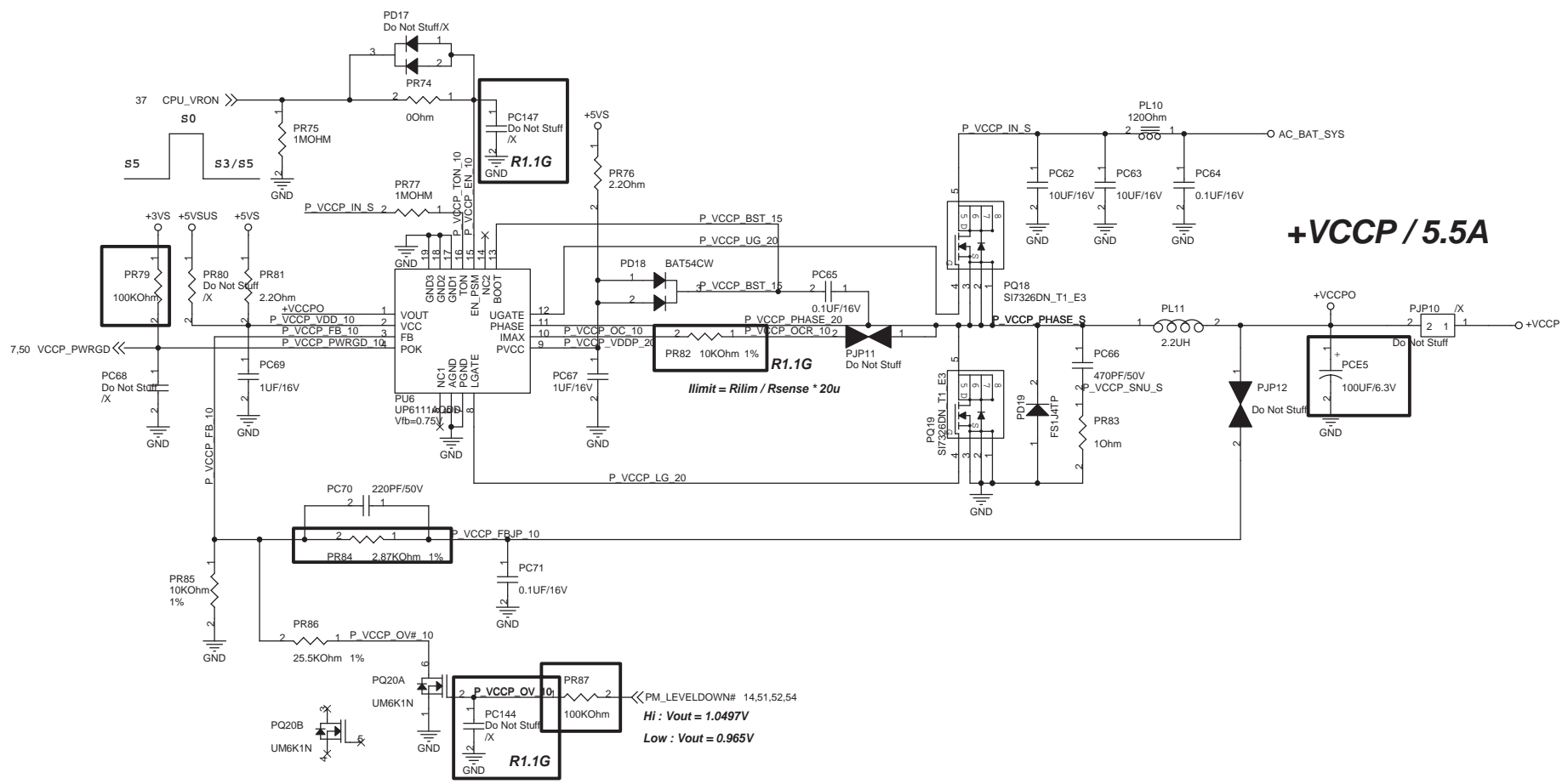
14,52,53,54 PM\_LEVELDOWN#  
**Hi : Vout = 5.0V**  
**Low : Vout = 4.86V**

14,52,53,54 PM\_LEVELDOWN#  
**Hi : Vout = 3.3V**  
**Low : Vout = 3.1V**

- SKIPSEL:**  
 +5V => Ultrasonic mode  
 REF => DEM mode  
 GND => PWM mode
- ENTRIP:**  
 GND => Disable  
 OCP => (10uA x R) / 10 / Rdson
- TONSEL:**  
 +5V => 400KHz / 500KHz  
 REF => 300KHz / 375KHz  
 GND => 200KHz / 250KHz







**+VCCP / 5.5A**

$I_{limit} = R_{ilim} / R_{sense} * 20u$

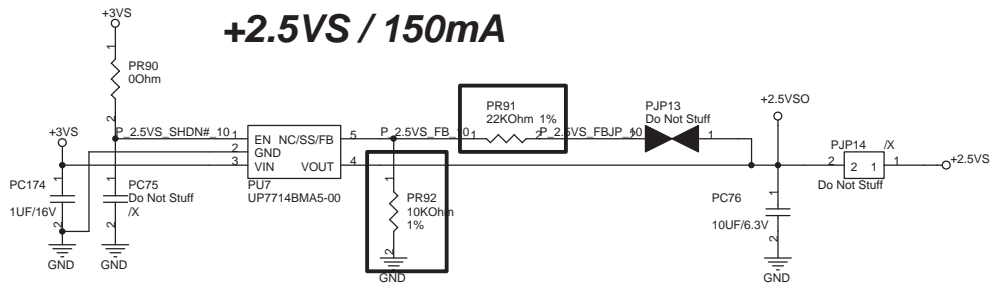
**Hi : Vout = 1.0497V**  
**Low : Vout = 0.965V**

PM_LEVELDOWN#	Voltage	Status
L	0.965V	Power Saving
H	1.0497V	Normal

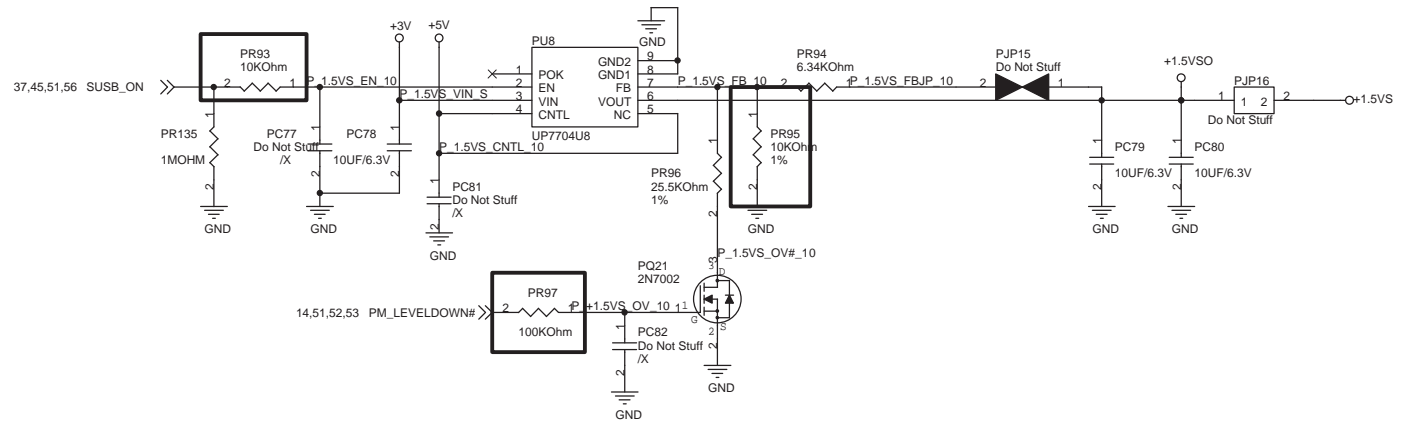
0106 1025

<b>ASUS</b>		<b>Title : VCCP</b>	
ASUSTek Computer INC.		<b>Engineer: Joy_Zhou</b>	
Size A3	Project Name <b>T91</b>	Rev 1.2G	
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**+2.5VS / 150mA**

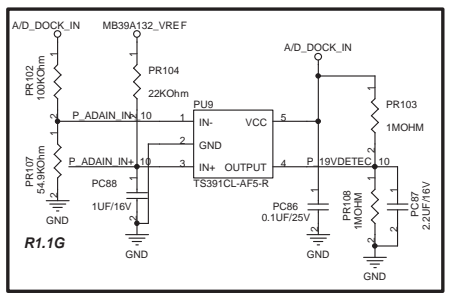


**+1.5VS / 1A**



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<b>ASUS</b>		<b>Title : +1.5VS &amp; +2.5VS</b>	
ASUSTek Computer INC.		Engineer: <i>Joy_Zhou</i>	
Size	Project Name	Rev	
A3	<b>T91</b>	1.2G	
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**Prevent Input from 19V :**  
 Adaptor > 14.2V, PQ603B Turn-off  
 Adaptor < 12.4V, PQ603B Turn-on

VREF = 5.0V  
 $f_{osc}(KHz) = 17000 / RT (KOhm)$   
 Soft start:  $t_s(s) = 0.13 * CS (uF)$   
 $VTH \text{ of } -IN1: 5V / 62 * (100+62) = 13.06V$   
 $VTH \text{ of } ACIN: 1.25V / 25 * (185+25) = 10.5V$   
 Change PR607 and PR608 value

**Prevent Input from 19V :**  
 Adaptor > 13.06V, PQ603B Turn-off  
 Adaptor < 13.06V, PQ603B Turn-on

**Battery Cell Selection :**  
 BAT\_LEARN = 1, Battery discharges  
 BAT\_ID = 1, 2 Cells; Vadj2 = 0.998V  
 => Icharge = 1.477A  
 BAT\_ID = 0, 4/6 Cells; Vadj2 = 1.648V  
 => Icharge = 2.517A

**Pre-Charging Mode :**  
 Precharging current = 150mA  
 Vadj2 = 168.75mV

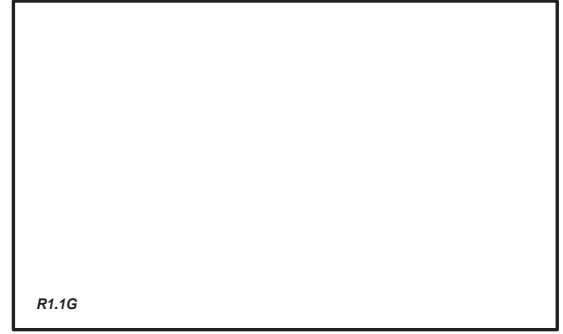
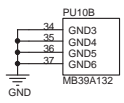
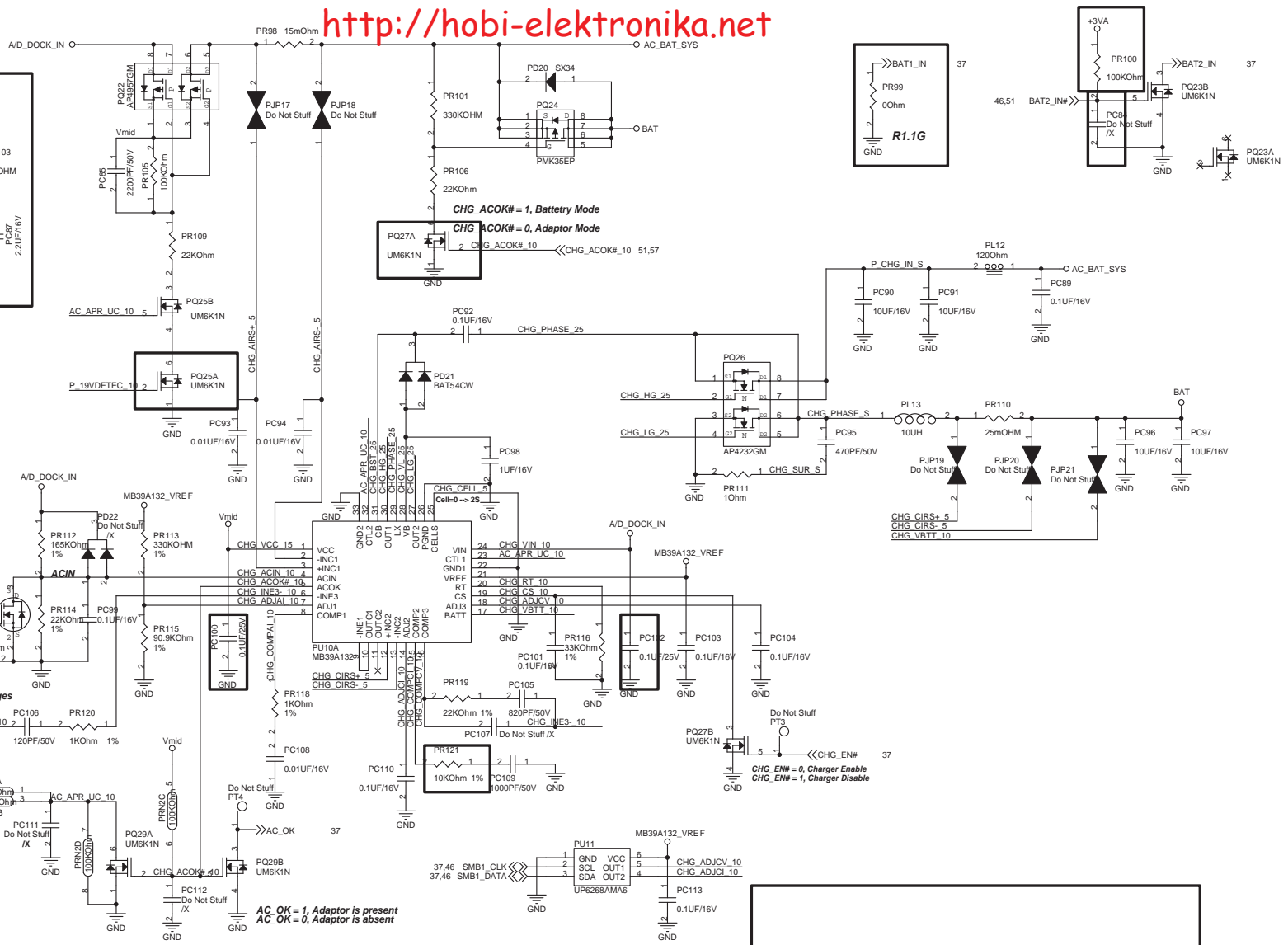
**Adaptor Max. Current :**  
 PR600=235.8K; Ilimit = 2.170A; 20.615W (9.5V/22W)  
 PR600=185.3K; Ilimit = 2.677A; 32.124W (12V/36W)

**ACIN Threshold = 1.25V**  
 Adaptor > 10.5V, System Powered by Adaptor  
 Adaptor < 10.5V, System Powered by Battery

**Battery Charging Voltage :**  
 Vadj3 > 4.1V ==> Vbat = 4.2V /cell  
 2.2V > Vadj3 > 1.1V ==> Vbat = 2 \* Vadj3 /cell

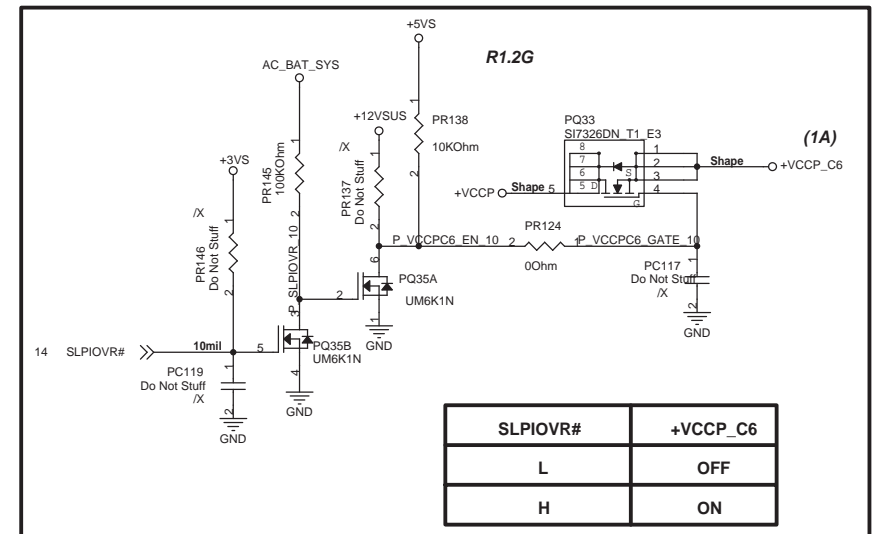
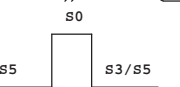
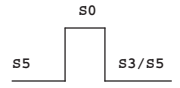
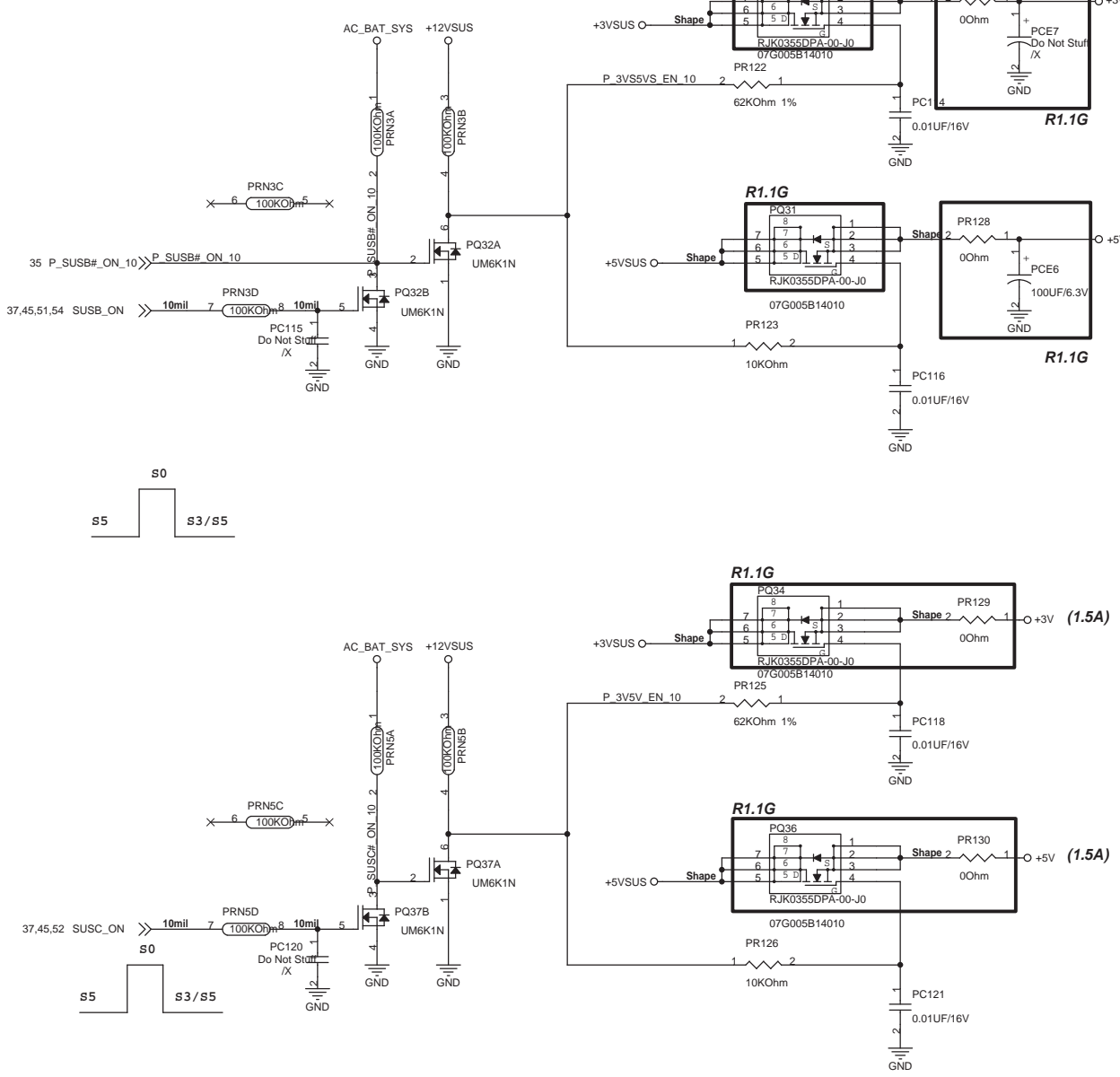
**Battery Charging Current :**  
 4.4V > Vadj2 >= 0V ==>  
 Ichg = (Vadj2 - 0.075) / (25 \* Rs)

**Input Adaptor Max. Current Limit :**  
 Ilimit\_current = (Vadj1 - 0.075) / (25 \* Rs)



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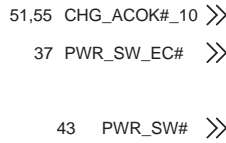
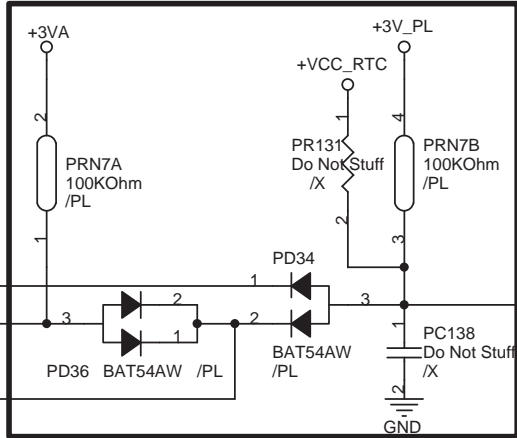
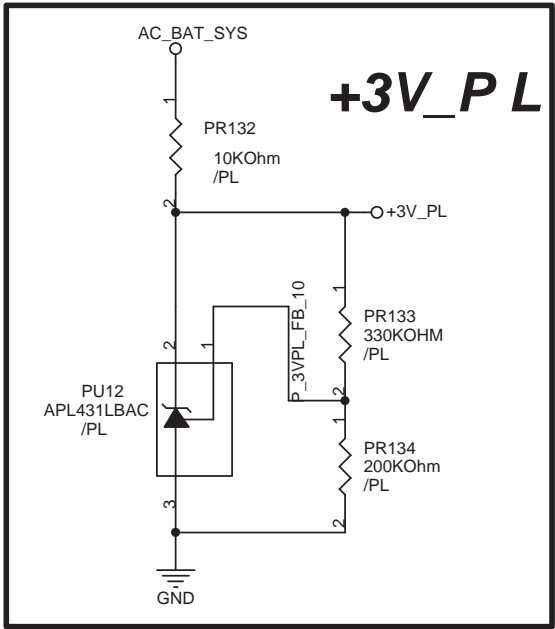
<b>ASUS</b>		<b>Title : CHARGER</b>	
ASUSTek Computer INC.		Engineer: Yachwa_Chen	
Size	Project Name	Rev	1.2G
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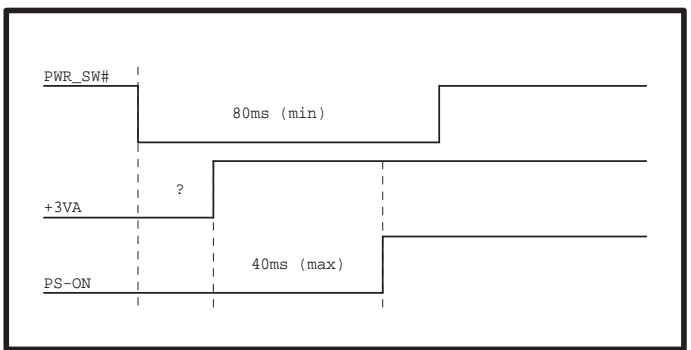
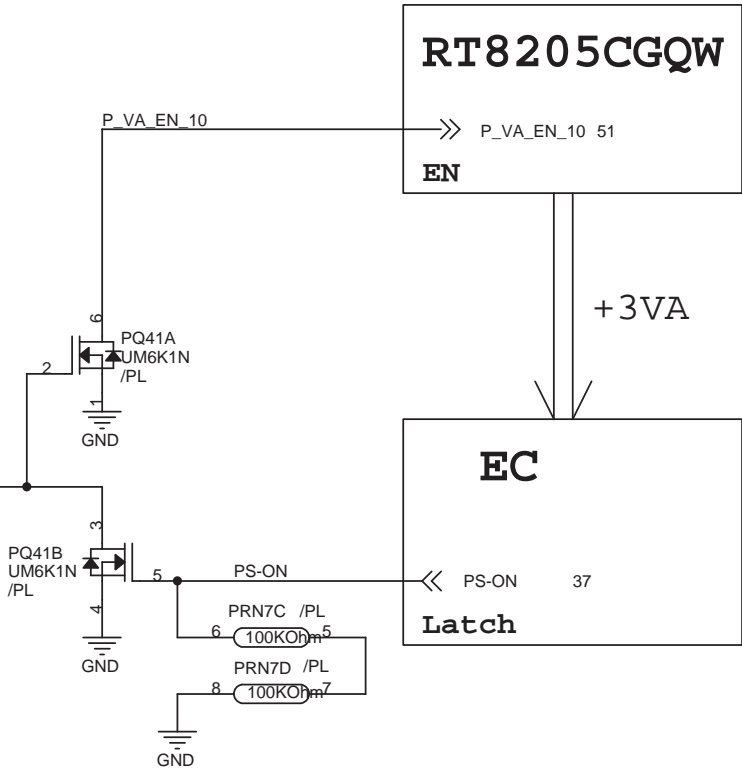
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Size	Document Number	Rev	<Rev/Code>
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<b>ASUS</b>		<b>Title : Power Latch</b>	
ASUSTek Computer INC.		<b>Engineer: Jerry Liu</b>	
Size	Project Name	Rev	
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