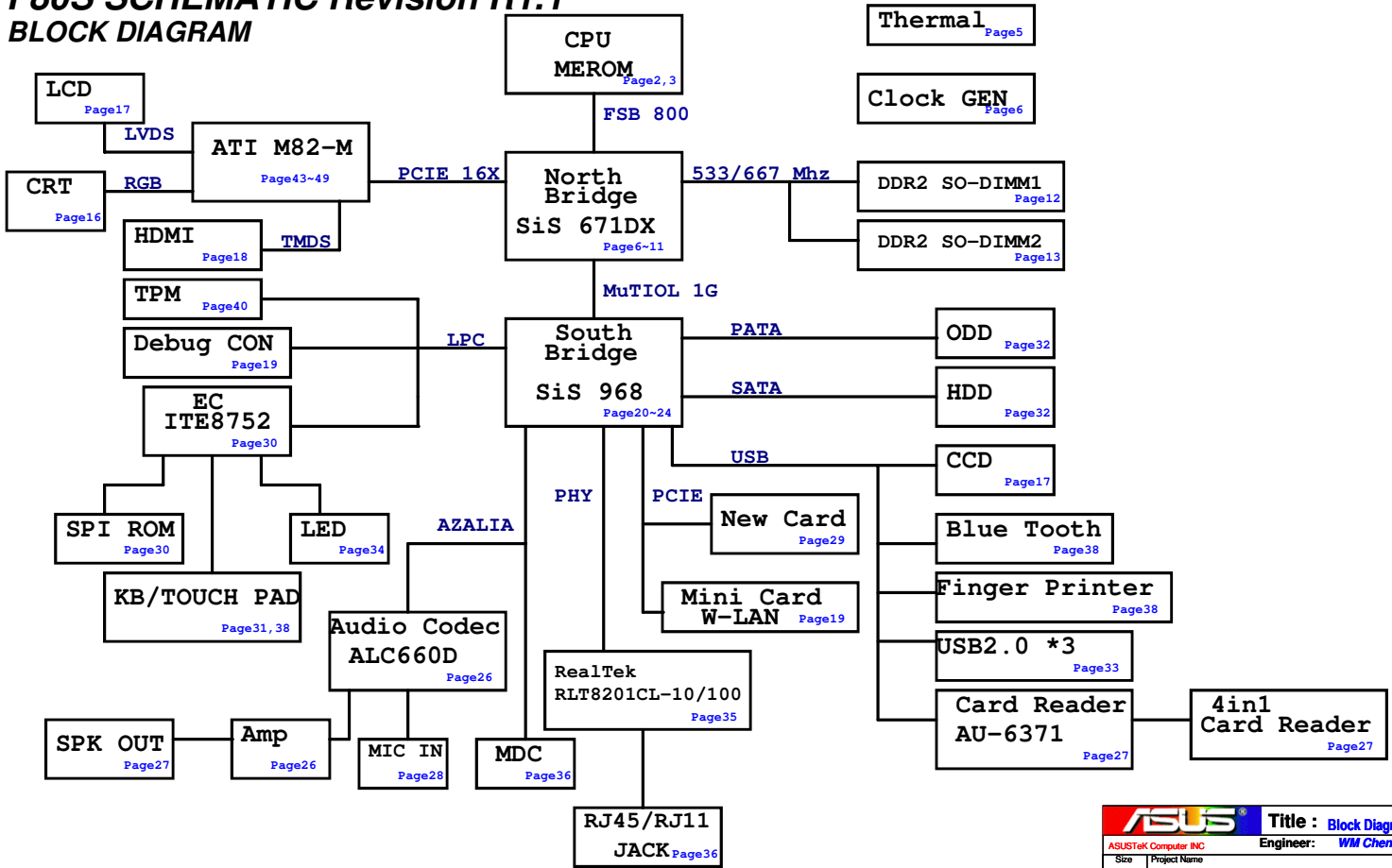
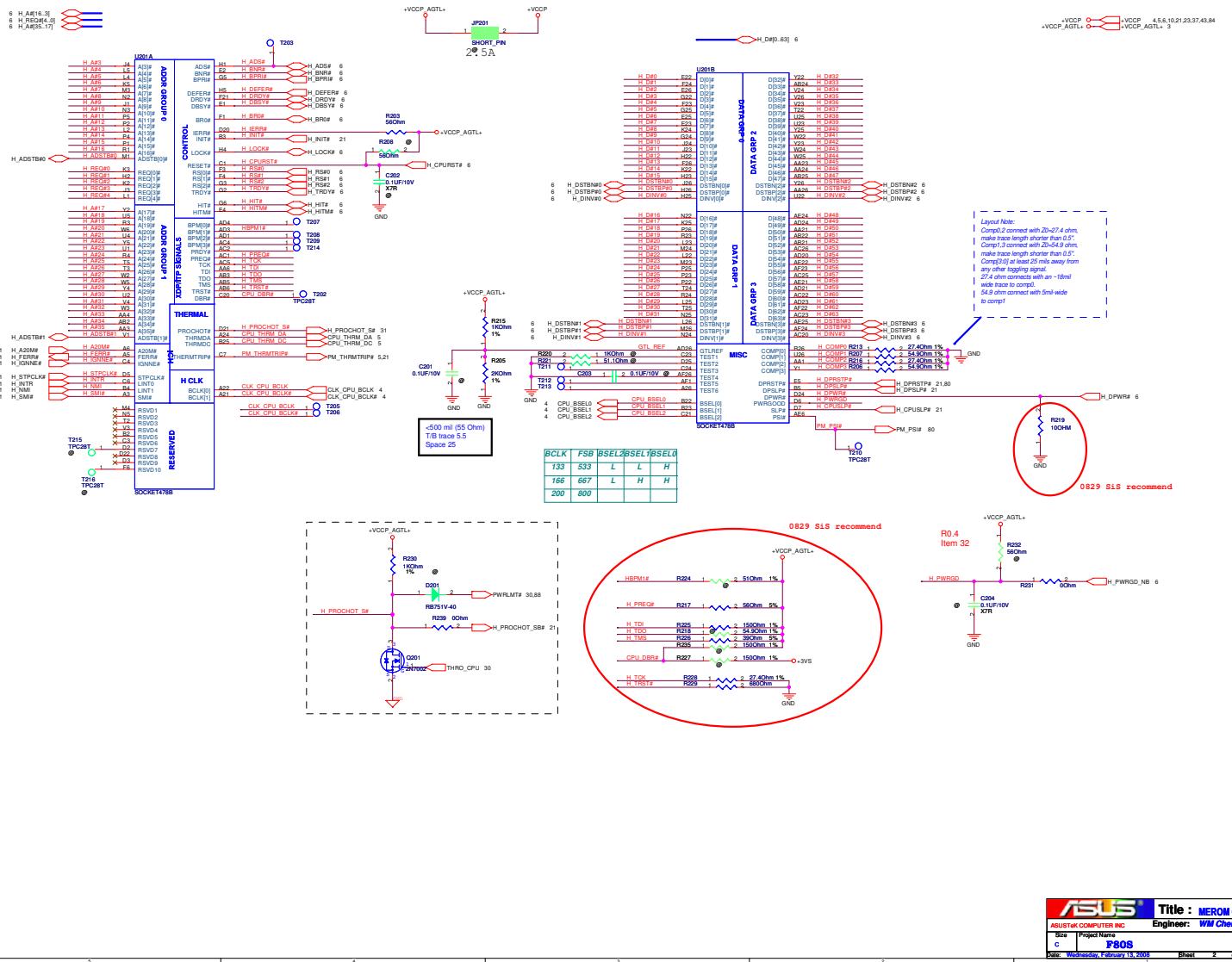
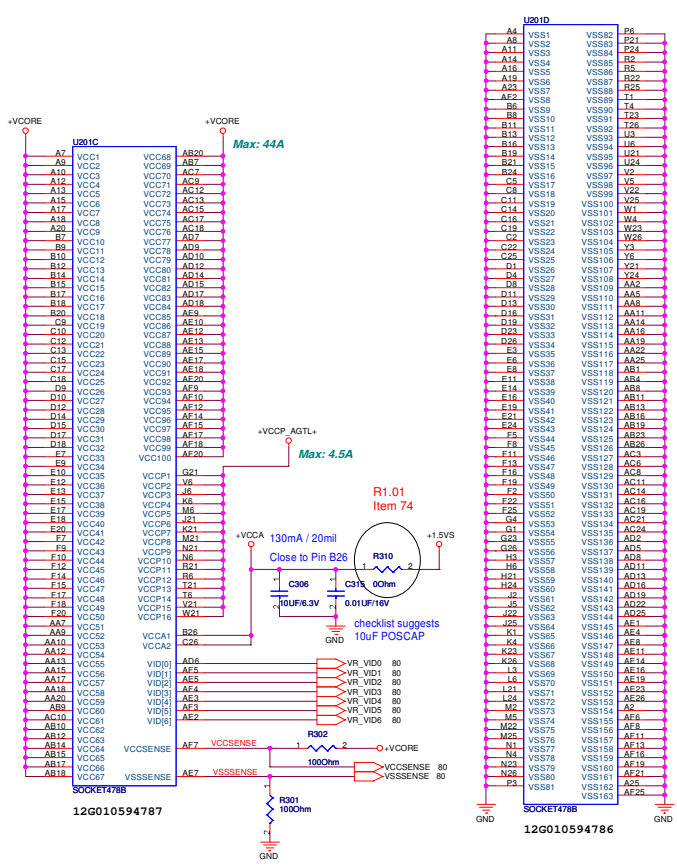


F80S SCHEMATIC Revision R1.1

BLOCK DIAGRAM

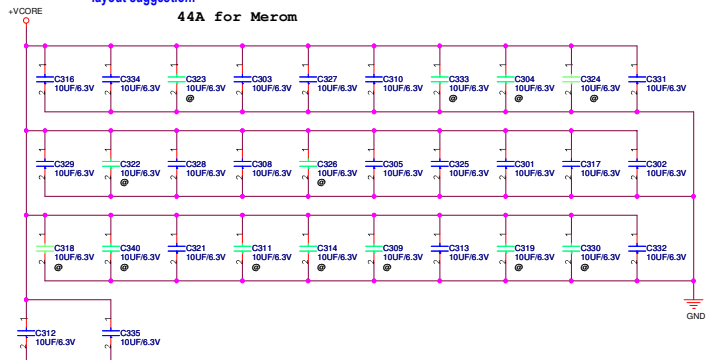




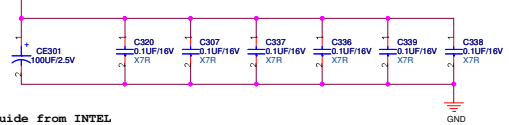


MEROM FSB 800			
VCCP	Min	Typ	Max
	1.00V	1.05V	1.10V
ICCP	Min	Typ	Max
			2.5A

Place on L1/L8, upper/lower side of inside socket, according intel layout suggestion.



+VCCP Decoupling Capacitor (Place near CPU)



Decoupling guide from INTEL

VCCORE	22uF/10V	* 32pcs
VCCP	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
VCCP	150uF	* 1pcs for CPU

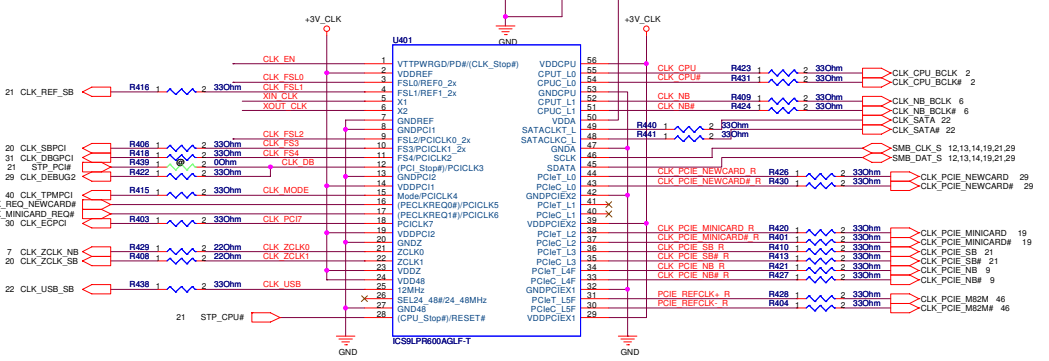
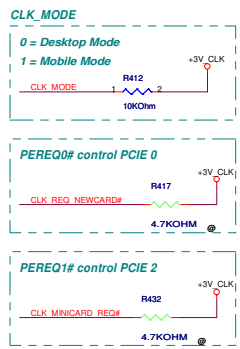
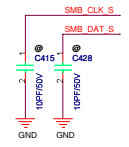
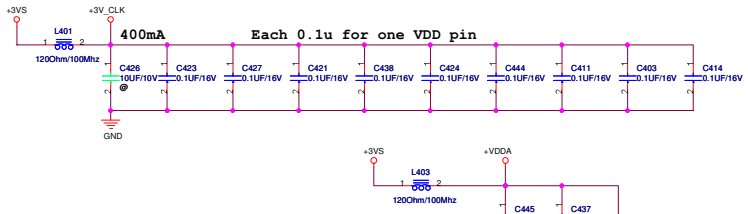
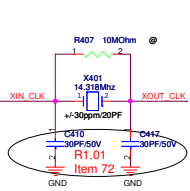
Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27-4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.

ASUS Title : MEROM CPU (2)

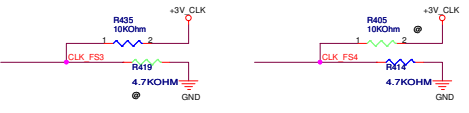
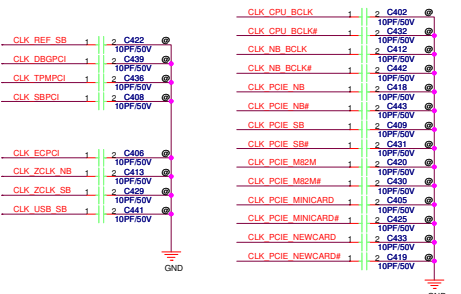
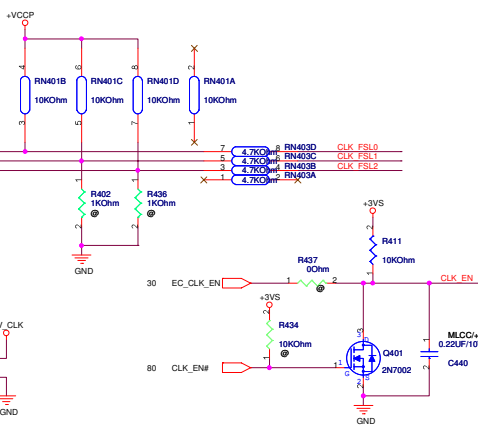
ASUSTeK COMPUTER INC. Engineer: WM Chen

Size	Project Name	Rev
A3	F80S	1.1

Date: Wednesday, February 13, 2008 Sheet 3 of 84

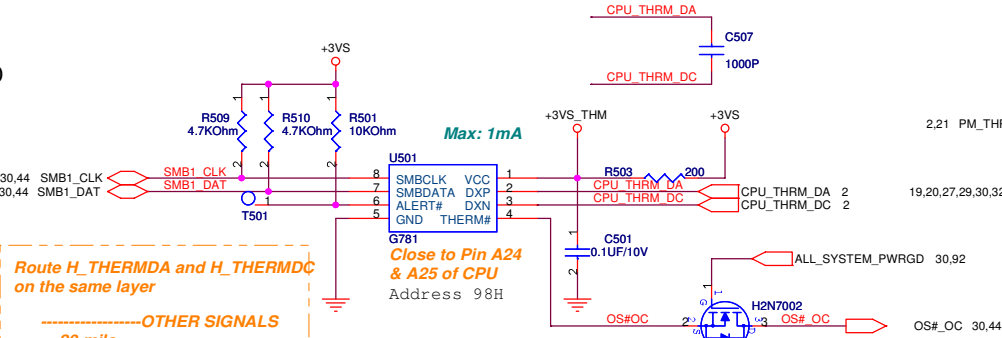


FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100



ASUS Title : Clock GEN
 ASUSTek Computer INC Engineer: **WM Chen**
 Size Project Name
 A3 F80S
 Date: Wednesday, February 13, 2008 Sheet 4 of 94

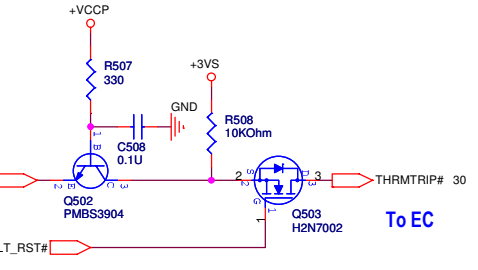
CPU Thermal Sensor



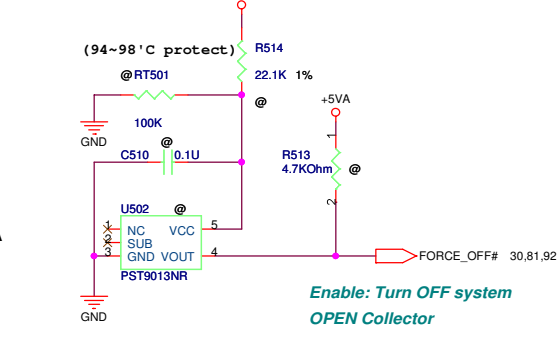
Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS
20 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
20 mils
-----OTHER SIGNALS

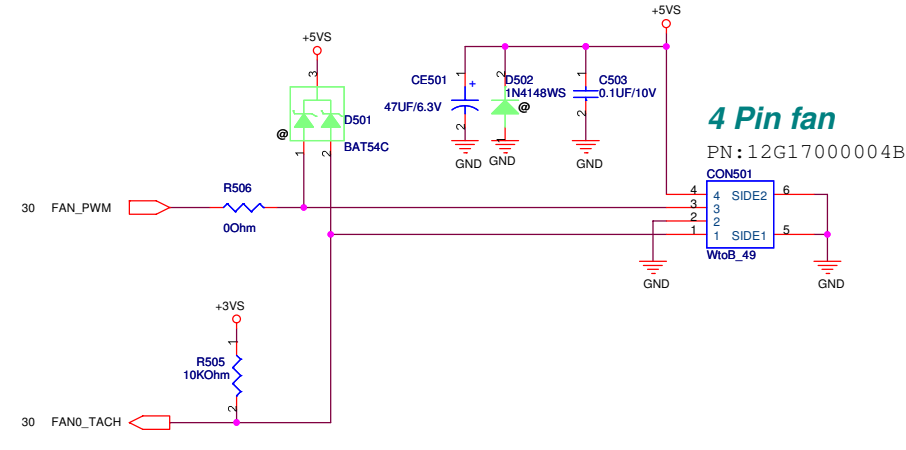
Avoid FSB,Power



H/W Thermal Protect

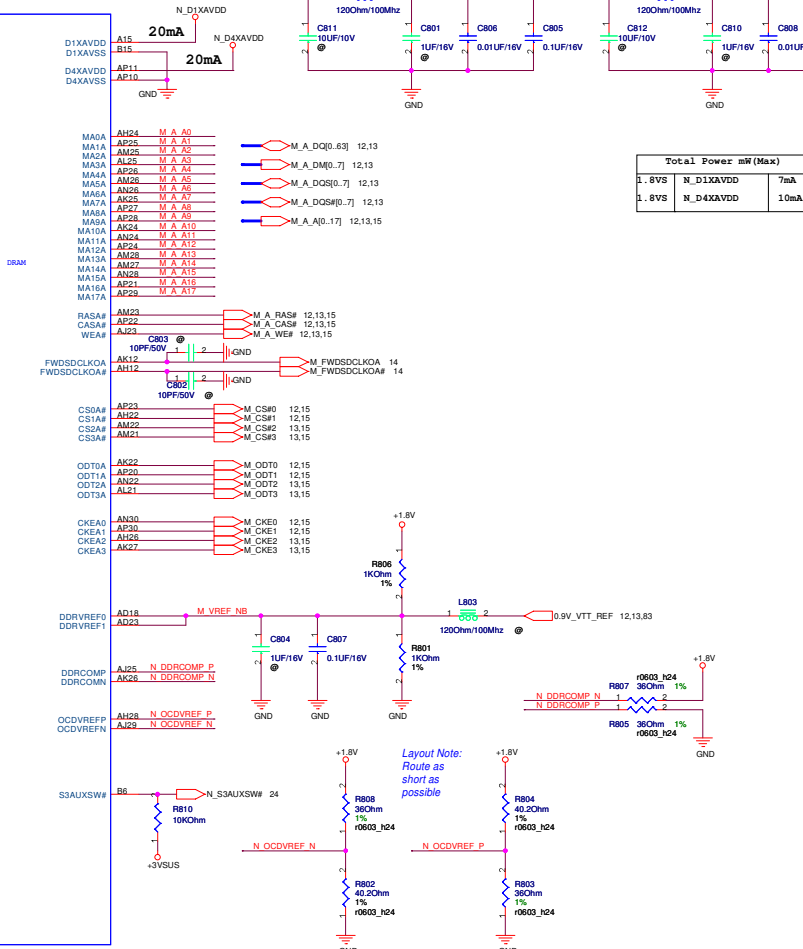


DC FAN Control



ASUS		Title : Thermal Sensor	
ASUSTeK Computer INC		Engineer: WM Chen	
Size A4	Project Name F80S	Date: Wednesday, February 13, 2008	Rev 1.1
Data: Wednesday, February 13, 2008		Sheet 5 of 94	

- M_A_D00 AD0A MD0A
- M_A_D01 AD30 MD10A
- M_A_D02 AG34 MD2A
- M_A_D03 AE32 MD5A
- M_A_D04 AE32 MD5A
- M_A_D05 AE34 MD6A
- M_A_D06 AE31 MD6A
- M_A_D07 AE34 MD6A
- M_A_D08 AE30 MD7A
- M_A_D09 AD28 DM06A
- M_A_D00 AE32 DQ50A
- M_A_D09 AE31 DQ50A
- M_A_D09 AE34 DQ50A
- M_A_D08 AE34 MD8A
- M_A_D09 AE34 MD8A
- M_A_D010 AH31 MD10A
- M_A_D011 AG30 MD12A
- M_A_D012 AE30 MD12A
- M_A_D013 AG32 MD13A
- M_A_D014 AE32 MD14A
- M_A_D015 AH31 MD15A
- M_A_D016 AH34 MD14A
- M_A_D017 AK34 MD18A
- M_A_D018 AE30 MD17A
- M_A_D018 AL32 MD18A
- M_A_D019 AK32 MD19A
- M_A_D020 AK32 MD20A
- M_A_D021 AK34 MD21A
- M_A_D022 AK34 MD22A
- M_A_D023 AL31 MD23A
- M_A_D024 AK32 MD23A
- M_A_D025 AK33 DM02A
- M_A_D025 AL34 DQ52A#
- M_A_D024 AK32 MD24A
- M_A_D025 AP31 MD26A
- M_A_D026 AP31 MD26A
- M_A_D027 AK30 MD27A
- M_A_D028 AK30 MD28A
- M_A_D029 AK29 MD29A
- M_A_D030 AK28 MD30A
- M_A_D031 AK28 MD31A
- M_A_D032 AK28 DM03A
- M_A_D033 AM30 DQ53A#
- M_A_D034 AM31 DQ53A#
- M_A_D035 AK20 MD32A
- M_A_D036 AM20 MD33A
- M_A_D037 AM19 MD34A
- M_A_D038 AM19 MD35A
- M_A_D039 AM18 MD36A
- M_A_D040 AP18 MD37A
- M_A_D041 AP18 MD38A
- M_A_D042 AP17 MD39A
- M_A_D043 AP17 DM04A
- M_A_D044 AP17 DM04A
- M_A_D045 AP18 MD40A
- M_A_D046 AP18 DQ54A#
- M_A_D047 AP17 MD41A
- M_A_D048 AM18 DM05A
- M_A_D049 AM17 DQ55A#
- M_A_D048 AN16 MD48A
- M_A_D049 AK16 MD49A
- M_A_D050 AN14 MD50A
- M_A_D051 AH15 MD51A
- M_A_D052 AP15 MD52A
- M_A_D053 AM16 MD53A
- M_A_D054 AK15 MD54A
- M_A_D055 AP14 MD55A
- M_A_D056 AM15 DM06A
- M_A_D057 AM15 DQ56A#
- M_A_D058 AL13 MD56A
- M_A_D059 AM13 MD57A
- M_A_D060 AM12 MD58A
- M_A_D061 AH14 MD59A
- M_A_D062 AN12 MD60A
- M_A_D063 AH14 MD61A
- M_A_D064 AN12 MD62A
- M_A_D065 AM12 MD63A
- M_A_D066 AP12 DM07A
- M_A_D067 AP12 DQ57A#
- M_A_D068 AP13 DQ57A#



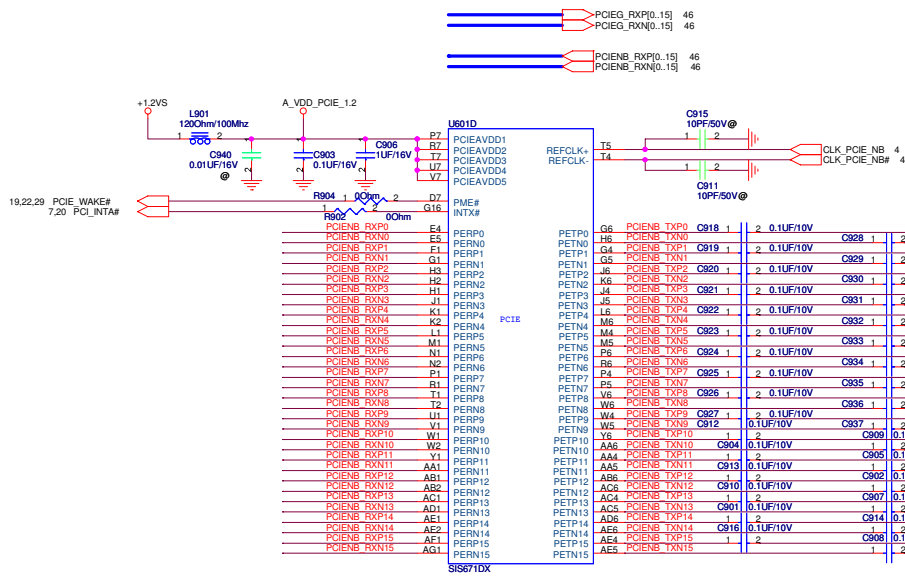
Total Power mW (Max)		
1.8VS	N_D1XAVDD	7mA
1.8VS	N_D4XAVDD	10mA

ASUS Title: M671DX (DDR2)

ASUSTek Computer INC Engineer: WM Chen

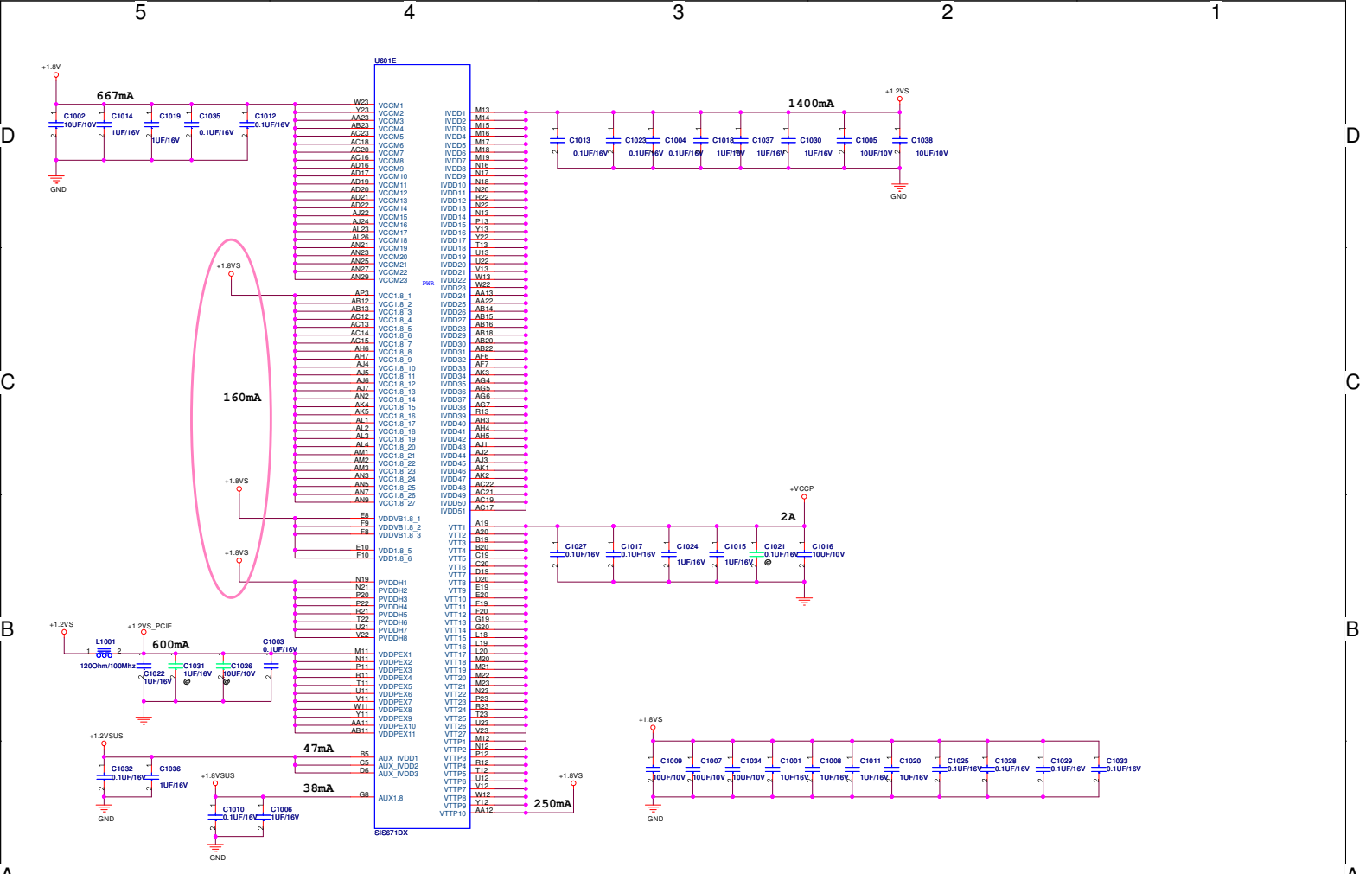
Size	Project Name	Rev
A3	F80S	1.1

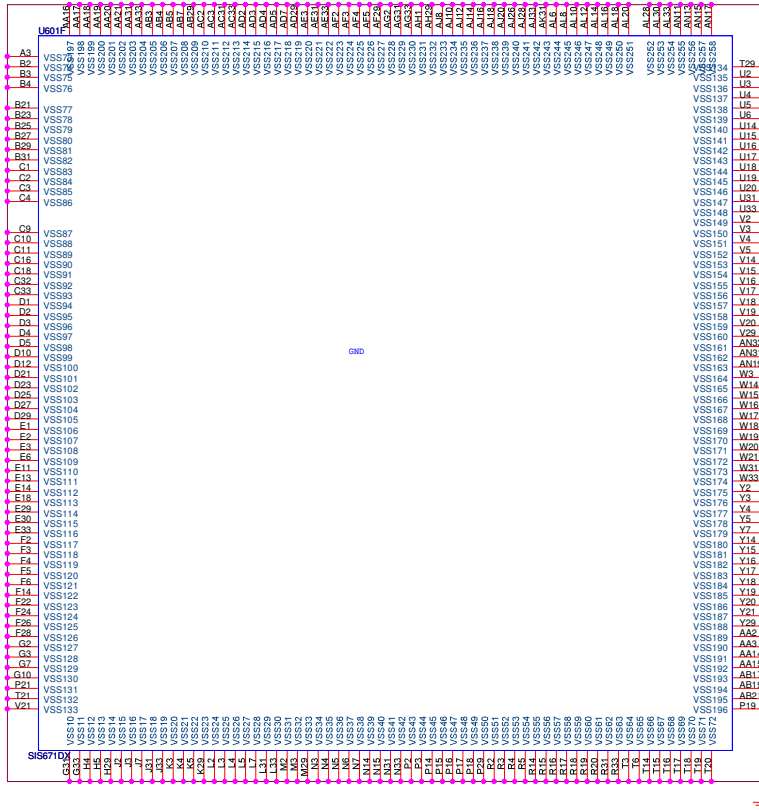
Date: Wednesday, February 13, 2008 Sheet 8 of 94



Pin	Signal	Value	Capacitor	Value	Capacitor	Signal
G6	PCIENB_TXP0	2	C918	0.1UF/10V		PCIENB_RXP0
H6	PCIENB_TXN0	2	C928	0.1UF/10V		PCIENB_RXN0
G4	PCIENB_TXP1	2	C919	0.1UF/10V		PCIENB_RXP1
G5	PCIENB_TXN1	2	C929	0.1UF/10V		PCIENB_RXN1
J6	PCIENB_TXP2	2	C920	0.1UF/10V		PCIENB_RXP2
K6	PCIENB_TXN2	2	C930	0.1UF/10V		PCIENB_RXN2
J4	PCIENB_TXP3	2	C921	0.1UF/10V		PCIENB_RXP3
J5	PCIENB_TXN3	2	C931	0.1UF/10V		PCIENB_RXN3
L6	PCIENB_TXP4	2	C922	0.1UF/10V		PCIENB_RXP4
M6	PCIENB_TXN4	2	C932	0.1UF/10V		PCIENB_RXN4
M4	PCIENB_TXP5	2	C923	0.1UF/10V		PCIENB_RXP5
M5	PCIENB_TXN5	2	C933	0.1UF/10V		PCIENB_RXN5
P6	PCIENB_TXP6	2	C924	0.1UF/10V		PCIENB_RXP6
R6	PCIENB_TXN6	2	C934	0.1UF/10V		PCIENB_RXN6
P4	PCIENB_TXP7	2	C925	0.1UF/10V		PCIENB_RXP7
V6	PCIENB_TXN7	2	C935	0.1UF/10V		PCIENB_RXN7
W6	PCIENB_TXP8	2	C926	0.1UF/10V		PCIENB_RXP8
W5	PCIENB_TXN8	2	C936	0.1UF/10V		PCIENB_RXN8
W4	PCIENB_TXP9	2	C927	0.1UF/10V		PCIENB_RXP9
W5	PCIENB_TXN9	2	C937	0.1UF/10V		PCIENB_RXN9
Y6	PCIENB_TXP10	2	C928	0.1UF/10V		PCIENB_RXP10
Y5	PCIENB_TXN10	2	C938	0.1UF/10V		PCIENB_RXN10
AA6	PCIENB_TXN10	0.1UF/10V	C904			PCIENB_RXN10
AA4	PCIENB_TXP11	1				PCIENB_RXP11
AA5	PCIENB_TXN11	0.1UF/10V	C913			PCIENB_RXN11
AB6	PCIENB_TXP12	1				PCIENB_RXP12
AC6	PCIENB_TXN12	0.1UF/10V	C910			PCIENB_RXN12
AC4	PCIENB_TXP13	1				PCIENB_RXP13
ACS	PCIENB_TXN13	0.1UF/10V	C901			PCIENB_RXN13
AD6	PCIENB_TXP14	1				PCIENB_RXP14
AE6	PCIENB_TXN14	0.1UF/10V	C916			PCIENB_RXN14
AE4	PCIENB_TXP15	1				PCIENB_RXP15
AE5	PCIENB_TXN15	2				PCIENB_RXN15

ASUS Title: M6710X (PCI-E)
 ASUSTeK Computer INC Engineer: WM Chen
 Size: Custom Project Name: F80S Rev: 1.1
 Date: Wednesday, February 13, 2008 Sheet: 9 of 94

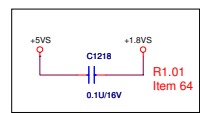
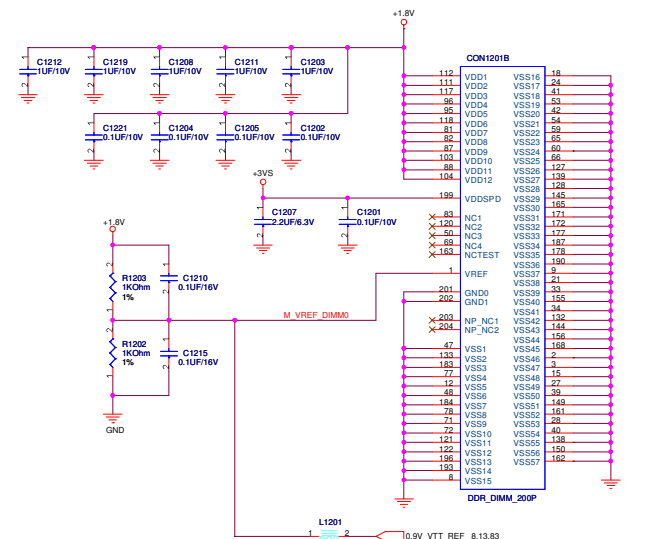
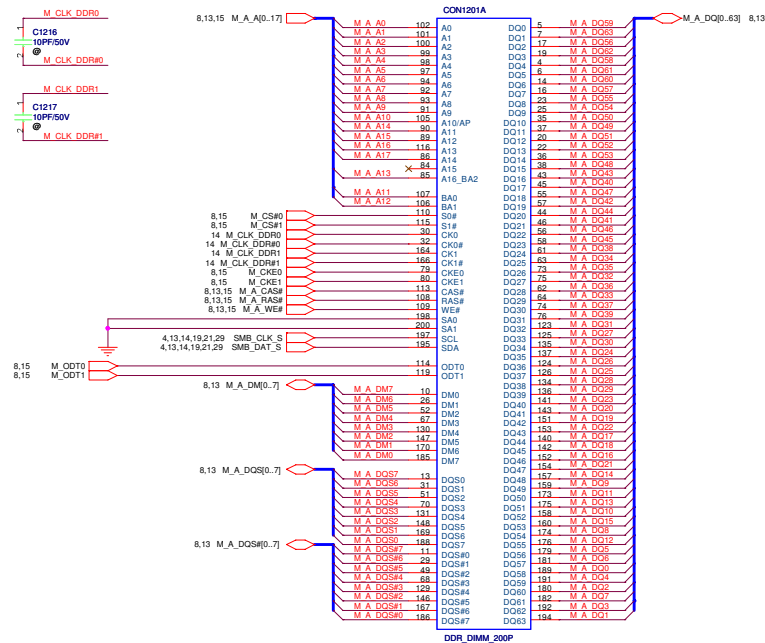




ASUS Title : M671DX (GND)
 ASUSTeK Computer INC Engineer: WM Chen
 Size Project Name Rev
 Custom F80S 1.1
 Date: Wednesday, January 30, 2008 Sheet 11 of 94

Reverse Type

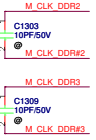
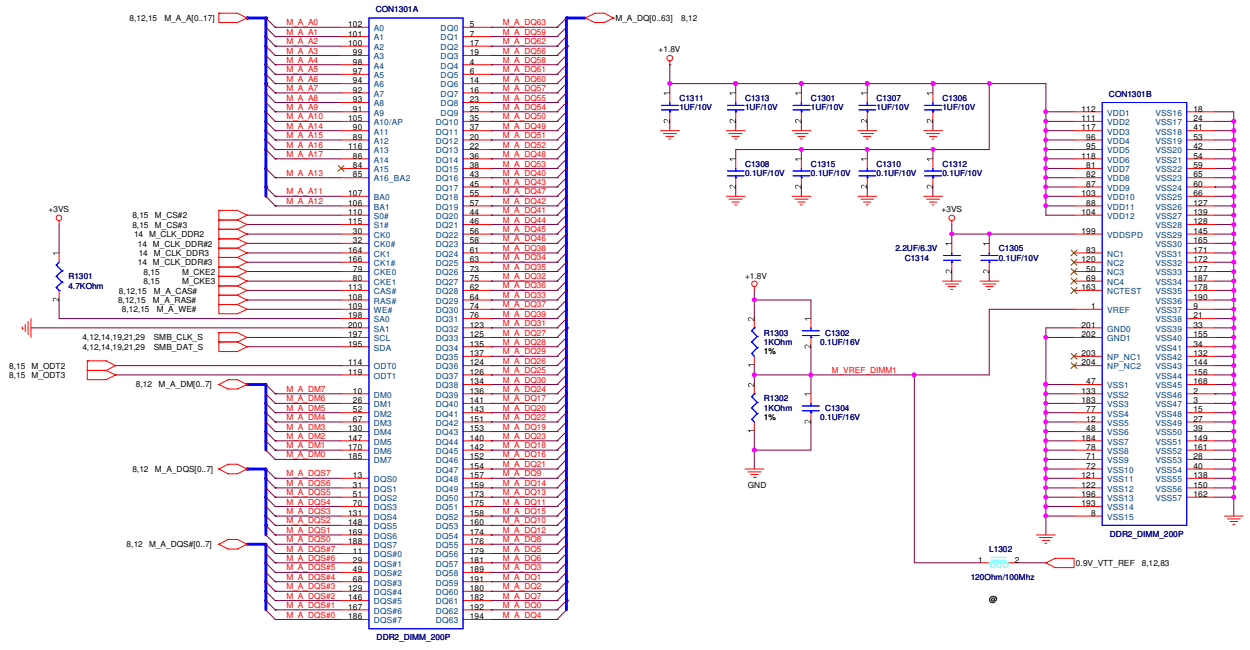
R0.4
Item 30
P/N : 12G025122006 H:5.2mm



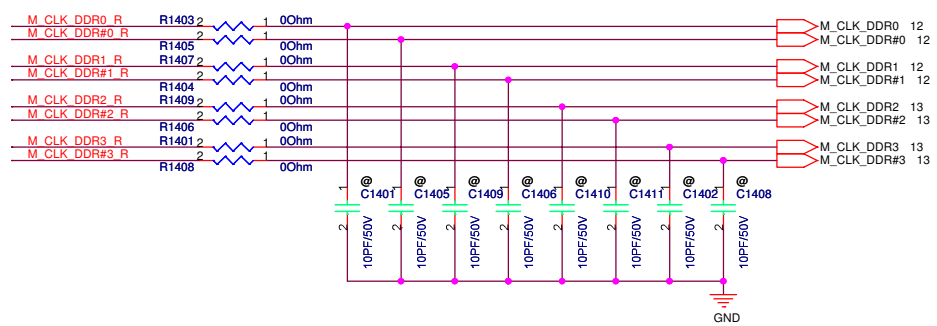
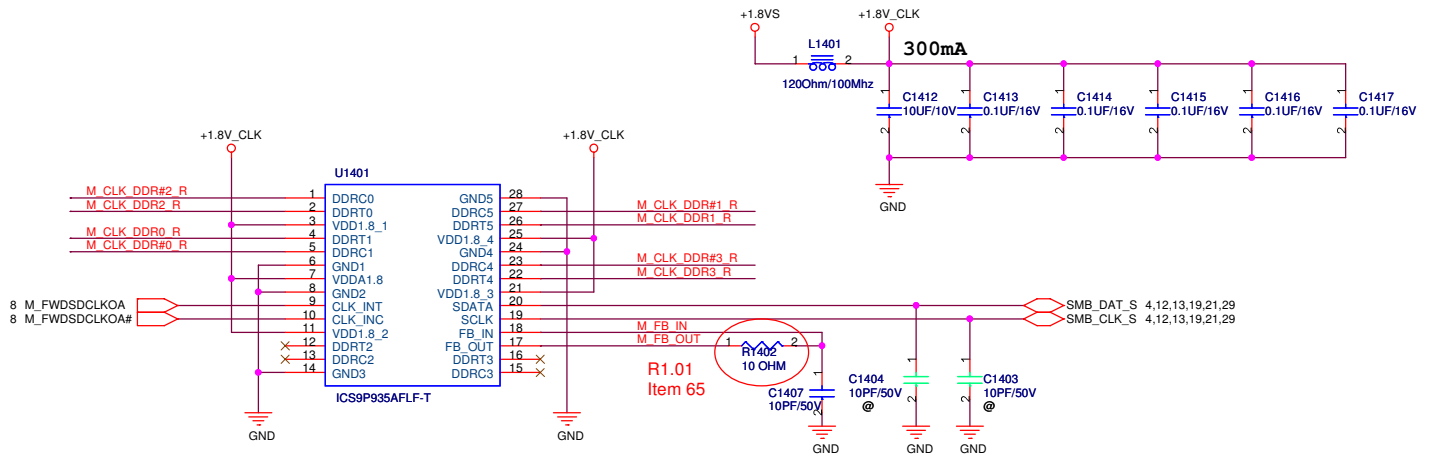
ASUS Title : DDR2 SO-DIMM1
 ASUSTeK Computer INC Engineer: *WM Chen*
 Size Project Name Rev
 A3 F80S 1.1
 Date: Wednesday, February 13, 2008 Sheet 12 of 94

R0.4
Item 30

P/N : 12G025C22002 H:9.2mm

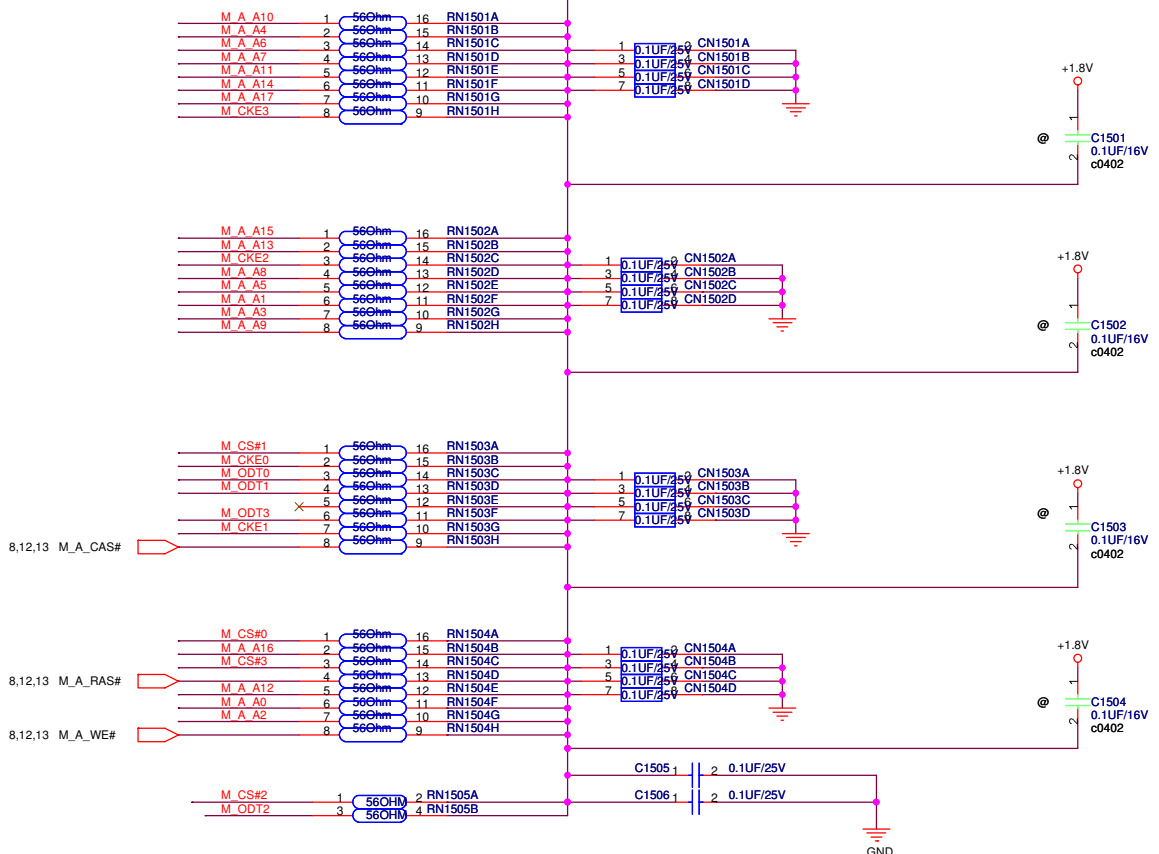


ASUS Title : DDR2 SO-DIMM2
 ASUSTeK Computer Inc. Engineer: WM Chen
 Size: A3 Project Name: F80S Rev: 1.1
 Date: Wednesday, February 13, 2008 Sheet: 13 of 34



ASUS		Title : DDR2 BUFFER	
ASUSTeK Computer INC		Engineer: WM Chen	
Size A4	Project Name F80S		Rev 1.1
Date: Wednesday, February 13, 2008		Sheet	14 of 94

8,12,13 M_A_A[17:0]
 8,12,13 M_CKE[0:3]
 8,12,13 M_CS#[0:3]
 8,12,13 M_ODT[0:3]

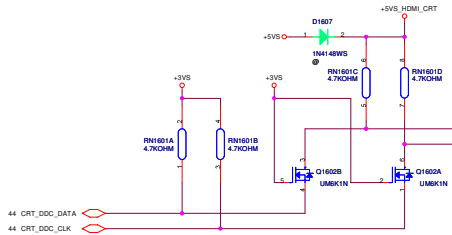
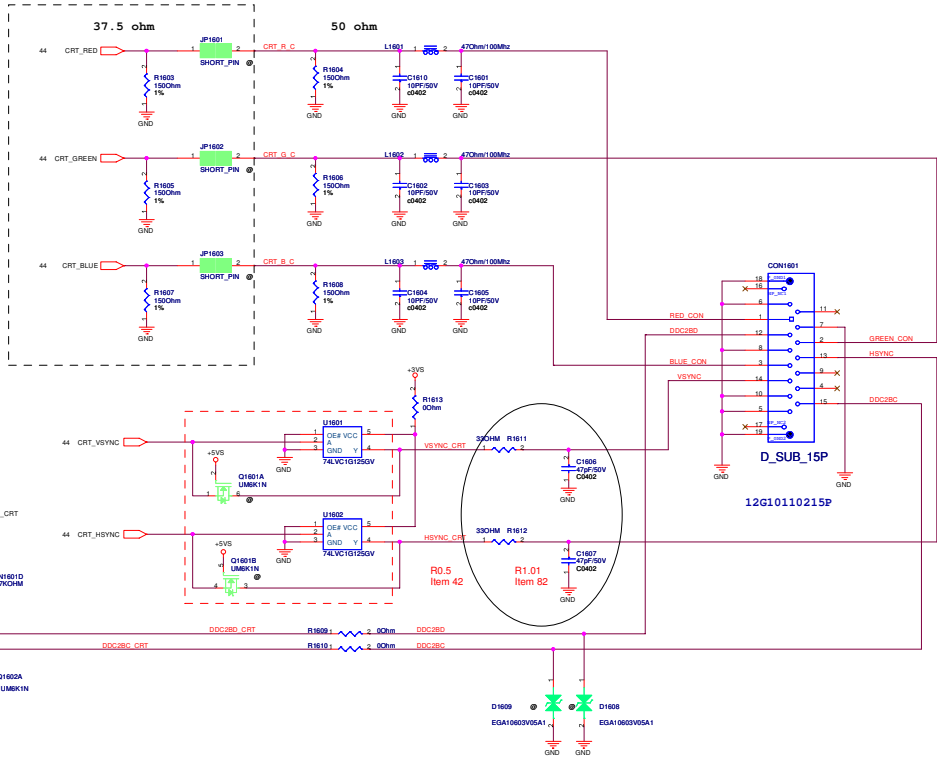
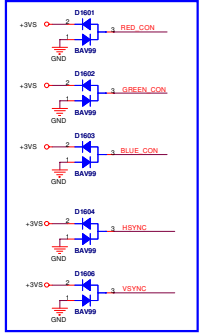


Layout note:
 Place one cap close to every 2 pull-up resistors terminated to +0.9VS

ASUS		Title : DDR2 TERMINATION	
ASUSTeK Computer INC		Engineer: WM Chen	
Size A4	Project Name F80S		Rev 1.1
Date: Wednesday, February 13, 2008		Sheet 15 of 94	

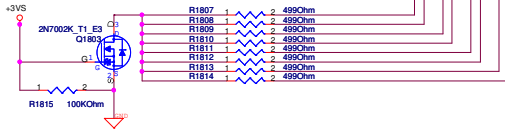
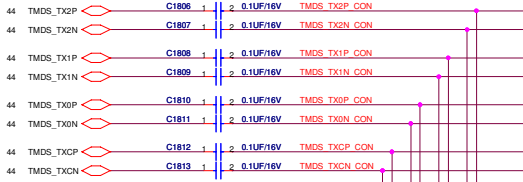
Layout note: Near U4401

PLACE ESD Diodes near connector

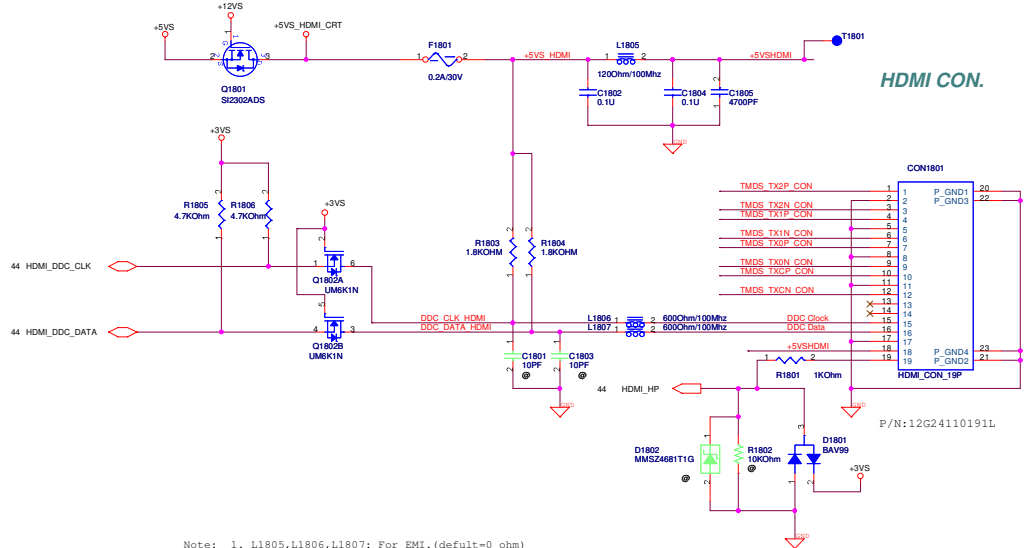
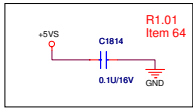


HDMI

near the HDMI connector



Reference should be +5V, but Avl answer that +3VS is fine. As long as it can turn the MOSFET on.



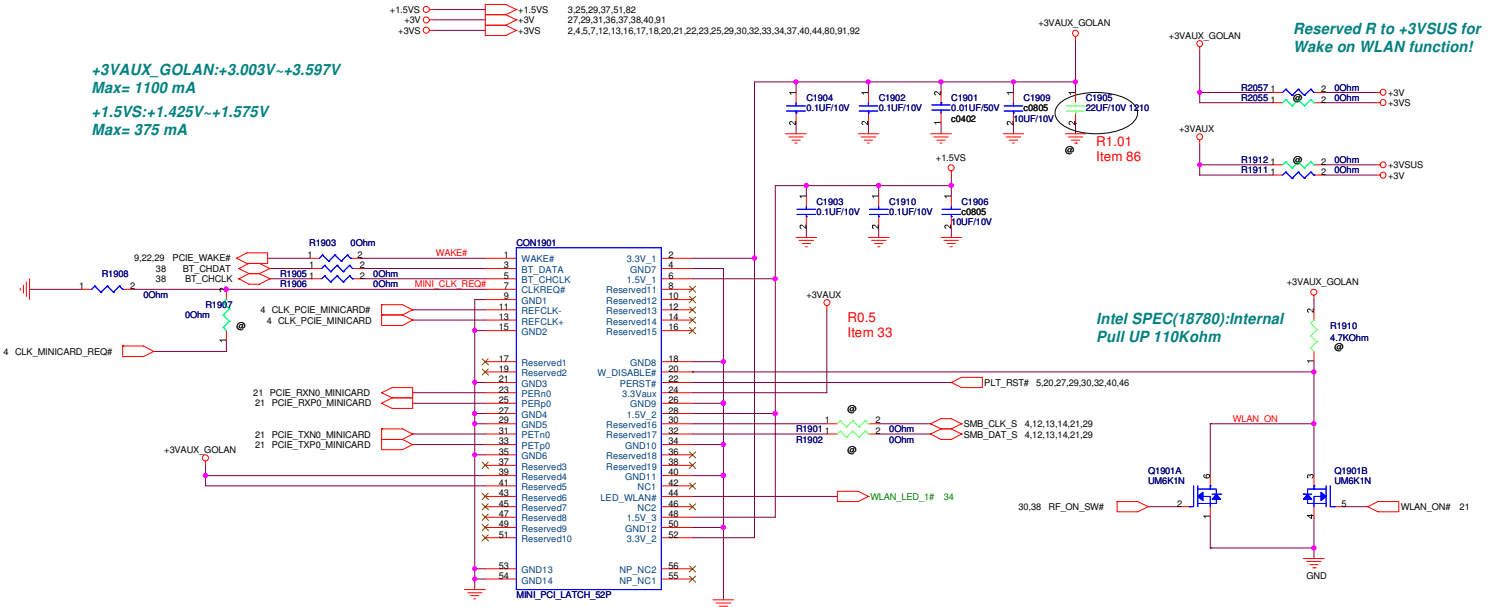
Note: 1. L1805,L1806,L1807: For EMI. (default=0 ohm)
 2. DDC_CLK_HDMI,DDC_DATA_HDMI: +5V tolerant

ASUS		Title : TV & HDMI	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, February 13, 2008	Sheet	18	of 34

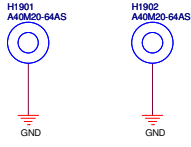
+3VAUX_GOLAN: +3.003V ~ +3.597V
Max= 1100 mA
+1.5VS: +1.425V ~ +1.575V
Max= 375 mA

+1.5VS 3,25,29,37,51,82
 +3V 27,29,31,36,37,38,40,91
 +3VS 2,4,5,7,12,13,16,17,18,20,21,22,23,25,29,30,32,33,34,37,40,44,80,91,92

Reserved R to +3VSUS for Wake on WLAN function!



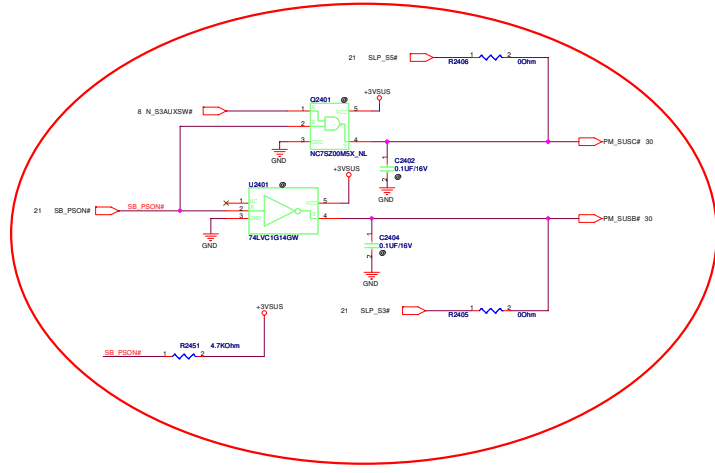
Intel SPEC(18780): Internal Pull UP 110Kohm

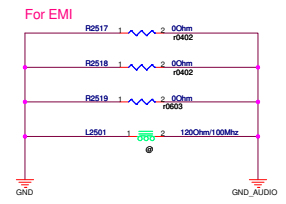
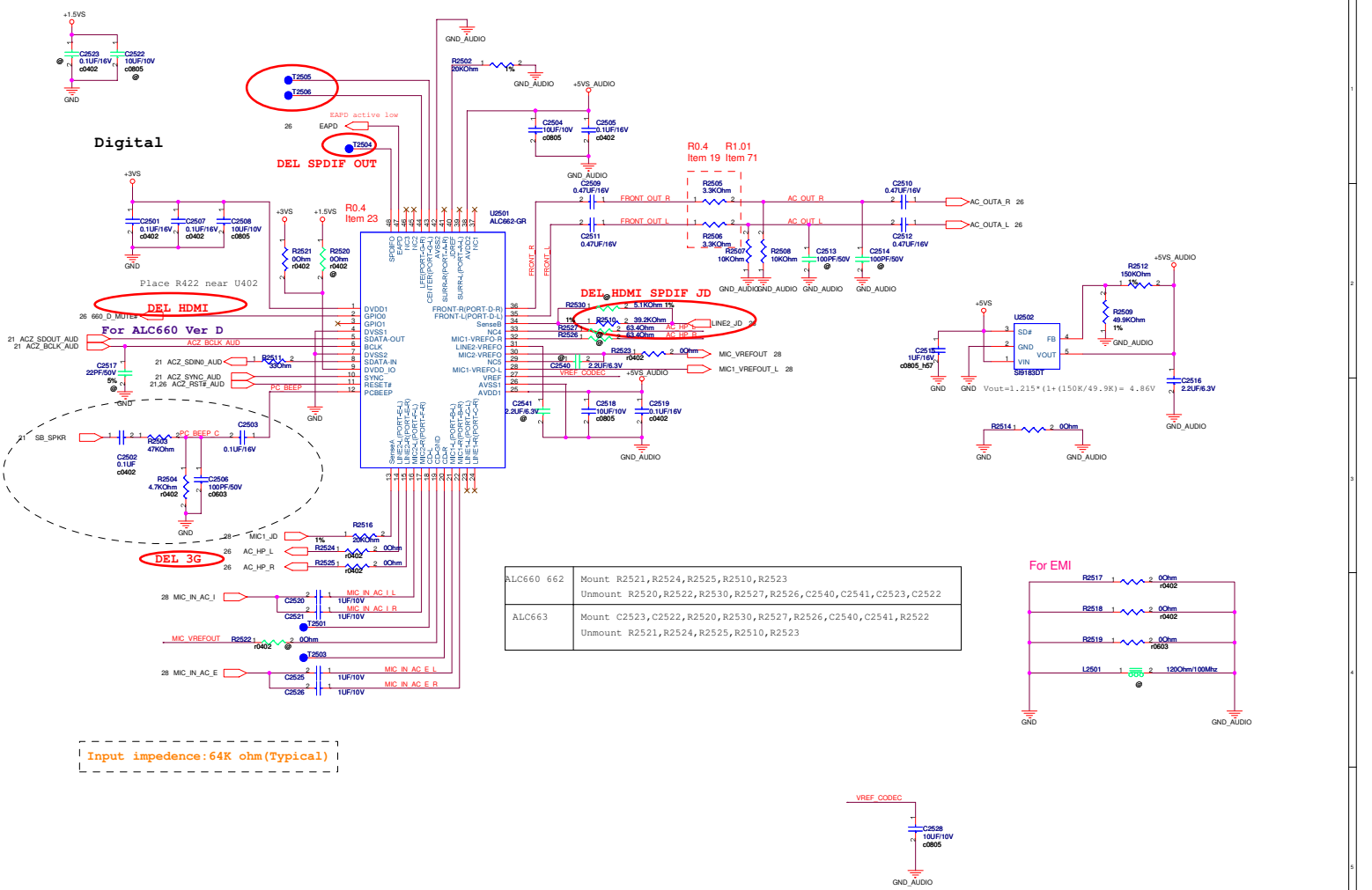


PN: 12G03000052B

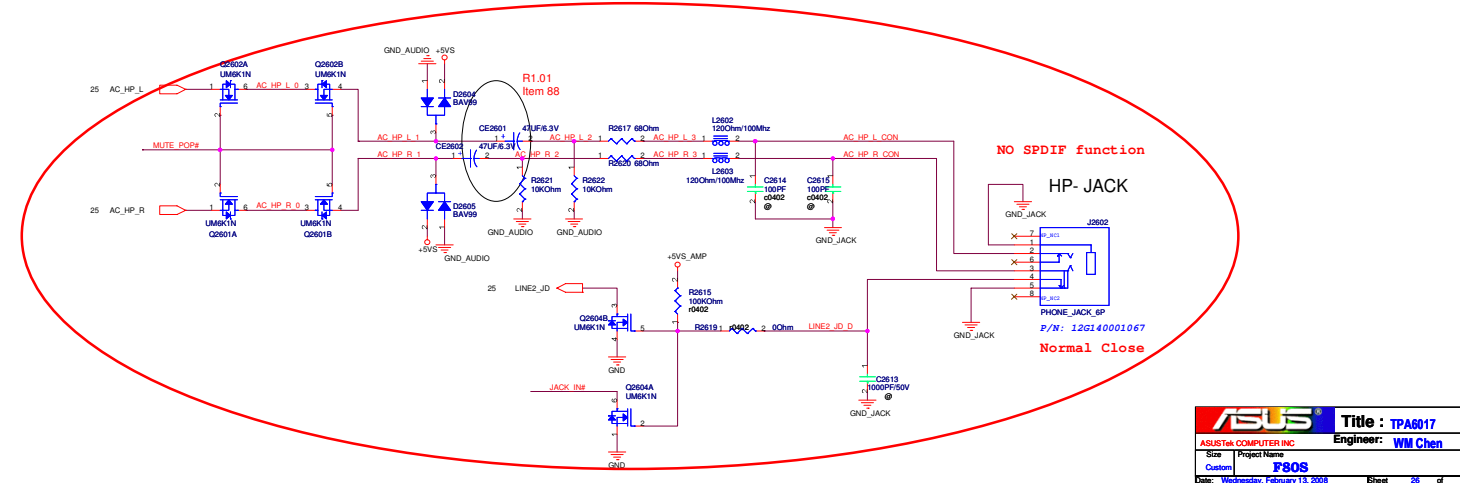
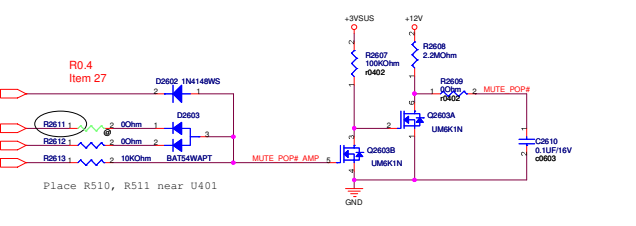
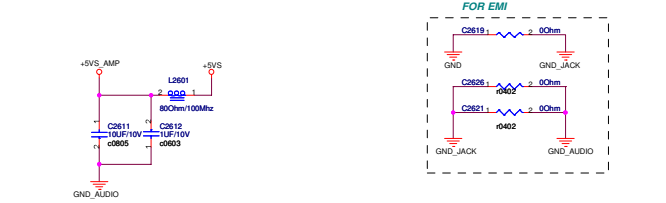
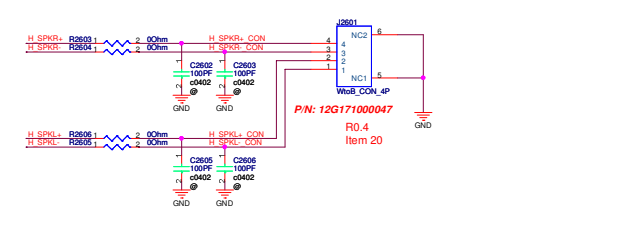
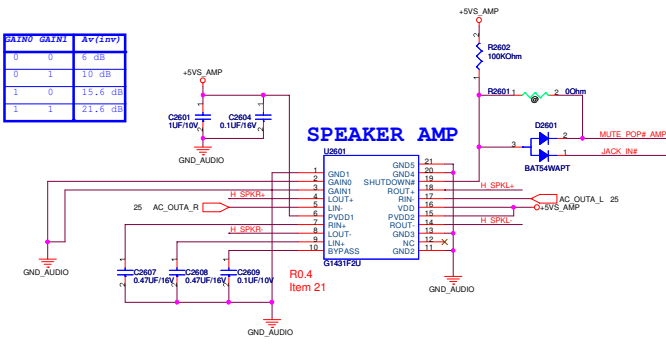
ASUS		Title : Mini card	
ASUSTek Computer INC		Engineer: WM Chen	
Size	Project Name	Rev	
B	F80S	1.1	
Date: Wednesday, February 13, 2008		Sheet	19 of 94

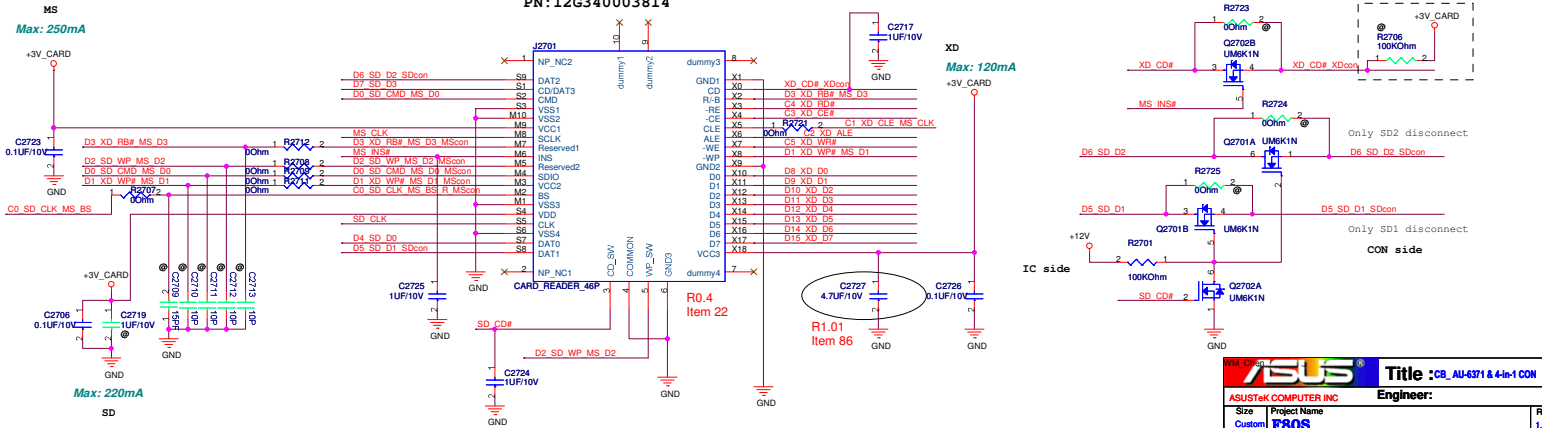
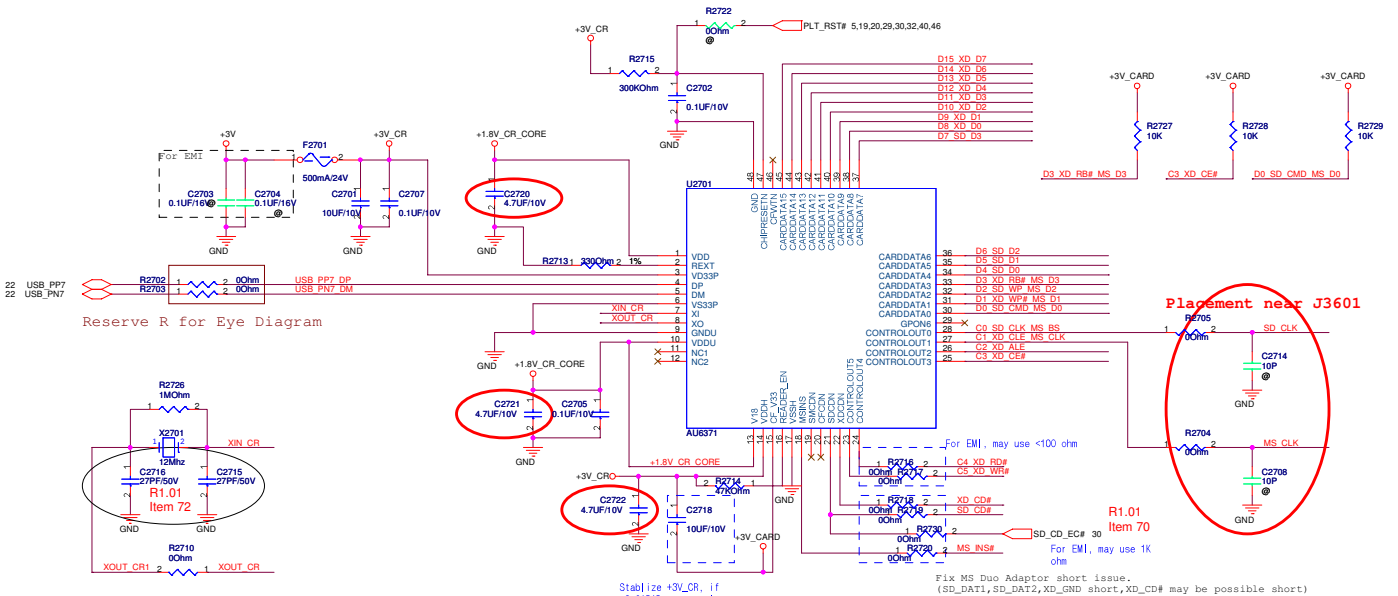
0829 SIS recommend





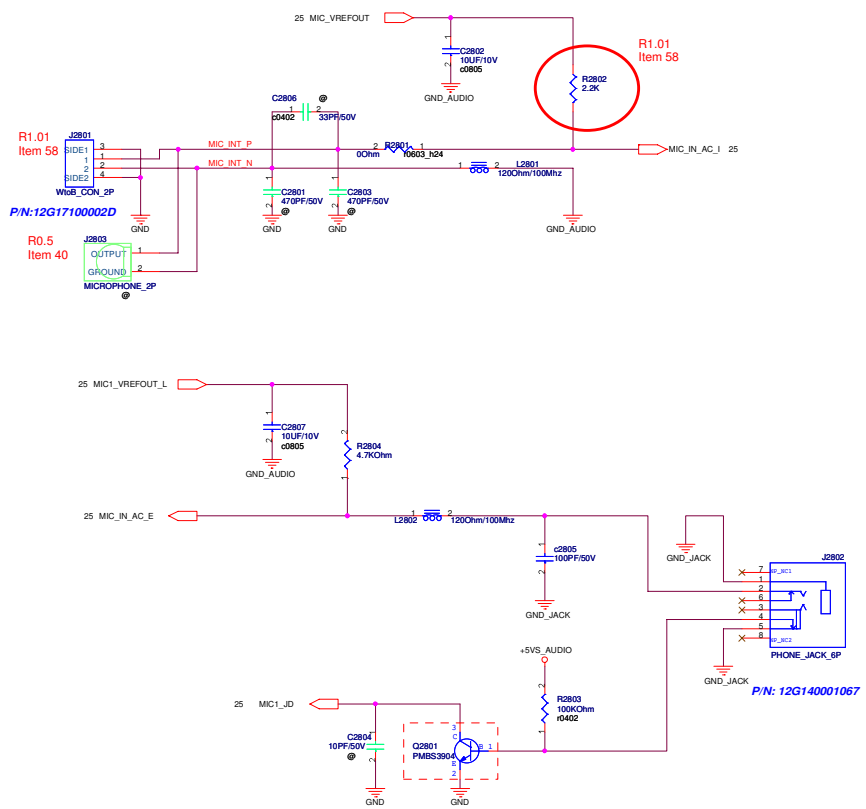
BALNO	GAIN1	Av(dB)
0	0	5 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB





ASUS		Title : CB_AU-4371 & 4-in-1 COM	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Customer	Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008		Sheet 27 of 84	

Internal MIC Pre-Amplifier

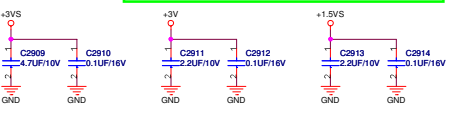
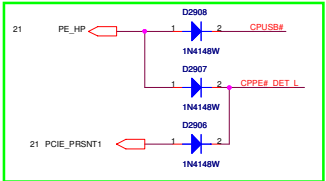
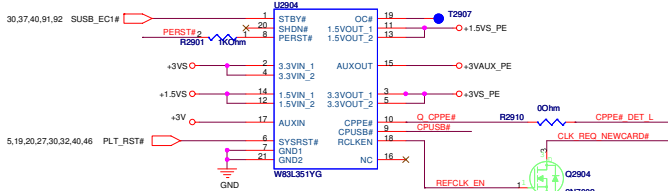


<Variant Name>

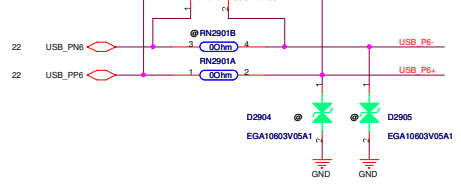
ASUS		Title : MICROPHONE
ASUSTEK COMPUTER INC		Engineer: WM Chen
Size	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, February 13, 2008		Sheet 28 of 34

New EC pin to avoid the re-recognize when resume from S3/S4.

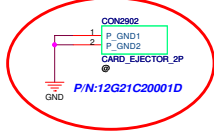
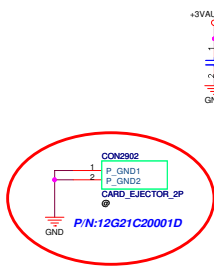
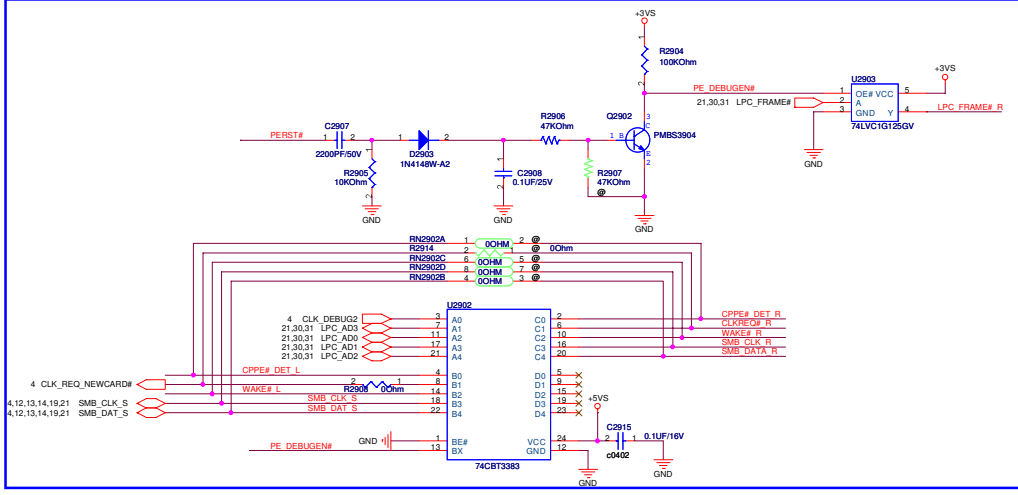
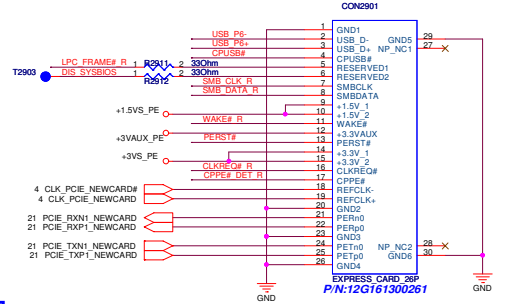
CHANGE TO WINBOND



R1.1 Item 60



NewCard Header



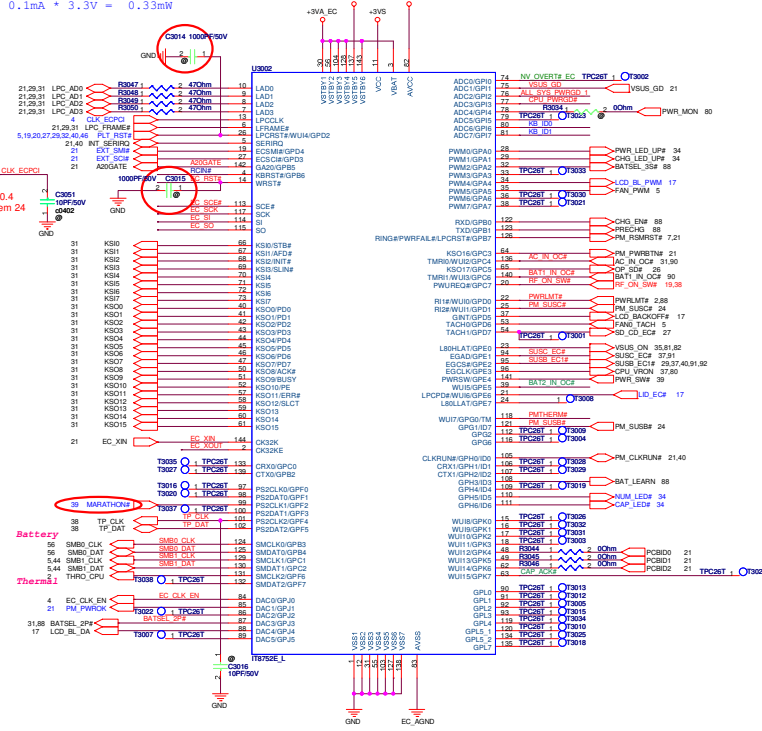
ASUSTek COMPUTER INC.

MM Chen Li-Te Rd. Taichung, Taiwan, ROC

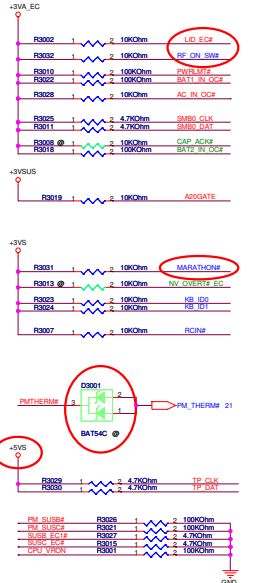
NEW CARD		
Size	Document Number	Rev
Custom	F80S	1.1
Date:	Wednesday, February 13, 2008	Sheet 28 of 84

IT8752 Core Chip

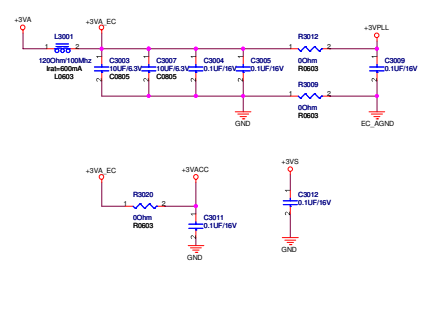
Standby (Sleep) Power Consumption:
0.1mA * 3.3V = 0.33mW



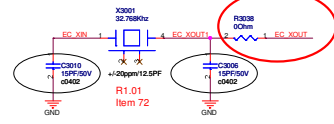
EC Pull-Up/Down



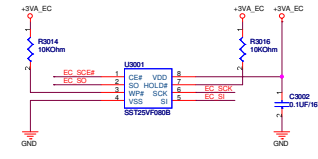
EC Power



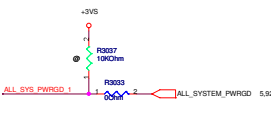
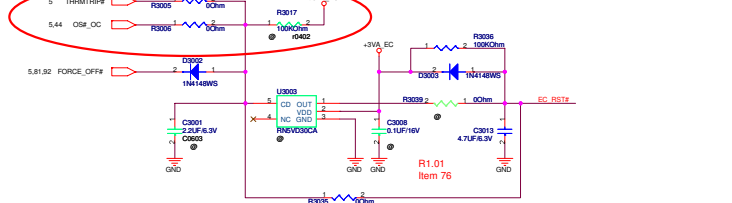
EC XTAL



SPI ROM

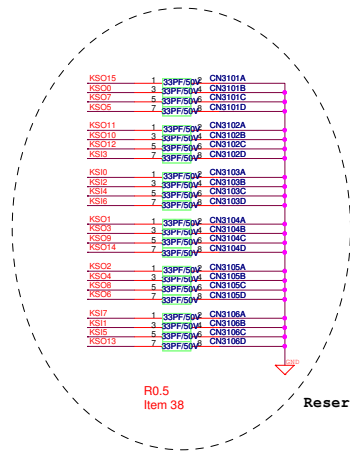
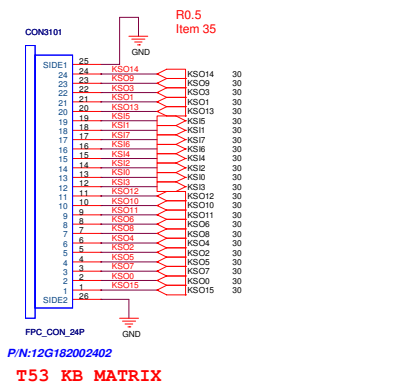


EC Reset

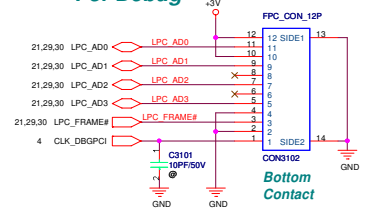


ASUS Title: EC-IT8752
ASUSTEK COMPUTER INC. Engineer:
Size: Project Name:
Date: PCB: P808
Rev: 1.1

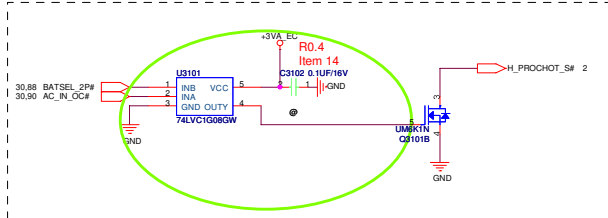
For Keyboard



For Debug



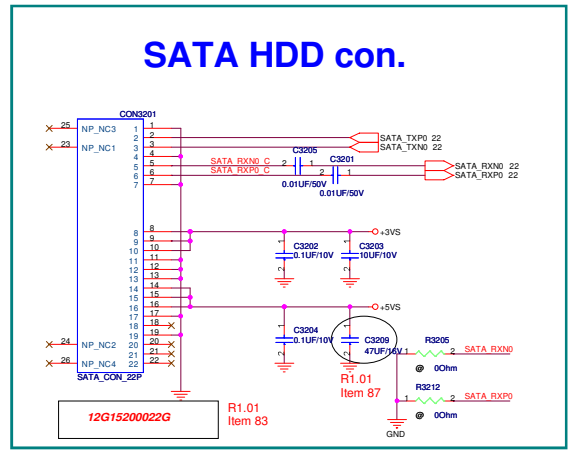
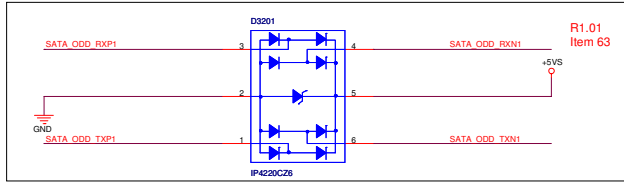
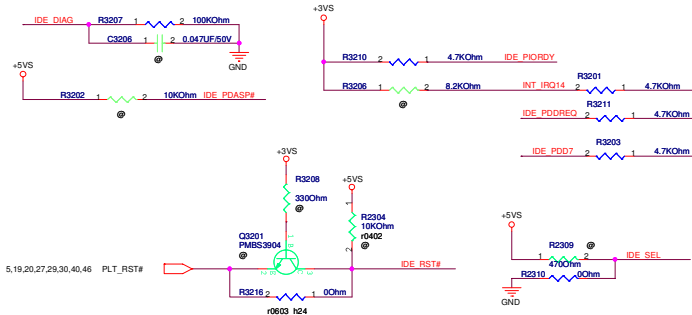
PWRLMT Circuit: For 65W adaptor.



<Variant Name>

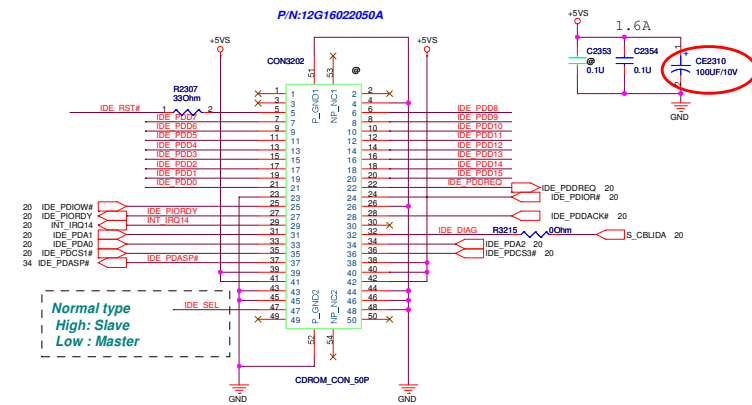
ASUS		Title : KB conn
ASUSTEK COMPUTER INC		Engineer: WM Chen
Site	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, February 13, 2008	Sheet	31 of 34





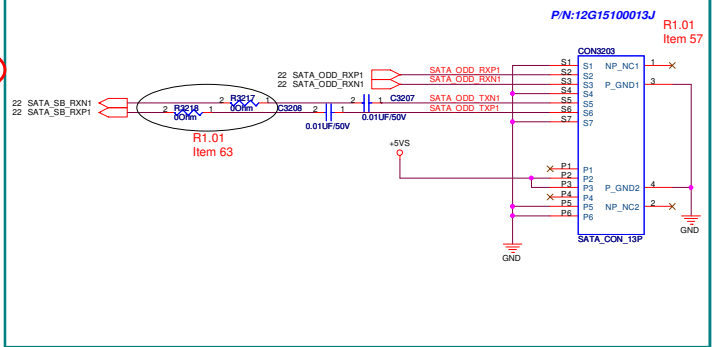
CD-ROM

PATA CD-ROM CON

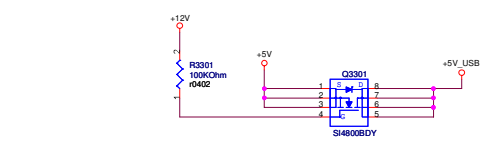
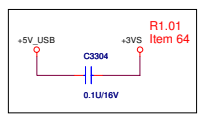
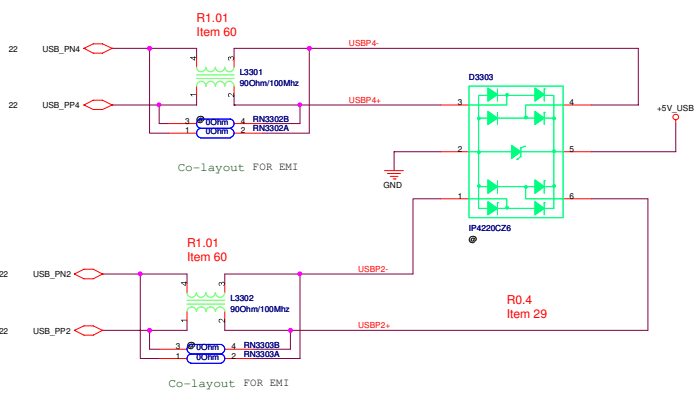


Normal type
High: Slave
Low: Master

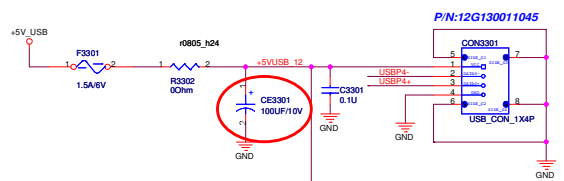
SATA CD-ROM con.



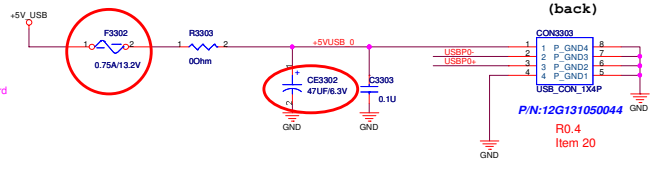
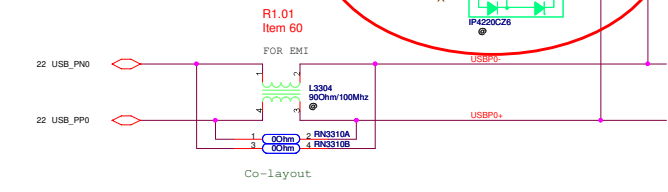
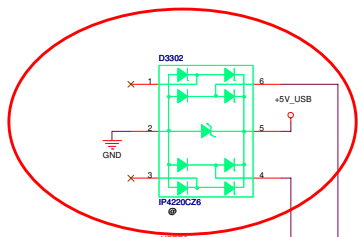
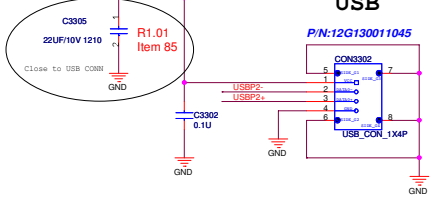
ASUS Title: HDD & CD-ROM
ASUSTEK COMPUTER INC Engineer: WM Chen
Site: Project Name: Review: 1.1
Custom: P80S
Date: Wednesday, February 13, 2008 Sheet: 32 of 34



USB



USB

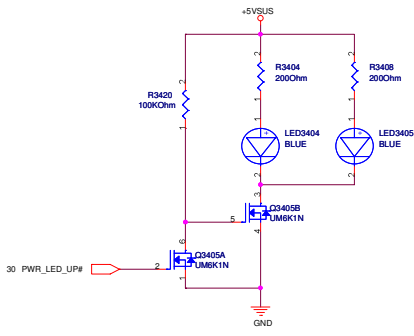


USB (back)

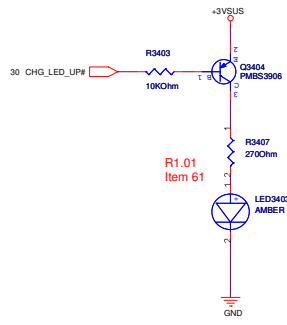
<Variant Name>

ASUS		Title : USB PORTS	
ASUSTeK COMPUTER INC		Engineer: WM Chen	
Site	Project Name	Rev	
Custom	FBOS	1.1	
Date: Wednesday, February 13, 2008		Sheet 33 of 34	

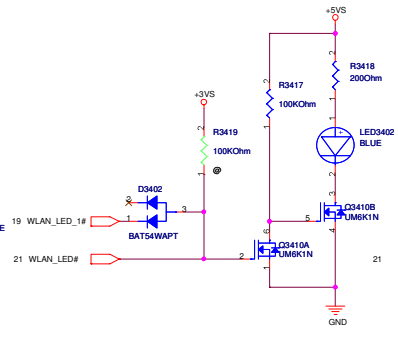
PWR LED



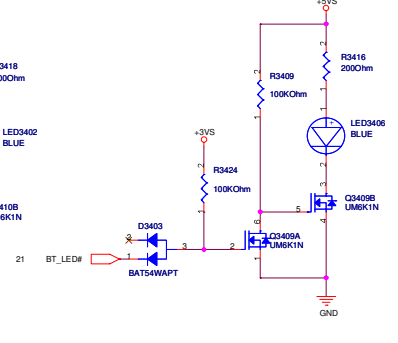
For BATTERY LED



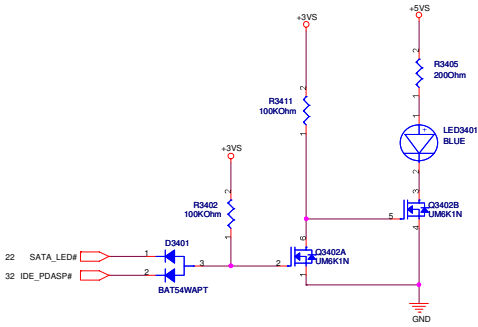
WireLess LED



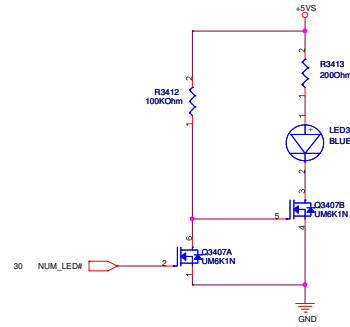
BT LED



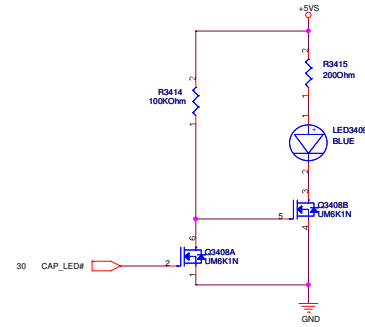
SATA/IDE LED



Num Lock

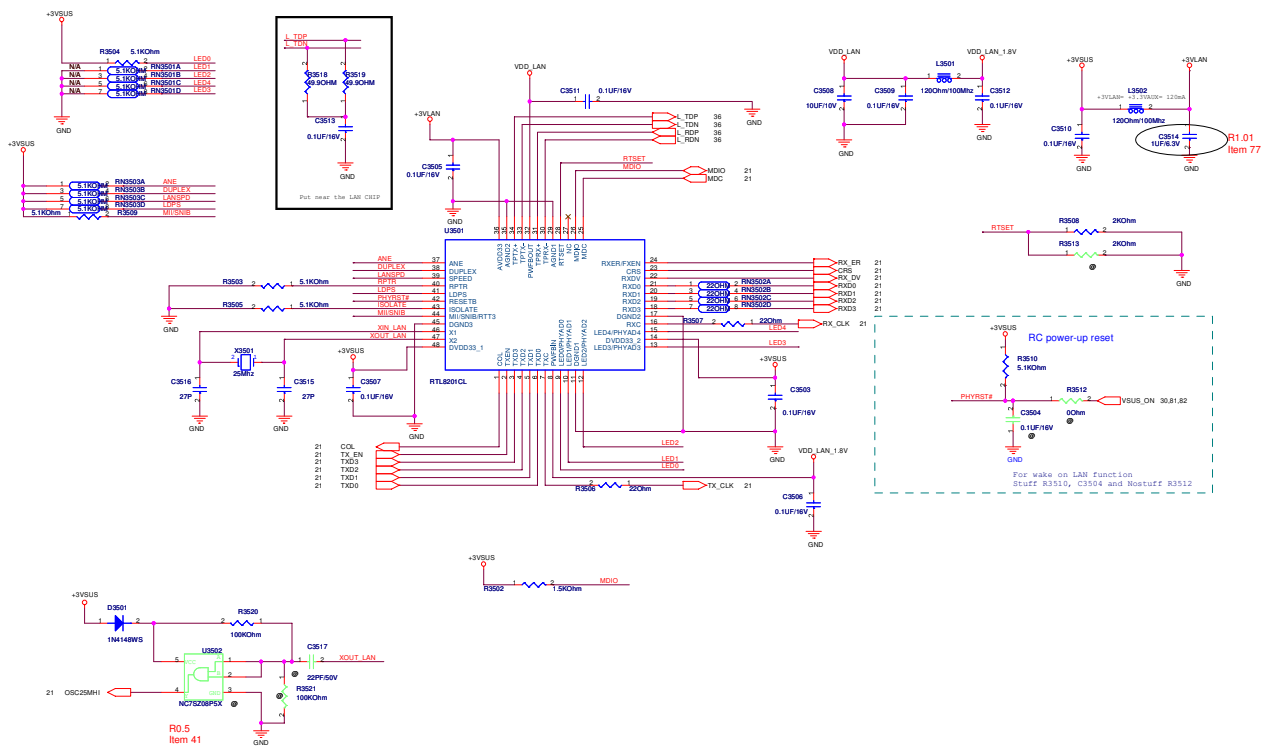


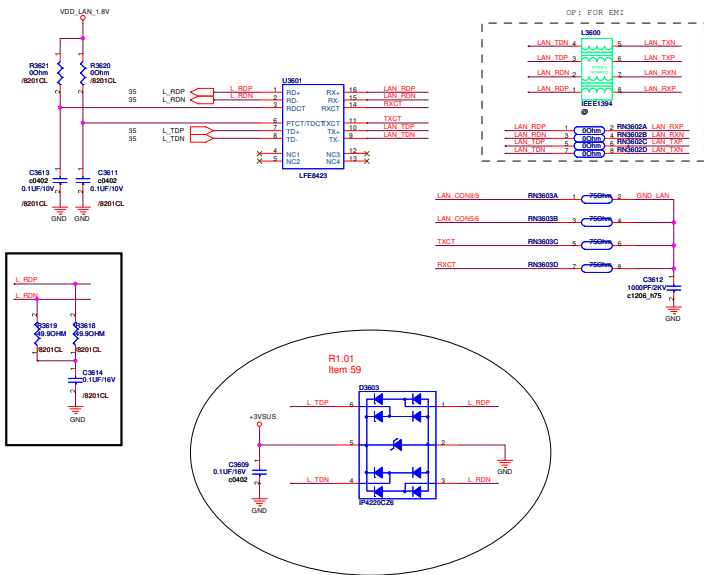
Cap. Lock



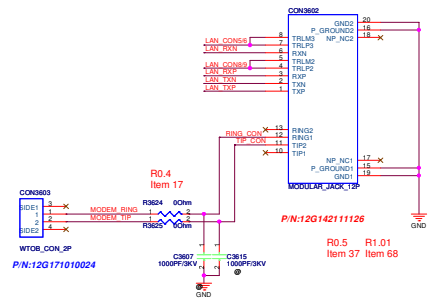
<Variant Name>

ASUS		Title : LED
ASUSTEK COMPUTER INC	Project Name	Engineer: WM Chen
Site	Customer	Rev
	F80S	1.1
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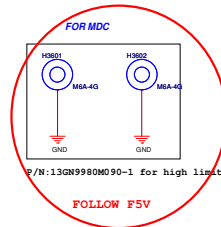
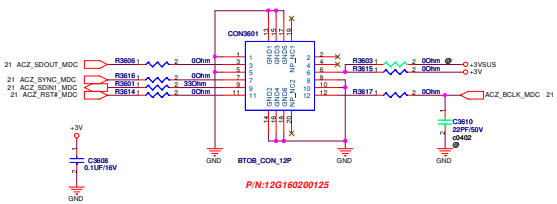




LAN / MODEM PORT

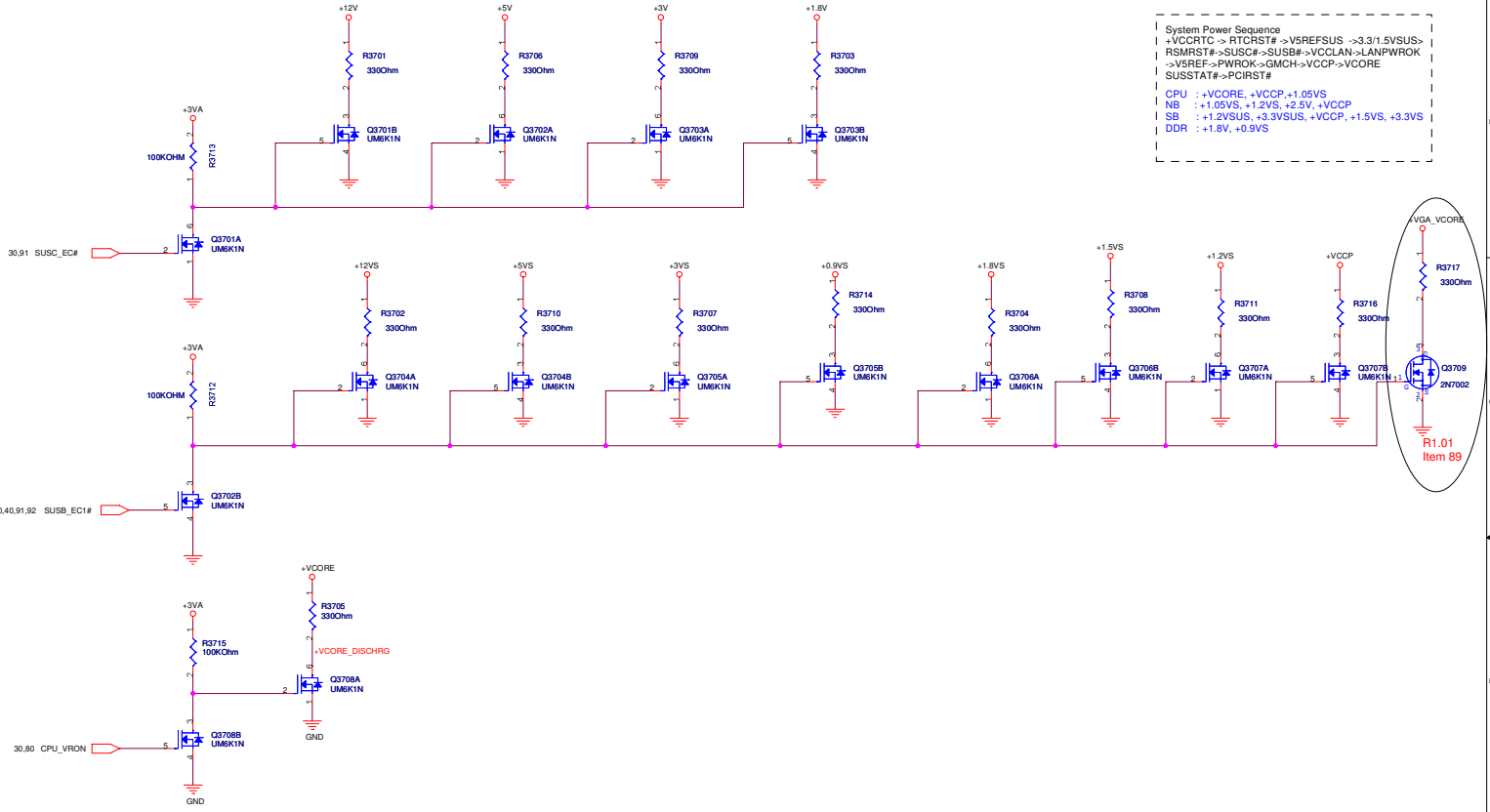


MDC



System Power Sequence
 +VCCRSTC -> RTCRST# -> V5REFSUS -> 3.3/1.5VSUS->
 RSMRST#->SUSC#->SUSB#->VCCLAN->LANPWROK->
 V5REF->PWROK->GMCH->VCCP->VCORE
 SUSSTAT#->PCIRST#

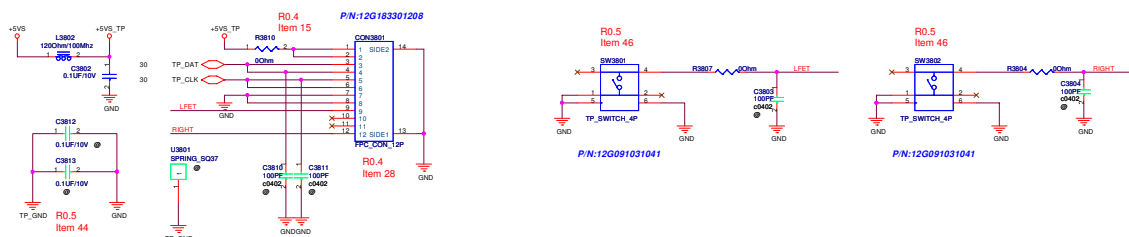
CPU : +VCORE, +VCCP, +1.05VS
 NB : +1.05VS, +1.2VS, +2.5V, +VCCP
 SB : +1.2VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
 DDR : +1.8V, +0.9VS



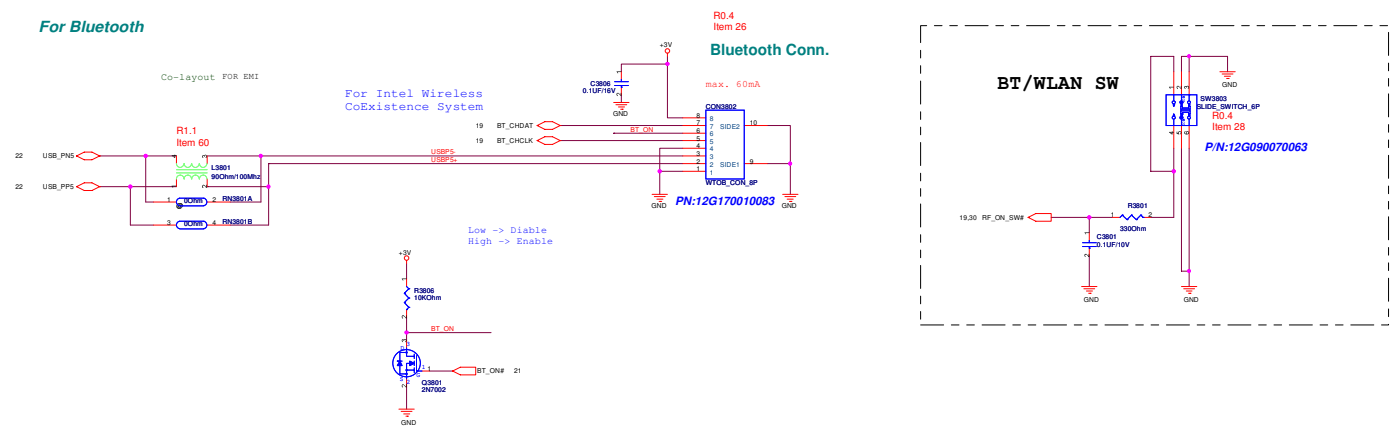
<Variant Name>

ASUS		Title : DISCHARGE CKT	
ASUSTEK COMPUTER INC		Engineer: WM Chen	
Size	Project Name		Rev
Custom	F80S		1.1
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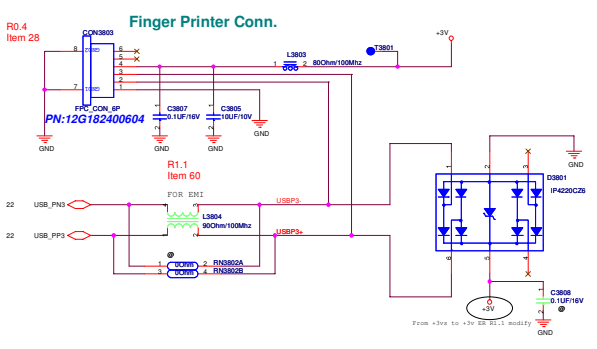
Touch-Pad



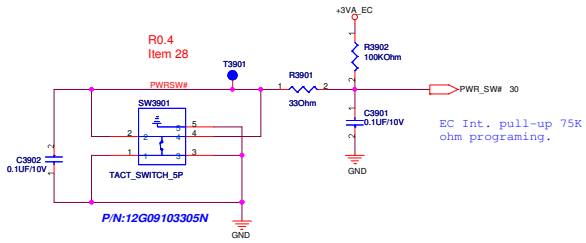
For Bluetooth



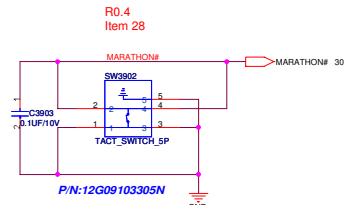
Finger Printer Conn.



Power Button

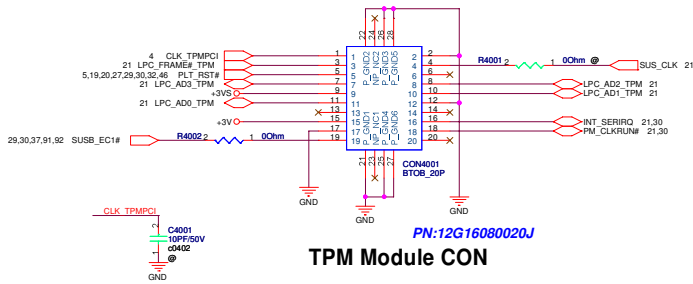


MARATHON#

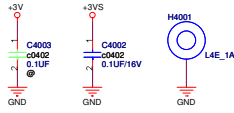


<Variant Name>

ASUS		Title : SWITCH	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Site	Project Name		Rev
Custom	F80S		1.1
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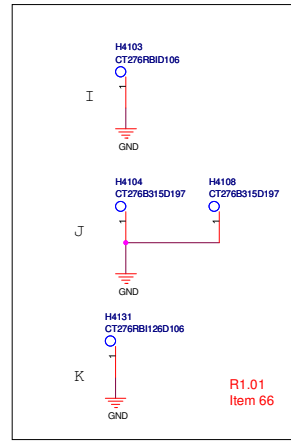
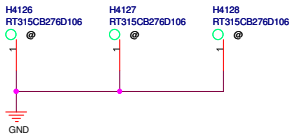
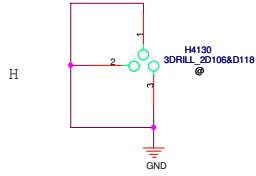
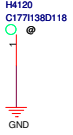
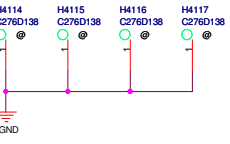
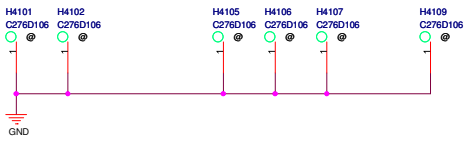
TPM Module CON



<Variant Name>

		Title : TPM	
ASUSTek COMPUTER INC. NBI		Engineer: WM Chen	
Site	Project Name	Rev	
Custom	F80S	1.1	
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Item 36

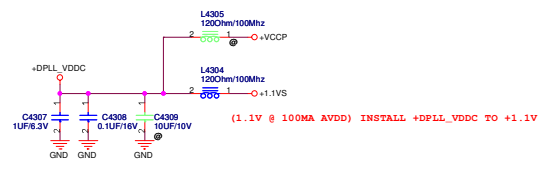
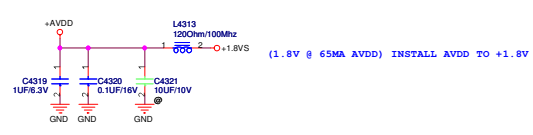
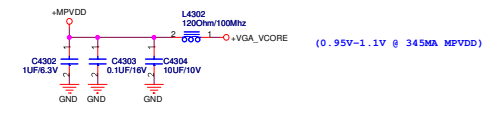
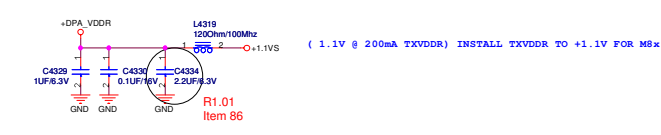
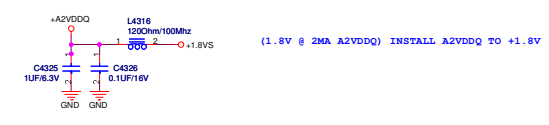
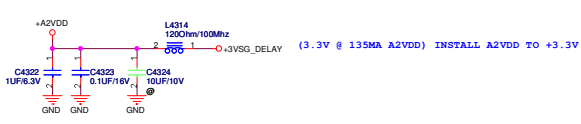
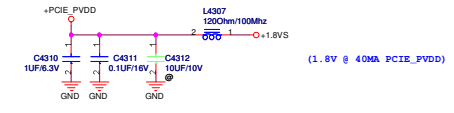


		Title : Screw hole	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>WM Chen</i>	
Size	Project Name		Rev
B	F80S		1.1
Date: Wednesday, January 30, 2008		Sheet	41 of 94



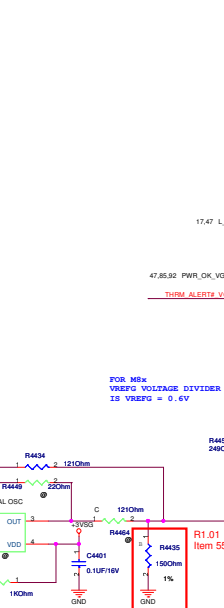
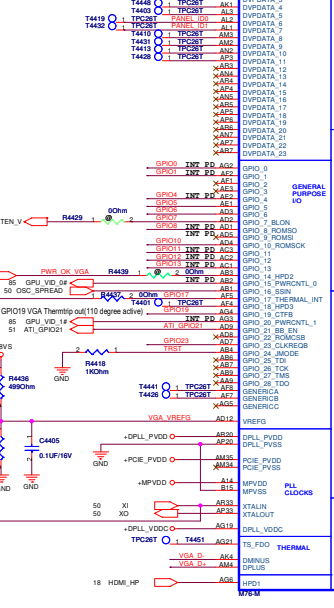
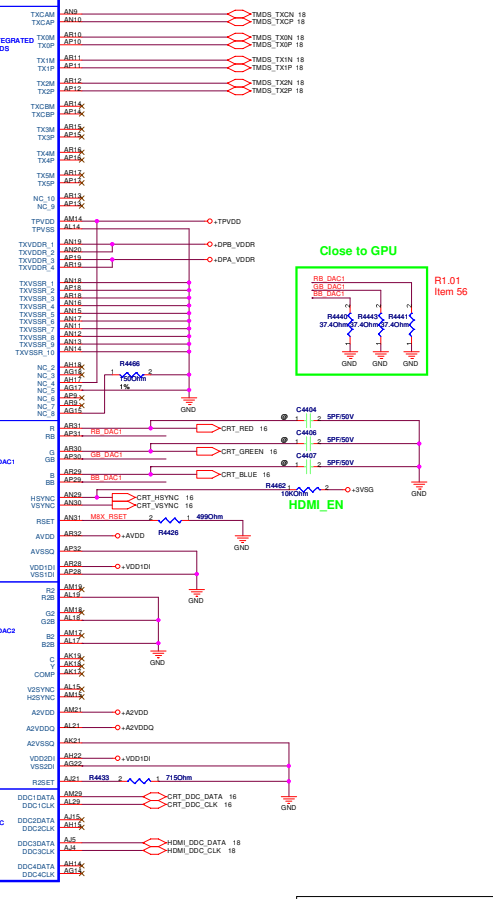
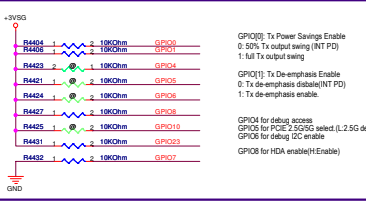
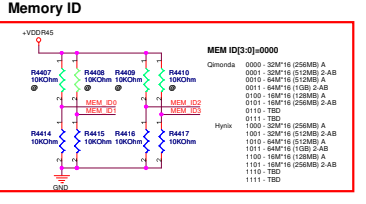
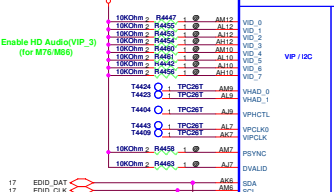
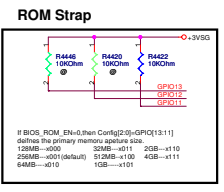
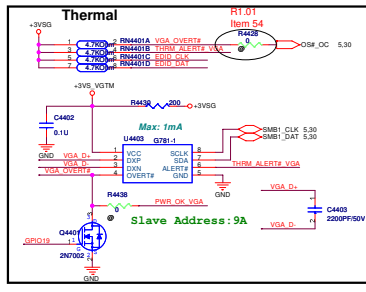
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ASUSTek COMPUTER INC		Engineer: WM Chen	
Size	Project Name		Rev
Custom	F80S		1-1
Date: Wednesday, February 13, 2008		Sheet	42 of 84

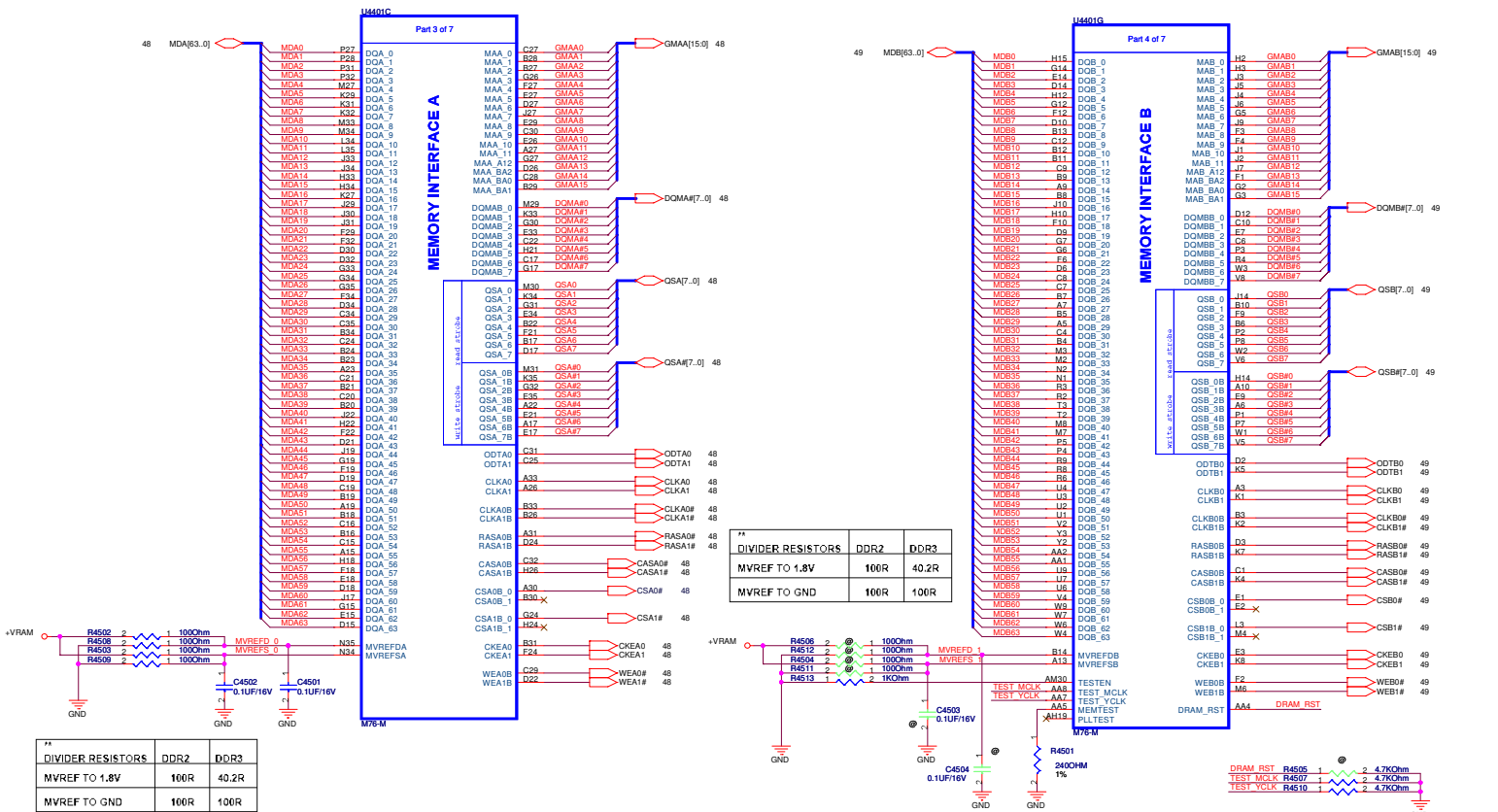
M8x Power
PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE

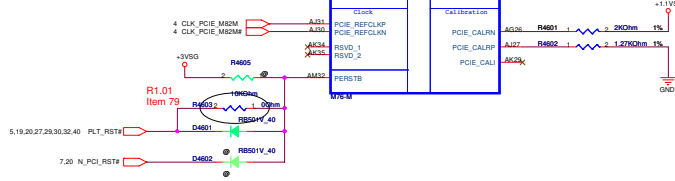
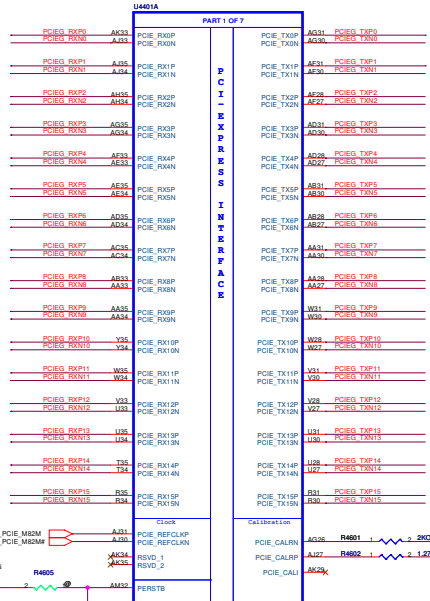
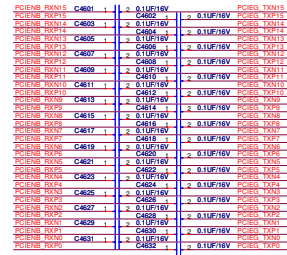
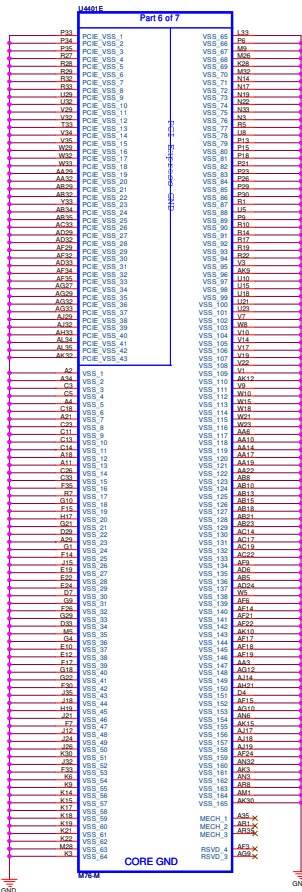


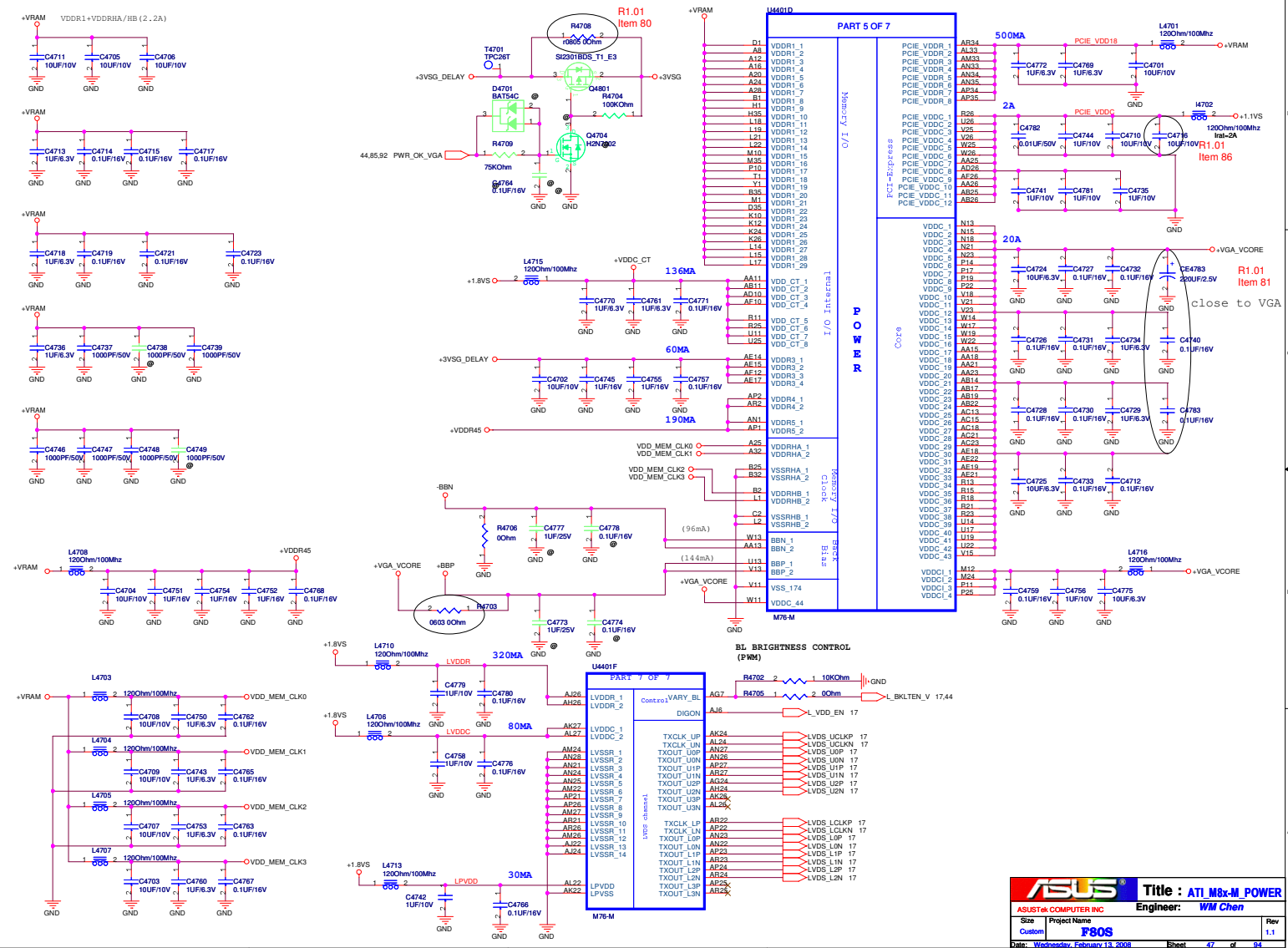
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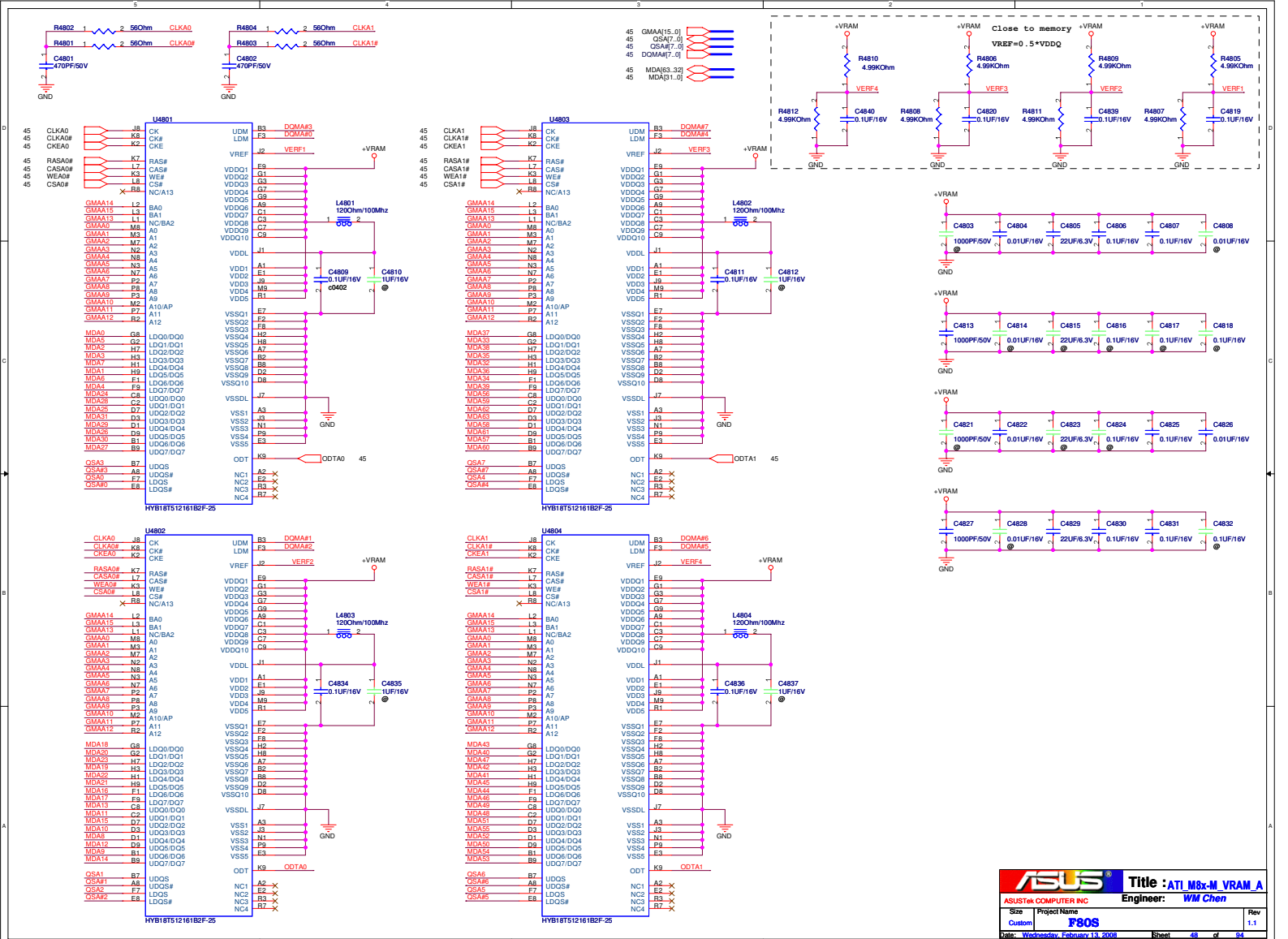
ASUS		Title : VGA M8x-M POWER	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Site	Project Name	Rev	
Custom	F80S	1.1	
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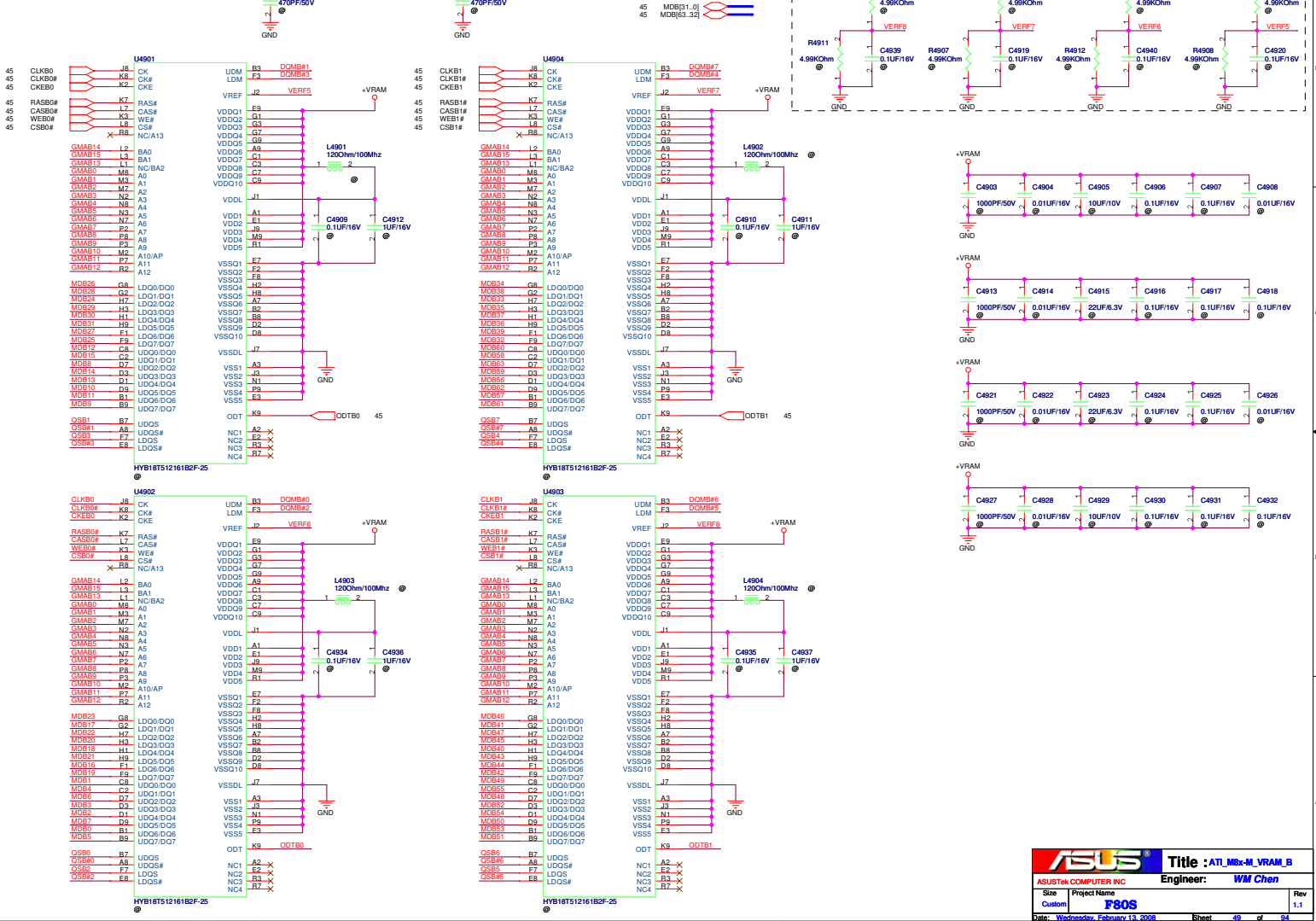




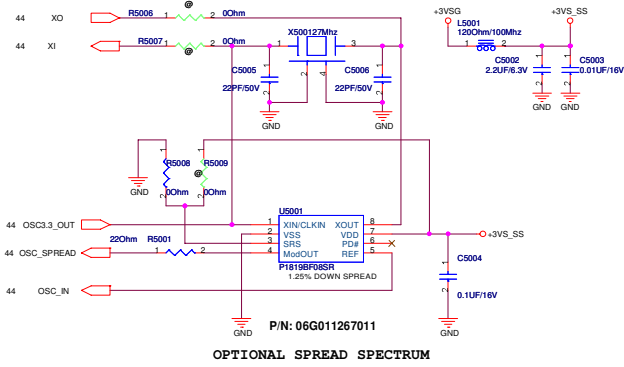




DO NOT INSTALL CHANNEL B WITH M82M

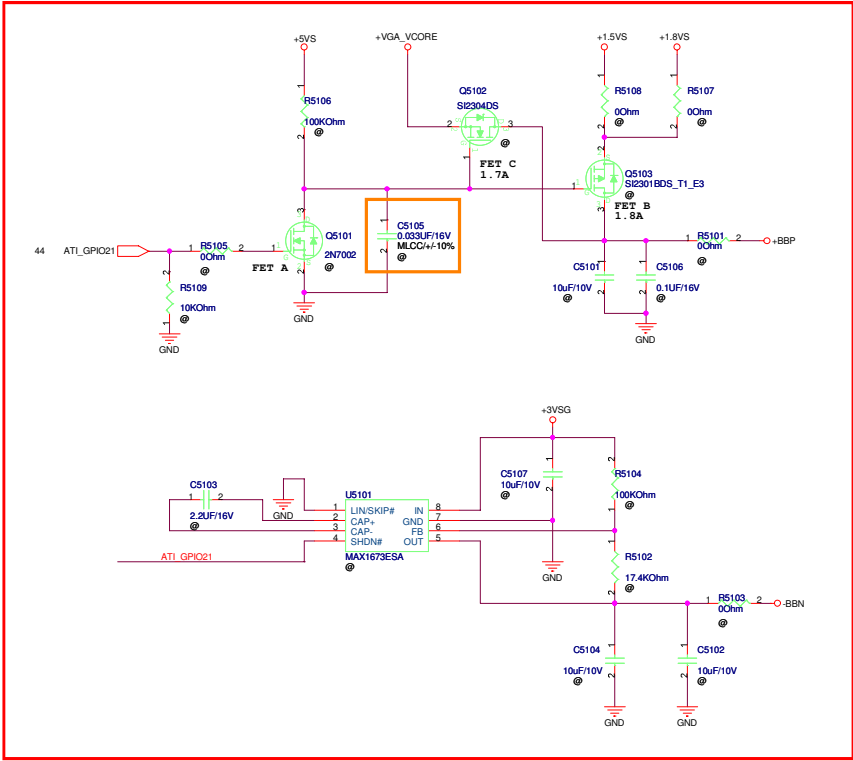


		Title : AT1_MBx-M_VRAM_B	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, February 13, 2008		Sheet	49 of 54



**COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED**

R0.4
Item 30



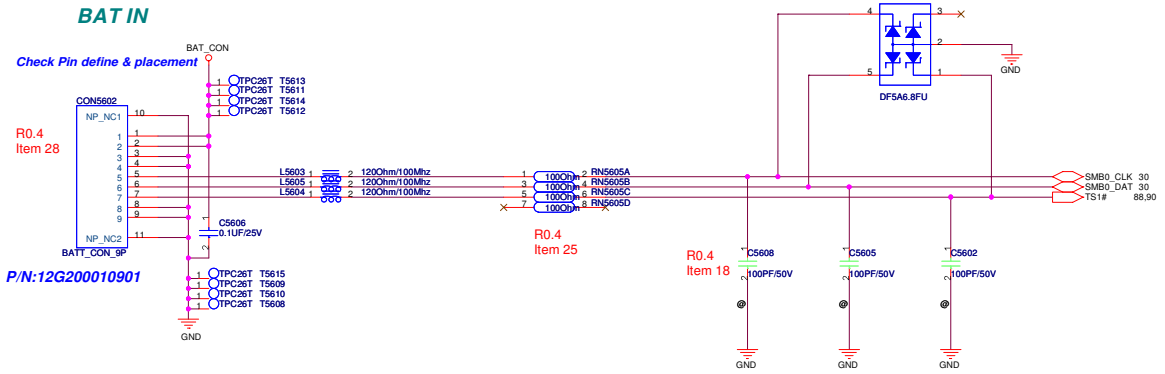
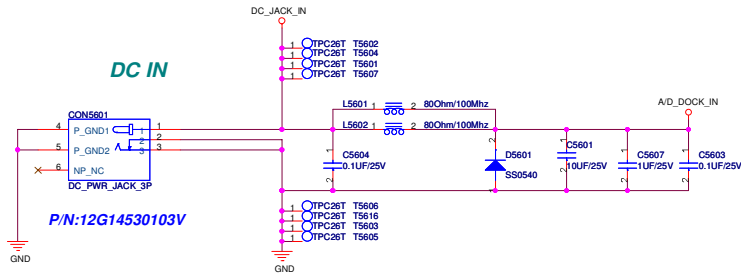
BB_ENA = 0V FOR BACK BIASING DISABLED
MAX1673 SHUTDOWN
-BBN = 0V VIA MAX1673 INTERNAL 1 OHM TO GROUND
N FET A = OFF, P FET B = OFF, N FET C = ON
+BBP = +VGA_CORE

BB_ENA = +3.3V FOR BACK BIASING ENABLED
MAX1673 ENABLED
-BBN = -.5V
N FET A = ON, P FET B = ON, N FET C = OFF
+BBP = +1.5V

GPIO_21_BB_EN	+BBP
0	1.1V
1	1.5V


GPIO_21_BB_EN	-BBN
0	GND
1	-0.5V


ASUS Title : **BACK BIAS**
 ASUSTeK COMPUTER INC. NB1 Engineer: **WM Chen**
 Size B Project Name **F80S** Rev 1.1
 Date: Wednesday, February 13, 2008 Sheet 51 of 94



ASUS		Title : AC/BAT JACK	
ASUSTek COMPUTER INC. NB1		Engineer: WM Chen	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, February 13, 2008	Sheet 56	of 94	

R0.4
Item 31

		Title : Empty
ASUSTeK COMPUTER INC. NB1		Engineer: WM Chen
Size	Project Name	Rev
A	F80S	1.1
Date: Wednesday, January 30, 2008		Sheet 57 of 94

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: WM Chen
Size	Project Name	Rev
A	F80S	1.1
Date: Wednesday, January 30, 2008		Sheet 58 of 94

R0.4 revision history:

1. Delete R511,R515,D503,C503,C509,Q505,R506 from 100K change to 0ohm for better signal quality .
2. Change D3302,D3303,D2107 from 1SS355 to 1N4148WS-L for cost down.
3. Change D3401,D3402,D2601,D2603 to BAT54WAPT for cost down and common part.
4. Change D2106 to BAT54C for cost down.
5. Change U1701 to AH180-WG-7 for cost down.
6. Delete RN301,RN302 for not use on board CPU cost down.
7. Add R3047-R3050 for newcard debug card.
8. Change CAP_ACK# from pin24 to pin63 for EC(page30) pin assignment R0.06.
9. Add R3028 for net:AC_IN_OC# pull hi.
10. Change C3002 from 1uF to 0.1uF for cost down.
11. Change Q4203 from 2N7002 to PMBS3904 for cost down and MIC jack.
12. Unmount R1727 for pull hi in p34.Change L1716 to R1710 for U1701 on MB.
13. Change USB connector J2401- J2403.
14. Unmount C3102 for cost down.
15. Reserve R3810 for prevent power short cause large current.
16. Change R3404,R3403,R3412,R3414 from 4.7K to 10K for power saving.
17. Change L3601,L3605 to R3622,R3623 for EMI fine tune cost down.
18. Unmount C5608,C5605,C5602 for EMI fine tune cost down.
19. Change R2505,R2506 from 680ohm to 2.7Kohm for 1W speaker.
20. Change CON3303,J2601 part number for ME request.
21. Change U2601 from TI to GMT,C2609 to 0.1uF for cost down.
22. Change card reader connector J2701 part number for connector in bottom side.
23. Change U2501 from 660 to 662 for the logo request codec need 2-ADC after 2008/6.
24. Reserve C3051 for fine tune CLK_ECPCI.
25. Add RN5605 for protect EC to prevent voltage damage.
26. Change CON3802 pin assignment for use W7 BT cable.
27. Unmount R2611 for ALC662 not need.
28. Change SW3901,SW3902,SW3801,SW3802,SW3803,J2801,CON5602,BAT2101,CON3801,CON3803 part number for ME request.
29. Delete D3301 for cost down.
30. Add VGA Back Bias on page51 for power play function
31. +1.2VSUS from page57 change to page82 for power circuit
32. Delete H_PWRGD_EC (Q202,R233) because it's not necessary.

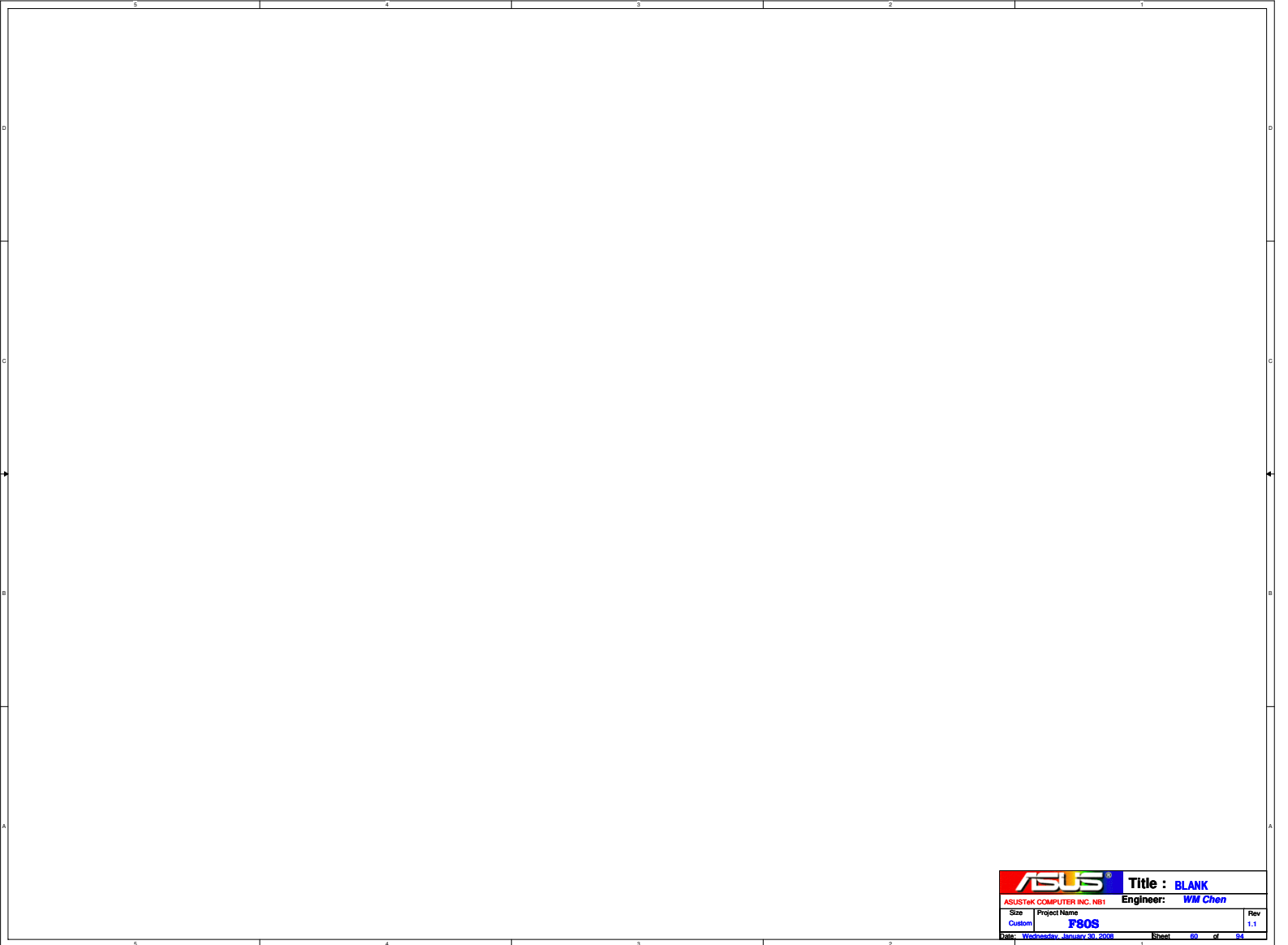
R0.5 revision history:

33. Reserve CON1901 pin24 to +3VAUX for Azurewave's Wireless-Lan Card.
34. Modify p25,p26 for colay ALC662 and ALC663 for sales reccommand.
35. Change KB connector CON3101 part number for ME request.
36. Change Screw hole for ME request .
37. Change CON3602 part number for ME request.
38. Cap. Array CN3101-CN3106 from 0805 change to 1206 size.
39. Add H4401,H4402 VGA NUT
40. Reserve internal mic J2803 for experiment.
41. Reserve U3502,U2103 circuit for experiment.
42. Add U1601,U1602 for NB output 3.3V level cost down.
43. Change page34 LED schematic for use Blue LED.
44. Reserve C3812,C3813 for EMI request TP_GND.
45. Modify Page 22,32 for sales require SATA ODD.
46. Change SW3801,SW3802 part number for ME request.
47. Change U3001 part number for cost down.
48. Reserve R208,C202 for H_CPURST#.
49. Add U3801 for EMI request.
50. Add RN1801-RN1804 for EMI request.
51. Delete VRAM termination
52. Add Q4405,R4411,C4466 for +3VSG
53. Change Hall-sensor U1701 part number for ME request.

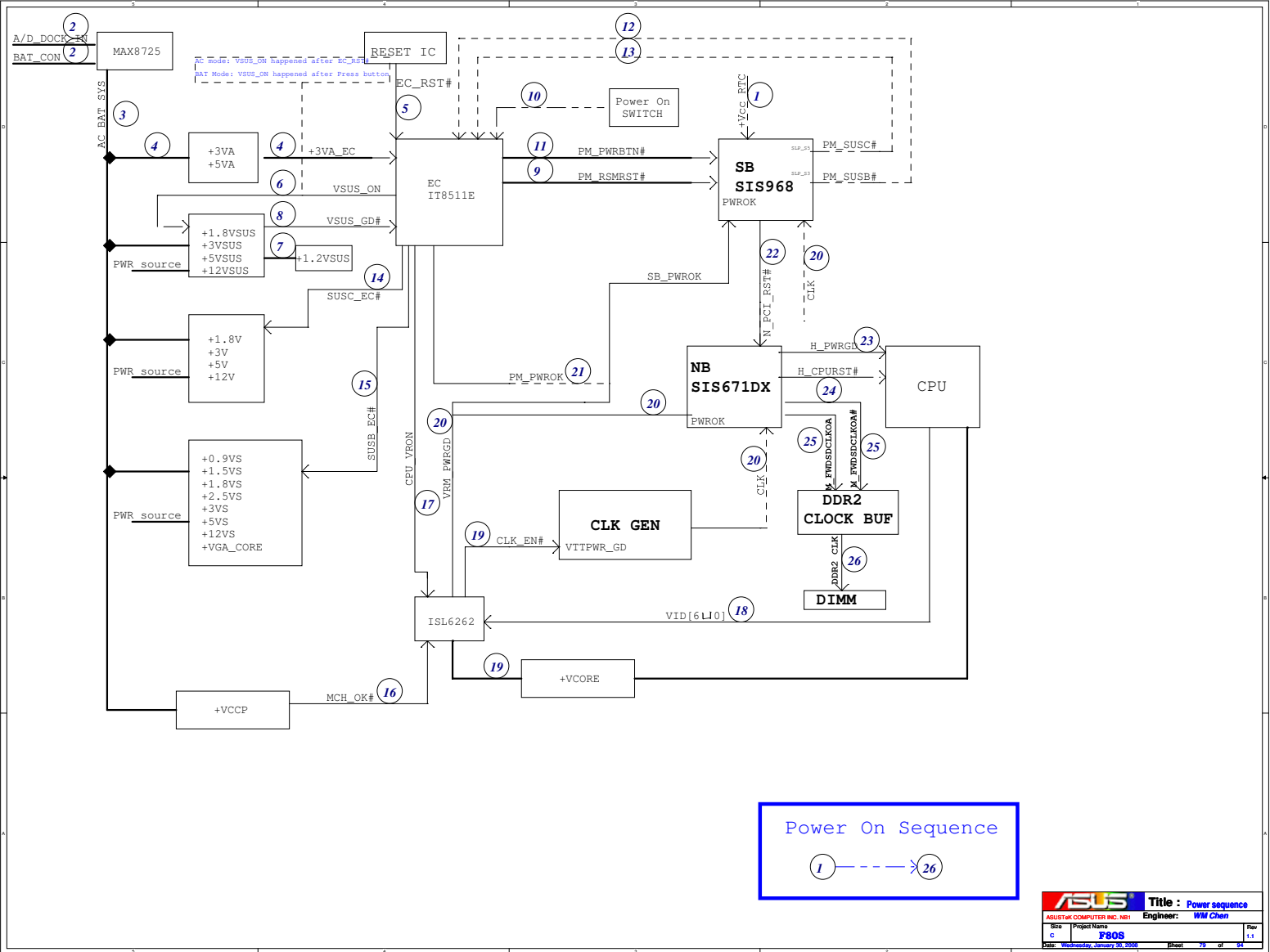
R1.01 revision history:

54. Unmount R4428 for leakage current issue.
55. Change R4435 from 71.5 to 150 for SIS request.
56. Mount R4440,R4441,R4443 37.4 ohm for VGA issue.
57. Change SATA ODD Connector CON3203 part number for ME request.
58. Change J2801 connector for Wire-MIC,change R2802 from 4.7K to 2.2K after test internal mic performance.
59. ADD D3603,C3609 for LAN ESD solution.
60. Change L1709,L3801,L3804,L3301,L3302,L3304,L2901 part number for colay footprint.
61. Change R3407,LED3403 value for meet factory LED spec.
62. Change VGA NUT H4401,H4402 to 13G021036001 for Thermal request.
63. Add D3201 IP4220C26 and R2225, R2226, R3217, R3218 0 ohm for EMI request.
64. Add C1218, C1707, C1814, C3304 0.1uF for EMI request.
65. Change R1402 from 22 to 10 for DDR Feedback quality.
66. Change Screw hole H4103, H4104, H4108 and Add H4131 for ME request.
67. Change USB external ports for controller.
68. Change CON3602 RJ11+45 part number for ME request.
69. Change R1705 from 100ohm to 330ohm for meet panel spec.
70. Add R2730 for factory recovery AU6371 driver CD.
71. Change R2505,R2506 from 2.7K to 3.3K for HDD-Speaker resonance issue.
72. Change C410,C417,C2101,C2115,C2715,C2716,C3006,C3010 value for TXC report suggest.
73. Del R1816,R1817 for SMT colay request.
74. Add R310 for +VCCA_CPU voltage ripple.
75. Add C2355 2.2uf for SB issue.
76. Unmount R3017,C3001,U3003,C3008,mount R3036,D3003,C3013,R3035,Add R3039 for cost down.
77. Add C3514 for Lan issue.
78. Mount R4459 and unmount Q4405, R4411,C4466 for cost down.
79. Add R4603 and unmount D4601 for cost down.
80. Mount R4708 and unmount Q4801,Q4704,R4709,R4704 for cost down.
81. ADD CE4783 220UF,C4740,C4783 0.1uF for VGA issue.
82. Mount R1611,R1612 from 0 ohm to 33 ohm and mount C1606,C1607 for meet spec.
83. Change CON3201 part number for ME request.
84. Add R2122,R2186 for SB issue.
85. Add C3305 22UF for meet spec.
86. Add C1905,C2727,C4333,C4334,C4335,C4716,Del C4331 for meet spec.
87. Del CE3202 100UF and Add C3209 47UF for ME request.
88. Change CE2601,CE2602 from 27uF to 47uF for better Low frequency response.
89. Add D4401,R3717,Q3709 for meet VGA spec.

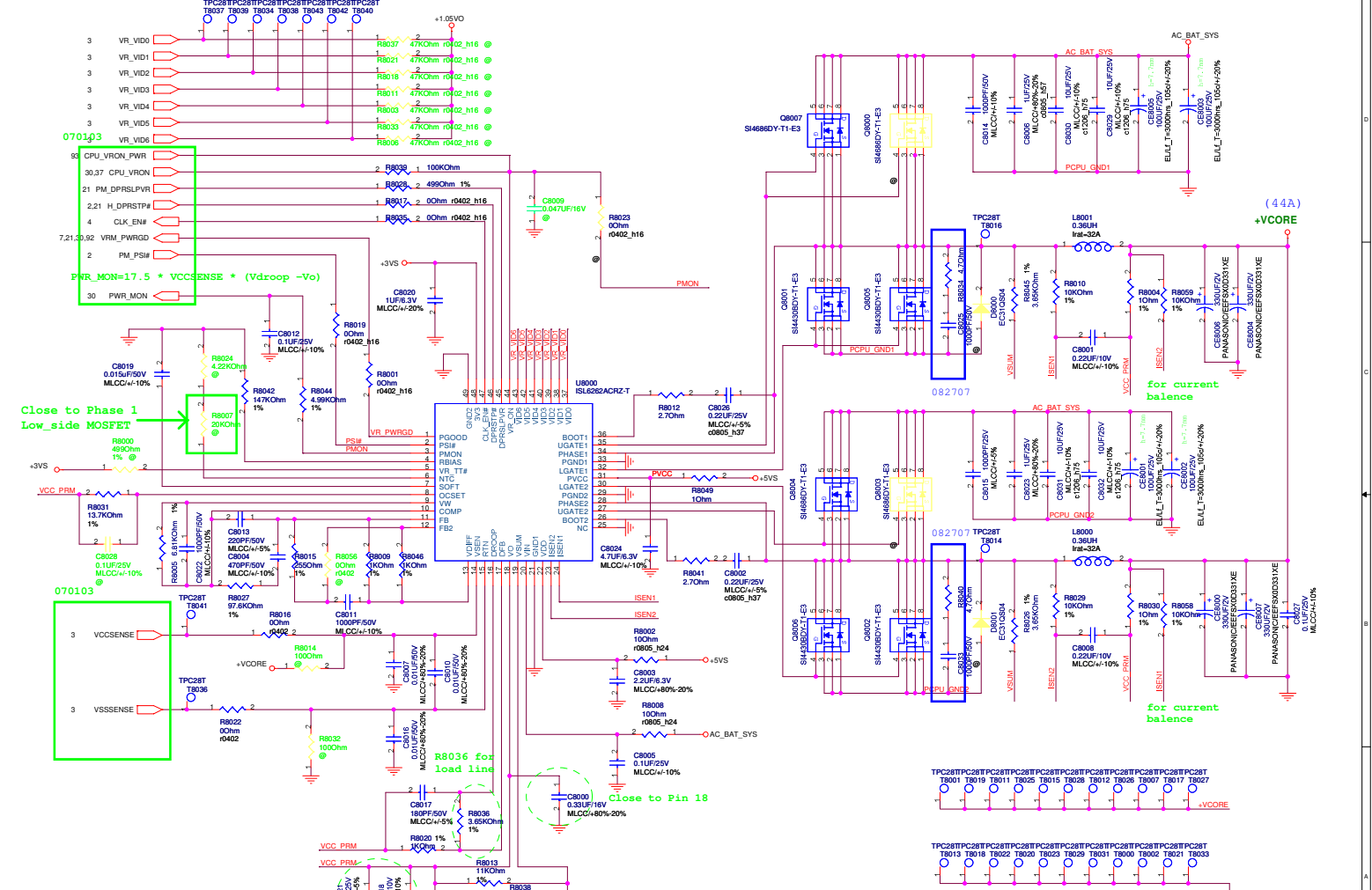
		Title :	
ASUSTek COMPUTER INC. NBI		Engineer: WM Chen	
Site	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, January 30, 2008		Sheet	59 of 84

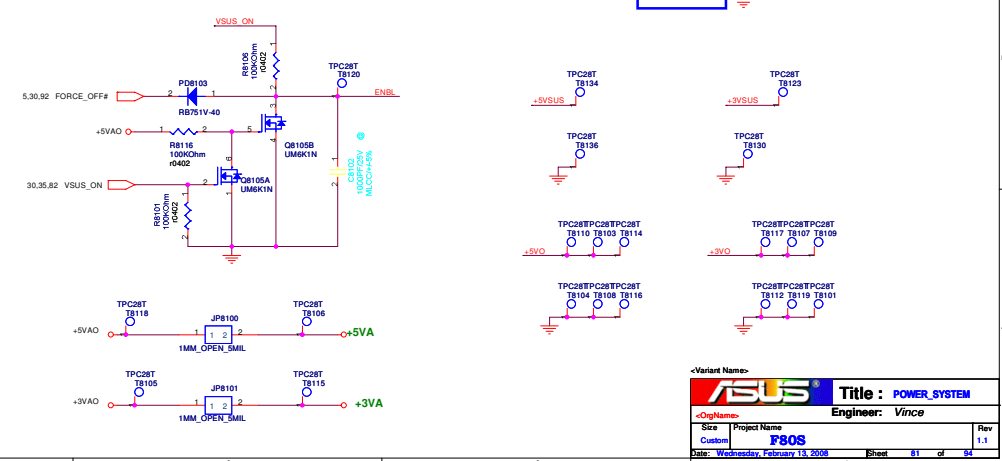
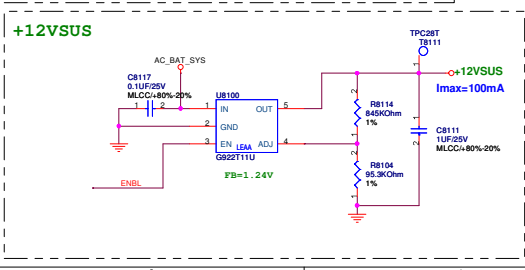
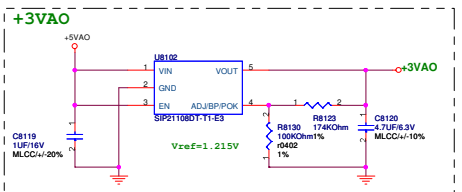
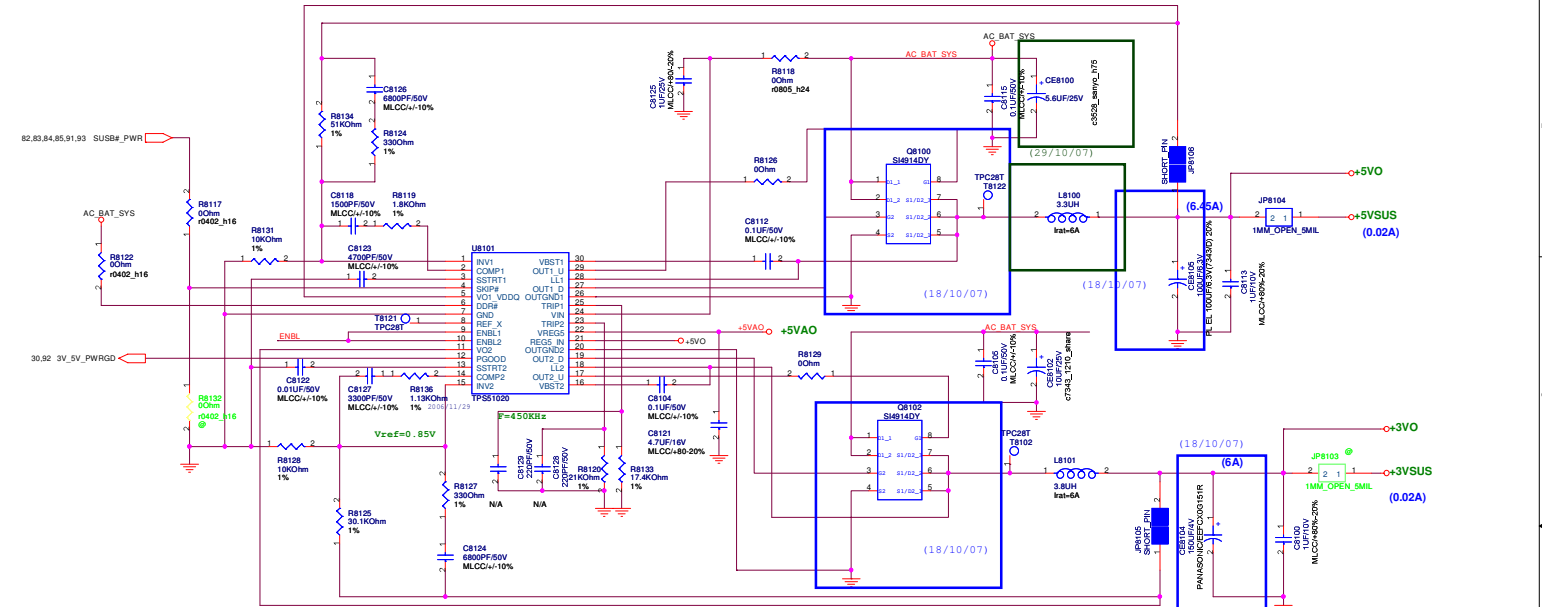


		Title : BLANK	
ASUSTEK COMPUTER INC. NB1		Engineer: WM Chen	
Site	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, January 30, 2008			Sheet 60 of 84

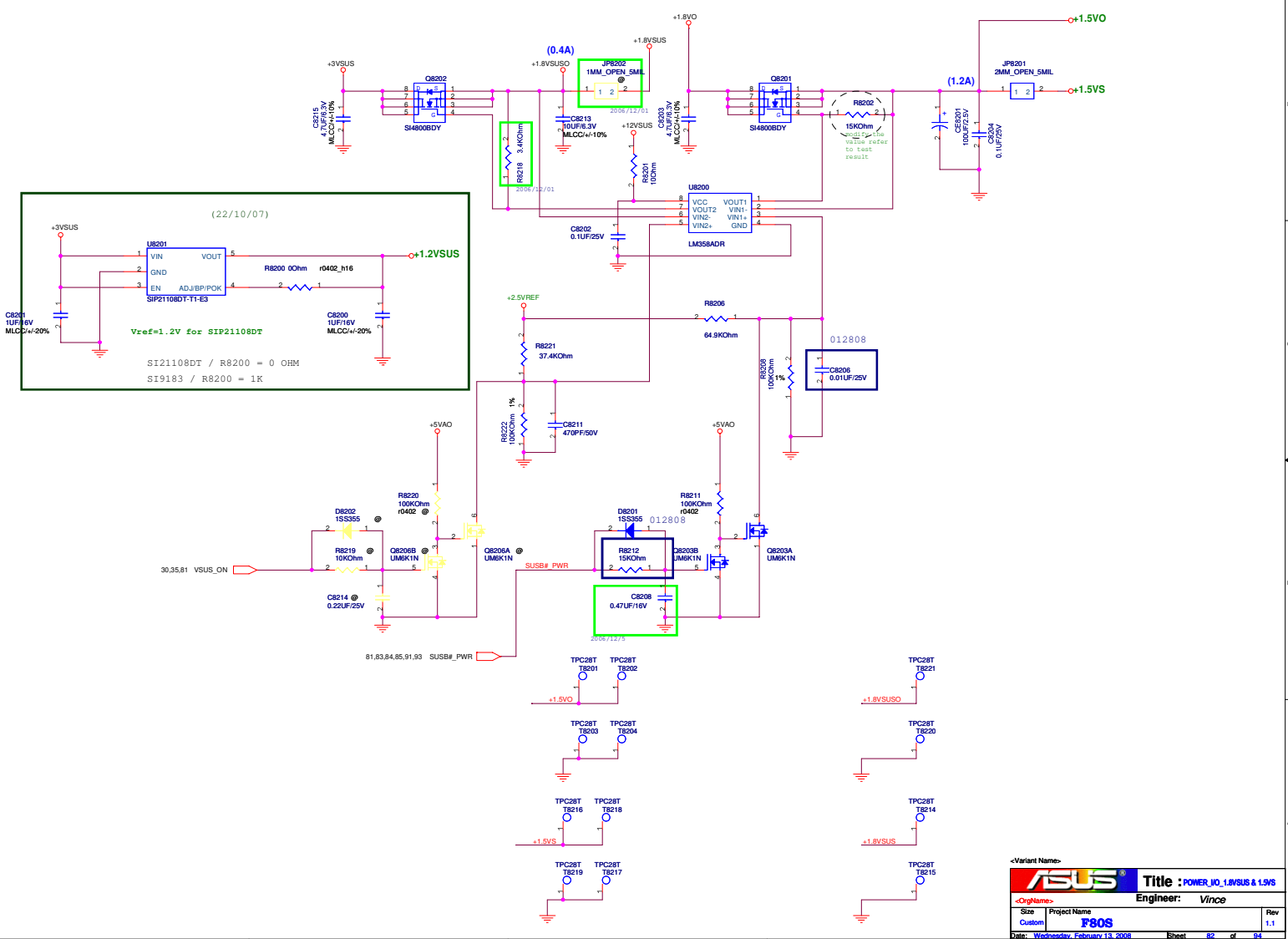
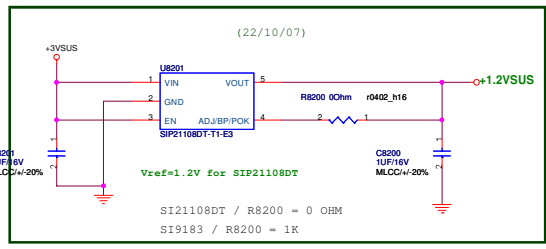


Power On Sequence
 1 -----> 26



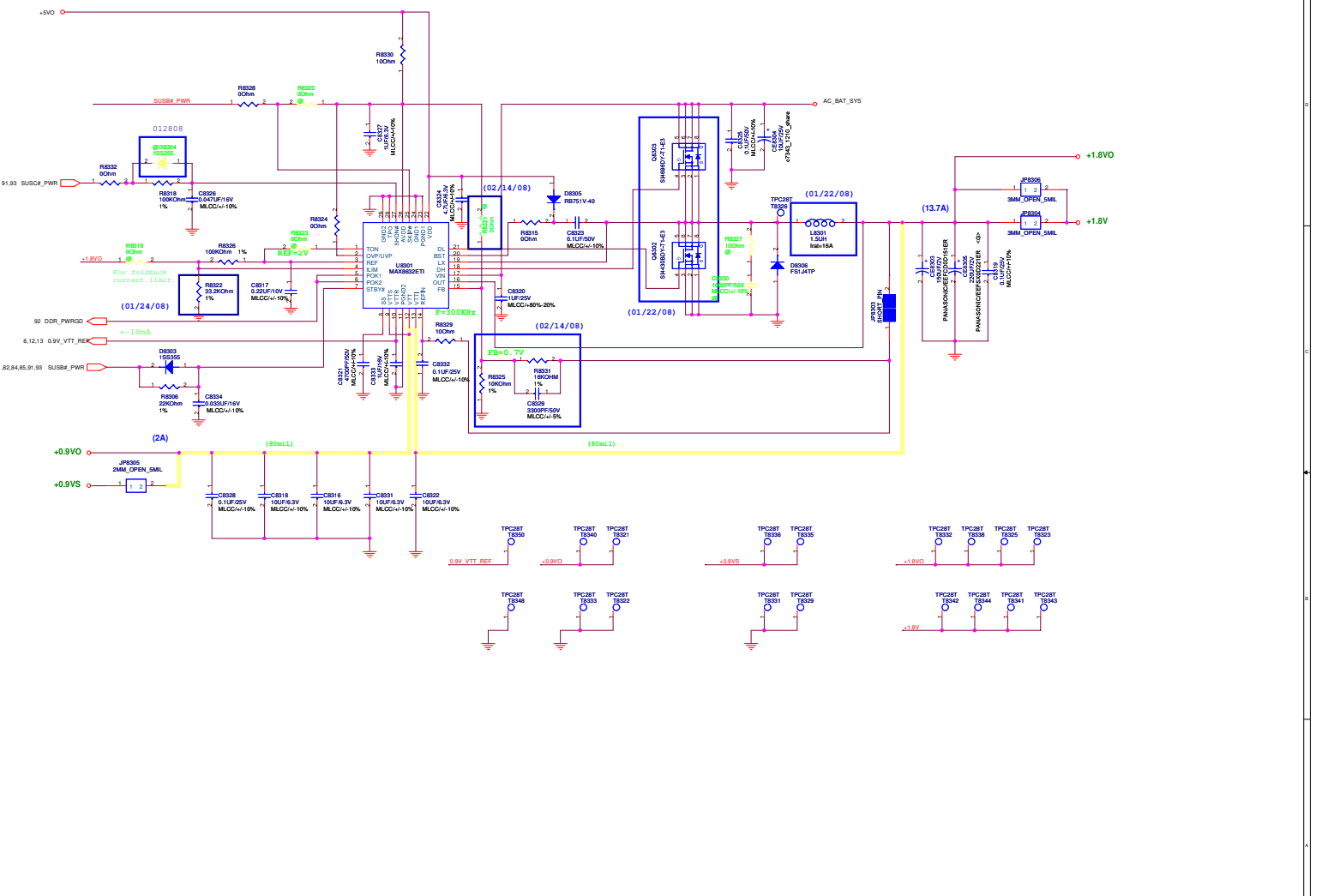


		Title : POWER_SYSTEM
Engineer: Vince		
Rev 1.1		
Date: Wednesday, February 13, 2008	Sheet 81	of 84



<Variant Name>

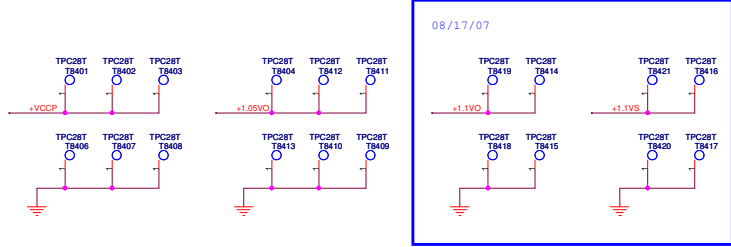
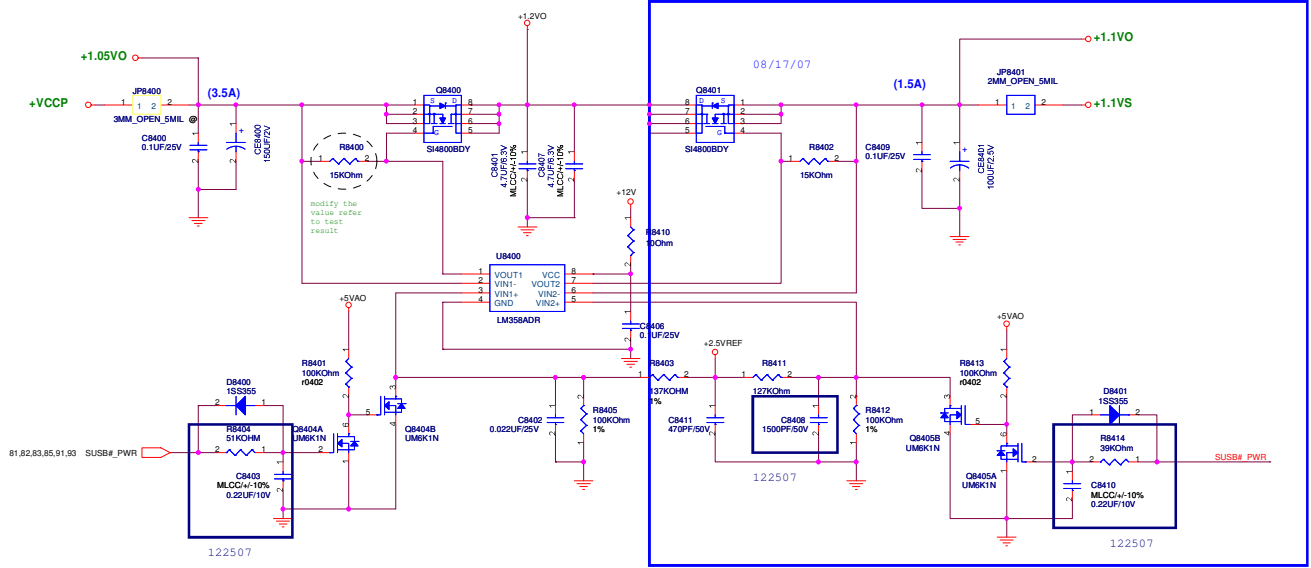
ASUS		Title : POWER_IO_1.8VSUS & 1.5VS	
<OrigName>	Project Name	Engineer:	Vince
Size	Custom	Rev	1.1
Date: Wednesday, February 13, 2008		Sheet	82 of 84



<Variant Name>

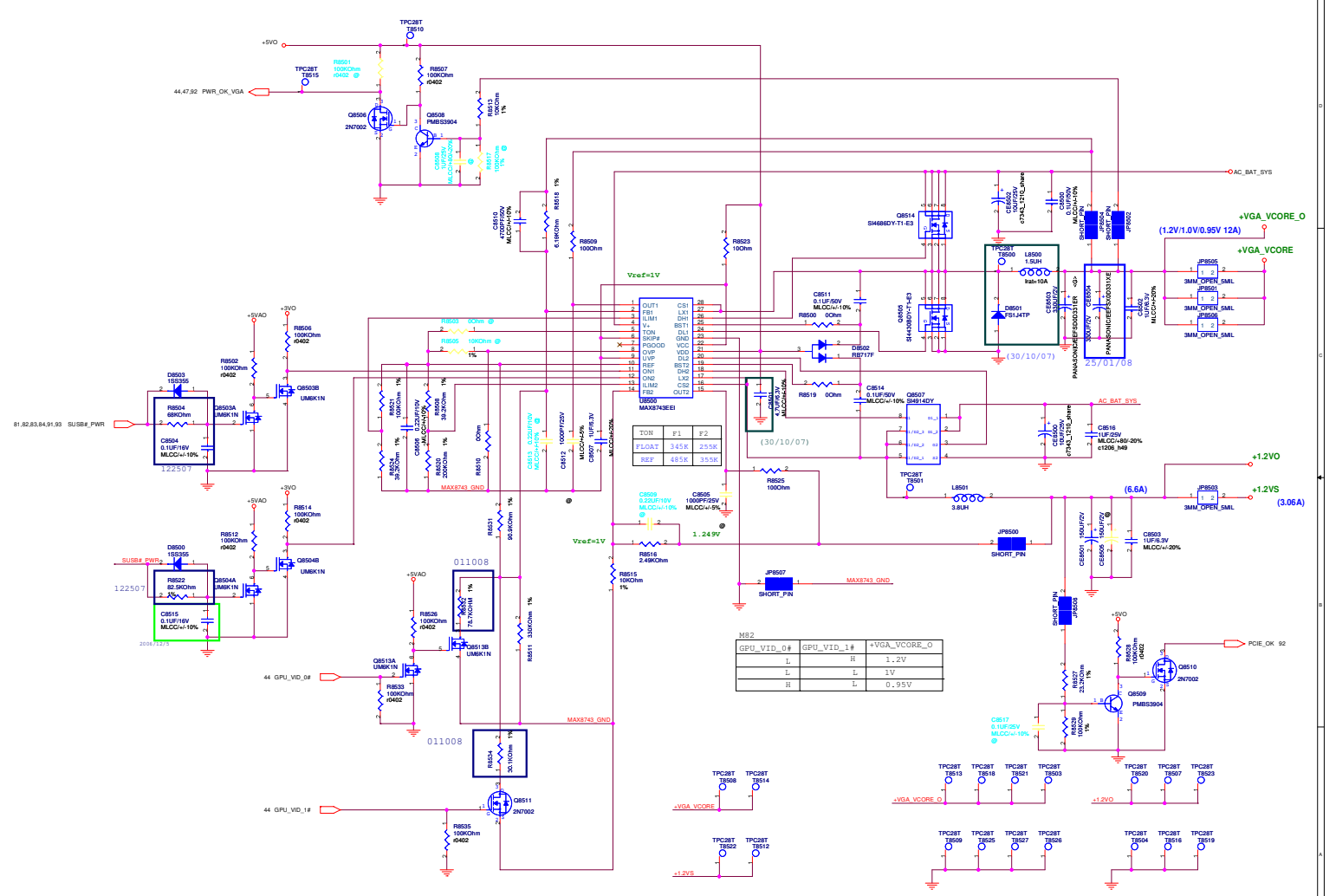
ASUS		Title : POWER_M0_DOR & VTT
<Signature>		Engineer: Vince
Size	Project Name	Rev
C	F80S	1.1

Date: Friday, February 15, 2008 Sheet: 03 of 04



<Variant Name>

ASUS		Title : POWER_IQ_VCCP & 1.1VS	
<OrigName>		Engineer: vince	
Size	Project Name		Rev
Custom	F80S		1.1
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TON	F1	F2
FL0AT	345K	255K
REF	495K	355K

GPU_VID_0#	GPU_VID_1#	+VGA_VCORE_O
L	H	1.2V
L	L	1V
H	L	0.95V

ASUS Title: POWER_VGA_CORE & RM
 Engineer: Vince
 Project Name: P80S
 Date: Wednesday, February 18, 2009

5

4

3

2

1

D

D

C


C

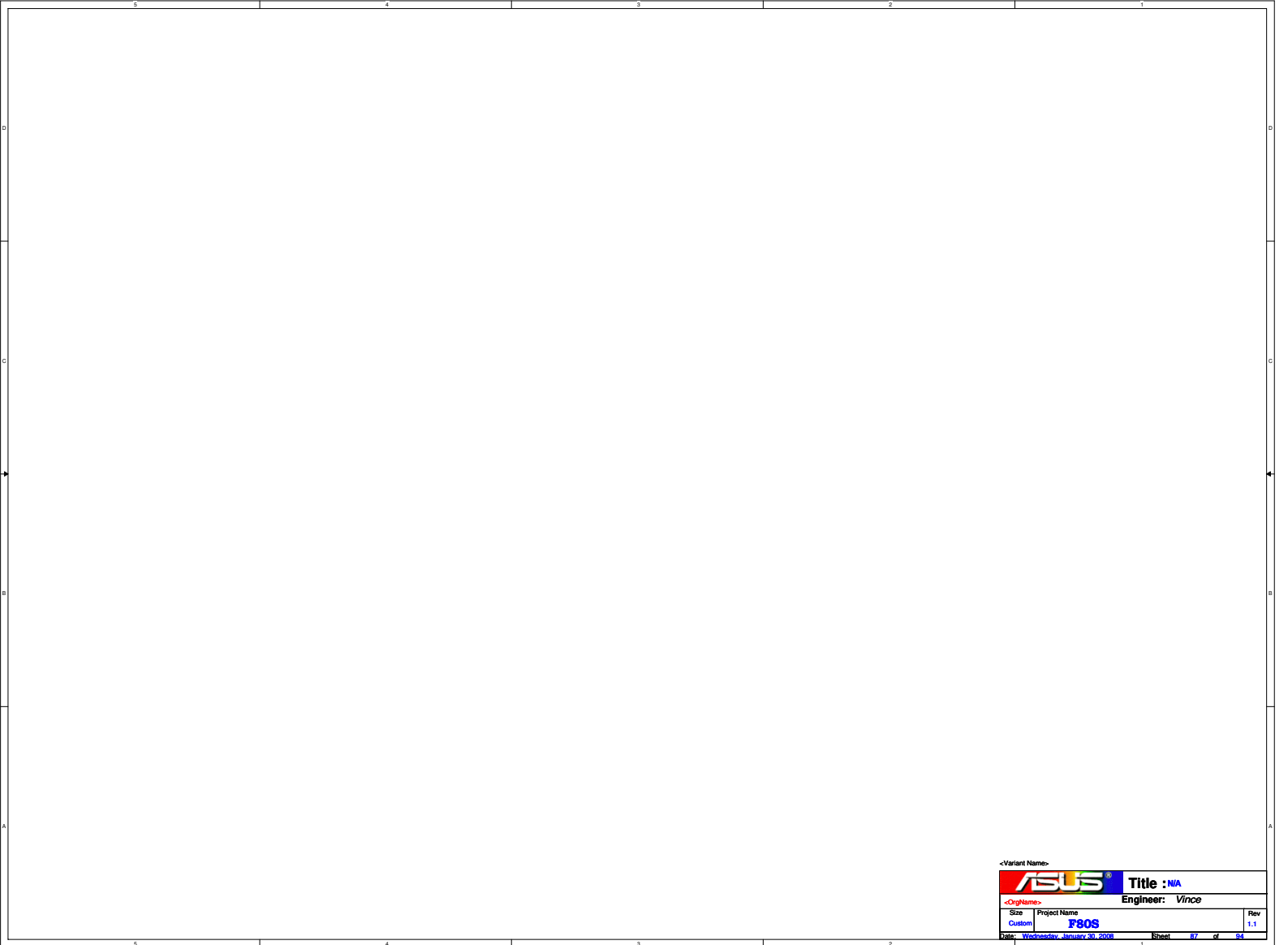
B


B

A

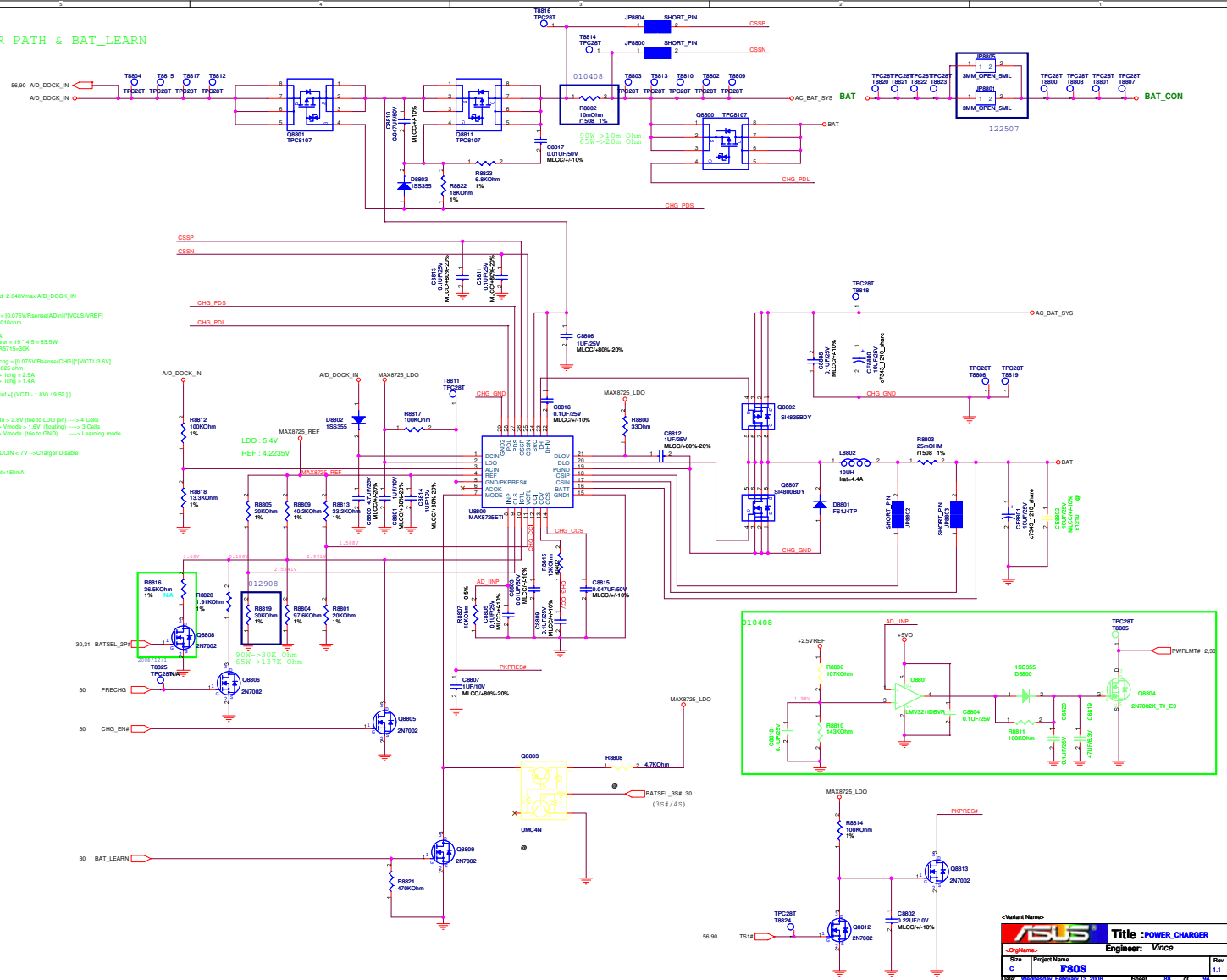
A

<Variant Name>		
		Title : <i>N/A</i>
<OrgName>		Engineer: <i>Vince</i>
Size B	Project Name F80S	Rev 1.1
Date: <i>Wednesday, January 30, 2008</i>		Sheet 86 of 94

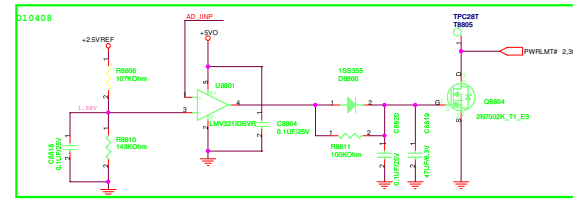


<Variant Name>		
		Title : N/A
<OrigName>		Engineer: Vince
Site	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, January 30, 2008		Sheet 87 of 84

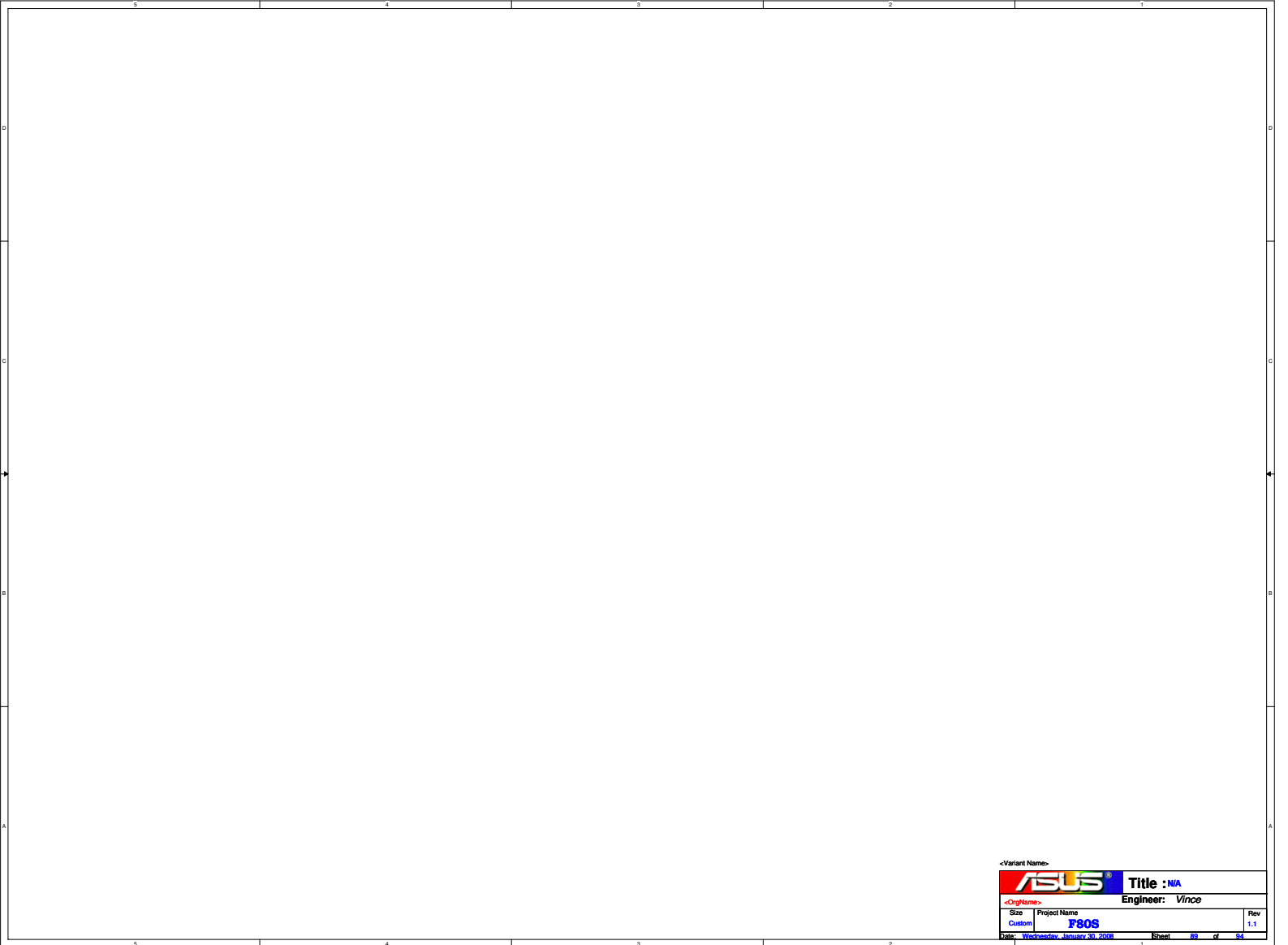
POWER PATH & BAT_LEARN




VC_IN Threshold 2.048Vmax AD_DOCK_IN
 17.44V active
 Adapter Inj(max) = (0.075V/Rsense/Adm)[VCL5/VREF]
 Resense/Adm=0.000m
 VCL5=2.534V
 => Inj(max)=4.5A
 => Constant Power = 13.145 + 85.5W
 => RST to 200mF/15.53mF
 Charge Current Ichg = (0.075V/Rsense/CHG)[VCTL3.6V]
 Resense/CHG=0.002m
 VCTL=3V => Ichg = 2.5A
 VCTL=1.588V => Ichg = 1.4A
 Mode pin: Vinode > 2.8V (96 to LDO pin) => 4 Cells
 2.0 > Vinode > 1.8V (Booting) => 3 Cells
 0.8 > Vinode (96 to DND) => Charging mode
 VICT=0.8V or DCIN = 7V => Charger Disable
 Precharge current=150mA

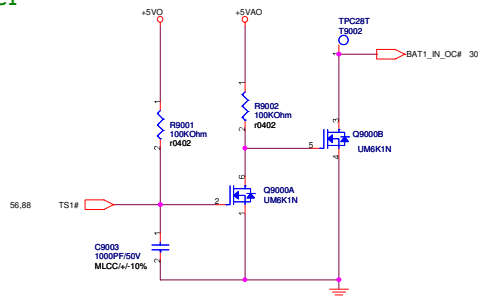


ASUS		Title: POWER CHARGER	
Design	Project Name	Engineer: Vince	
C	F808	Rev	1.1
Date: Wednesday, February 18, 2009	Sheet: 85	of	84

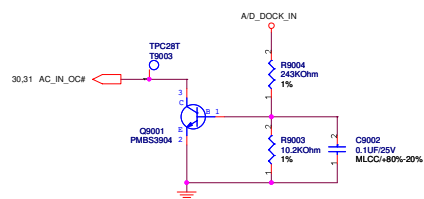


<Variant Name>		
		Title : N/A
<OrigName>		Engineer: Vince
Site	Project Name	Rev
Custom	F80S	1.1
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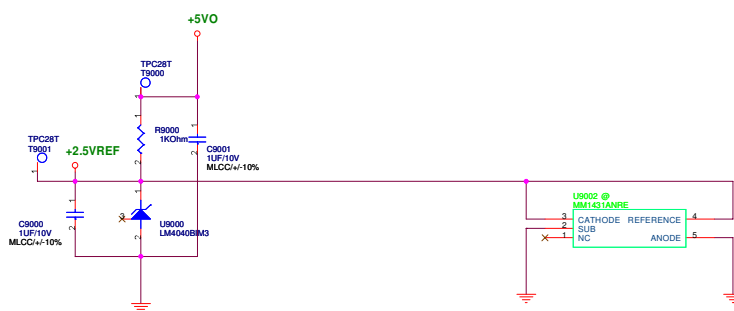
BATTERY IN DETECT



ADAPTER IN DETECT



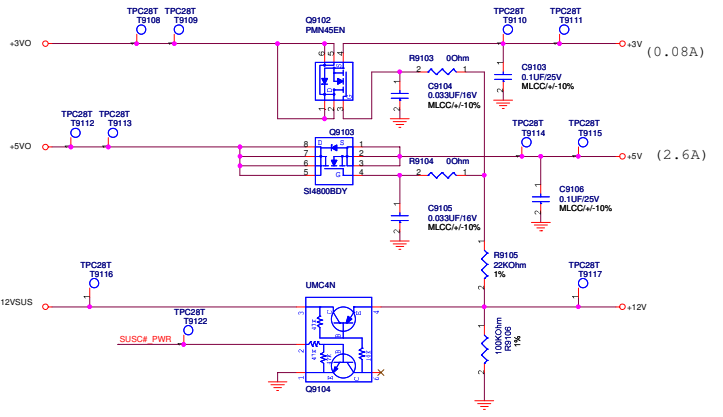
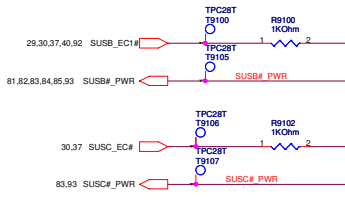
+2.5VREF



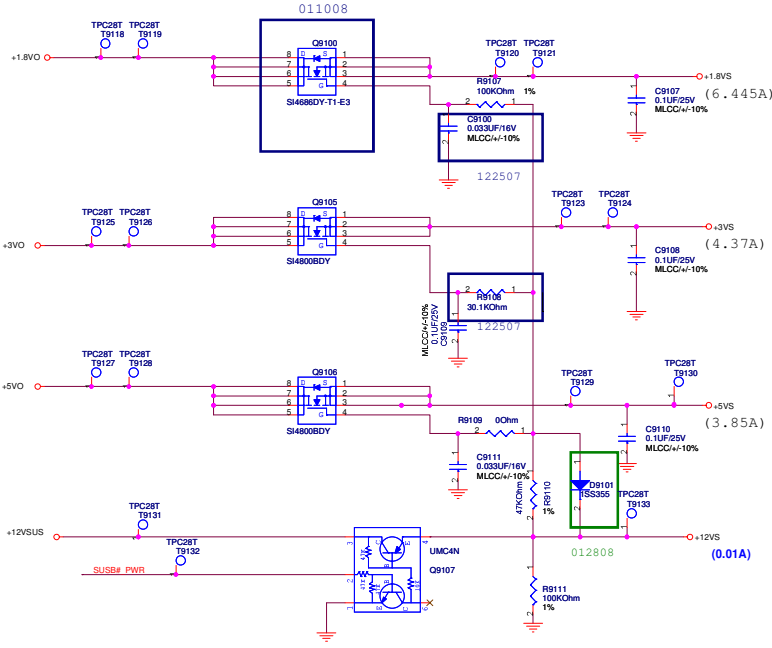
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		Title : POWER_DETECT
<OrigName>		Engineer: Vince
Size	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, February 13, 2008		Sheet 90 of 94

SUSC#_STAGE POWER

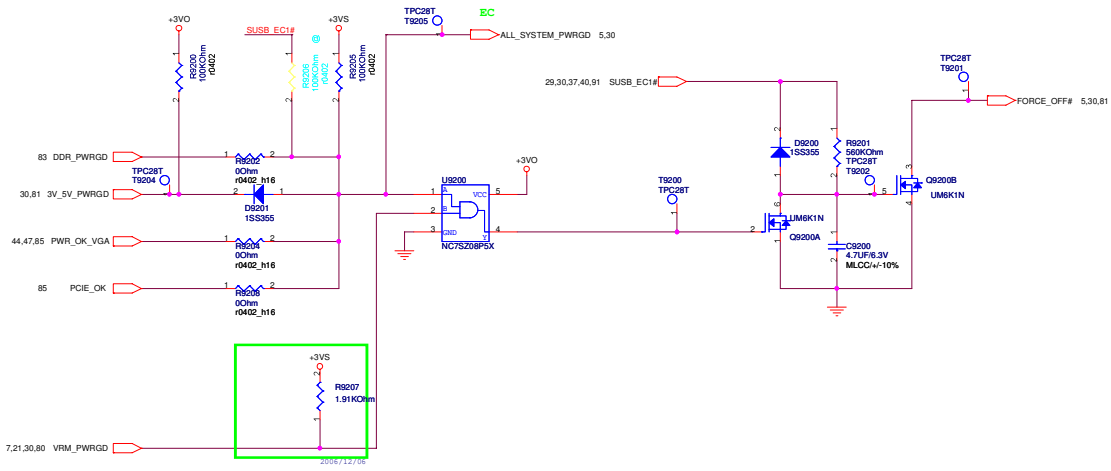


SUSB#_PWR POWER



ASUS		Title : POWER_LOAD SWITCH	
Engineer: Vince		Rev	
Size	Project Name	Custom	Rev
Custom	F80S	Custom	1.1
Date: Wednesday, February 13, 2008	Sheet	91	of 94

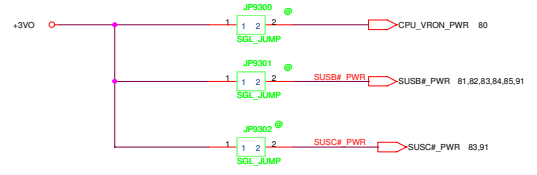
POWER GOOD DETECTOR



<Variant Name>		
ASUS		Title : POWER_PROTECT
<OrigName>		Engineer: Vince
Size	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, February 13, 2008		Sheet 82 of 84

AC_BAT_SYS	AC_BAT_SYS	17,80,81,83,85,88
+3VA	+3VA	17,21,30,37,81
+5VA	+5VA	5,81
+5VD	+5VD	81,83,85,88,90,91
+3VD	+3VD	81,85,91,92
+3VSUS	+3VSUS	8,17,19,20,21,22,23,24,26,30,34,35,36,81,82
+5VSUS	+5VSUS	34,81
+3V	+3V	19,27,29,31,36,37,38,40,91
+3VS	+3VS	2,4,5,7,12,13,16,17,18,19,20,21,22,23,25,29,30,32,33,34,37,40,44,80,91,92
+12VSUS	+12VSUS	81,82,91
+12V	+12V	26,27,33,37,84,91
+12VS	+12VS	17,18,37,44,91
+5V	+5V	17,33,37,91
+5VS	+5VS	5,12,16,18,25,26,29,30,32,34,37,38,51,80,91
+1.8VD	+1.8VD	82,83,91
+1.8VSUS	+1.8VSUS	10,21,22,23,82
+1.8V	+1.8V	8,10,12,13,15,37,83
+1.8VS	+1.8VS	6,7,8,10,12,14,20,21,22,23,37,43,44,45,47,51,91
+1.5VS	+1.5VS	3,19,25,29,37,51,82
+VCCP	+VCCP	2,4,5,6,10,21,23,37,43,84
+0.9VS	+0.9VS	15,37,83
BAT	BAT	88
+2.5VREF	+2.5VREF	62,84,88,90
+VCCORE	+VCCORE	3,37,80
+VGA_VCCORE	+VGA_VCCORE	37,43,47,51,85
+1.2VD	+1.2VD	84,85
+1.2VS	+1.2VS	9,10,37,85
BAT_CON	BAT_CON	56,88

FOR POWER TEST



-Variant Name-		Title : POWER SIGNAL	
-CtgName-		Engineer: Vince	
Size	Project Name		Rev
Custom	F80S		1.1
Date:	Wednesday, February 13, 2008	Sheet	83 of 84

