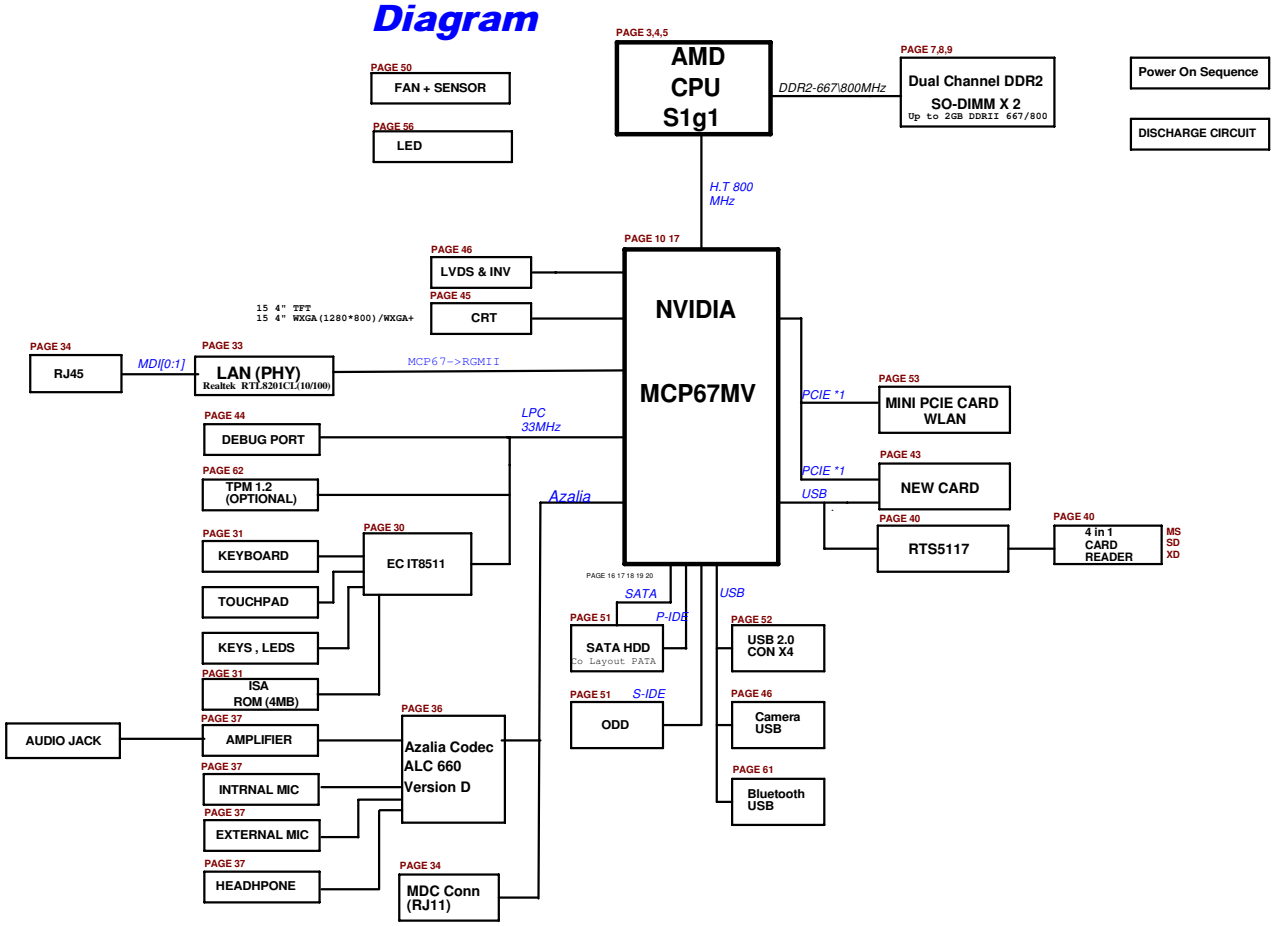
F5N Block Diagram



ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size: C | Project Name: F5U | Rev: 1.0

Date: 星期三, 五月 23, 2007 | Sheet 1 of 88

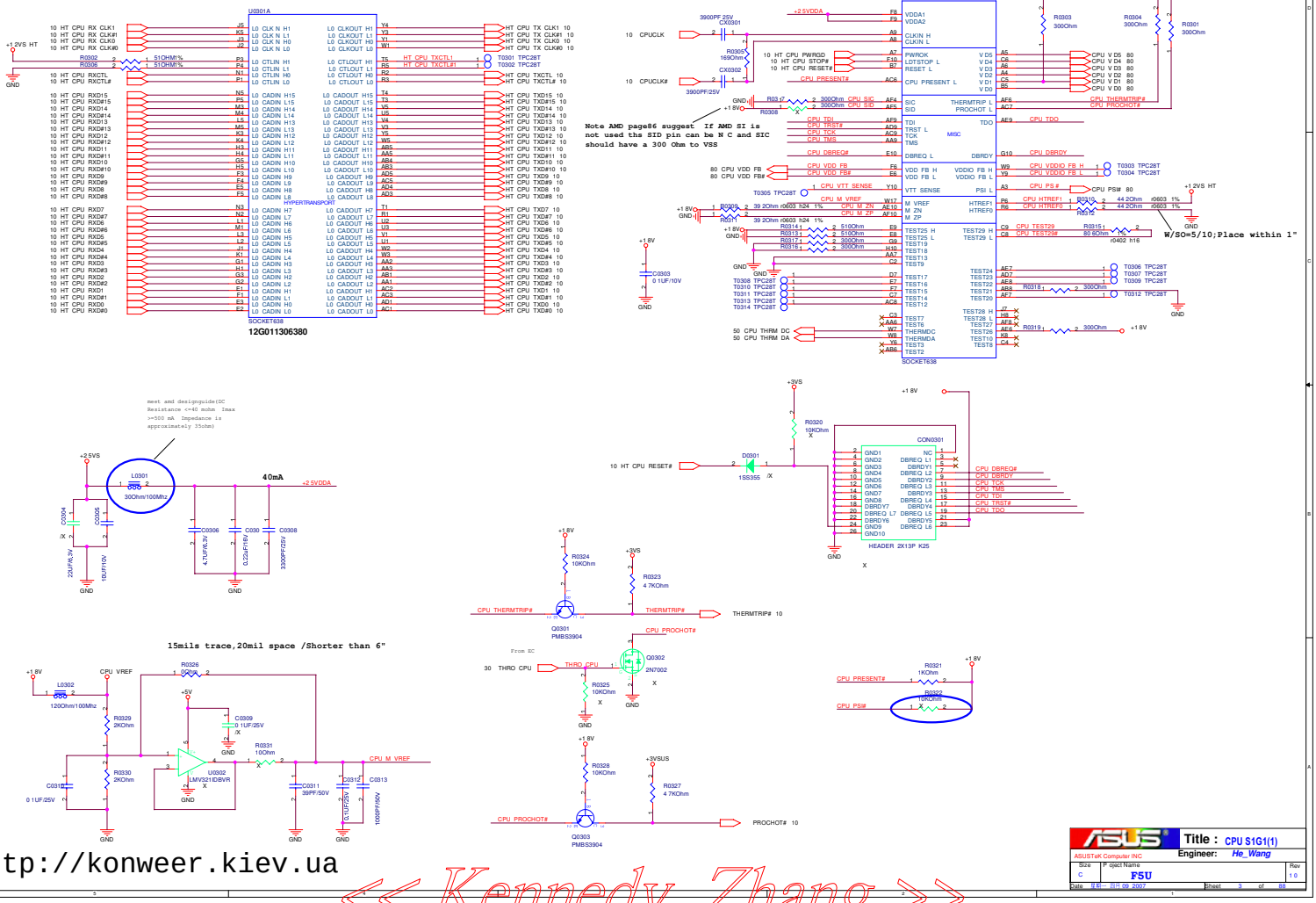
ASUSTeK Computer INC

Title : F5U

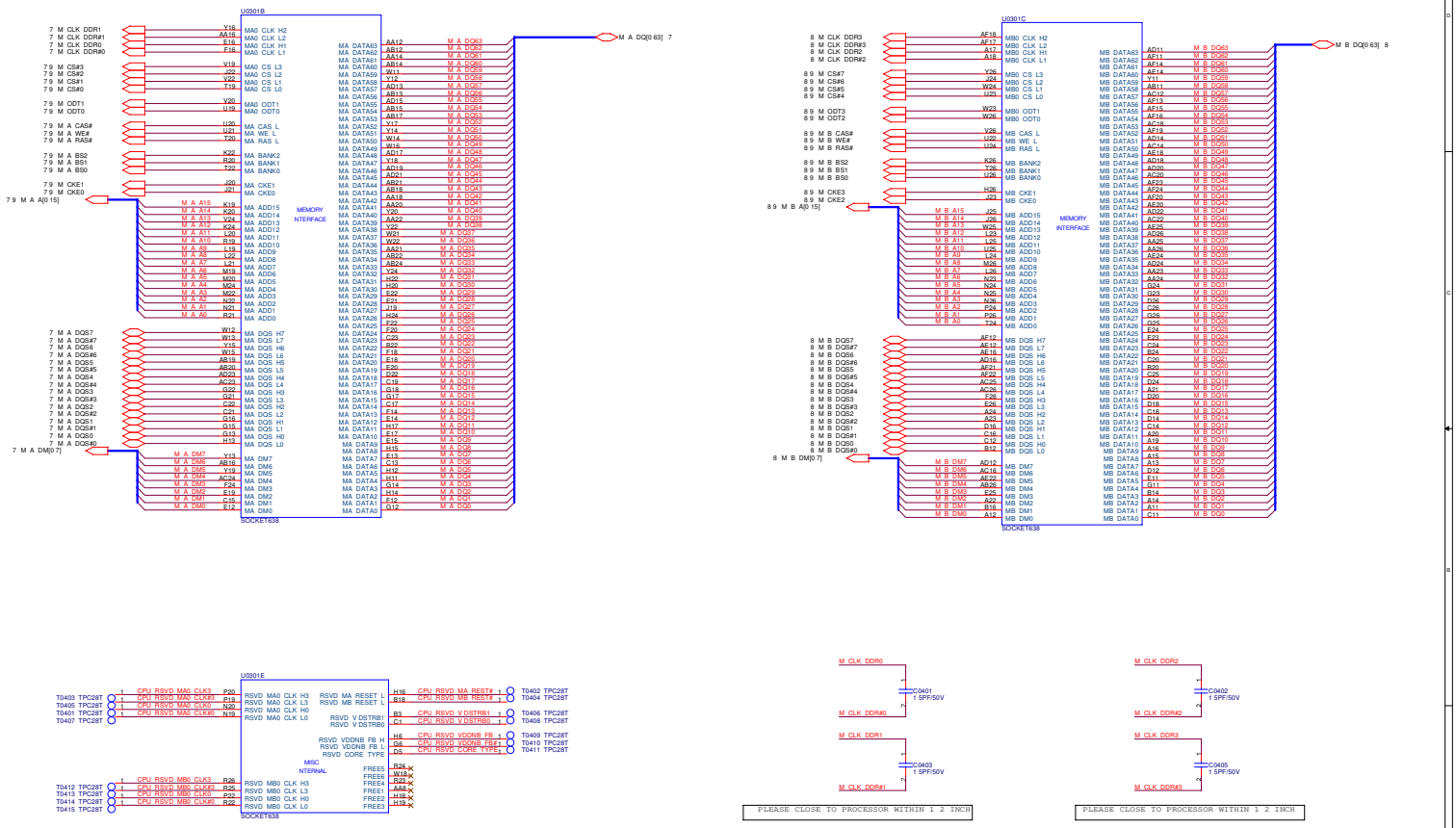
Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 日 8月 28 2007 Sheet 2 of 88



ASUSTeK Computer INC	Title : CPU S1G1(1)		
	Engineer: He_Wang		
Size: C	Project Name: FSU		Rev: 1.0
Date: 星期一 09, 2007	Sheet 3 of 38		



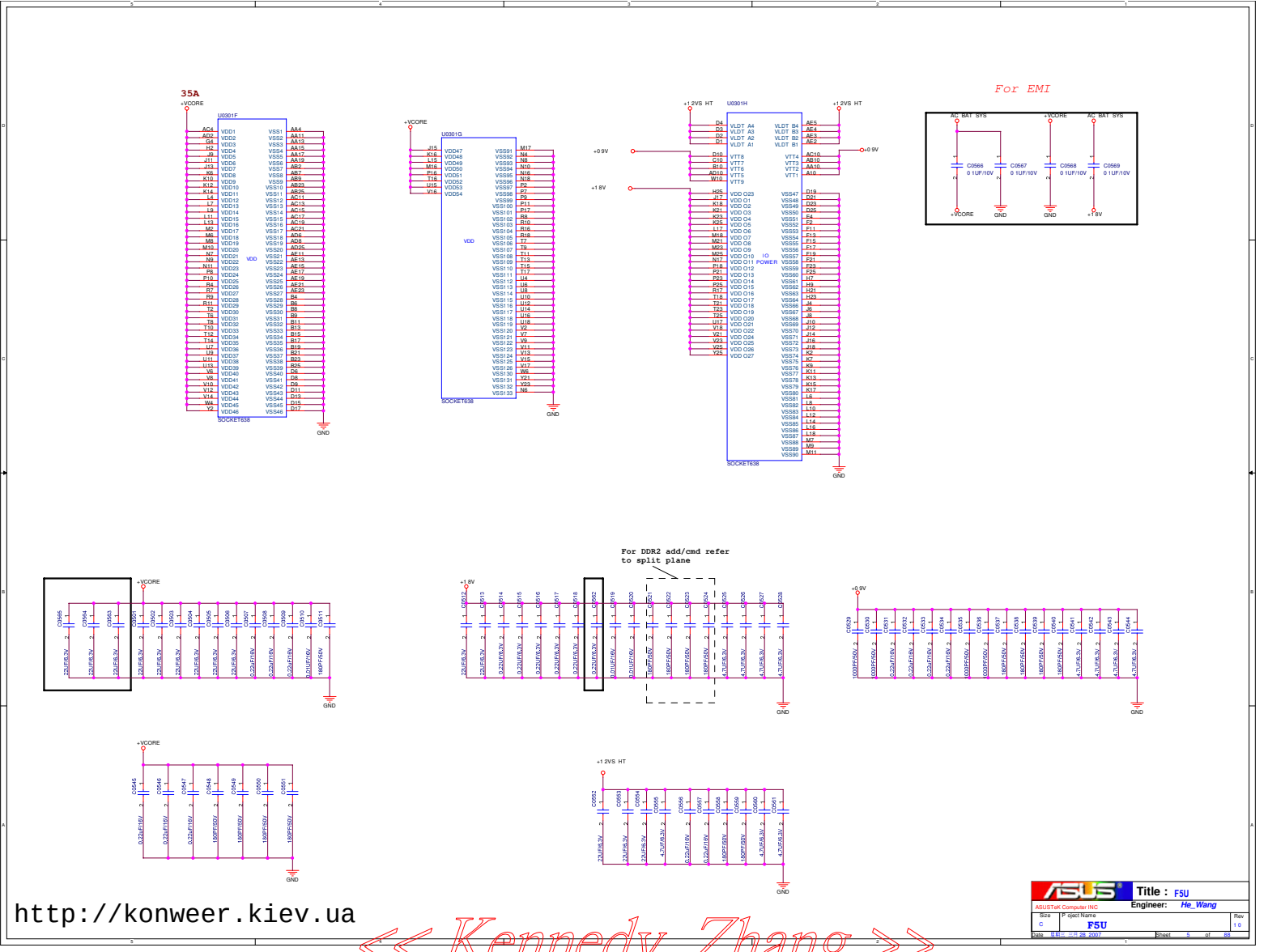
ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size: C | Project Name: F5U | Rev: 1.0

Date: 星期二, 09 2007 | Sheet 4 of 38



http://konweer.kiev.ua

<< Kennedy_Zhang >>

ASUSTeK Computer INC	Title : F5U	
	Engineer: He_Wang	
Size: C	Project Name: F5U	Rev: 1.0
Date: 星期三, 十月 28, 2007	Sheet 5 of 88	

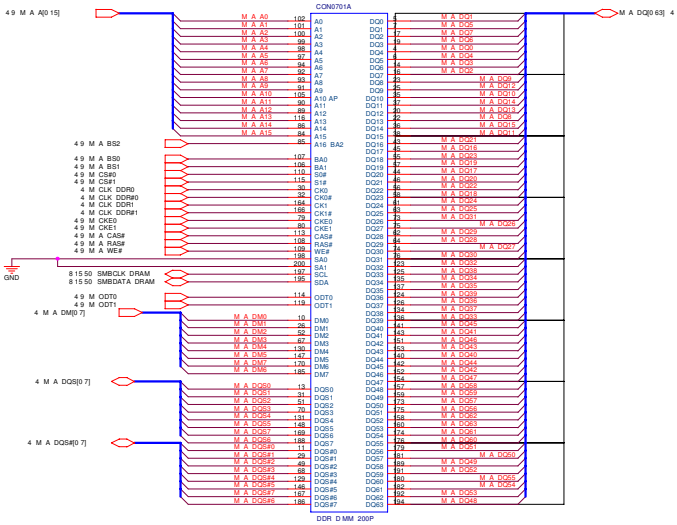
ASUSTeK Computer INC

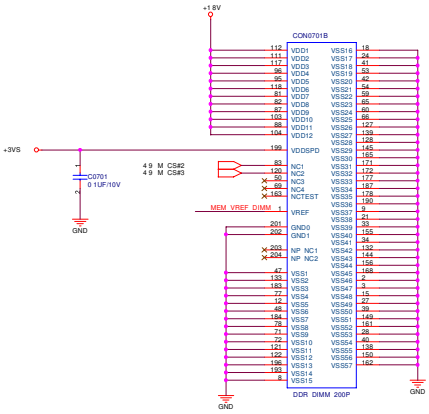
Title : F5U

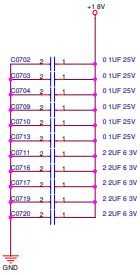
Engineer: He_Wang

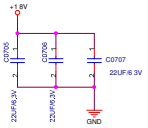
Size	Project Name	Rev
C	F5U	1.0

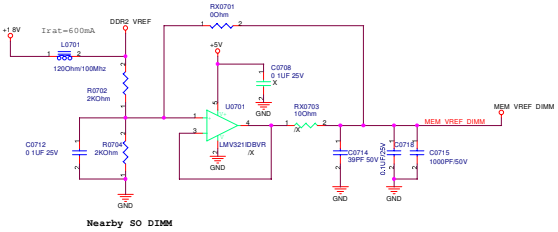
Date: 星期三, 四月 25, 2007 Sheet 6 of 88







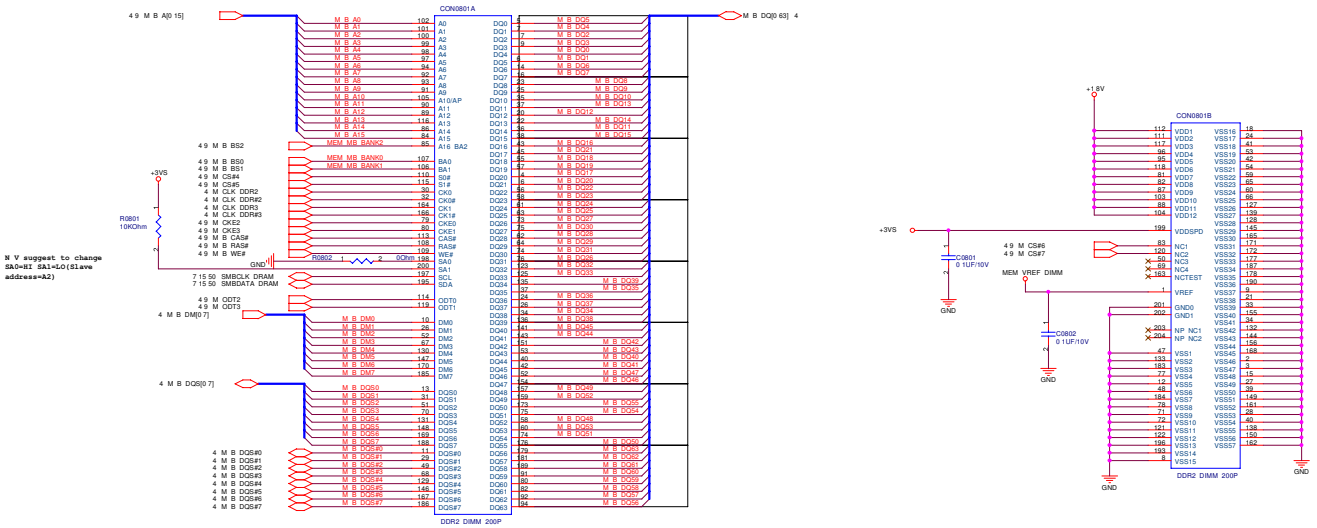




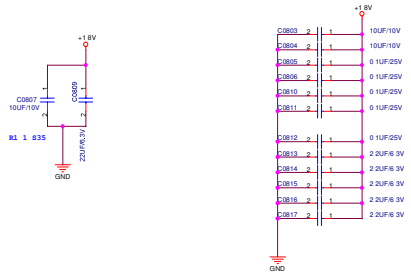
http://konweer.kiev.ua

<< Kennedy_Zhang >>

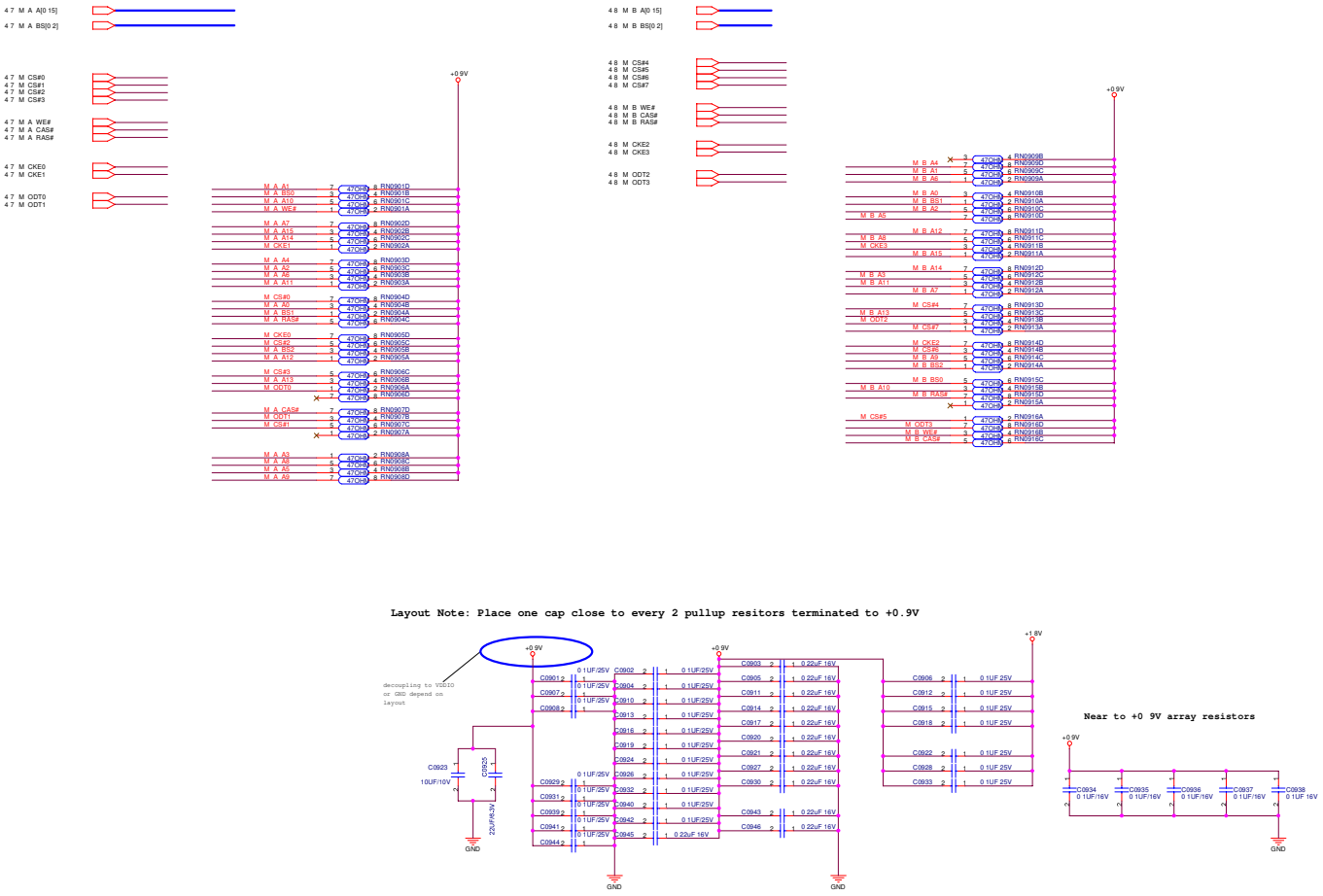
ASUSTeK Computer INC	Title : F5U		
	Engineer: He_Wang		
Size: C	Project Name: F5U		Rev: 1.0
Date: 星期一 09, 2007	Sheet 7 of 38		



PN:12G025C22002

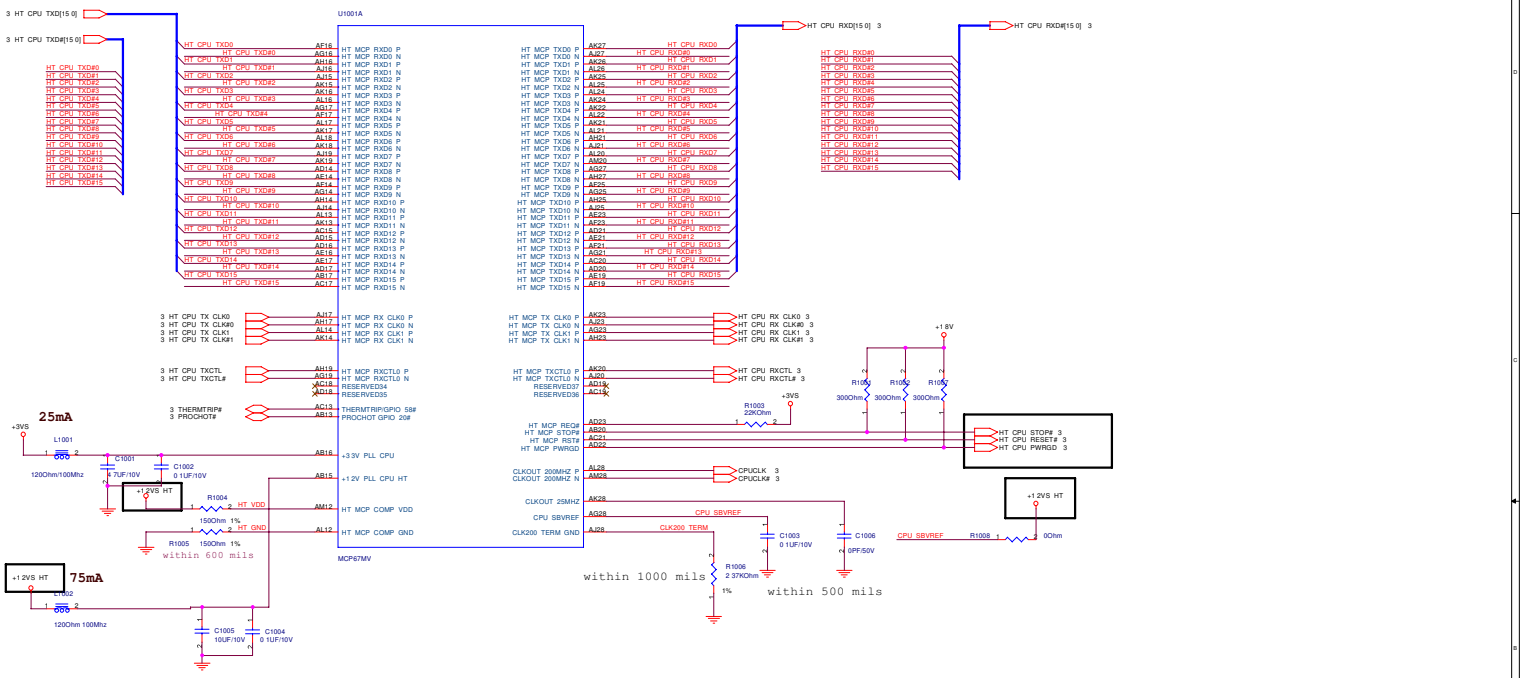


ASUSTeK Computer INC	Title : F5U		
	Engineer: He_Wang		
Size C	Project Name F5U		Rev 1.0
Date: 星期一 09, 2007	Sheet 8	of 88	



Layout Note: Place one cap close to every 2 pullup resitors terminated to +0.9V

ASUSTeK Computer INC	Title : F5U		
	Engineer: He_Wang		
Size: C	Project Name: F5U		Rev: 1.0
Date: 星期二 09 2007	Sheet 9 of 88		



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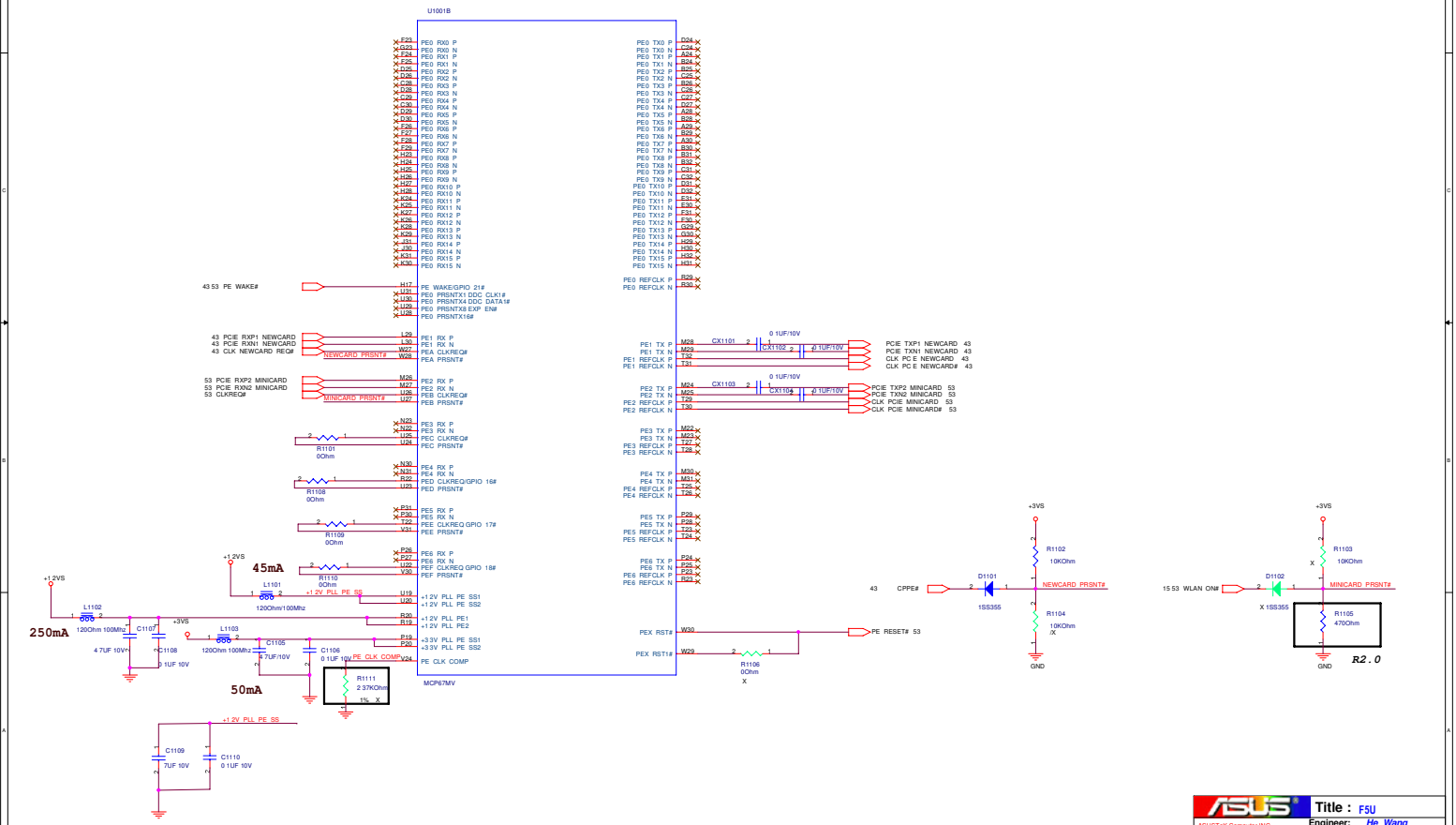
<< Kennedy_Zhang >>

ASUSTeK Computer INC	Title : F5U	
	Engineer: He_Wang	
Size: C	Project Name: F5U	Rev: 1.0
Date: 星期一 09, 2007	Sheet 10 of 88	



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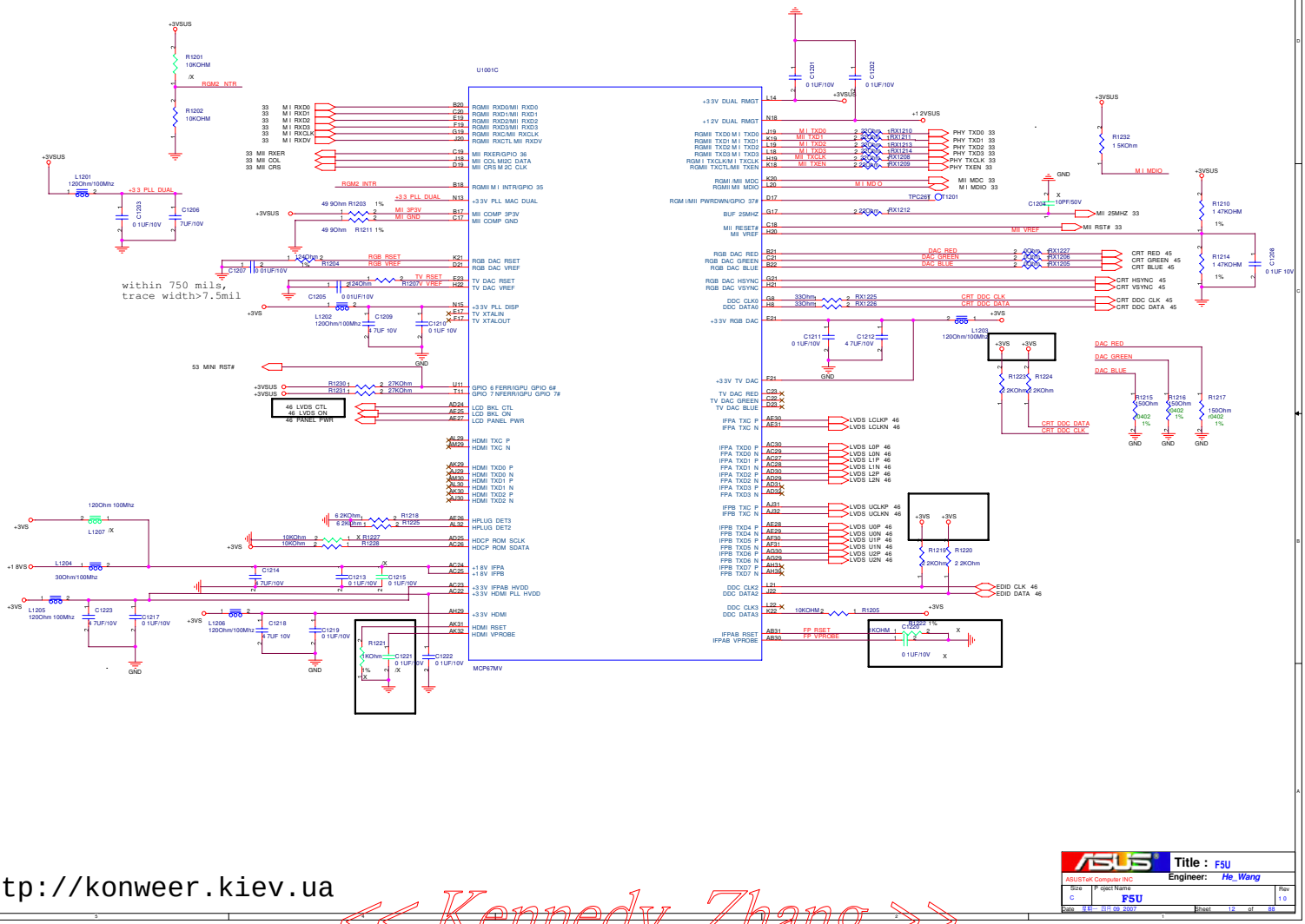
<< Kennedy_Zhang >>

ASUSTeK Computer INC	Title : F5U		
	Engineer: He_Wang		
Size: C	Project Name: F5U		Rev: 1.0
Date: 星期一 四月 09, 2007	Sheet 11 of 88		



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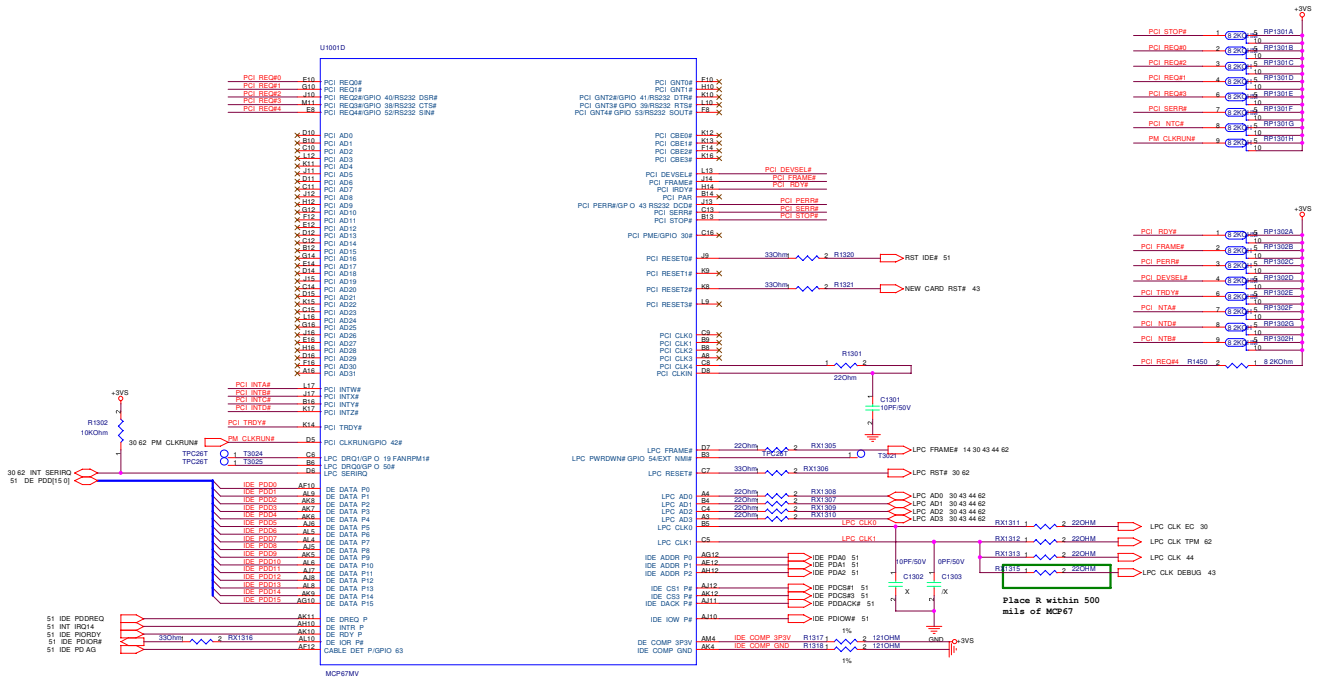
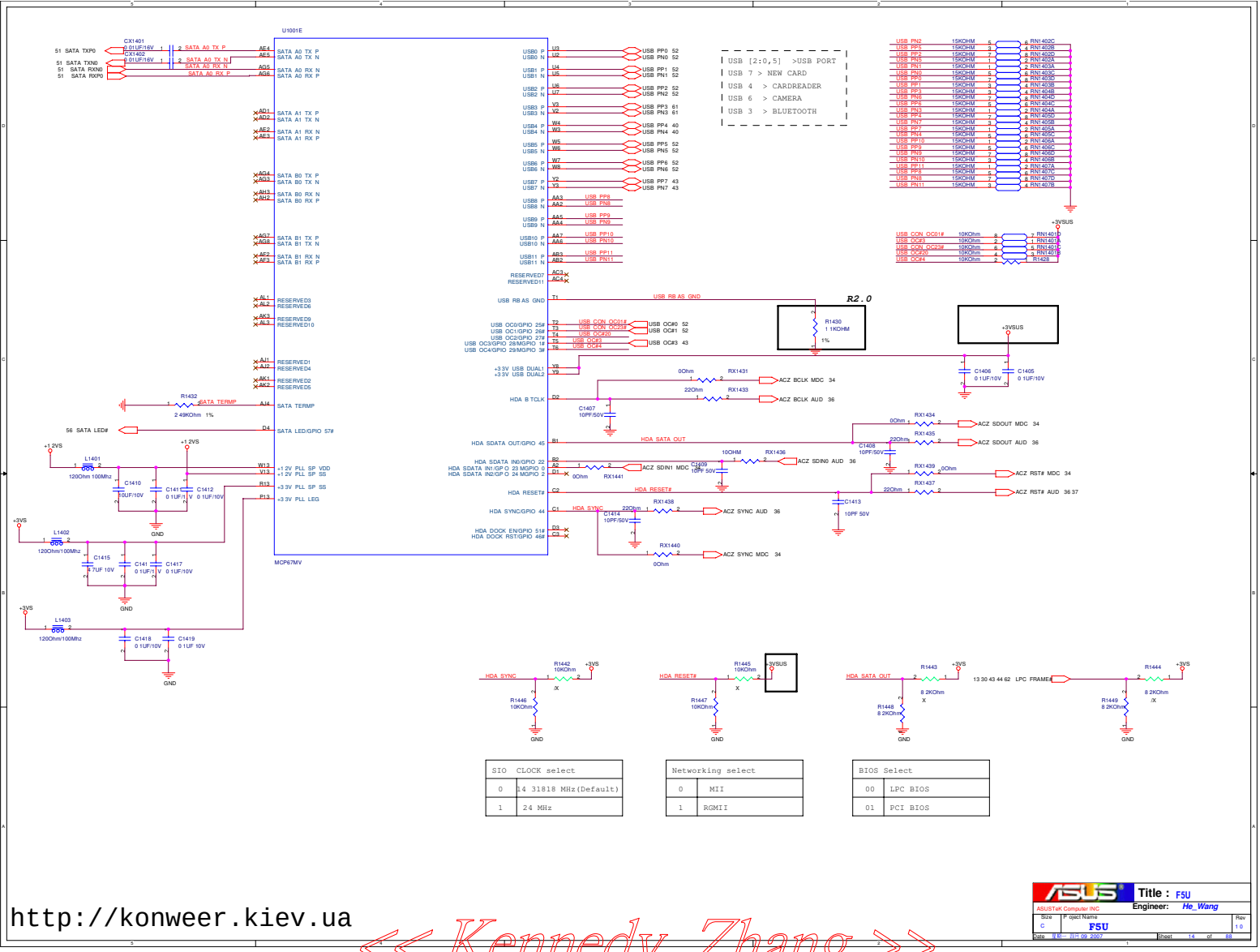
<< Kennedy_Zhang >>

ASUSTeK Computer INC	Title : F5U		
	Engineer: He_Wang		
Size: C	Project Name: F5U		Rev: 1.0
Date: 星期一 09 2007	Sheet 12 of 88		



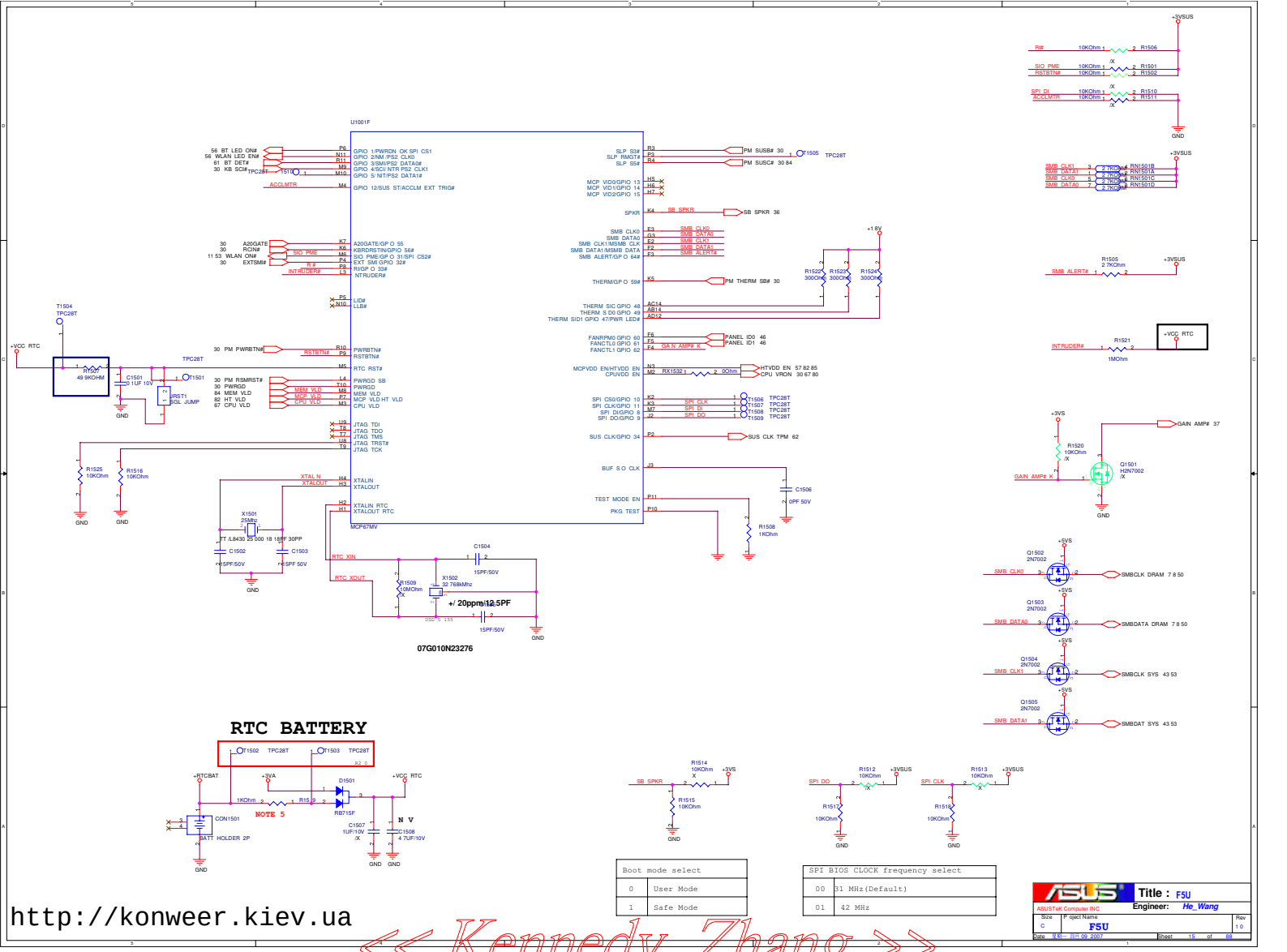


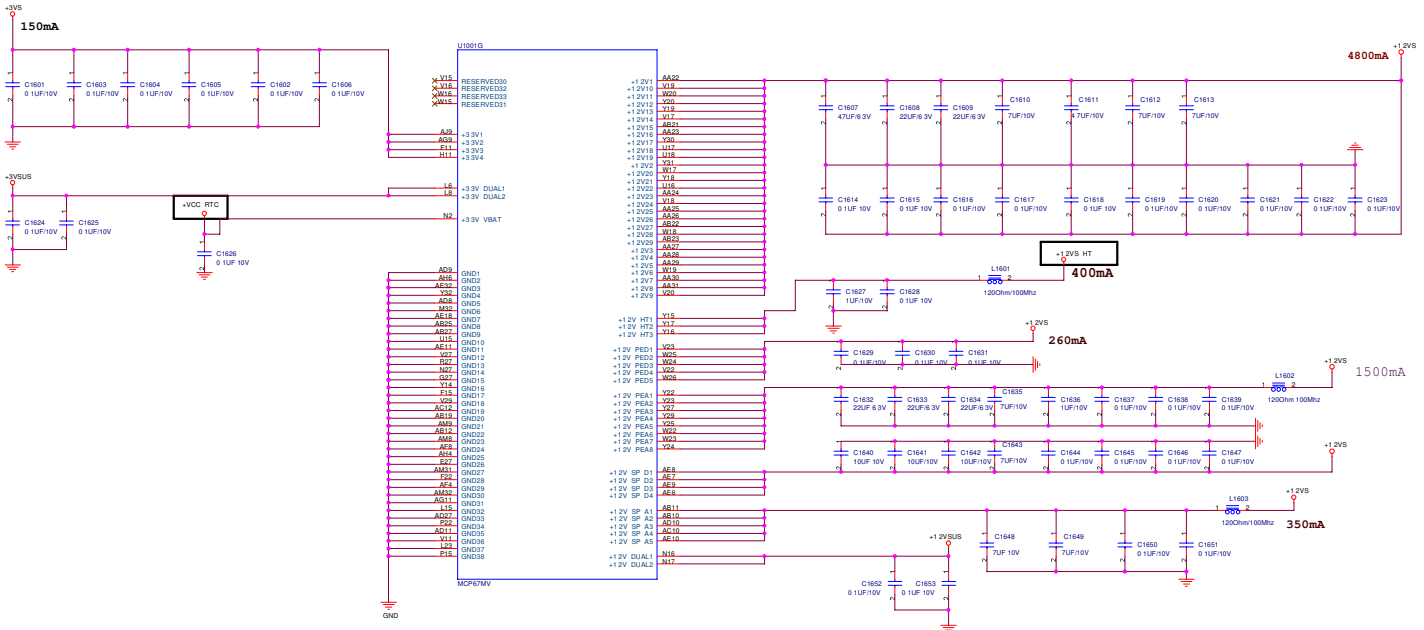
SIO CLOCK select	
0	14 31818 MHz(Default)
1	24 MHz

Networking select	
0	MII
1	RGMII

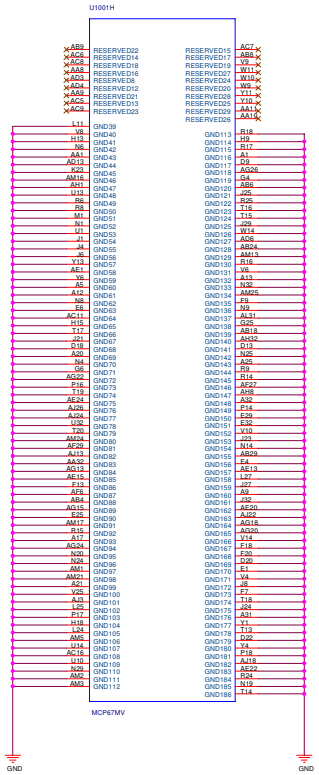
BIOS Select	
00	LPC BIOS
01	PCI BIOS

Title : F5U
Engineer: He_Wang
ASUSTeK Computer INC
Size: C | Project Name: F5U | Rev: 1.0
Date: 星期一 09 2007 | Sheet 14 of 88





Title : F5U
ASUSTeK Computer INC
Engineer: He_Wang
Size: C
Project Name: F5U
Rev: 1.0
Date: 星期三, 三月 28, 2007
Sheet 18 of 88



ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 星期三, 三月 28, 2007 Sheet 17 of 88

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 星期三, 四月 25, 2007 Sheet 18 of 88

ASUSTeK Computer INC

Title : F5U

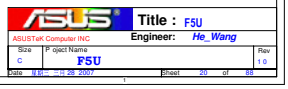
Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 星期三, 四月 25, 2007 Sheet 19 of 88

http://konweer.kiev.ua

<< Kennedy_Zhang >>



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<< Kennedy_Zhang >>

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 星期一, 十月 29, 2007 Sheet 21 of 88

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 日 01 一月 28 2007 Sheet 22 of 88

http://konweer.kiev.ua

<< Kennedy_Zhang >>

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 日 8月 26 2007 Sheet 23 of 88

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 日 8月 26 2007 Sheet 24 of 88

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 日 8月 19 28 2007 Sheet 25 of 88

ASUSTeK Computer INC

Title : F5U

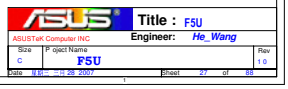
Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 日 8月 26 2007 Sheet 28 of 88

http://konweer.kiev.ua

<< Kennedy_Zhang >>



ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 日 01 一月 28 2007 Sheet 28 of 88

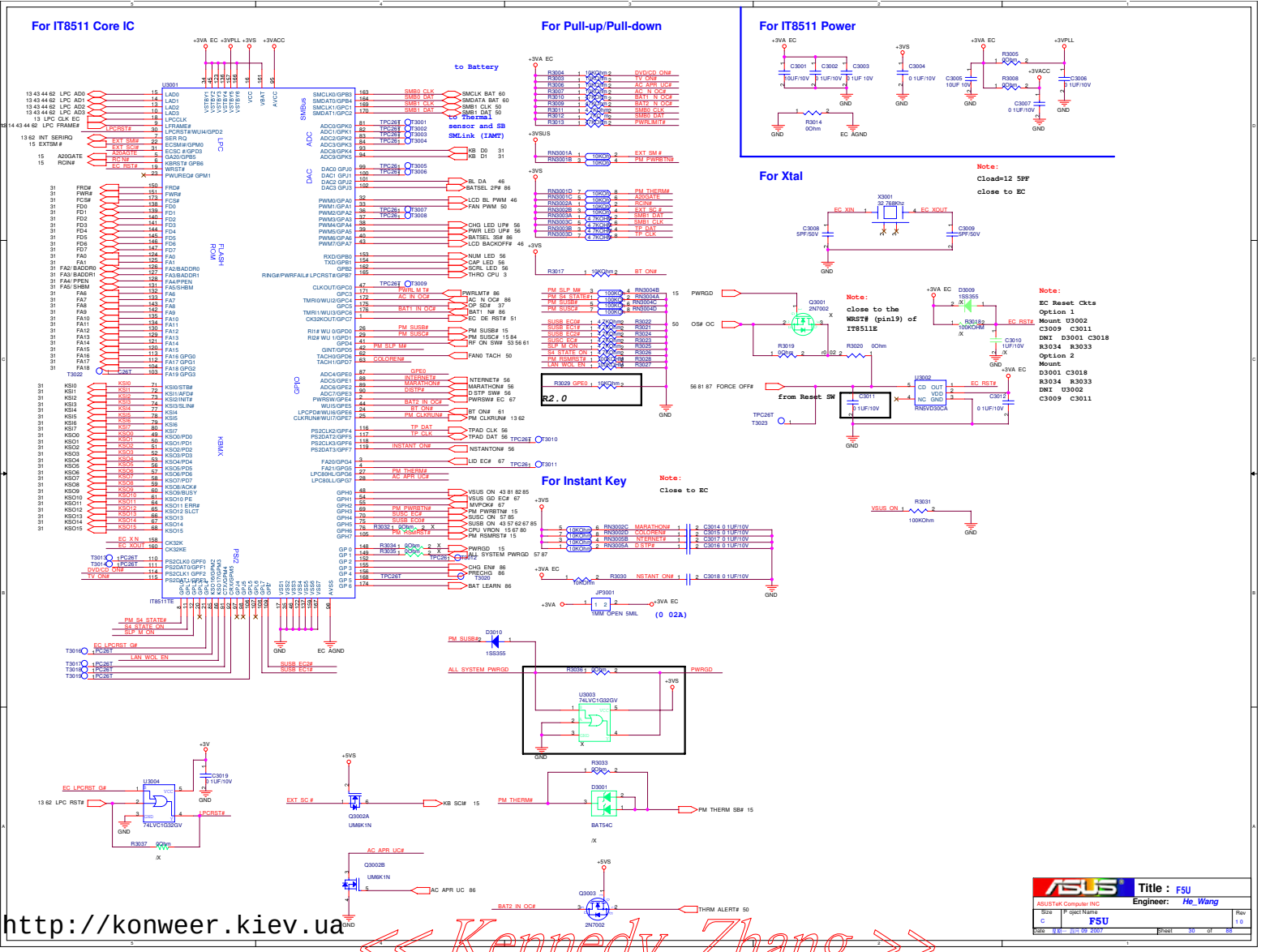
ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

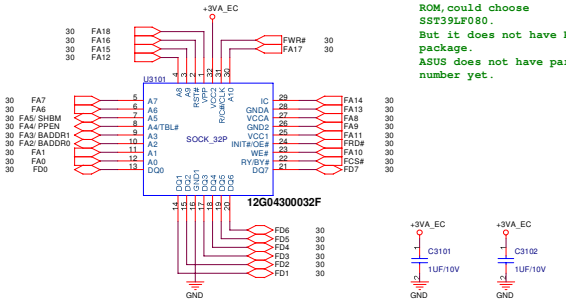
Size	Project Name	Rev
C	F5U	1.0

Date: 日 8月 19 28 2007 Sheet 29 of 88



Title : F5U	
ASUSTeK Computer INC	Engineer: He_Wang
Size C	P oject Name F5U
Rev 1.0	
Date 日期: 09 2007	Sheet 30 of 88

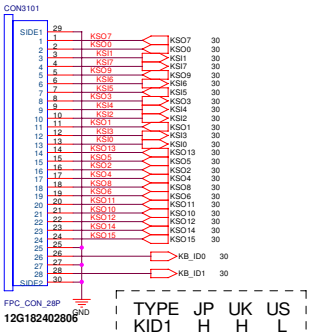
ISA ROM
(4Mbits)



SST-PLCC32 4Mbits Flash ROM
PN:05G001014110
(FLASH SST SST39VF040-70-4C-NHE
4M-70 PLCC-32)

If need to use 8Mbits ISA ROM, could choose SST39LF080.
But it does not have PLCC32 package.
ASUS does not have part number yet.

KBC connector



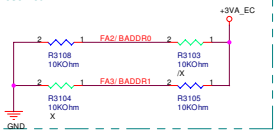
TYPE	JP	UK	US
KID1	H	H	L
KID2	L	H	L

ISA ROM

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

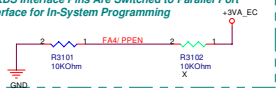
00: PNPCNG Access Register Pair Are 002Eh and 002Fh
10: PNPCNG Access Register Pair Are 004Eh and 004Fh
01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
11: Reserved



Note: Sampled at VSTBY Power Up Reset

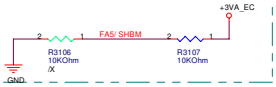
FA4/ PPEN

0: Normal
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

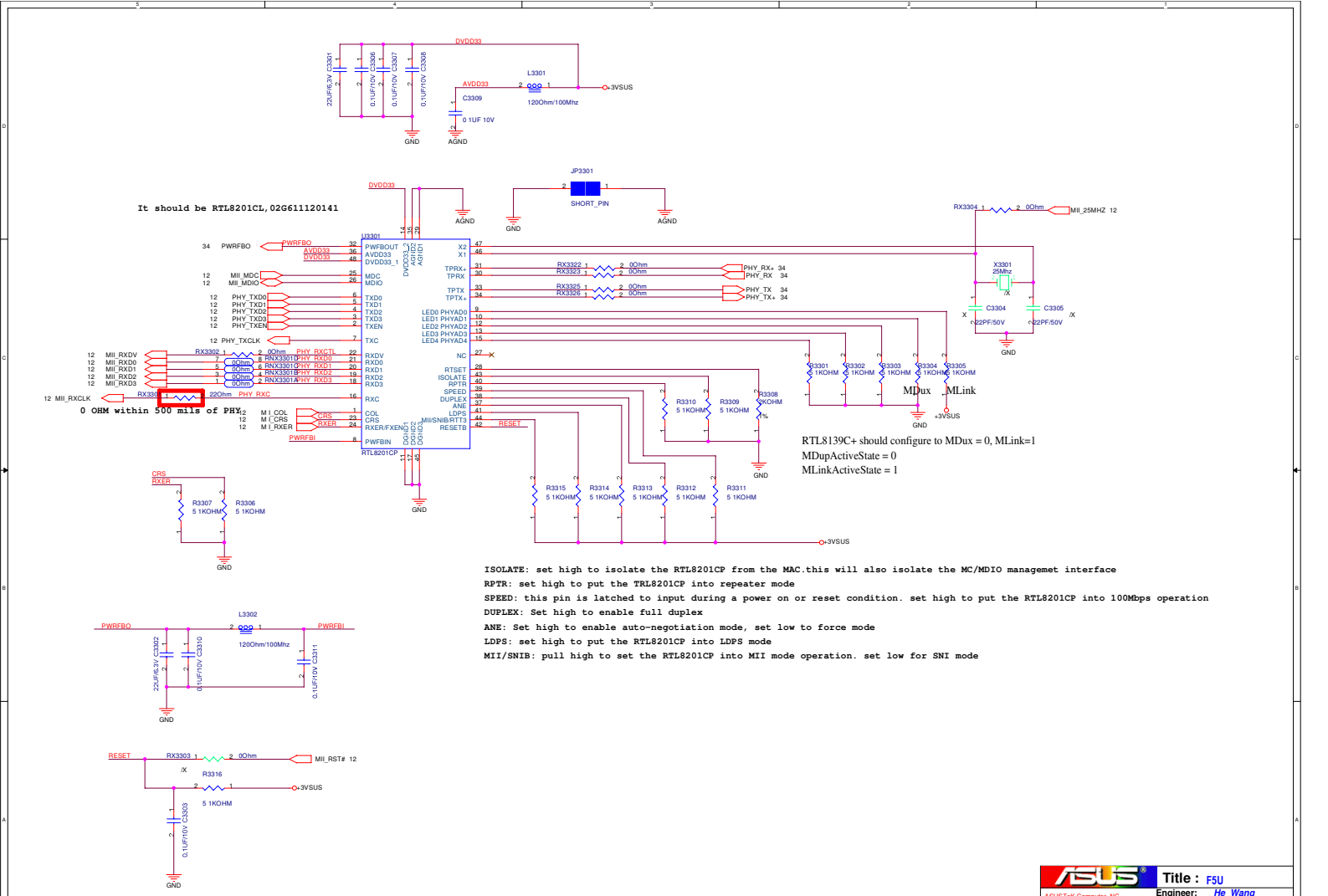


FA5/ SHBM

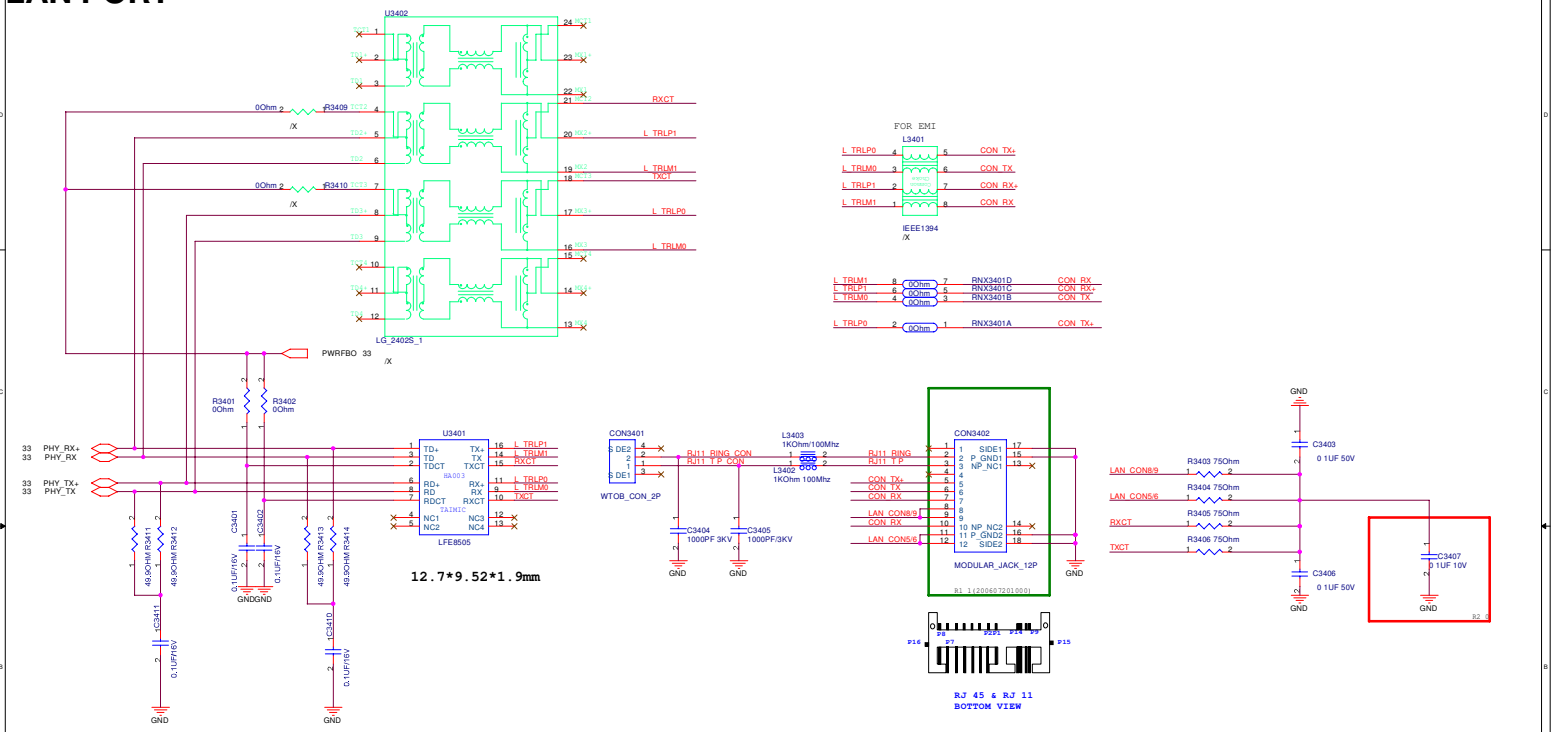
0: Disable Shared Memory with Host BIOS
1: Enable Shared Memory with Host BIOS



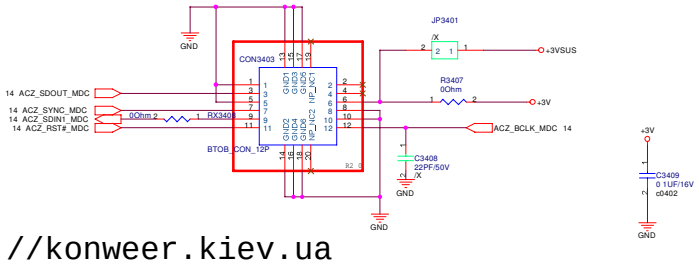
Title : F5U		
ASUSTeK Computer NC	Engineer: He_Wang	
Size: Custom	Project Name: F5U	Rev: 1.0
Date: 四月 09, 2007	Sheet 31 of 88	



LAN PORT



MDC CONN.



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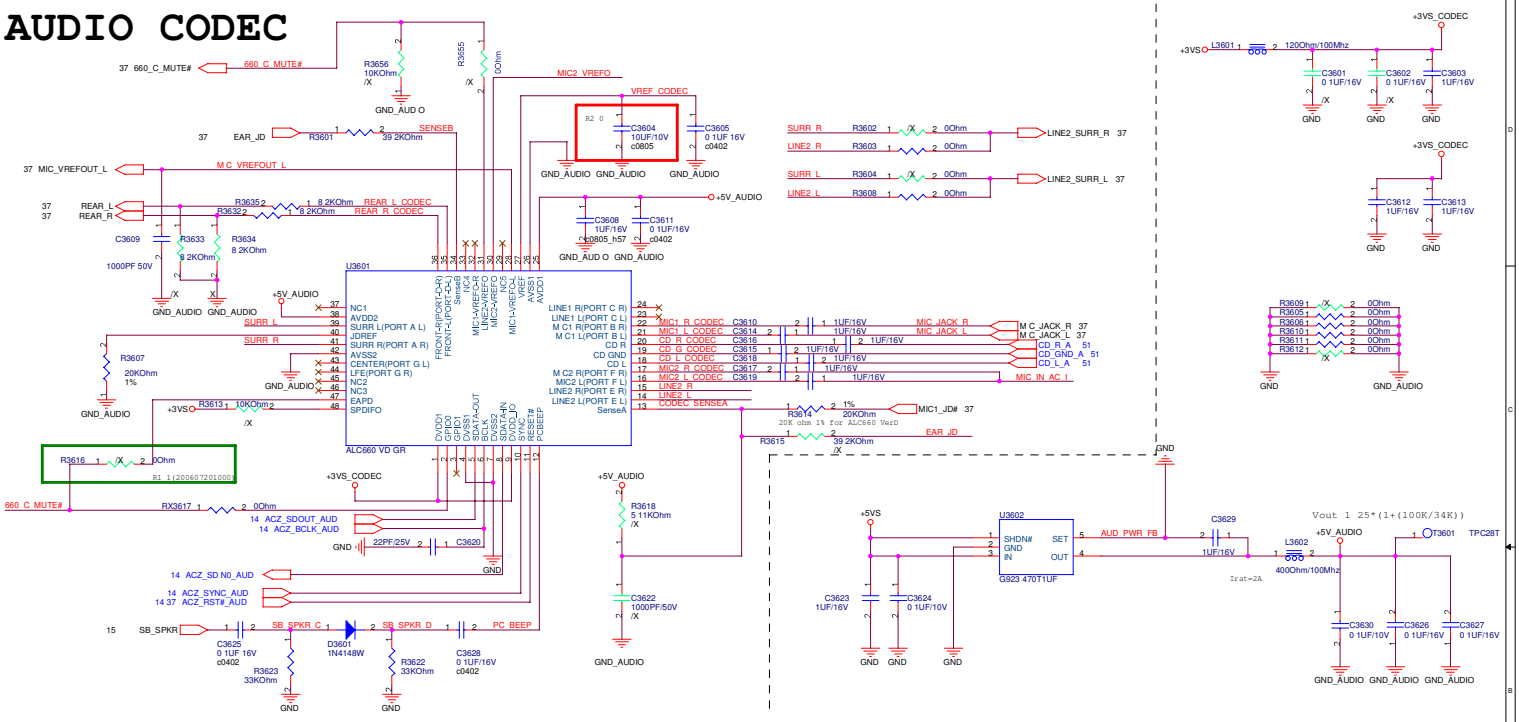
ASUSTeK Computer NC	Title : F5U	
	Engineer: He_Wang	
Size: Custom	Project Name: F5U	Rev: 1.0
Date: 試題一 四月 09 2007	Sheet 34 of 88	

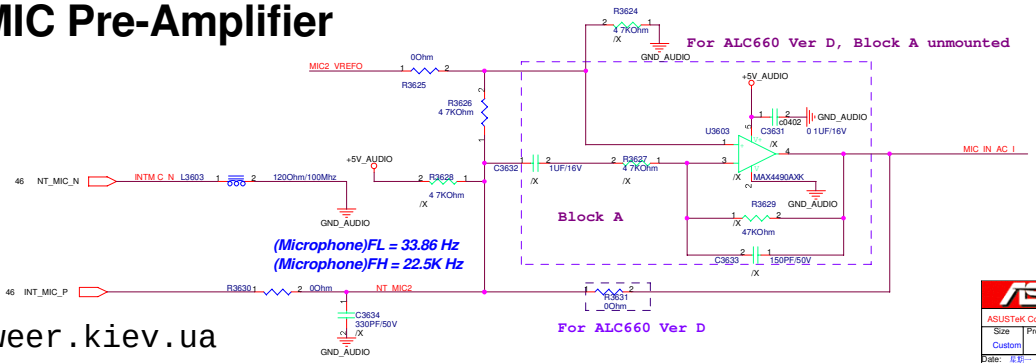
<< Kennedy_Zhang >>

Title :	F5U
ASUSTeK Computer INC	Engineer: He_Wang
Size: Custom	Project Name: F5U
Rev: 1.0	
Date: 星期一, 一月 28, 2007	Sheet 35 of 88

AUDIO CODEC



Internal MIC Pre-Amplifier



ASUSTeK Computer INC	Title : F5U		
	Engineer: He_Wang		
Size: Custom	Project Name: F5U		Rev: 1.0
Date: 星期一 四月 09 2007	Sheet 36 of 88		

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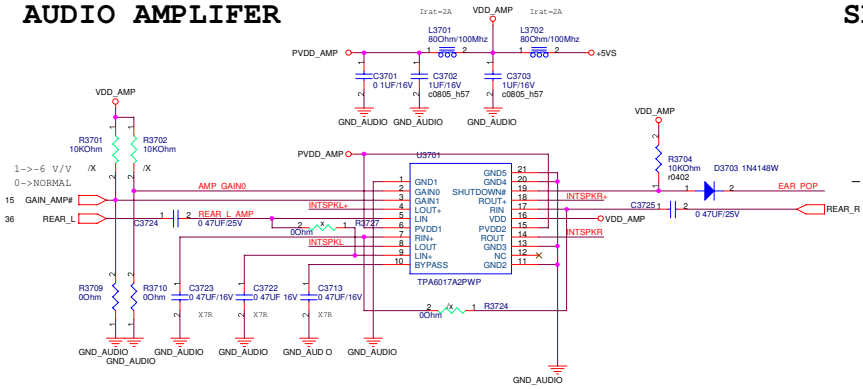
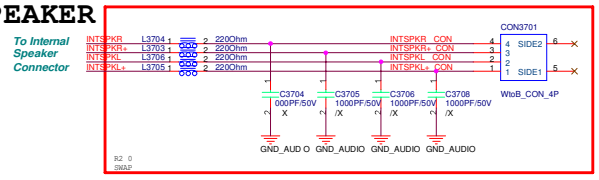
<< Kennedy_Zhang >>

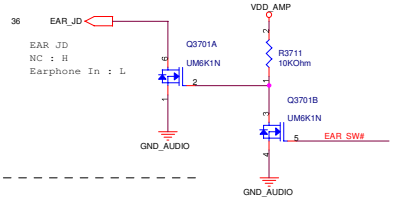
AUDIO AMPLIFER



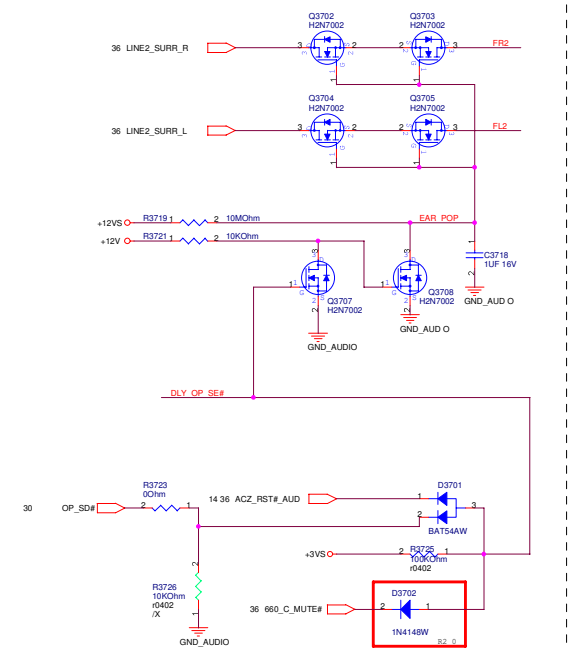
SPEAKER

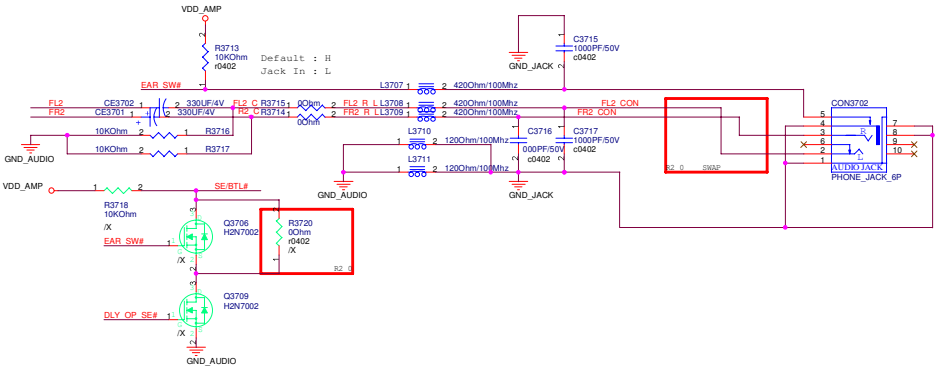


HeadPhone

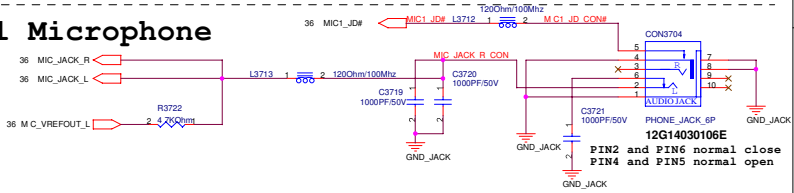


DEPOP CIRCUIT





External Microphone



ASUSTeK Computer INC	Title : F5U	
	Engineer: He_Wang	
Size: Custom	Project Name: F5U	Rev: 1.0
Date: 星期一 四月 09 2007	Sheet 37 of 88	

ASUSTeK Computer INC	Title : F5U		
	Engineer: He_Wang		
Size: Custom	Project Name: F5U		Rev: 1.0
Date: 星期三, 十月 28, 2007		Sheet 38 of 88	

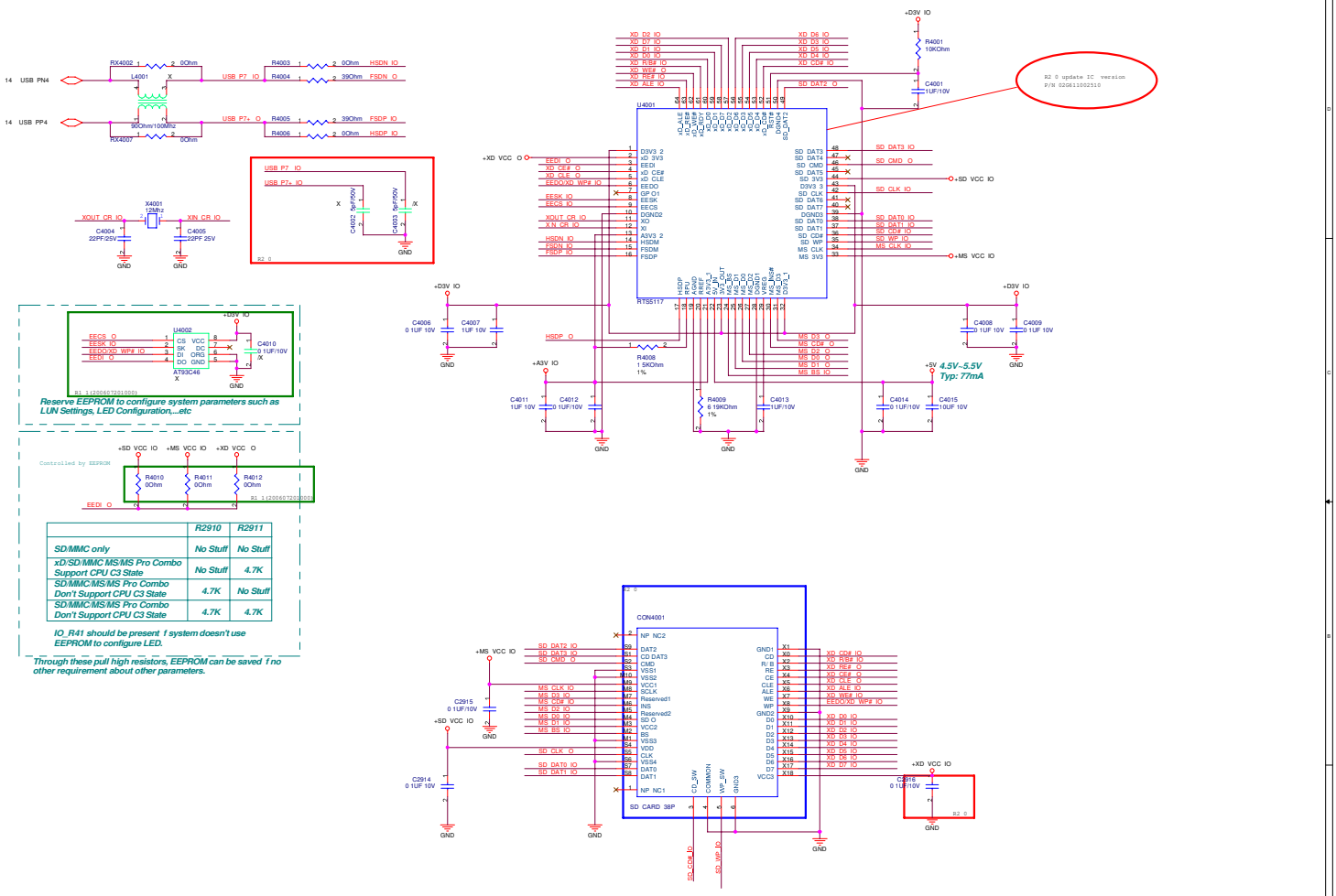
ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

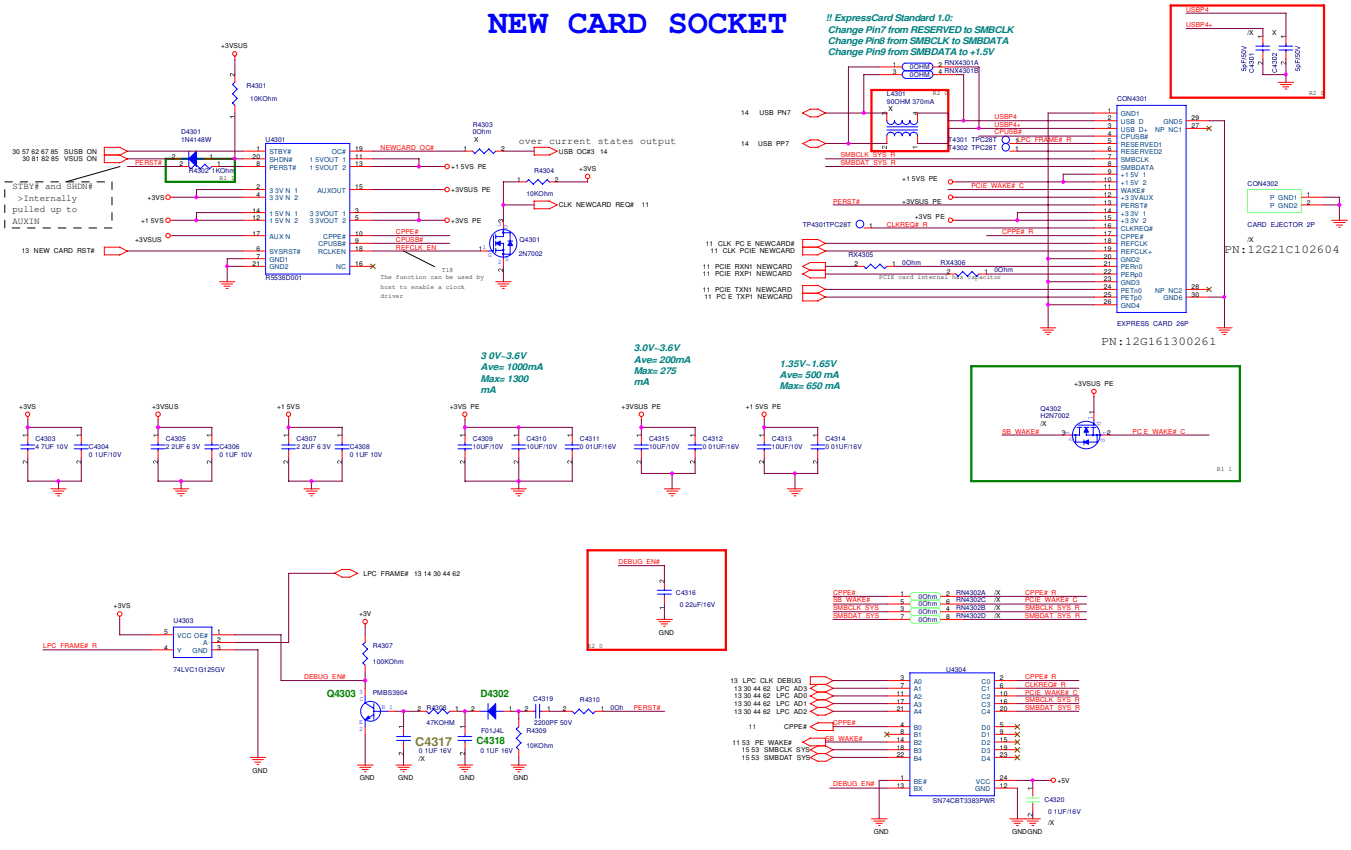
Date: 星期三, 四月 25, 2007 Sheet 39 of 88

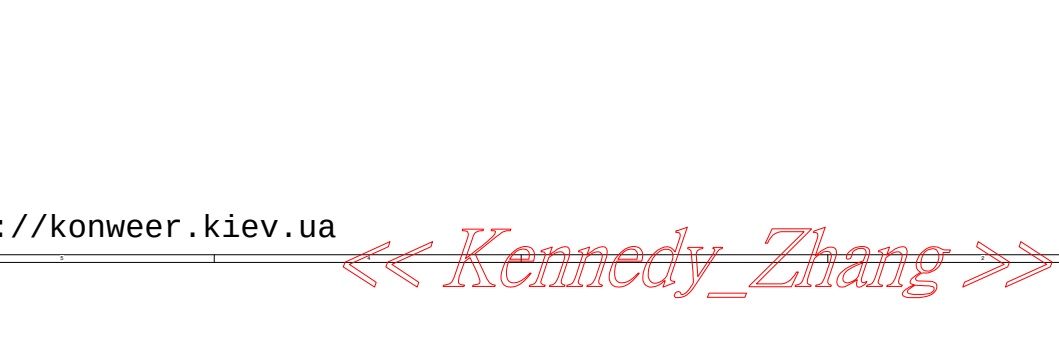


	R2910	R2911
SD/MMC only	No Stuff	No Stuff
xD/SD/MMC MS/MS Pro Combo Support CPU C3 State	No Stuff	4.7K
SD/MMC/MS/MS Pro Combo Don't Support CPU C3 State	4.7K	No Stuff
SD/MMC/MS/MS Pro Combo Don't Support CPU C3 State	4.7K	4.7K

ASUSTeK Computer INC	Title : F5U	
	Engineer: He_Wang	
Size: C	Project Name: F5U	Rev: 1.0
Date: 星期一 09, 2007	Sheet 40 of 88	

NEW CARD SOCKET

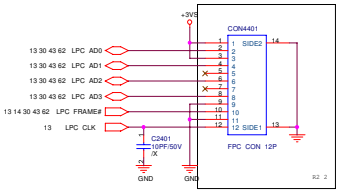




http://konweer.kiev.ua

ASUSTeK Computer INC	Title : F5U		
	Engineer: He_Wang		
Size: C	Project Name: F5U		Rev: 1.0
Date: 星期一 09, 2007	Sheet 43 of 88		

LPC DEBUG CONNCTOR



ASUSTeK Computer INC

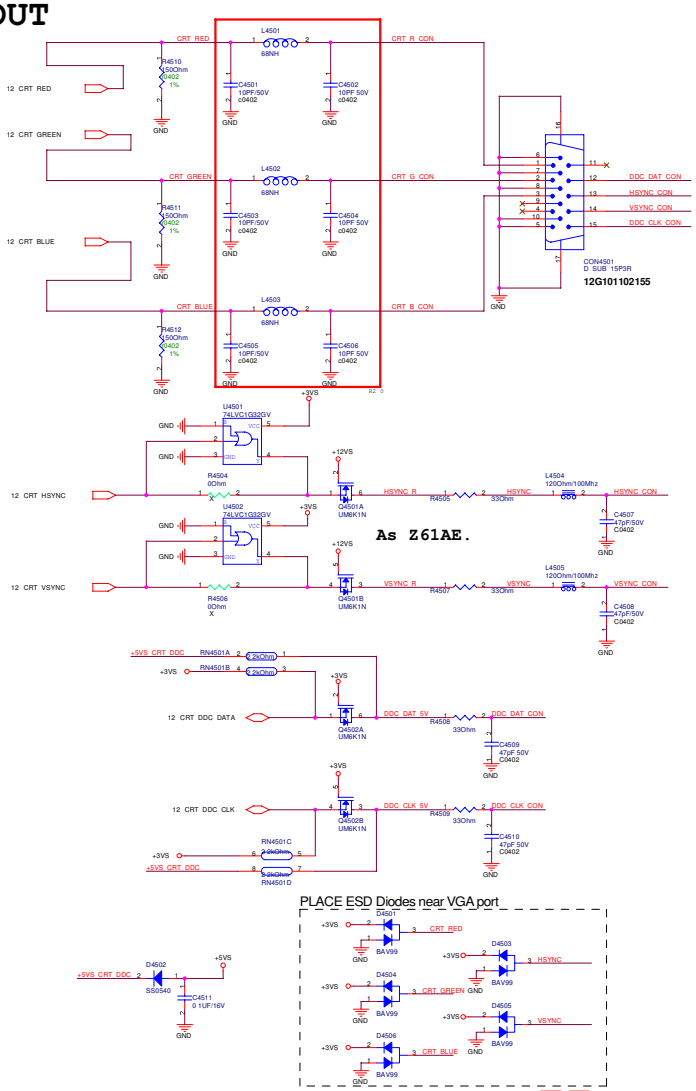
Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 日期 09, 2007 Sheet 44 of 88

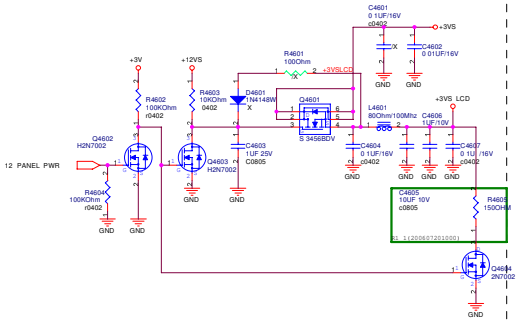
VGA OUT



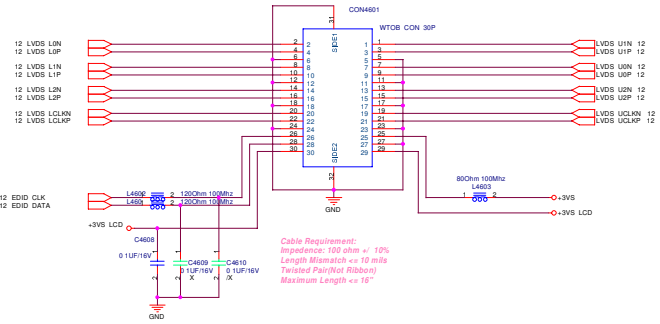
As Z61AE.

ASUSTeK Computer INC	Title : F5U	
	Engineer: He_Wang	
Size: C	Project Name: F5U	Rev: 1.0
Date: 星期二 09, 2007	Sheet 45 of 88	

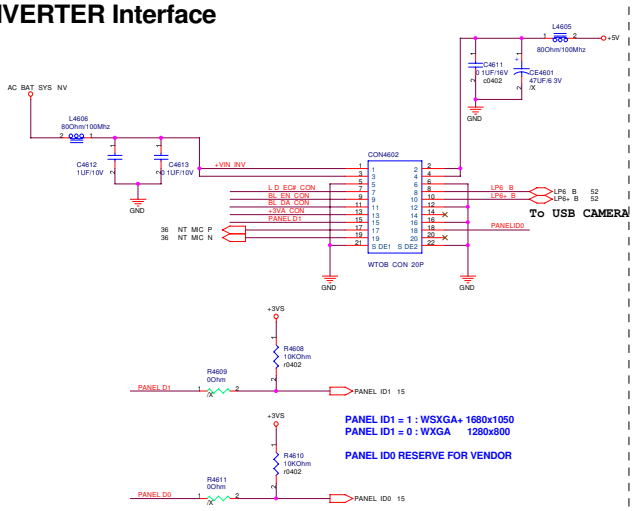
LCD Power



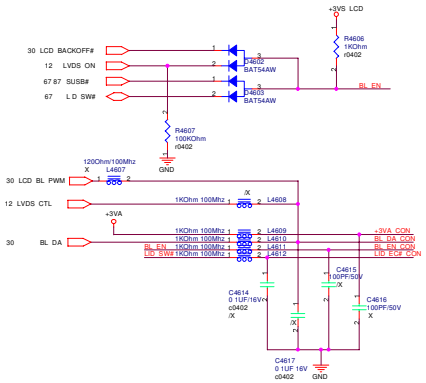
LCD LVDS Interface



INVERTER Interface



Backlight Enable



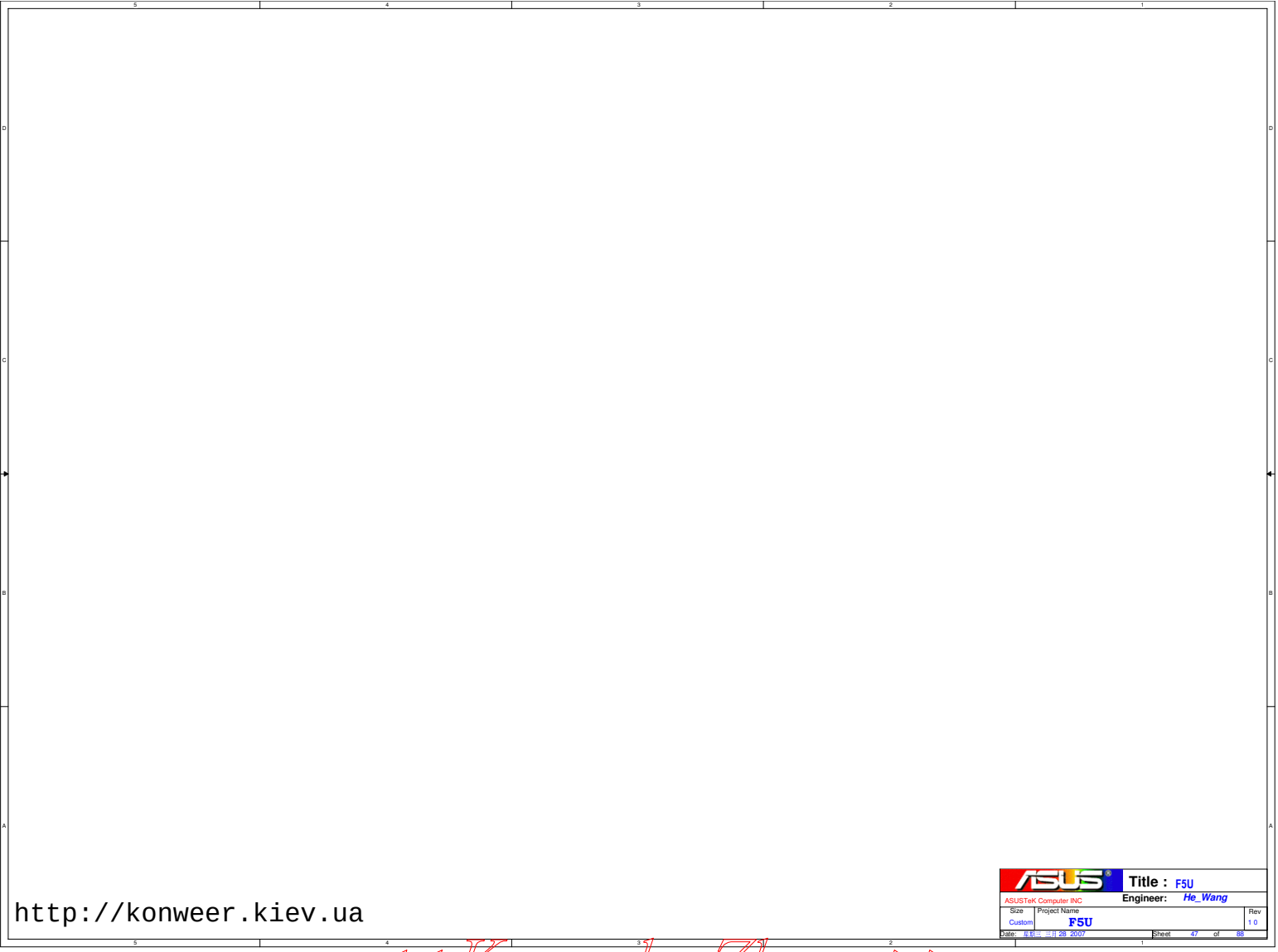
ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 日期 09, 2007 Sheet 46 of 88



Title : F5U

ASUSTeK Computer INC

Engineer: He_Wang

Size	Project Name	Rev
Custom	F5U	1.0

Date: 星期三, 二月 28, 2007 Sheet 47 of 88

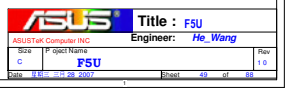
http://konweer.kiev.ua

<< Kennedy_Zhang >>

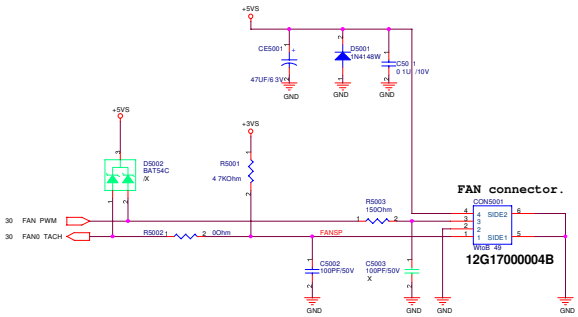
ASUSTeK Computer INC	Title : F5U	
	Engineer: He_Wang	
Size: C	Project Name: F5U	Rev: 1.0
Date: 星期三, 四月 25, 2007	Sheet 48 of 88	

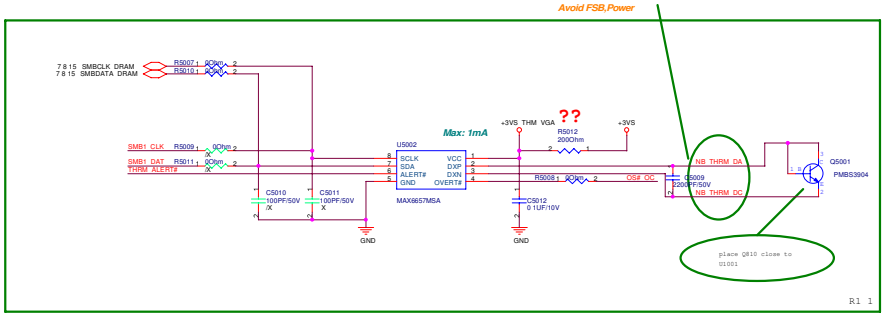
http://konweer.kiev.ua

<< Kennedy_Zhang >>



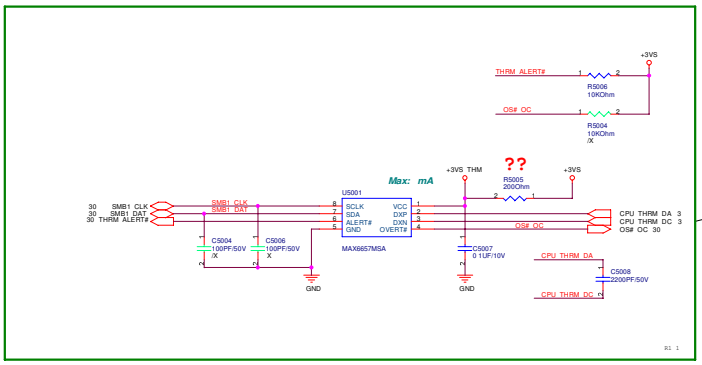
DC FAN control





OTHER SIGNALS
15 mils
==========GND
10 mils
========NB_THRM_DA(0 mils)
10 mils
========NB_THRM_DC(0 mils)
10 mils
========GND
15 mils
OTHER SIGNALS
Avoid FSB,Power

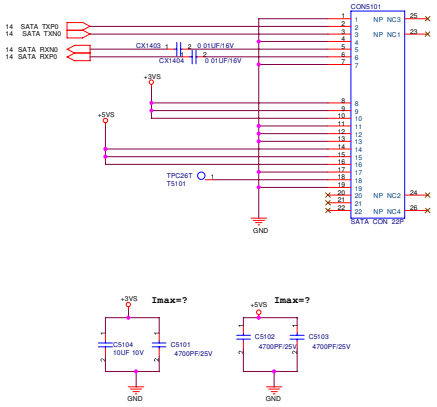
Thermal Sensor



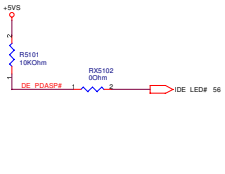
Route CPU_THRM_DA and CPU_THRM_DC on the same layer
OTHER SIGNALS
15 mils
==========GND
10 mils
========H_THERMDA(10 mils)
10 mils
========H_THERMDC(10 mils)
10 mils
========GND
15 mils
OTHER SIGNALS
Avoid FSB,Power

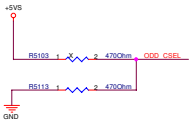
ASUSTeK Computer INC	Title : F5U		
	Engineer: He_Wang		
Size: C	Project Name: F5U		Rev: 1.0
Date: 日期: 09 2007	Sheet 50 of 88		

SATA_HDD(Default)

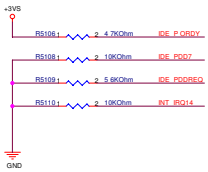


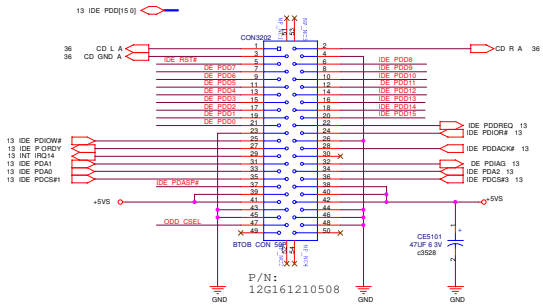
CD-ROM

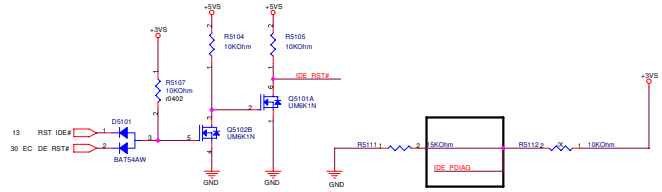




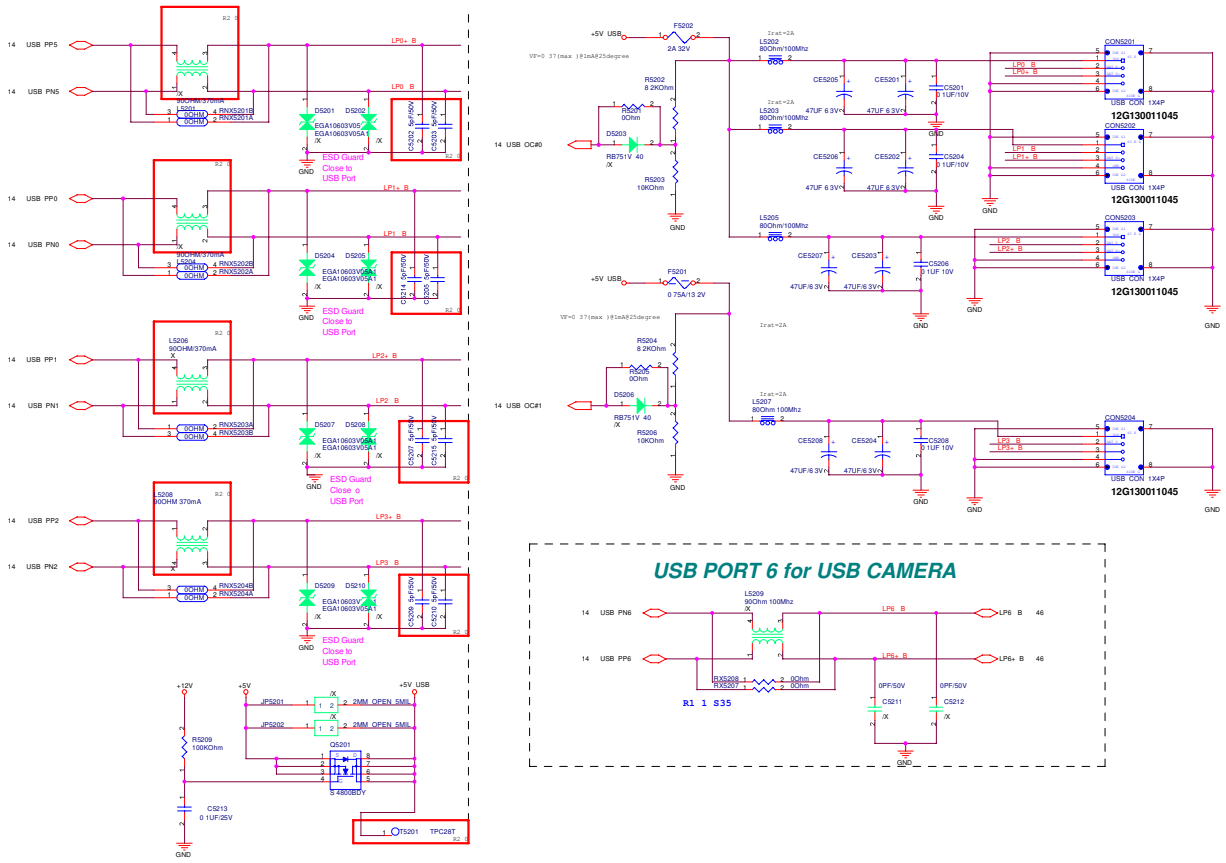
ODD CSEL
Pull Up: CDROM as Slave
Pull Down: CDROM as Master







ASUSTeK Computer INC	Title : F5U		
	Engineer: He_Wang		
Size: C	Project Name: F5U		Rev: 1.0
Date: 星期二 09 2007	Sheet 51 of 88		



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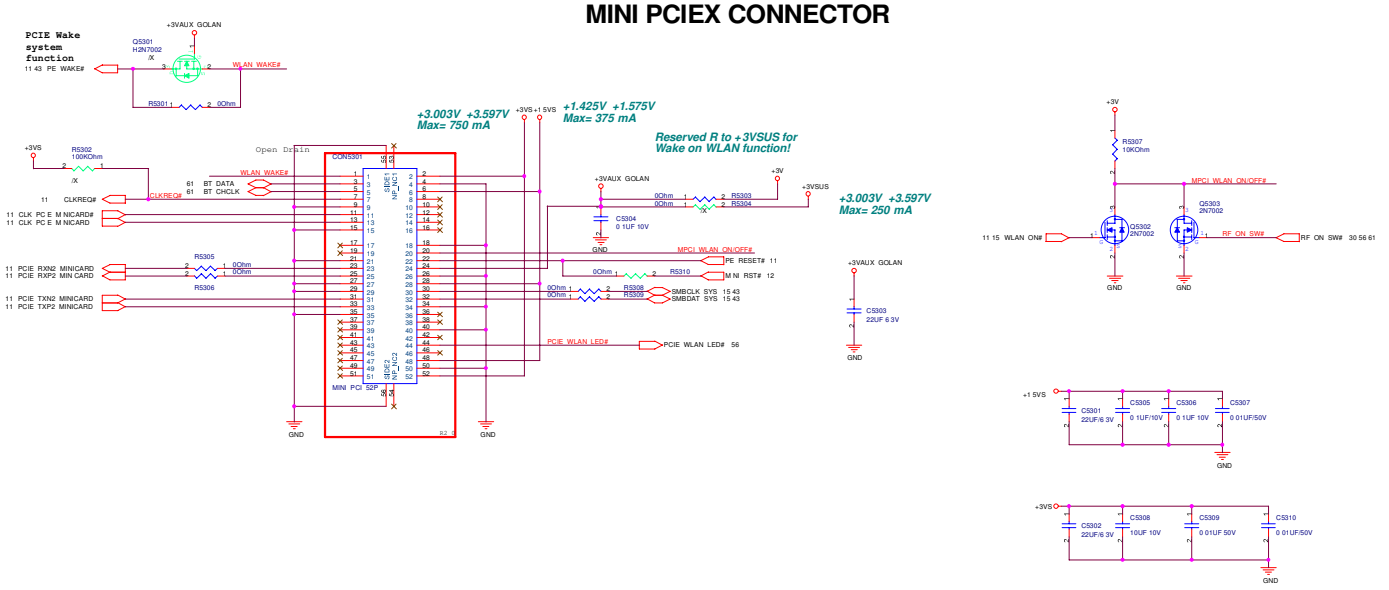
<< Kennedy_Zhang >>

ASUSTeK Computer INC	Title : F5U		
	Engineer: He_Wang		
Size: C	Project Name: F5U		Rev: 1.0
Date: 星期一 09 2007	Sheet 52 of 88		

MINI PCIEX CONNECTOR



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<< Kennedy_Zhang >>

ASUSTeK Computer INC	Title : F5U	
	Engineer: He_Wang	
Size: C	Project Name: F5U	Rev: 1 0
Date: 日期 日 09 2007	Sheet 53 of 88	

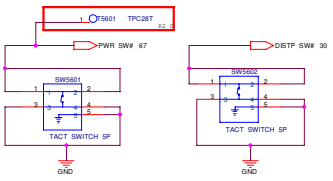
ASUSTeK Computer INC

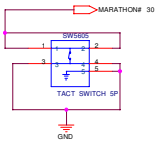
Title : F5U

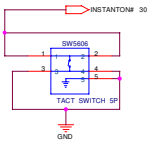
Engineer: He_Wang

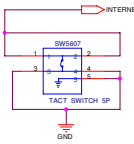
Size	Project Name	Rev
C	F5U	1.0

Date: 星期三, 四月 25, 2007 Sheet 55 of 88

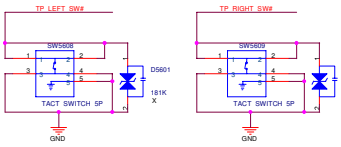


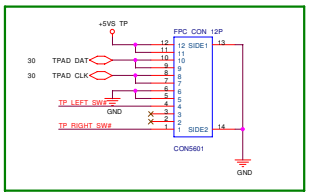




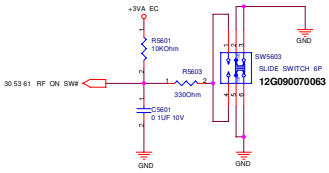


TOUCH PAD SWITCH

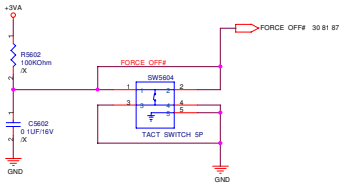




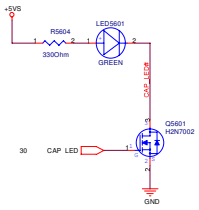
RF ON/OFF SWITCH
For Side SW
(Left side is turn ON.)



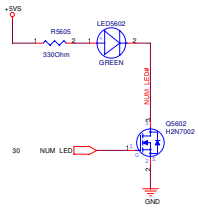
SHUT_DOWN#



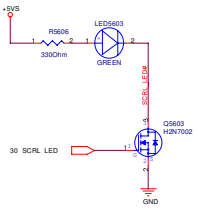
for Cap. Lock



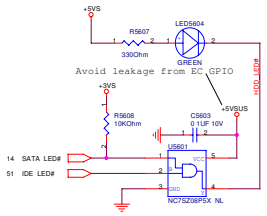
for Num Lock



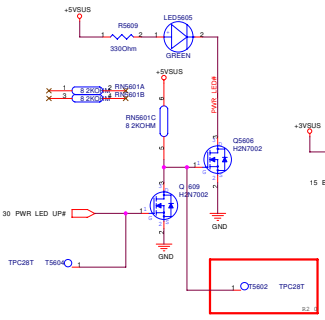
for Scroll Lock



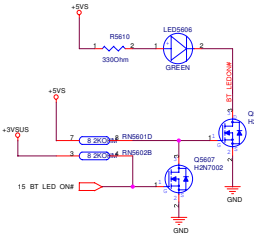
For SATA/IDE LED



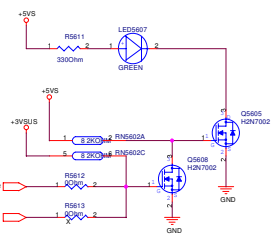
For POWER LED



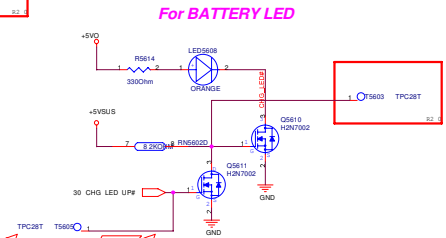
For BT LED



For WireLess LED

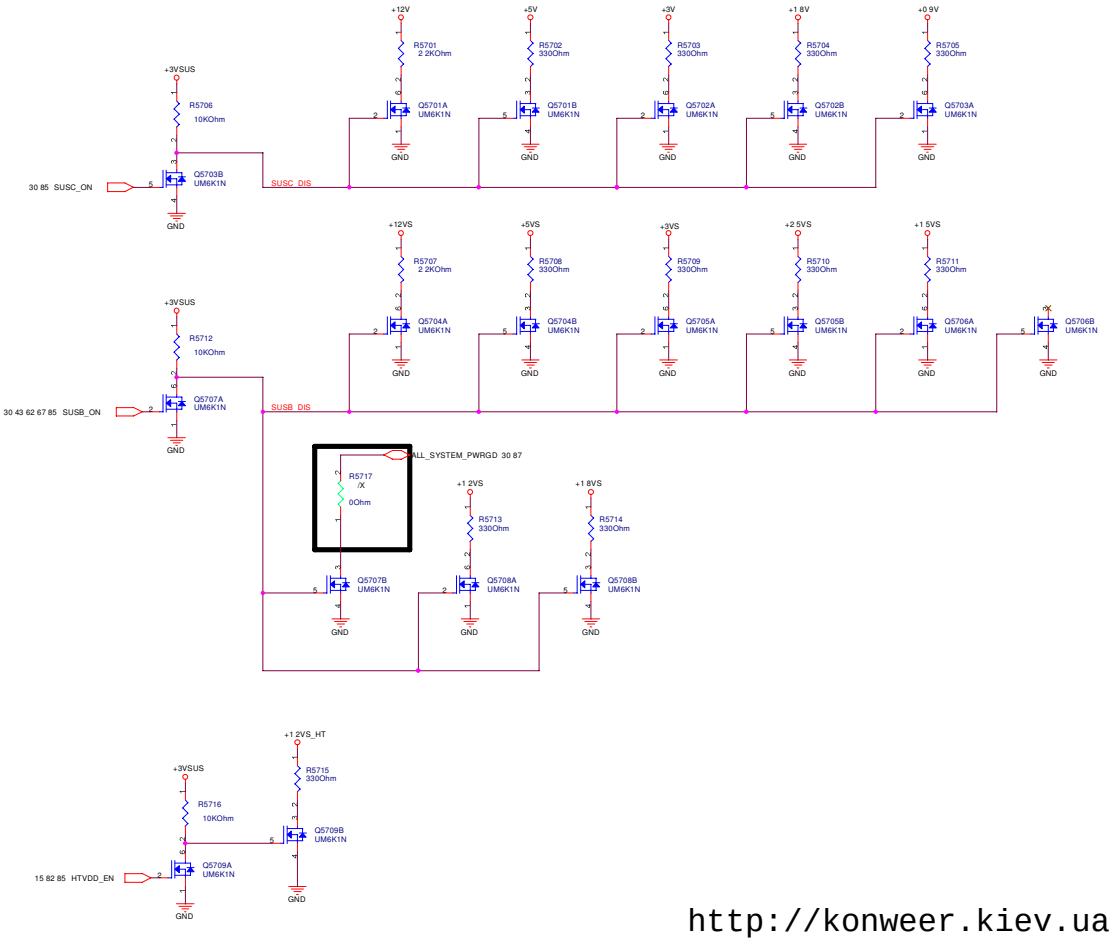


For BATTERY LED



ASUSTeK Computer INC	Title : F5U		
	Engineer: He_Wang		
Size: C	Project Name: F5U		Rev: 1.0
Date: 日期 09, 2007	Sheet 56 of 88		

DISCHARGE CIRCUIT



ASUSTeK Computer NC	Title : F5U	
	Engineer: He_Wang	
Size: Custom	Project Name: F5U	Rev: 1.0
Date: 星期一 四月 09 2007	Sheet 57 of 88	

ASUSTeK Computer INC

Title : F5U

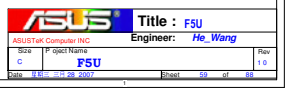
Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

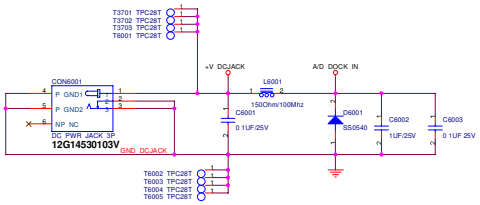
Date: 星期三, 四月 25, 2007 Sheet 58 of 88

http://konweer.kiev.ua

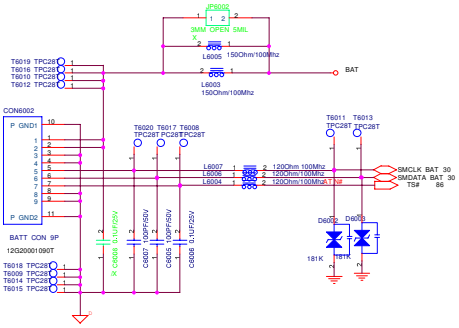
<< Kennedy_Zhang >>



Adaptor IN Circuit



BATTERY IN CIRCUIT

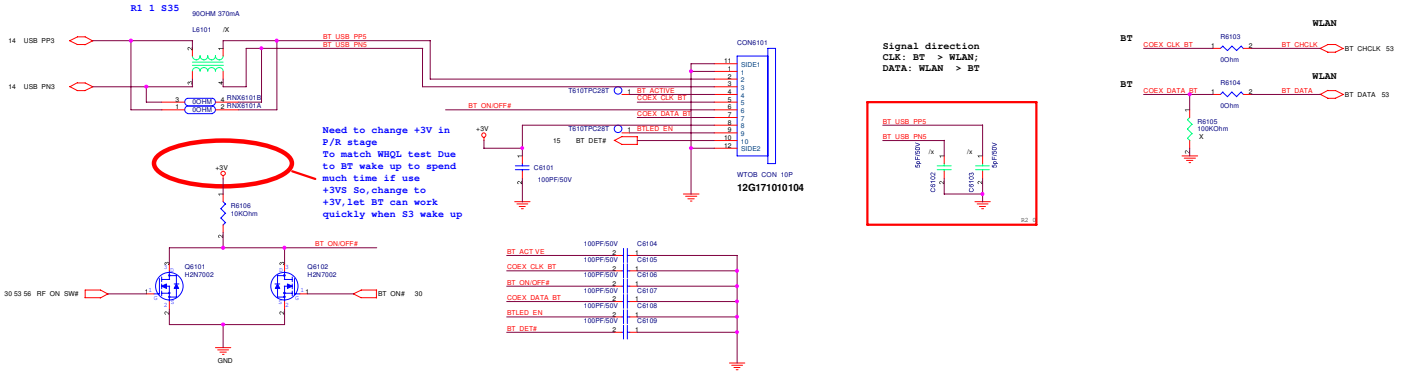


http://konweer.kiev.ua

<< Kennedy_Zhang >>

ASUSTeK Computer INC	Title : F5U	
	Engineer: He_Wang	
Size: C	Project Name: F5U	Rev: 1.0
Date: 星期一 09, 2007	Sheet 60 of 88	

BLUETOOTH CONNECTOR

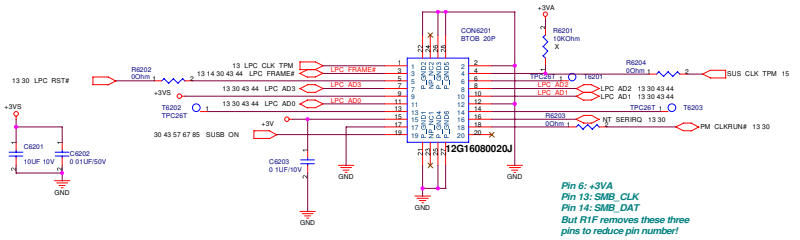


http://konweer.kiev.ua

<< Kennedy_Zhang >>

ASUSTeK Computer INC	Title : F5U	
	Engineer: He_Wang	
Size: C	Project Name: F5U	Rev: 1.0
Date: 星期一 09, 2007	Sheet 61 of 88	

TPM CONN.



Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

ASUSTeK Computer INC	Title : F5U	
	Engineer: He_Wang	
Size: C	Project Name: F5U	Rev: 1.0
Date: 星期一 09, 2007	Sheet 62 of 88	

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 星期三, 四月 25, 2007 Sheet 63 of 88

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 星期三, 四月 25, 2007 Sheet 64 of 88

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 星期三, 四月 25, 2007 Sheet 65 of 88

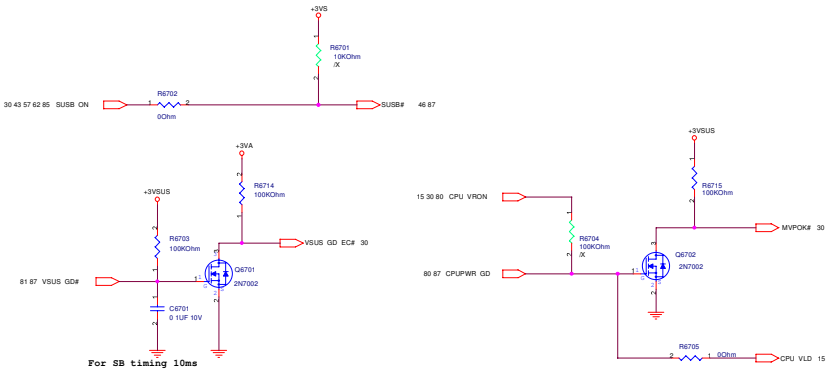
ASUSTeK Computer INC

Title : F5U

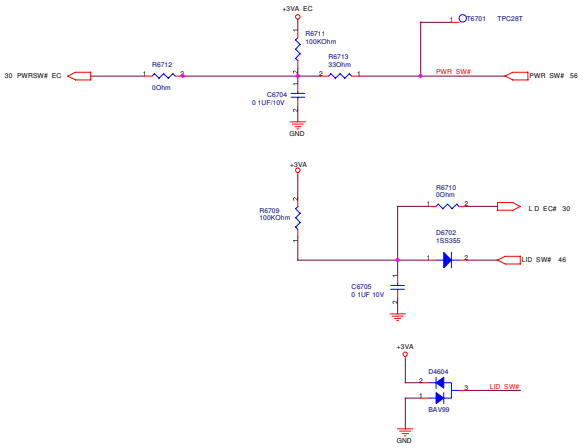
Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

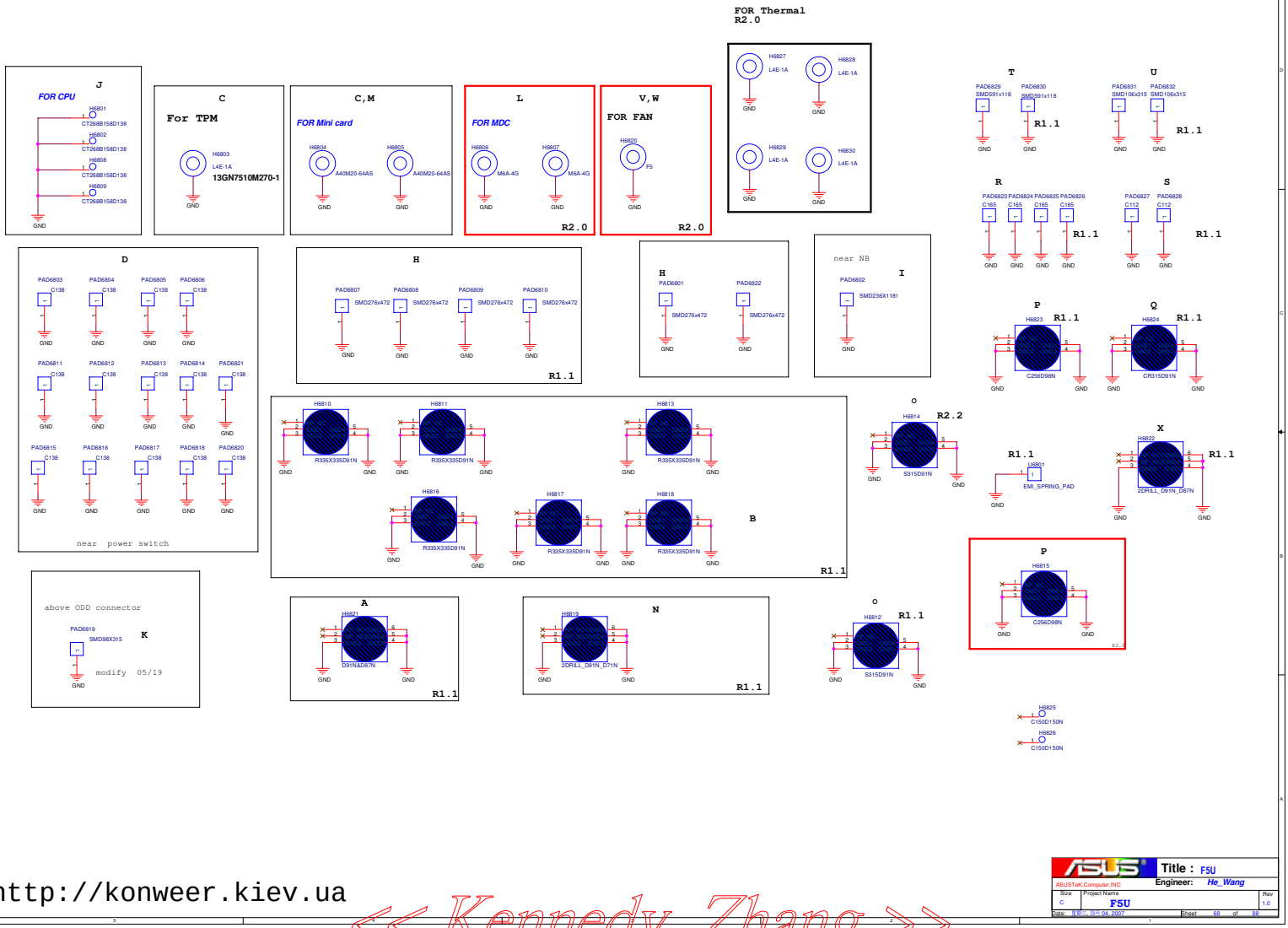
Date: 星期三, 四月 25, 2007 Sheet 66 of 88



POWER SWITCH



ASUSTeK Computer INC	Title : F5U	
	Engineer: He_Wang	
Size: C	Project Name: F5U	Rev: 1.0
Date: 星期一 09, 2007	Sheet 67 of 88	



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ASUSTeK Computer INC	Title : F5U		
	Engineer: He_Wang		
Size: C	Project Name: F5U		Rev: 1.0
Date: 星期三, 四月 04, 2007	Sheet 68 of 88		

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 星期三, 四月 25, 2007 Sheet 69 of 88

ASUSTeK Computer INC	Title : F5U	
	Engineer: He_Wang	
Size: C	Project Name: F5U	Rev: 1.0
Date: 星期三, 四月 25, 2007	Sheet 70 of 88	

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 日 8月 - 月 28 2007 Sheet 71 of 88

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 日 8月 - 月 28 2007 Sheet 72 of 88

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 日 8月 26 2007 Sheet 73 of 88

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 星期一, 十月 29, 2007 Sheet 74 of 88

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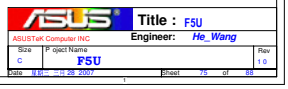
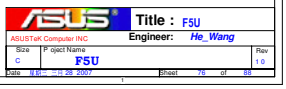
<< Kennedy_Zhang >>





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<< Kennedy_Zhang >>

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 日 8月 26 2007 Sheet 77 of 88

ASUSTeK Computer INC

Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 日 8月 - 月 28 2007 Sheet 78 of 88

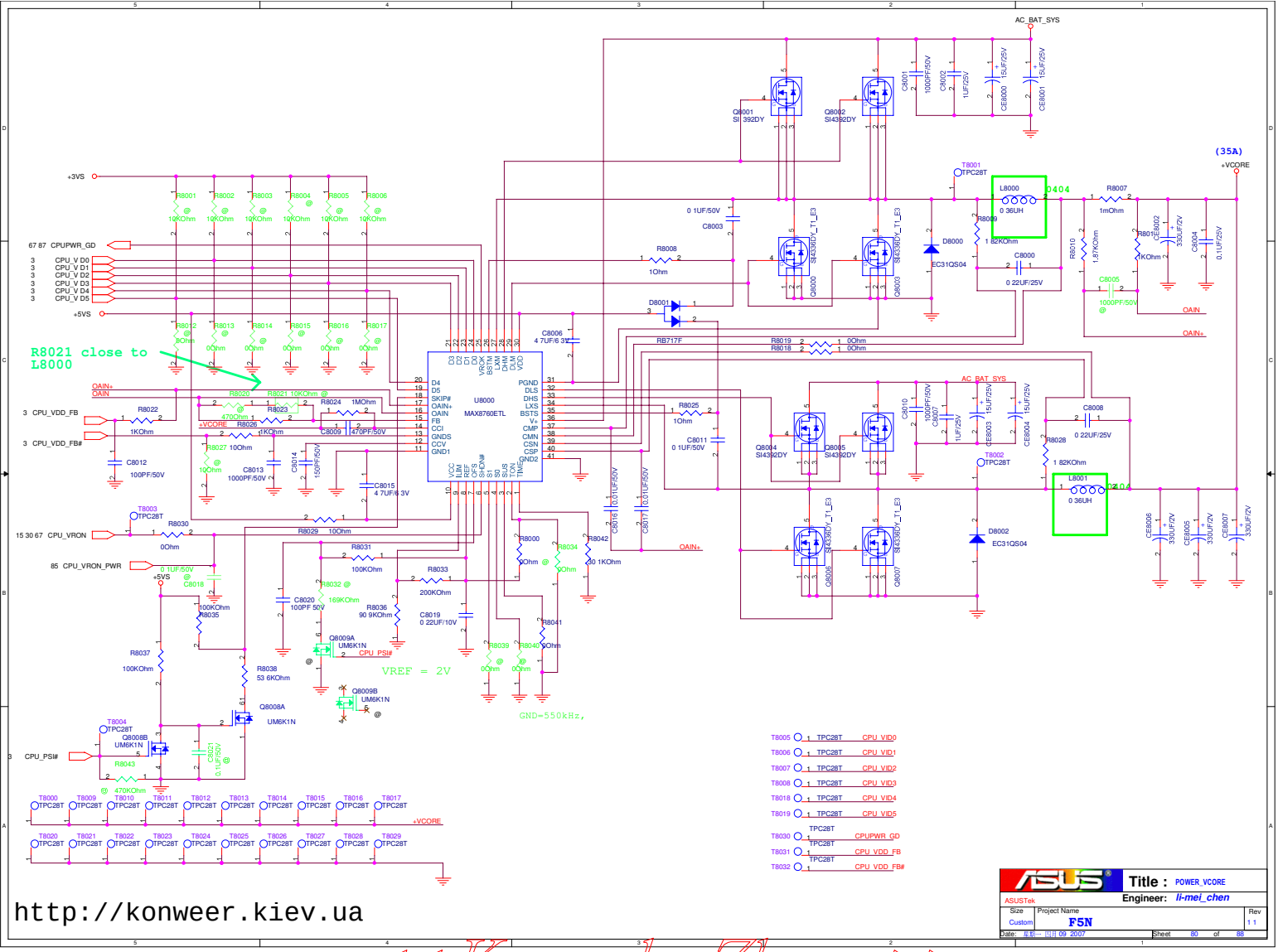
ASUSTeK Computer INC

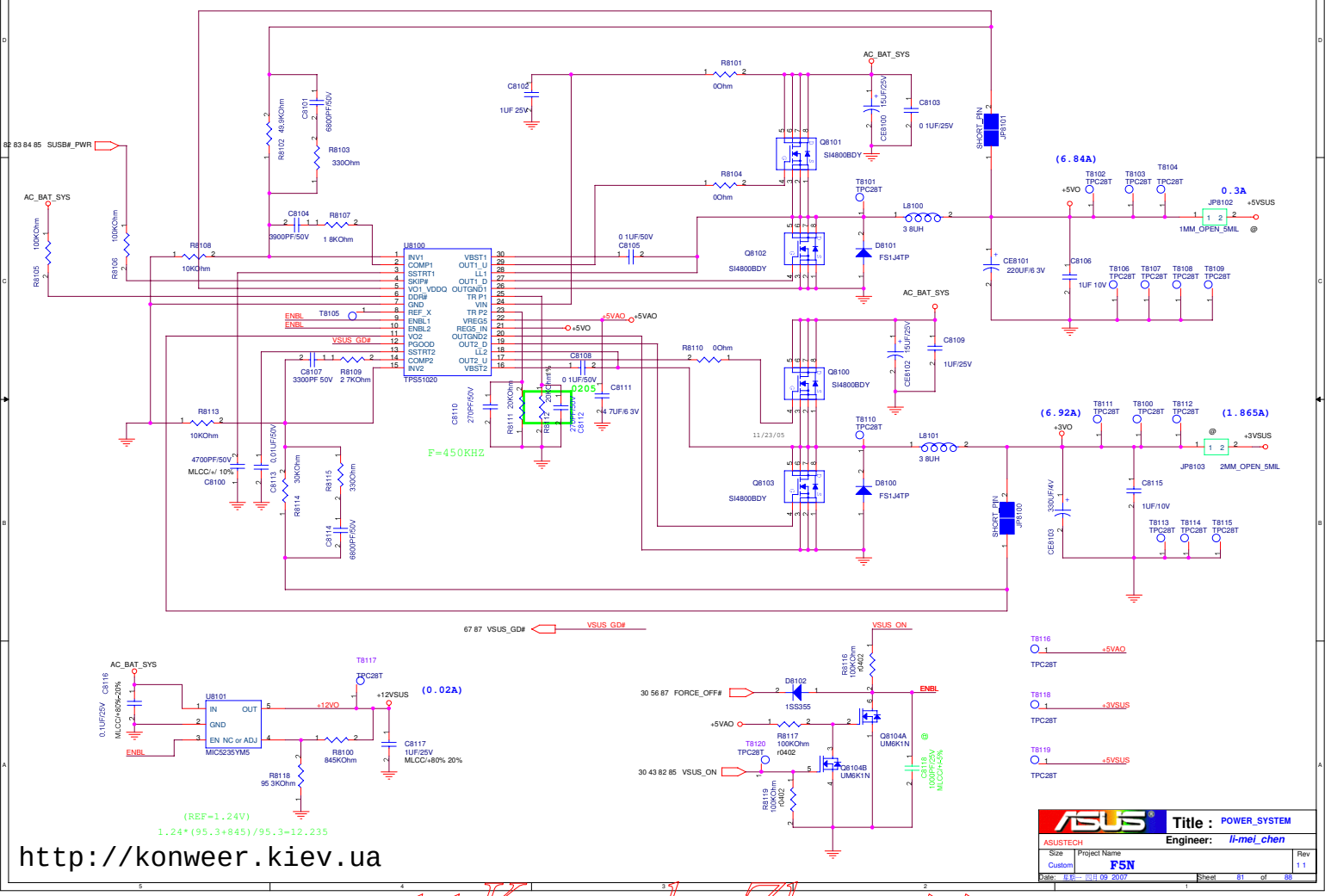
Title : F5U

Engineer: He_Wang

Size	Project Name	Rev
C	F5U	1.0

Date: 星期三, 四月 25, 2007 Sheet 79 of 88





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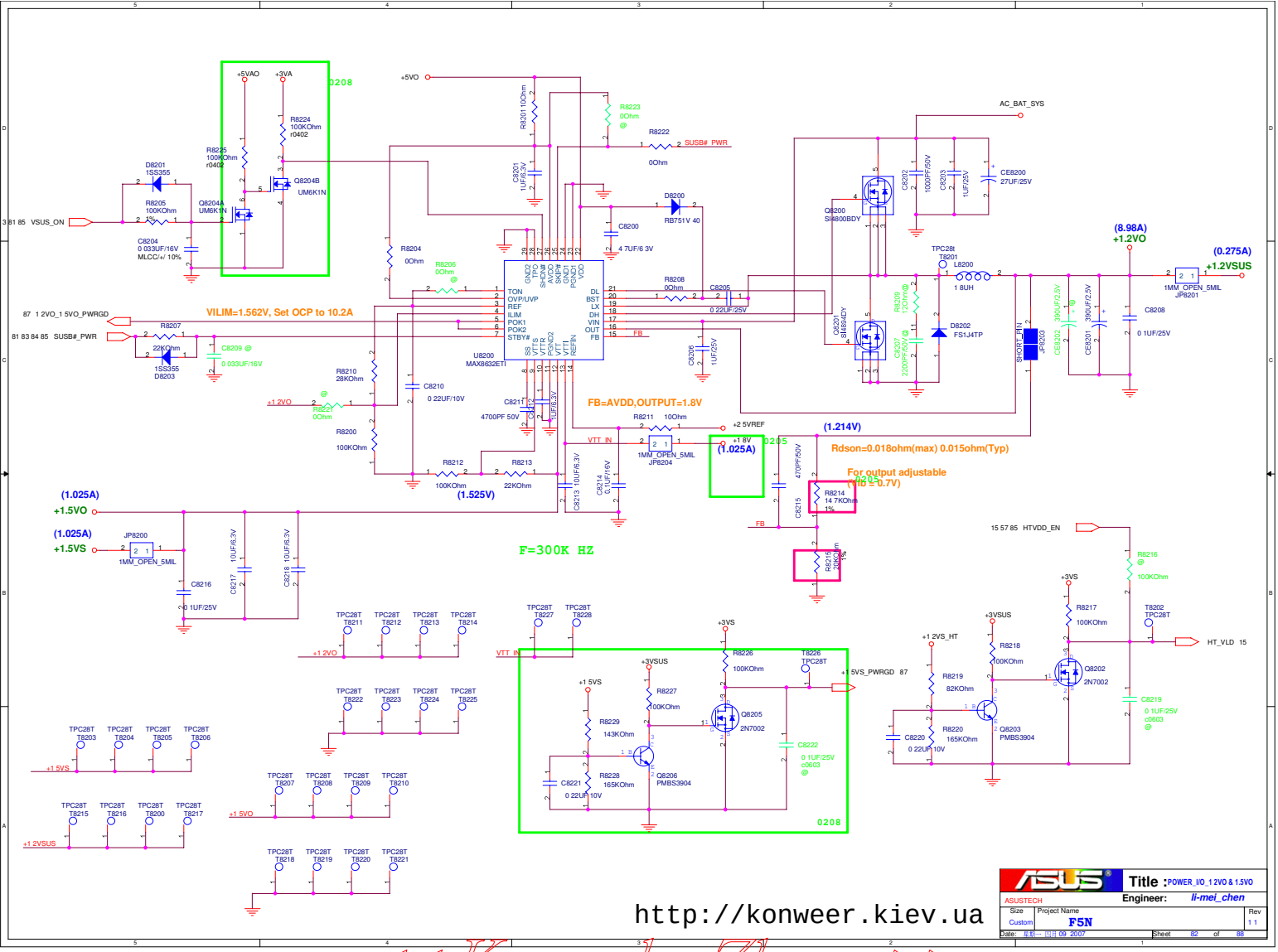

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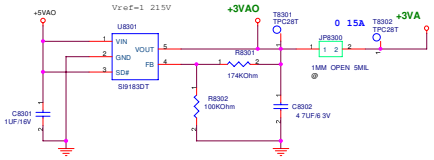

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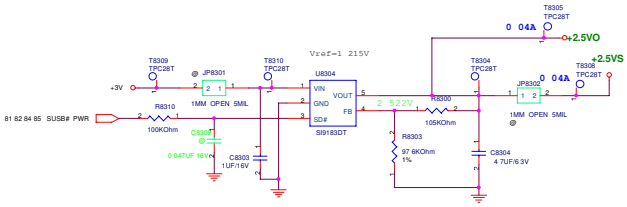

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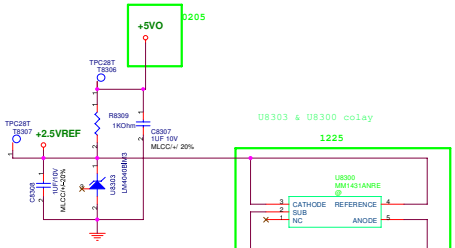

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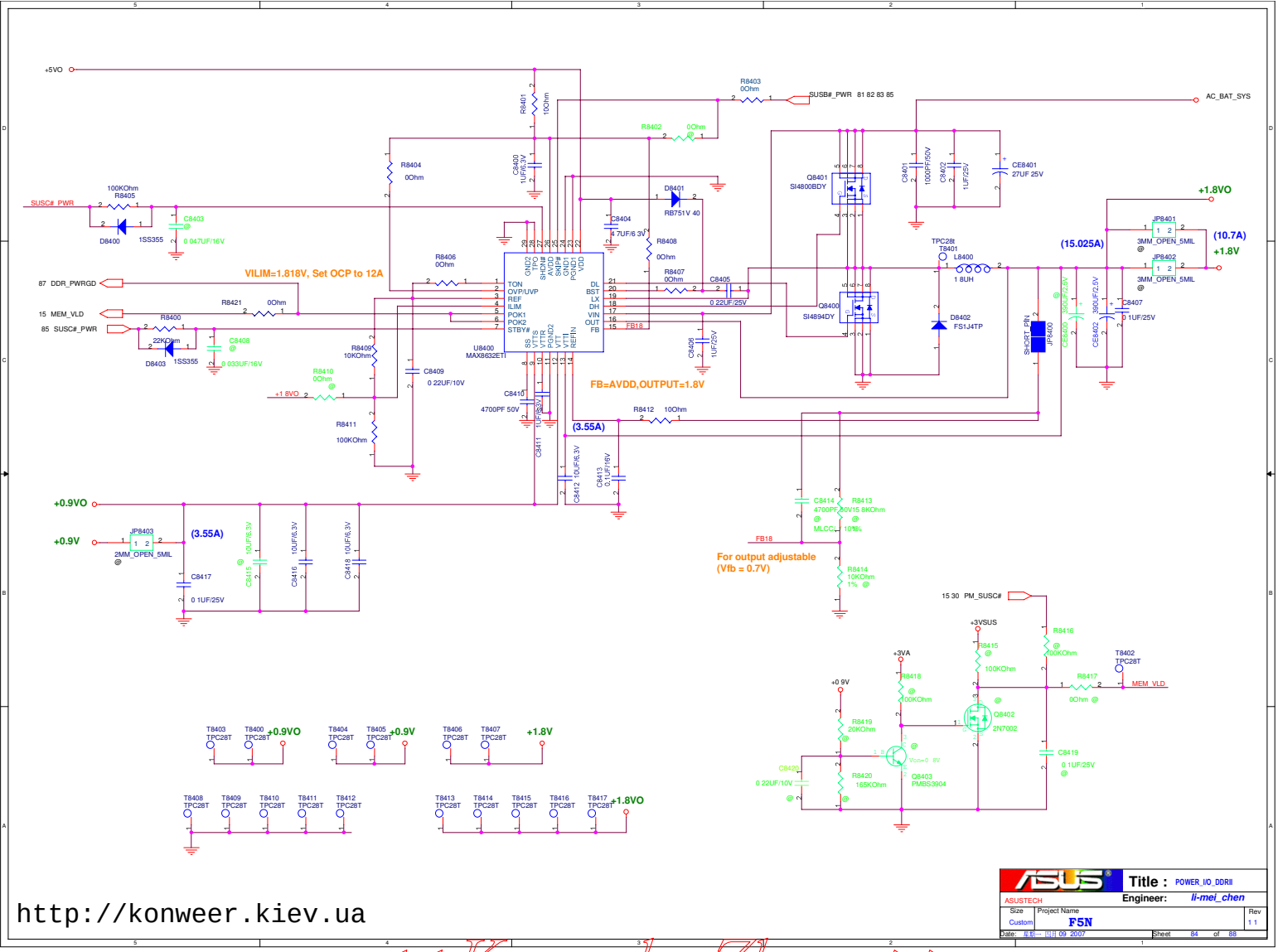
ASUSTECH	Title : POWER_IO_LDO		
	Engineer: li mei_chen		
Size: C	Project Name: F5N		Rev: 1 1
Date: 星期二 09 2007	Sheet 83 of 88		



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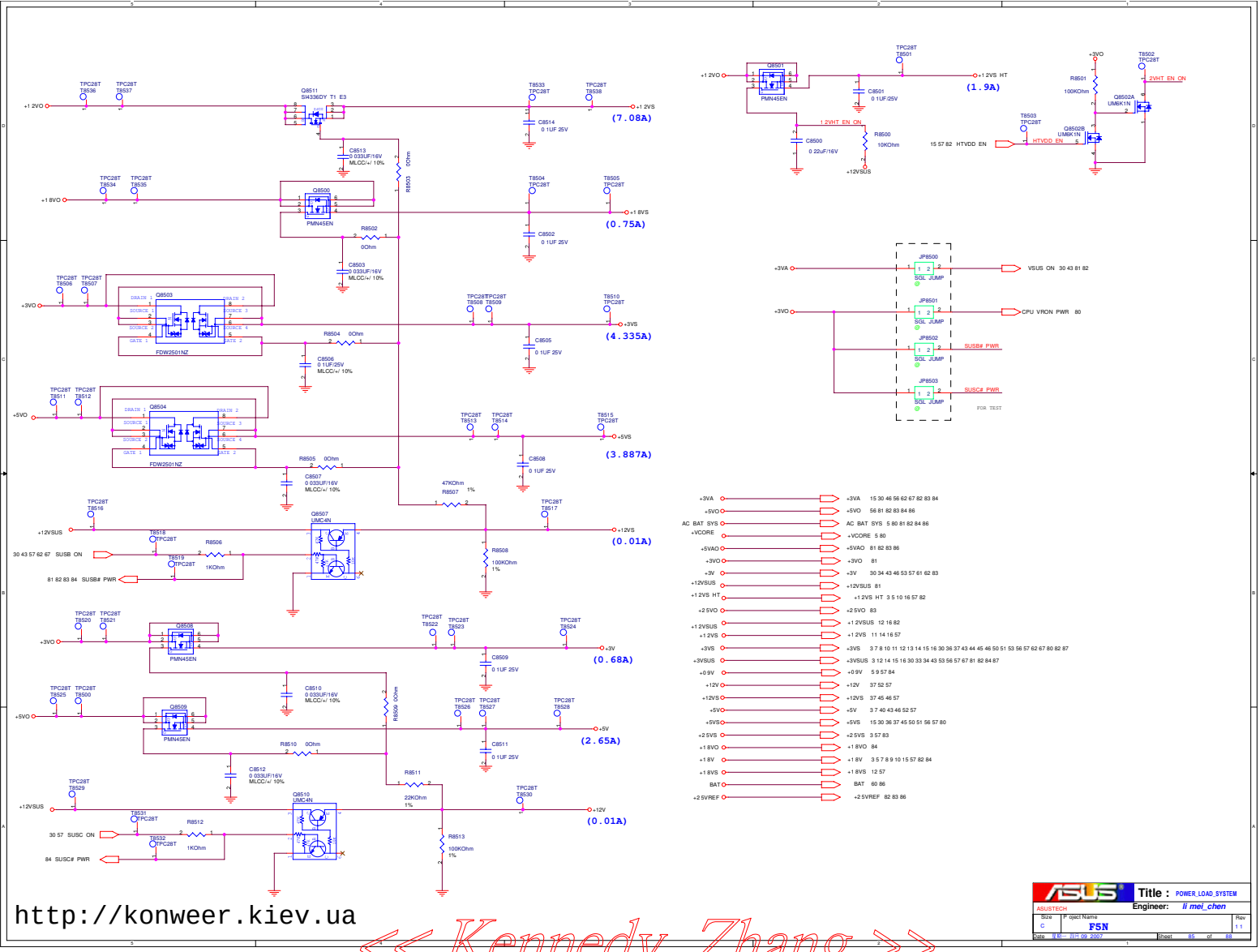
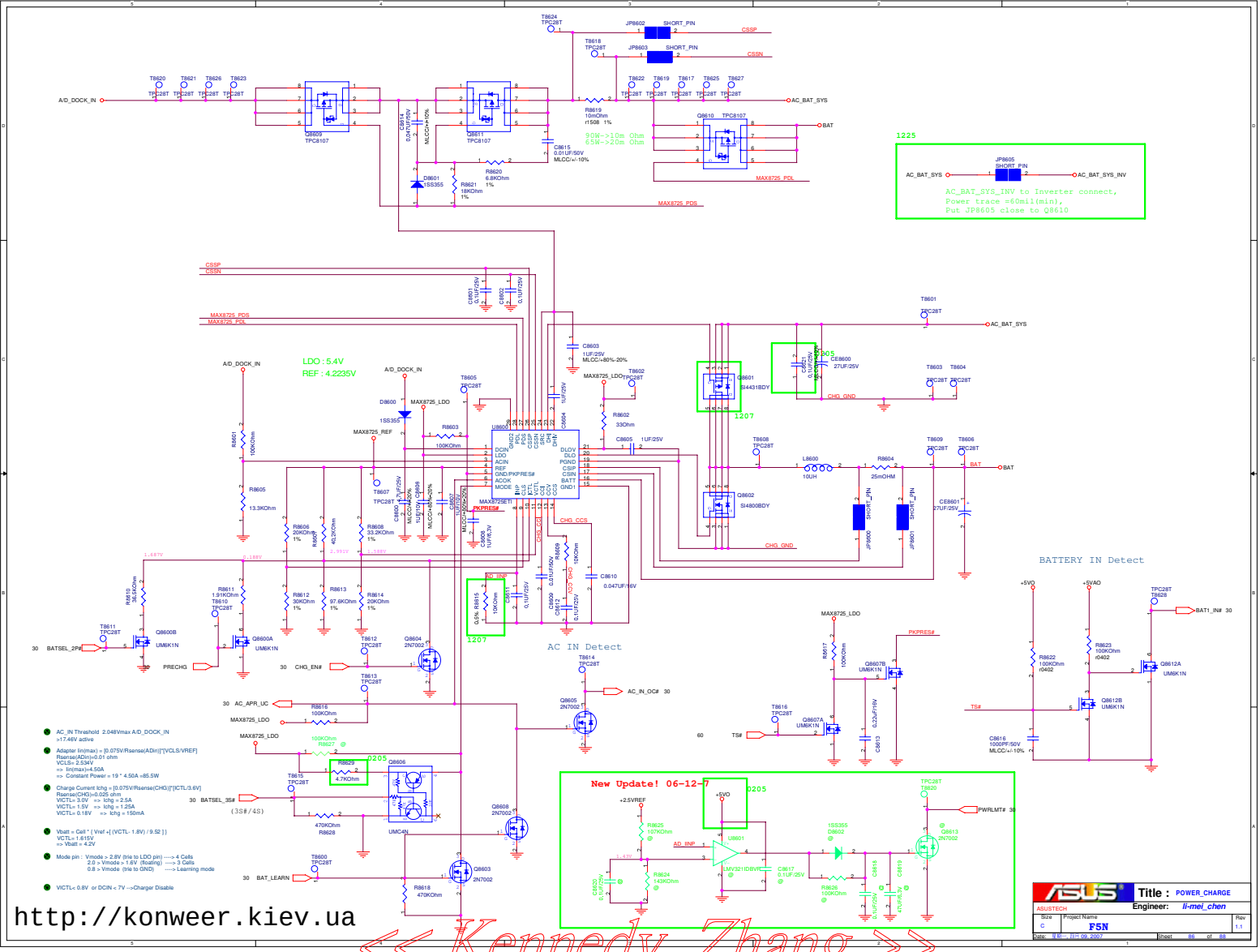
<< Kennedy_Zhang >>





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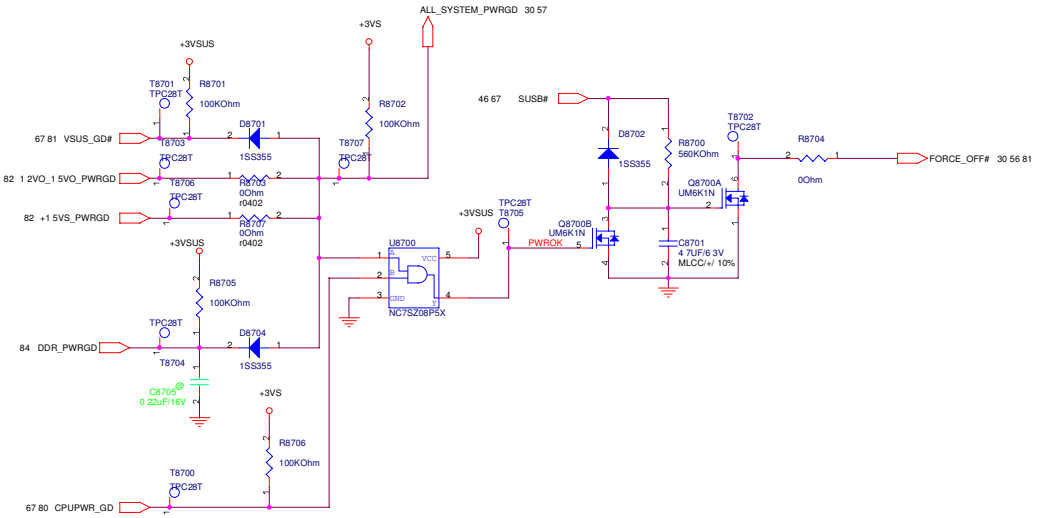

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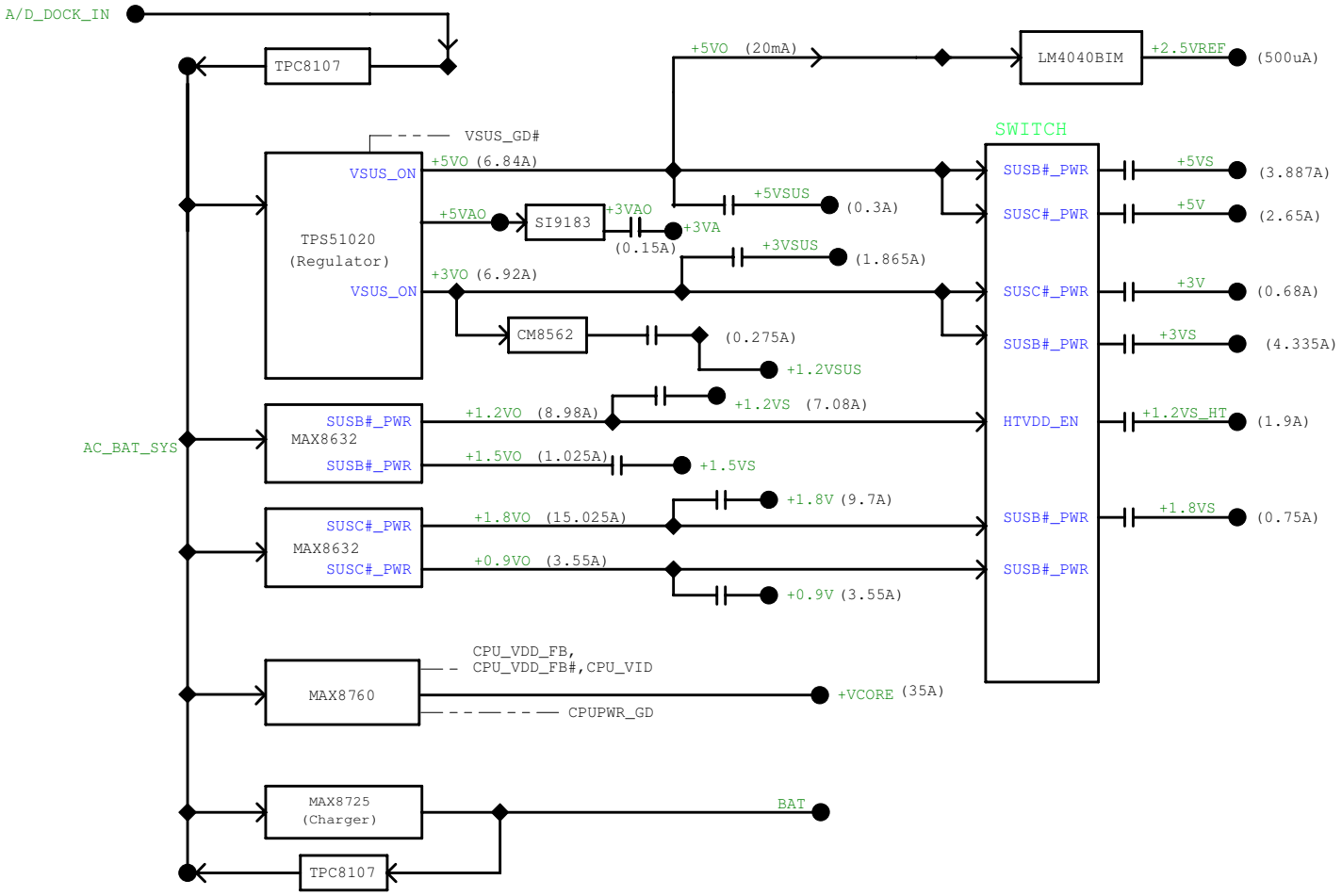
ASUSTECH

Title : POWER_PROTECT

Engineer: li-mei_chen

Size	Project Name	Rev
Custom	F5N	1 1

Date: 星期一 四月 09 2007 Sheet 87 of 88



Title : POWER DIAGRAM
ASUSTECH
Engineer: li-mei_chen
Size: Custom
Project Name: F5N
Rev: 1.1
Date: 星期一 四月 09 2007
Sheet 88 of 88